**105-2 CA with Embedded DSD Homework 3 Report**

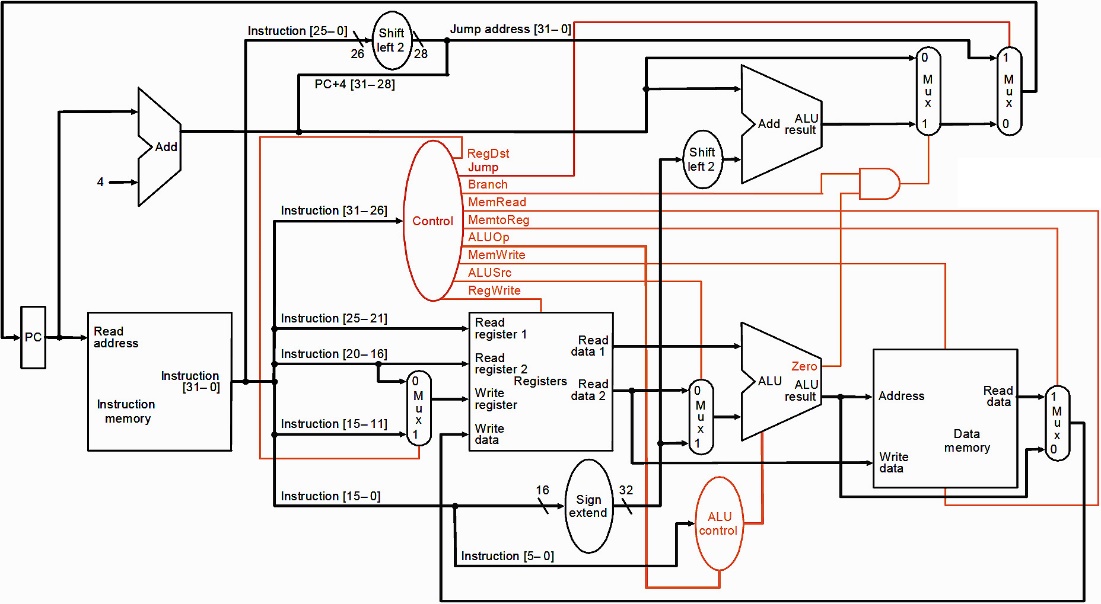
*Hardware Implementation of Single Cycle MIPS*

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1. **RTL simulation**

**The implementation of module SingleCycle\_MIPS :**

According to the datapath on the below, I implemented several sub modules at the first, and then utilize them in module SingleCycle\_MIPS.

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**Sub modules:**

1. PC (Program Counter)
2. Add\_ALU
3. register\_file
4. mainControl
5. ALU
6. ALUControl
7. signExtend
8. Mux

**In module SingleCycle\_MIPS:**

Cell Reference

\_PC PC

\_mainControl mainControl

\_ALU ALU

\_ALUControl ALUControl

\_signExtend signExtend

\_regFile register\_file

MUXX\_RegDST Mux\_WIDTH5\_0

MUXX\_Src Mux\_WIDTH32\_0

MUXX\_MemToReg Mux\_WIDTH32\_5

PC\_adder Add\_ALU\_0

branch\_adder Add\_ALU\_1

MUXX\_Branch Mux\_WIDTH32\_4

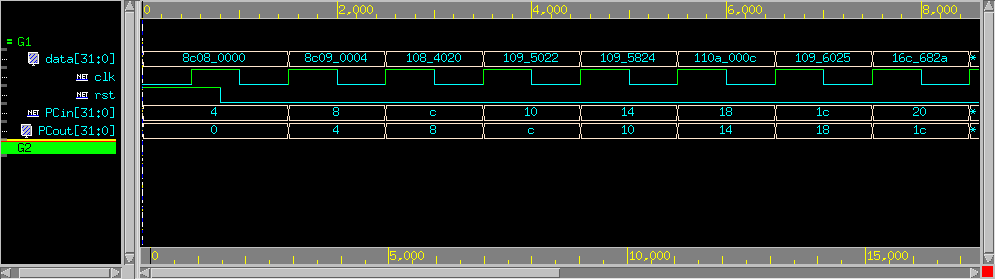
MUXX\_JumpRegister Mux\_WIDTH32\_2

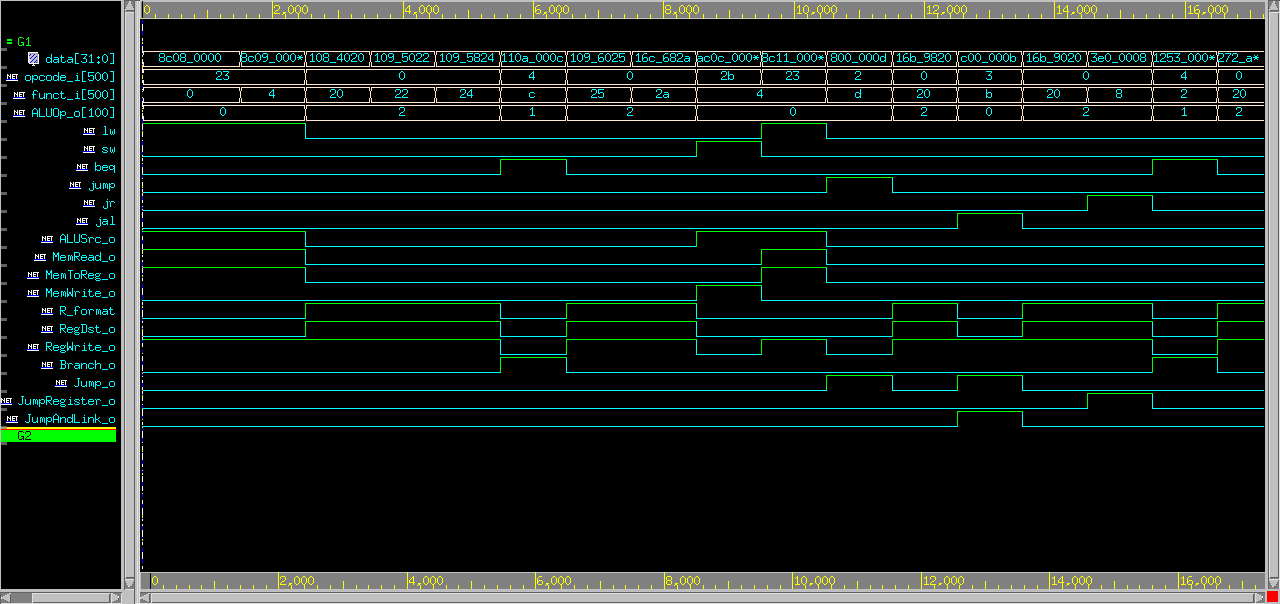
MUXX\_Jump Mux\_WIDTH32\_3

MUXX\_JumpAndLink\_1 Mux\_WIDTH5\_1

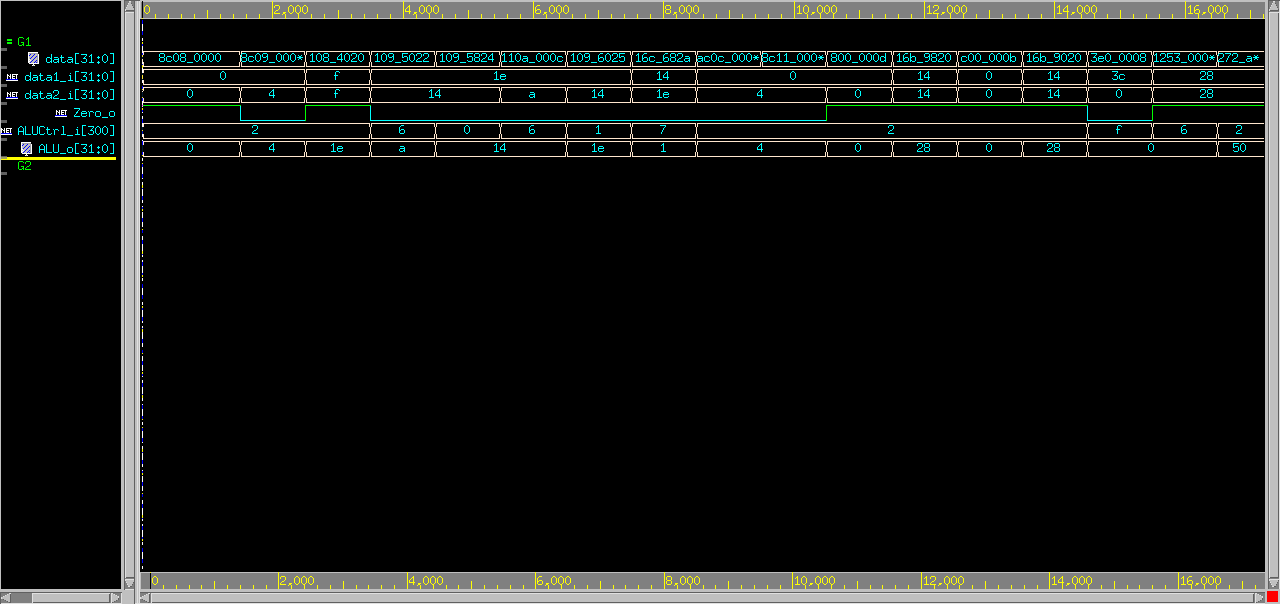
MUXX\_JumpAndLink\_2 Mux\_WIDTH32\_1

而每個cell所得波形圖如下所示:

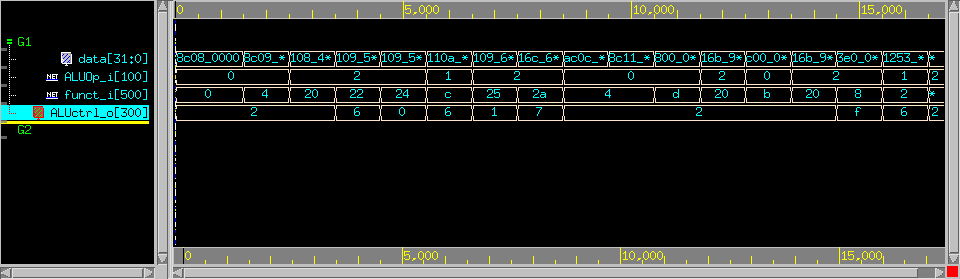
1. \_PC
2. \_mainControl



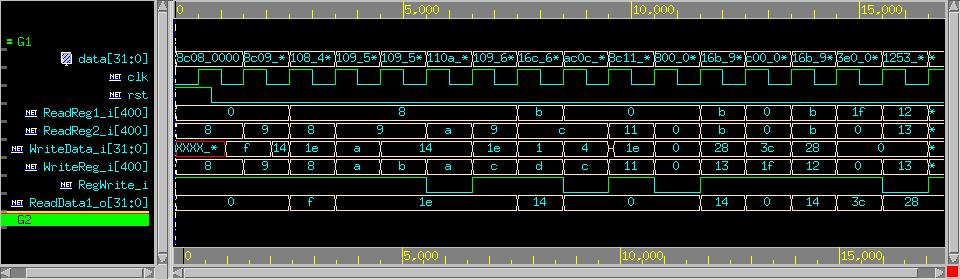
1. \_ALU



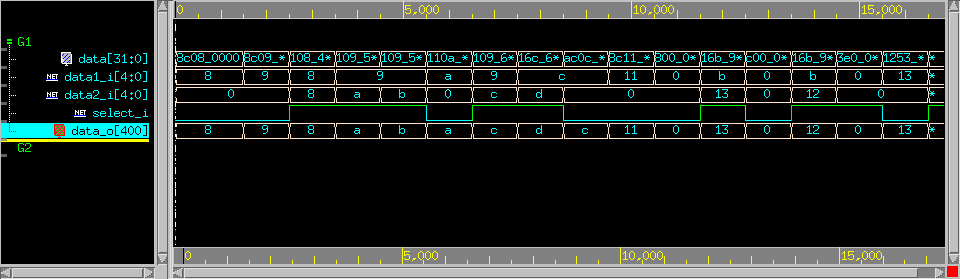
1. \_ALUControl



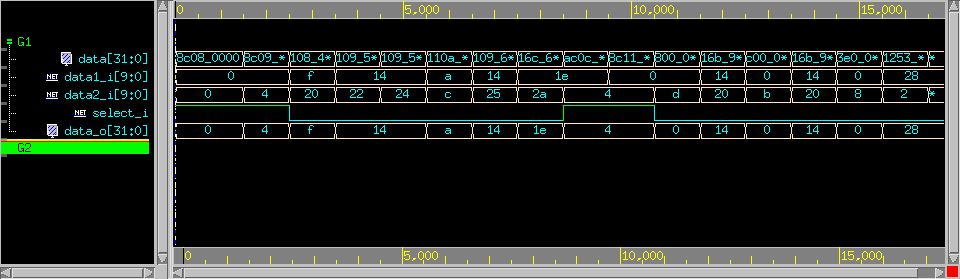
1. \_regFile



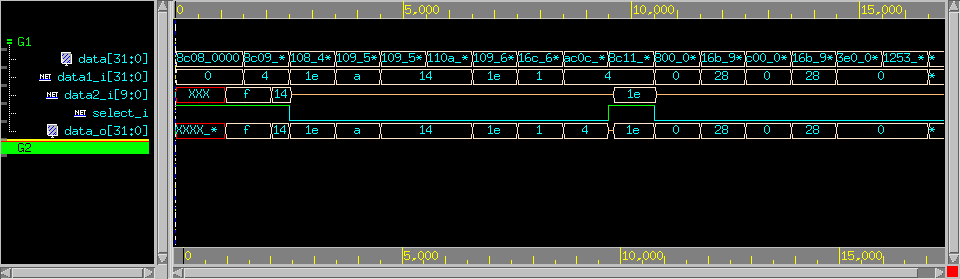
1. MUXX\_RegDST



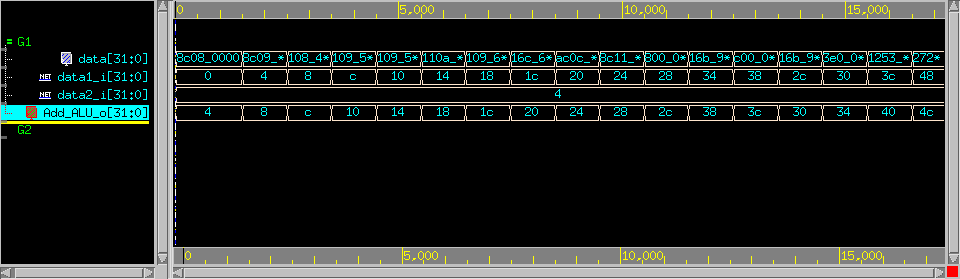
1. MUXX\_Src



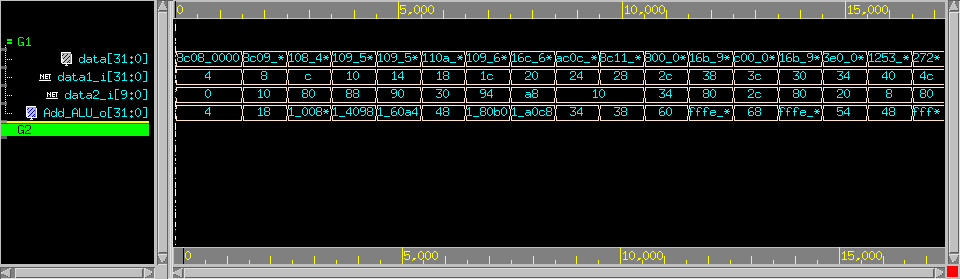
1. MUXX\_MemToReg



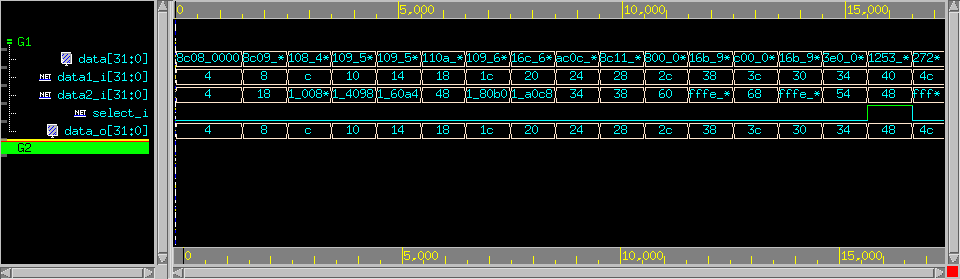
1. PC\_adder



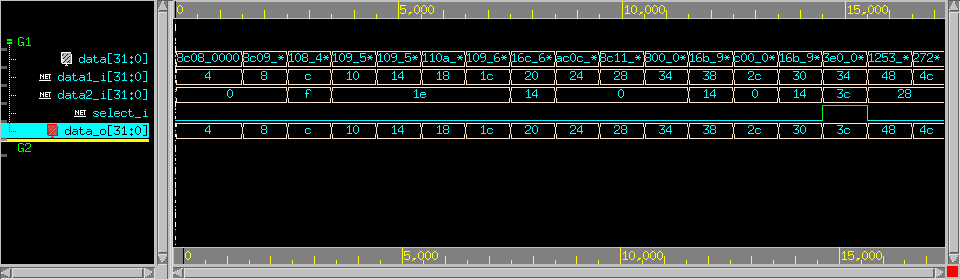
1. branch\_adder



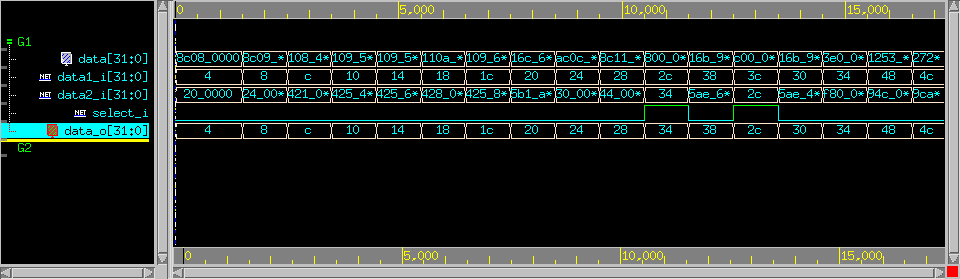
1. MUXX\_Branch



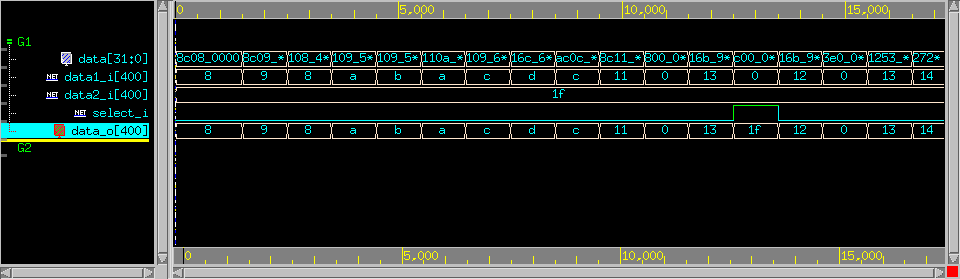
1. MUXX\_JumpRegister



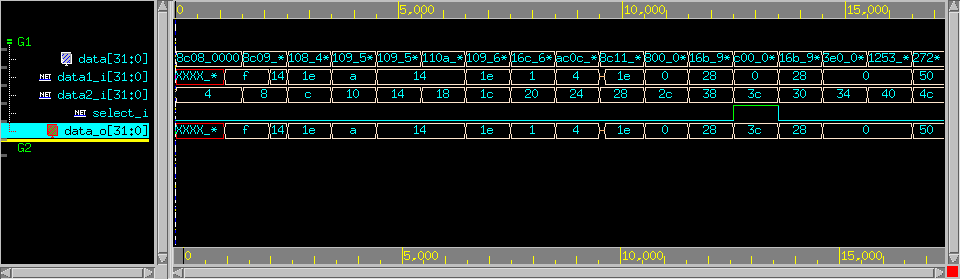
1. MUXX\_Jump



1. MUXX\_JumpAndLink\_1



1. MUXX\_JumpAndLink\_2



1. **Synthesis**

**Area Report:**

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Report : area

Design : SingleCycle\_MIPS

Version: G-2012.06

Date : Thu Apr 20 03:26:55 2017

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Library(s) Used:

typical (File: /home/raid7\_2/course/cvsd/CBDK\_IC\_Contest/CIC/SynopsysDC/db/typical.db)

Number of ports: 172

Number of nets: 533

Number of cells: 38

Number of combinational cells: 22

Number of sequential cells: 0

Number of macros: 0

Number of buf/inv: 20

Number of references: 21

Combinational area: 45503.898122

Noncombinational area: 34056.632446

Net Interconnect area: undefined (No wire load specified)

Total cell area: **79560.530569**

Total area: undefined

**Timing Path Report:**

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Report : timing

-path full

-delay max

-max\_paths 1

-sort\_by group

Design : SingleCycle\_MIPS

Version: G-2012.06

Date : Thu Apr 20 03:28:45 2017

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# A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: slow Library: slow

Wire Load Model Mode: top

Startpoint: \_regFile/register\_reg[31][1]

(rising edge-triggered flip-flop clocked by CLK)

Endpoint: A[6] (output port clocked by CLK)

Path Group: CLK

Path Type: max

Point Incr Path

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clock CLK (rise edge) 0.00 0.00

clock network delay (ideal) 0.50 0.50

\_regFile/register\_reg[31][1]/CK (DFFRX1) 0.00 # 0.50 r

\_regFile/register\_reg[31][1]/Q (DFFRX1) 0.26 0.76 r

\_regFile/U732/Y (MXI4X1) 0.20 0.96 f

\_regFile/U676/Y (MX4X1) 0.16 1.12 f

\_regFile/U674/Y (MXI2X1) 0.07 1.20 r

\_regFile/ReadData2\_o[1] (register\_file) 0.00 1.20 r

MUXX\_Src/data1\_i[1] (Mux\_WIDTH32\_0) 0.00 1.20 r

MUXX\_Src/U14/Y (AO22X1) 0.19 1.39 r

MUXX\_Src/data\_o[1] (Mux\_WIDTH32\_0) 0.00 1.39 r

\_ALU/data2\_i[1] (ALU) 0.00 1.39 r

\_ALU/sub\_371/B[1] (ALU\_DW01\_sub\_0) 0.00 1.39 r

\_ALU/sub\_371/U4/Y (CLKINVX1) 0.04 1.43 f

\_ALU/sub\_371/U2\_1/CO (ADDFXL) 0.38 1.81 f

\_ALU/sub\_371/U2\_2/CO (ADDFXL) 0.22 2.04 f

\_ALU/sub\_371/U2\_3/CO (ADDFXL) 0.22 2.26 f

\_ALU/sub\_371/U2\_4/CO (ADDFXL) 0.22 2.48 f

\_ALU/sub\_371/U2\_5/CO (ADDFXL) 0.22 2.71 f

\_ALU/sub\_371/U2\_6/CO (ADDFXL) 0.22 2.93 f

\_ALU/sub\_371/U2\_7/CO (ADDFXL) 0.22 3.16 f

\_ALU/sub\_371/U2\_8/S (ADDFXL) 0.14 3.30 f

\_ALU/sub\_371/DIFF[8] (ALU\_DW01\_sub\_0) 0.00 3.30 f

\_ALU/U20/Y (AOI221XL) 0.19 3.49 r

\_ALU/U18/Y (OAI211X1) 0.07 3.56 f

\_ALU/ALU\_o[8] (ALU) 0.00 3.56 f

A[6] (out) 0.00 3.56 f

data arrival time 3.56

clock CLK (rise edge) 10.00 10.00

clock network delay (ideal) 0.50 10.50

clock uncertainty -0.10 10.40

output external delay -6.00 4.40

data required time 4.40

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data required time 4.40

data arrival time -3.56

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slack (MET) 0.84

1. **Gate-level simulation**

**Simulated timing (ns) : 10ns**