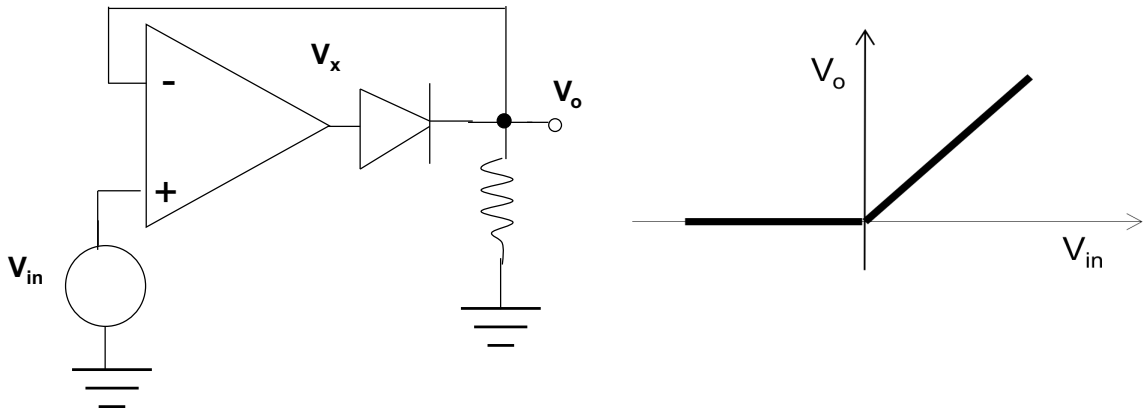
Assignment -3

Precision Rectifier (Absolute value) and RMS-DC Circuit Design

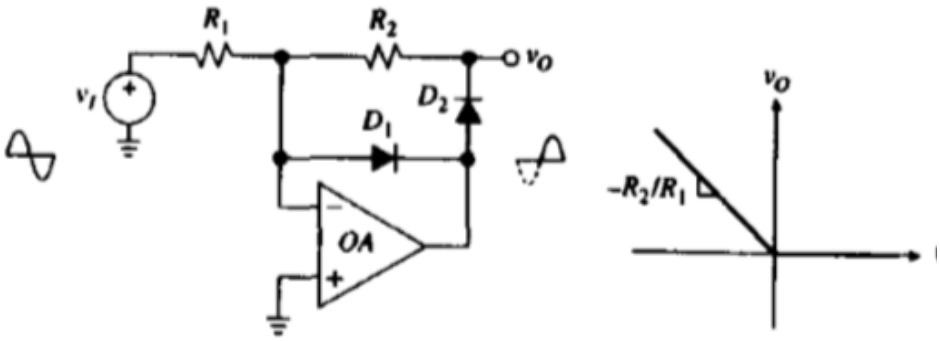
Objective: To design a full-wave precision rectifier to given specs and simulate it using LTSpice. Characterize the precision rectifier at DC and high frequency.

Background: You have already studied Half-Wave and Full-wave rectifier circuits in earlier courses and labs. One issue with such rectifier circuits is that the rectified output has an error equal to approximately the cut-in voltage (Vγ) of the diode (typically 0.6 V). The objective of the present assignment is to design a precision rectifier which gives an output approximately equal to the absolute value of the input. One way to understand precision rectifier is to start with a **super-diode** circuit shown below. This circuit is explained in chapter 3 of the Sedra-Smith book as well as chapter 9 of the Franco book. The super-diode circuit is a half-wave precision rectifier. This circuit works as follows: for a positive input voltage the current through the load resistor is positive (i.e. flows from V_o to ground). This current flows as the diode current in the forward biased condition. Thus the op-amp output node V_x is greater than V_o equal to the diode forward voltage that is approximately equal to the cut-in voltage of the diode. Since V_x follows or tracks V_o the op-amp is in negative feedback. If the gain of the op-amp is sufficiently large V_o becomes equal to V_{in}. For negative input voltages the diode prevents current in the opposite direction and therefore the current through the load resistor is equal to a very small value equal to the reverse saturation current of the diode. Therefore the output voltage is clamped to almost 0V (ground). The output of the op-amp is clamped to the negative saturation voltage $-V_{sat}$.



The super-diode circuit has a few disadvantages. For example when the input goes negative the op-amp does not have negative feedback and the op-amp output saturates at $-V_{sat}$. As the input again becomes positive the op-amp swings back to a diode drop above V_o. This rapid change in V_x results in poor settling of the output waveform due to slew-rate limitation of the op-amp as well as non-linearity in the op-amp. Another disadvantage of the super-diode circuit

is that it does not provide any gain. The half-wave precision rectifier circuit shown below is an improvement over the super-diode in this respect.



Study the precision full-wave rectifier circuits shown in Fig. 9.30 and Fig. 9.31 of the text-book by Franco and understand the corresponding equations for A_p (gain during positive) and A_n (gain during negative) cycles.

Problem Statement: Design an RMS-DC converter using a precision full-wave rectifier (FWR) that accepts an input of up to 2V sine (or any other waveform) and rectifies it to give a 2X gain output i.e. a 2V amplitude sine wave will produce a rectified output of 4V at its peak. The output should be **equal** to the RMS value. The design should require the least number of matched resistors. The % accuracy of the average value (ideally the average value should be 63.7% of peak value as shown in Fig. 9.32) should be within 4%. Minimize the ripple by following the FWR by a simple one-pole RC low-pass filter. The minimum frequency at which the circuit should work is 50 Hz.

(1) Derive the worst case percent mismatch between positive and negative gains in your circuit assuming each of your resistors are mismatched by 1%.

(2) Design the circuit such that it meets the accuracy requirements. Note that the accuracy will depend upon matching of the resistors as well as the DC gain and unity-gain frequency of the op-amps. Choose suitable op-amps and diodes from the LTSpice library. A suggested fast-settling op-amp with J-FET input (that results in extremely large input impedance) is LT1122. Use as small value of supply as possible to minimize the power dissipation requirement while at the same time making sure the op-amps do not saturate. Design the value of the R and C of the low-pass filter so as to attenuate ripple by at least 40 dB (1/100).

(3) Place the components and connect the circuit in LTSpice. Simulate the circuit with matched resistors. Measure the average value of the output waveform for one period of the waveform in transient analysis. Use the .MEASURE statement (see Help in LTSpice GOI) as a Spice Directive under Edit menu. Alternatively you may use .FOURIER statement and get the average value. Plot the DC error as a function of the input amplitude.

(4) Note the value of the offset of the op-amp in the data-sheet and place a voltage in series with the positive input of the op-amps equal to the offset value. Add 1% mismatch to the resistors. Simulate the circuit again and repeat the measurement of average value. Plot the DC error again as a function of the input voltage but now with op-amp offset and resistor mismatch included.

(5) Apply a pulsed input waveform from -1V to +1V at approximately 1 KHz frequency for a few cycles to the circuit. In case you observe instability (decaying oscillations) identify the cause of the instability apply a suitable compensation method to improve the stability of the circuit (from among the methods given in chapter 8 of the book by Franco).