Session 07

Programmable Peripherals

Overview

- Recap of 8085 Interrupts
- Offloading Interface functions
- Programmable Controllers
  - Programmable Interval Timer
  - Programmable Interrupt Controller
  - Programmable Peripheral Controller
  - Programmable DMA Controller
  - Programmable Keyboard/Display Controller
- Lab Exercises

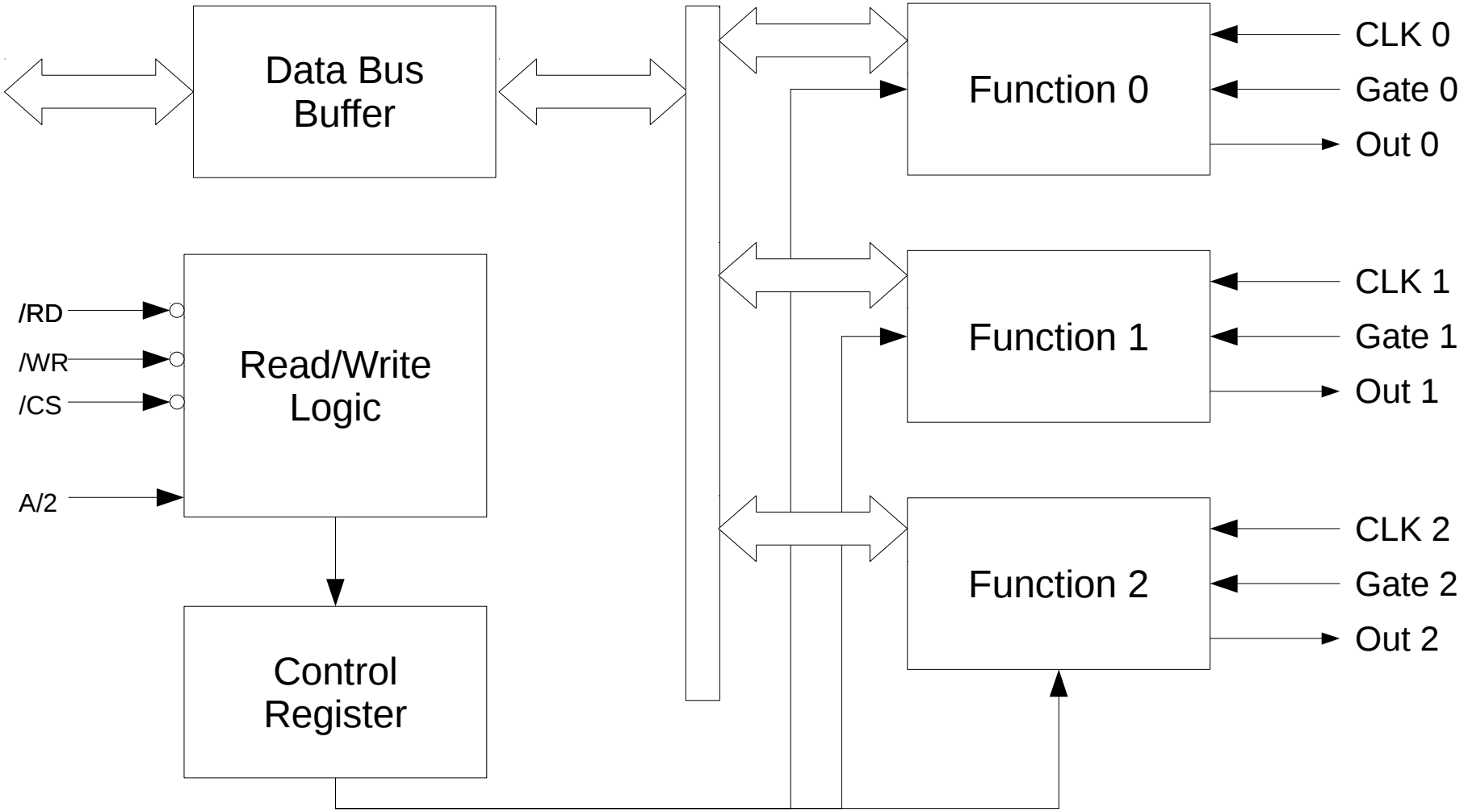
Recap – 8085 Interrupts

- Pins - TRAP, RST 7.5, RST 5.5, RST 6.5, INTR, INTA
- Instructions – RST, SIM, RIM
- Computing address of an interrupt service routine (ISR)
- Hard-wired addresses (aka vector) for RST *.5 and TRAP
- “Soft” addresses supplied by peripheral or software
- Recognising and acknowledging an interrupt in an instruction cycle
- Enabling and Disabling interrupts globally
- Masking and Unmasking interrupts using SIM/RIM instructions
- Resetting RST 7.5 Flip/Flop (why?)
- Priorities amongst interrupts

Interface circuits

- 8085 needs many logic circuits (“chipset”) to decode, demux, buffer or latch digital signals between itself and other chips like memory or peripherals
- 8085 is much, much faster than any of its supporting chips. It is also expensive and power hungry, so idling must be minimized and most of its cycles must be used for computation
- Therefore, the it off loads decoding, demuxing, control and timing logic to a set of Programmable functional circuits. These circuits perform fixed, stable functions under instructions from 8085 but at a much lower cost, power and can be re-used across multiple CPU generations. They are known as “Programmable Controllers”
  - 8259 Programmable Interrupt Controller (PIC)
  - 8257 DMA Controller
  - 8253 Programmable Interval Timer (PIT)
  - 8255 Programmable Peripheral Interface (PPI)
  - 8279 Programmable Keyboard/Display Controller
  - 8251 Programmable Communication Interface

General Structure



8259 PIC

- Combines multiple sources of interrupts into one (or more) CPU interrupt pins.
- PICs may be cascaded to handle more than 8 IR lines (upto 8 slaves)
- 28-pin chip
  - 8 Dx lines, 1 Ax line, 4 RD/WR/CS/EN lines, 8 IR lines, 2 INT/INTA lines, 3 cascade lines, 2 power lines.
- Three registers – Interrupt Mask, Interrupt Request, In-service
- EOI (End of Interrupt) for completion of an in-progress request.
- Programmable – edge/level, priority types (fixed, rotating)
- Supports 8080, 8085, 8086.
- Supplies vector on the data bus for INTR cycle on 8080/8085
- See Intel Datasheet for programming details.

8257 DMA Controller

- 40-pin complex chip to transfer data between memory and input/output devices without putting them through CPU registers.
- 4 – channels for data transfer. Each channel
  - has 16-bit registers for address, count
  - can be programmed to transfer upto 16KB at a time.
- Built-in logic for interrupts, priority.
- Sequential data transfer at full bus speed – start address, count, destination address.
- Uses HOLD/HLDA pins on the CPU to steal cycles for transfer.
- Master and Slave modes.
- Does not select itself (CS) while performing DMA transfer.
- Two registers – Mode Set and Status.

8253 Interval Timer

- An interval timer consists of a precise timing signal, a pre-set count and a counter (register) periodically decremented (or incremented) until it reaches zero. It generates a signal when the count reaches zero (pre-set limit).
- Interval timers may be one-shot or repeating (periodic). In the latter case, the counter is reloaded at the end and the decrement cycle begins.
- 8253 contains three such timers with 16-bit counters in one 24-pin chip:
  - Generate interrupt at steady intervals (e.g. for keeping accurate time)
  - Generate a pulse after a specific delay (e.g. timeout waiting for input)
  - Generate a pulse train on a pin (e.g. SOD)
  - Measure time delays between two events.
  - Count events happening within an interval (e.g. bytes received per second)
  - Run a real-time clock and calendar

8251 Communication I/F

- A universal (a)synchronous serial receiver/transmitter (USART)
- 8-bit data (CPU) <-> 1-bit serial port on the peripheral side
  - Framing bits (start/stop)
  - error detection with parity bits
  - pause-resume (xon/xoff) handshake, modem controls (DSR/DTR, CTS/RTS)
- Handles multiple serial encoding/decoding of 8-bit data
- Buffers on Tx and Rx side.
- Single pin for Control/Data
- Mode – BAUD RATE, LENGTH, PARITY, STOP BITS, START BITS ...
- TxRDY-> interrupt -> write bytes, RxRDY -> interrupt -> read bytes

8255 PPI

- 40-pin chip
- Provides three 8-bit ports (24 lines) – A, B, C
- Ports A and B may be used at 8-bit input or output ports
- Port C may be used a single 8-bit I/O or two 4-bit I/O ports or produce handshake signals for A and B.
  - Group A – Port A and upper nibble of Port C
  - Group B – Port B and lower nibble of Port C
- Interfaces directly with 808x for RESET logic. All lines are input on reset.
- 2-bit address lines (demuxed)
  - 0 (A), 1 (B), 2 (C), 3 (Control)
- 8-bit control code for setting operating modes and bits.
- Modes – Simple I/O, Strobed I/O, Strobed Bi-Di I/O.

8279 Keyboard/Display Ctrlr.

- 40-pin chip to interface keyboard and 7-segment LED display
- Keyboard
  - Scans 8x8 key matrix, plus shift and control bits.
  - debouncing, 2-key lockout, N-key rollover, auto-repeat
  - 8-byte FIFO queue
- Display
  - 2x4-lines or 1x8 lines
  - 16-byte buffer random-access.
- Scan logic
  - Scans keyboard matrix and LED matrix – 4 lines
  - Encoded (2-bits) or decoded (4-bits) are supported.
- Interface – 8-bit data, 8-bit control registers, 8 commands
- Interrupt request line to processor.

References

- Intel Component Data Catalog (1982)
  - Chapter 7 Microprocessors (8085, 8257, 8259A)
  - Chapter 9 Microprocessor Peripherals (8251A, 8253, 8255A, 8279)
- Warning:
  - Controllers may be from different vendors with slightly different specs.
  - Beware of downloading from unknown sites on the Web.