Session 2

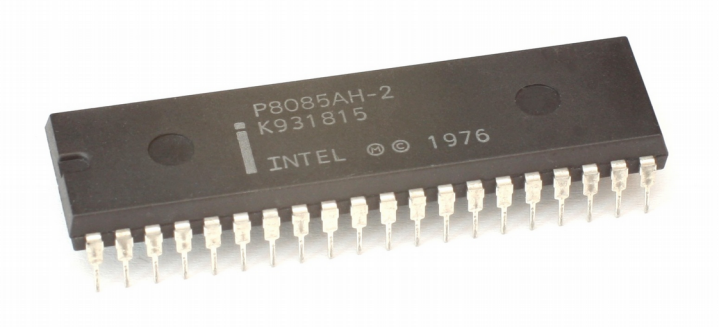
Architecture and Organization of 8085

Recap

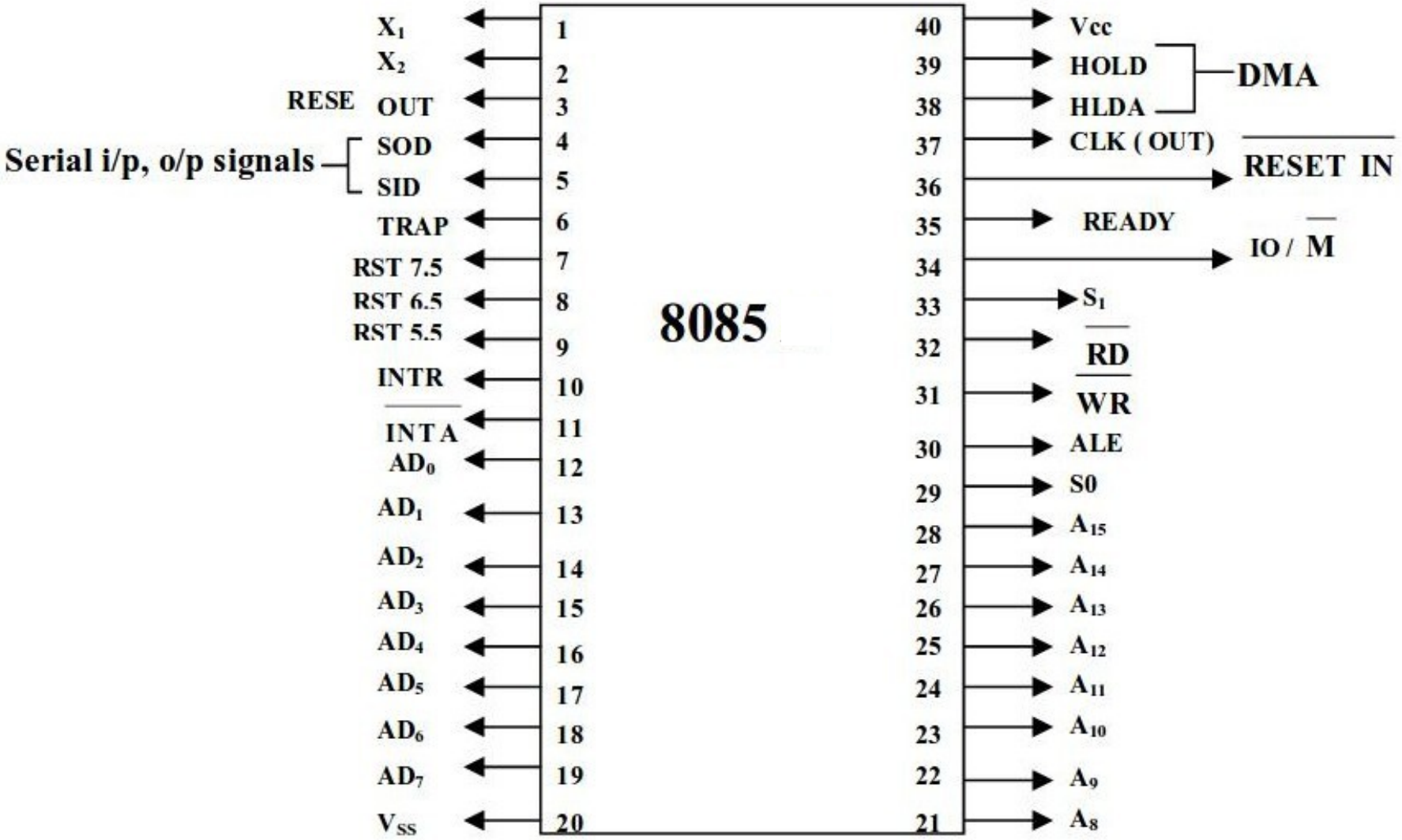
- History of Microprocessor and computing
- Intel 4004 architecture

8085 Microprocessor

- 40-pin IC released 1976 (41 ya)
- 8 bit Data but 16-bit Address
- Uses single 5v pin instead of (+5v/-5v/+12v of 8080)
- Software compatible with 8080
  - 80 instructions (+2 from 8080)
  - Added Serial I/O and Interrupts



8085 Pin Diagram



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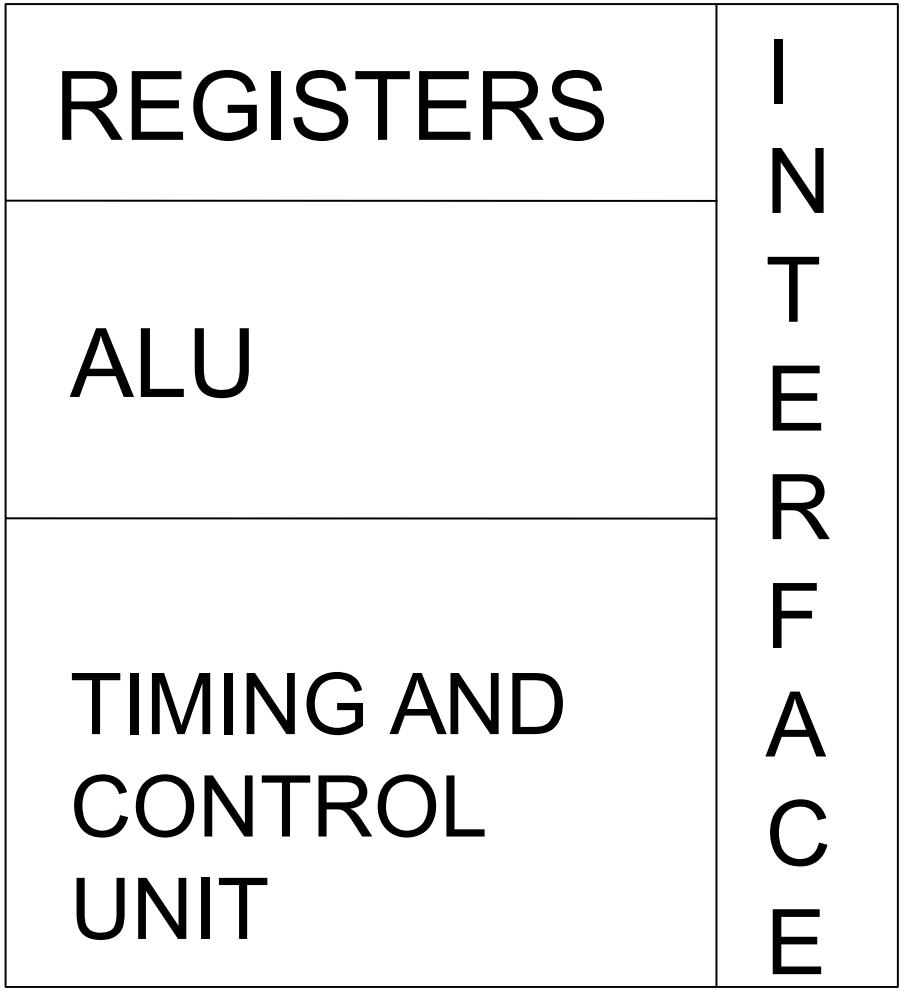
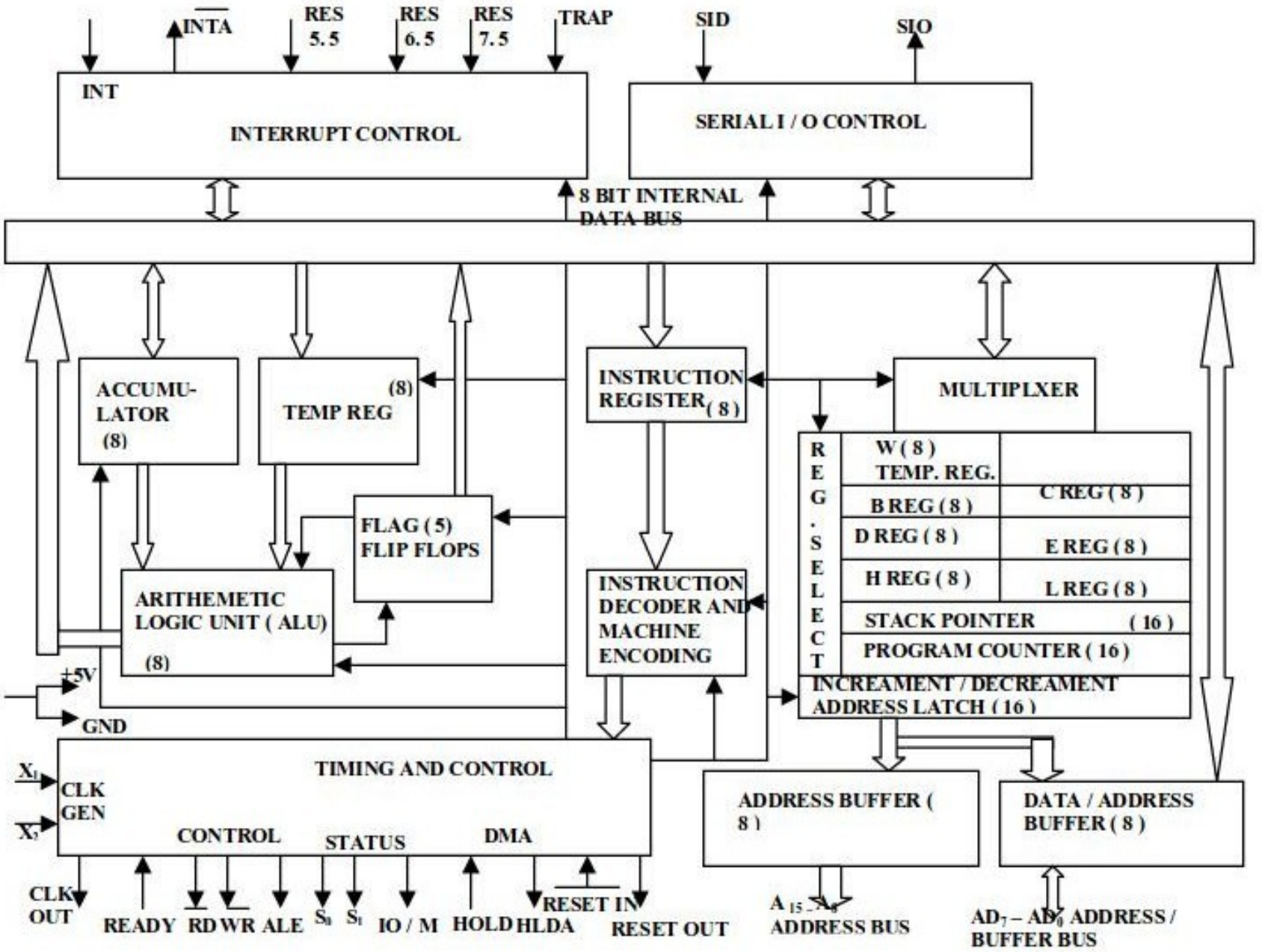
8085 Microprocessor Architecture



8085 Microprocessor Architecture



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Registers

Accumulator	Flag
B (8)	C (8)
D (8)	E (8)
H (8)	L (8)
PC (16)	
SP (16)	

Flag Registers

S	Z	-	AC	-	P	-	CY

Arithmetic and Logic Unit

Arithmetic Operations	Logical Operations
Addition	AND
Subtraction	OR
Increment	EXOR
Decrement	NOT
	CLEAR
	COMPARE
	SHIFT/ ROTATE

Timing and Control Unit

- Co-ordinates and controls the subsystems within the CPU and also outside the CPU.
- Bus Control Response
  - HOLD: Indicates that another master is requesting the use of the address and data buses. The CPU, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer.
  - HLDA (HOLD Acknowledge): Indicates that the CPU has received the HOLD request and that it will relinquish the bus in the next clock cycle.
- Reset Response
  - RESET IN: When this signal goes low, the Program Counter (PC) is set to zero.
  - RESET OUT: This signal indicates that Microprocessor is being reset. This signal can be used to reset other devices.

Interrupts

Priority	Name	Sensitivity	Mask Bit	Vector Address
1	TRAP	Both Level and edge sensitive	No	24H
2	RST 7.5	Edge Sensitive	Yes	3CH
3	RST 6.5	Level Sensitive	Yes	34H
4	RST 5.5	Level Sensitive	Yes	2CH
5	INTR	Level Sensitive	Yes	Supplied by Interrupt Controller