density e_{no} is related to the individual source densities e_n as $e_{no} = e_n/\sqrt{N}$. (*b*) Find the maximum value of the resistances in terms of e_n so that the rms noise contributed by the resistances is less than 10% of the rms noise due to the sources.

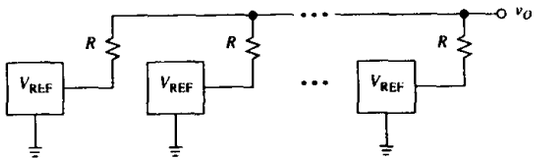


FIGURE P7.37

REFERENCES

1. H. W. Ott, *Noise Reduction Techniques in Electronic Systems,* 2d ed., John Wiley & Sons, New York, 1988.
2. C. D. Motchenbacher and J. A. Connelly, *Low-Noise Electronic System Design,* John Wiley & Sons, New York, 1993.
3. A. P. Brokaw, "An IC Amplifiers User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change," Application Note AN-202, *Applications Reference Manual,* Analog Devices, Norwood, MA, 1993.
4. A. Rich, "Understanding Interference-Type Noise," Application Note AN-346, and "Shielding and Guarding," Application Note AN-347, *Applications Reference Manual,* Analog Devices, Norwood, MA, 1993.
5. A. Ryan and T. Scranton, "Dc Amplifier Noise Revisited," *Analog Dialogue,* Vol. 18, No. 1, Analog Devices, Norwood, MA, 1984.
6. M. E. Gruchalla, "Measure Wide-Band White Noise Using a Standard Oscilloscope," *EDN,* June 5, 1980, pp. 157–160.
7. P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits,* 3d ed., John Wiley & Sons, New York, 1993.
8. S. Franco, "Current-Feedback Amplifiers," *Analog Circuit Design: Art, Science, and Personalities,* J. Williams ed., Butterworth-Heinemann, Stoneham, MA, 1991.
9. W. Kester, "High Speed Operational Amplifiers," *High-Speed Design Techniques,* Analog Devices, Norwood, MA, 1996.
10. R. M. Stitt, "Circuit Reduces Noise from Multiple Voltage Sources," *Electronic Design,* Nov. 10, 1988, pp. 133–137.
11. J. G. Graeme, *Photodiode Amplifiers–Op Amp Solutions,* McGraw-Hill, New York, 1996.
12. G. Erdi, "Amplifier Techniques for Combining Low Noise, Precision, and High Speed Performance," *IEEE J. Solid-State Circuits,* Vol. SC-16, Dec. 1981, pp. 653–661.
13. A. Jenkins and D. Bowers, "NPN Pairs Yield Ultralow-Noise Op Amp," *EDN,* May 3, 1984, pp. 323–324.

8

STABILITY

Since its conception by Harold S. Black in 1927, negative feedback has become a cornerstone of electronics and control, as well as other areas of applied science, such as biological systems modeling. As seen in the previous chapters, negative feedback results in a number of performance improvements, including gain stabilization against process and environmental variations, reduction of distortion stemming from component nonlinearities, broadbanding, and impedance transformation. These advantages are especially startling if feedback is applied around very high-gain amplifiers such as op amps.

Negative feedback comes at a price, however: the possibility of an oscillatory state. In general, oscillation will result when the system is capable of sustaining a signal around the loop regardless of any applied input. For this to occur, the system must provide enough phase shift around the loop to turn feedback from negative to positive, and enough loop gain to sustain an output oscillation without any applied input.

This chapter provides a systematic investigation of the conditions leading to instability as well as suitable cures, known as *frequency-compensation techniques,* to stabilize a circuit so that the benefits of negative feedback can be fully realized.

8.1 THE STABILITY PROBLEM

The advantages of negative feedback are realized only if the circuit has been stabilized against the possibility of oscillations. For an intuitive discussion,[1] refer again to the feedback system of Fig. 1.21. As we know, whenever the amplifier detects an input error x_d, it tries to reduce it. It takes some time, however, for the amplifier to react and then transmit its response back to the input via the feedback network. The consequence of this combined delay is a tendency on the part of the amplifier to overcorrect the input error, especially if the loop gain is high. If the overcorrection exceeds the original error, a regenerative effect results, whereby the magnitude of x_d diverges, instead of converging, and instability results. Signal amplitudes grow exponentially until inherent circuit nonlinearities limit further growth, forcing the system either to saturate or to oscillate, depending on the order of its system function. By contrast, a circuit that succeeds in making x_d converge is stable.

Gain Margin

Whether a system is stable or unstable is determined by the manner in which its loop gain T varies with frequency. To substantiate, suppose a frequency exists at which the phase angle of T is $-180°$; call this frequency $f_{-180°}$. Then, $T(jf_{-180°})$ is real and negative, indicating that feedback has turned from negative to positive. If $|T(jf_{-180°})| < 1$, then Eq. (1.40), rewritten here as

$$A(jf_{-180°}) = \frac{a(jf_{-180°})}{1 + T(jf_{-180°})}$$

indicates that $A(jf_{-180°})$ is greater than $a(jf_{-180°})$ because the denominator is less than unity. The circuit is nonetheless stable because any signal circulating around the loop will progressively decrease in magnitude and eventually die out; consequently, the poles of $A(s)$ must lie in the left half of the s plane.

If $|T(jf_{-180°})| = 1$, the above equation predicts $A(jf_{-180°}) \to \infty$, indicating that the circuit can now sustain an output signal even with zero input! The circuit is an oscillator, indicating that $A(s)$ must have a conjugate pole pair right on the imaginary axis. Oscillations are initiated by ac noise, which is always present in some form at the amplifier input. An ac noise component x_d right at $f = f_{-180°}$ results in a feedback component $x_f = -x_d$, which is further multiplied by -1 in the summing network to yield x_d itself. Thus, once this ac component has entered the loop, it will be sustained indefinitely.

If $|T(jf_{-180°})| > 1$, mathematical tools other than the foregoing equation are needed to predict circuit behavior. Suffice it to say here that now $A(s)$ may have a conjugate pole pair in the right half of the s plane. Consequently, once started, oscillation will grow in magnitude until some circuit nonlinearity, either inherent, such as a nonlinear VTC, or deliberate, such as an external clamping network, reduces the loop gain to exactly unity. Henceforth, oscillation is of the sustained type.

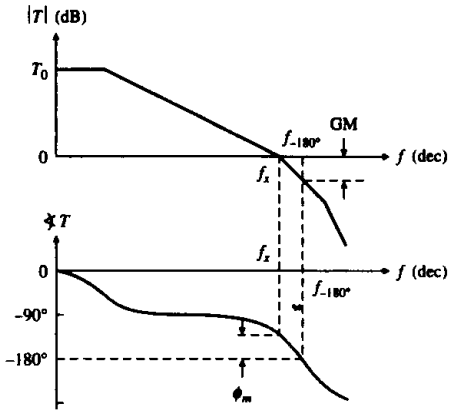


FIGURE 8.1
Visualizing gain margin GM and phase margin ϕ_m.

A quantitative measure of stability is offered by the *gain margin*, defined as

$$\text{GM} = 20 \log \frac{1}{|T(jf_{-180°})|} \tag{8.1}$$

The GM represents the number of decibels by which we can increase $|T(jf_{-180°})|$ before it becomes unity and thus leads to instability. For instance, a circuit with $|T(jf_{-180°})| = 1/\sqrt{10}$ has $\text{GM} = 20 \times \log_{10} \sqrt{10} = 10$ dB, which is considered a reasonable margin. By contrast, a circuit with $|T(jf_{-180°})| = 1/\sqrt{2}$ has GM = 3 dB, not much of a margin: only a modest increase in the gain a because of manufacturing process variations or environmental changes may easily lead to instability! The GM is visualized in Fig. 8.1 (top).

Phase Margin

An alternative and more common way of quantifying stability is via phase. In this case we focus on $\sphericalangle T(jf_x)$, the phase angle of T at the crossover frequency f_x, where $|T| = 1$ by definition, and we define the *phase margin* ϕ_m as the number of degrees by which we can lower $\sphericalangle T(jf_x)$ before it reaches $-180°$ and thus leads to instability. We have $\phi_m = \sphericalangle T(jf_x) - (-180°)$, or

$$\phi_m = 180° + \sphericalangle T(jf_x) \tag{8.2}$$

The phase margin is visualized in Fig. 8.1 (bottom). To investigate its significance, we write $T(jf_x) = 1 \underline{/\phi_m - 180°} = -\exp(j\phi_m)$. The error function is then

$1/|1 + 1/T(jf_x)| = 1/|1 - \exp(-j\phi_m)|$. Using Euler's identity $\exp(-j\phi_m) = \cos\phi_m - j\sin\phi_m$, along with Eq. (1.43), we get

$$|A(jf_x)| = |A_{\text{ideal}}(jf_x)| \times \frac{1}{\sqrt{(1-\cos\phi_m)^2 + \sin^2\phi_m}}$$

Calculating the error function for different values of ϕ_m we get 0.707 for $\phi_m = 90°$, 1 for $\phi_m = 60°$, 1.31 for $\phi_m = 45°$, 1.93 for $\phi_m = 30°$, 3.83 for $\phi_m = 15°$, and ∞ for $\phi_m = 0°$. It is apparent that for $\phi_m < 60°$ we have $|A(jf_x)| > |A_{\text{ideal}}(jf_x)|$, indicating a peaked closed-loop response. Moreover, the lower ϕ_m is, the more pronounced the peaking. In the limit $\phi_m \to 0$ we get $|A(jf_x)| \to \infty$, or oscillatory behavior. In practical designs, a typical lower limit for ϕ_m is 45°, with 60° being more common.

EXAMPLE 8.1. The loop gain of Fig. 8.1 has been drawn for $T_0 = 10^4$ and three pole frequencies at 100 Hz, 1 MHz, and 10 MHz. Find (*a*) GM, (*b*) ϕ_m, and (*c*) T_0 for $\phi_m = 60°$.

Solution. We have

$$|T(jf)| = \frac{10^4}{|[1+(f/10^2)^2][1+(f/10^6)^2][1+(f/10^7)^2]|^{1/2}} \tag{8.3a}$$

$$\measuredangle T(jf) = -\{\tan^{-1}(f/10^2) + \tan^{-1}(f/10^6) + \tan^{-1}(f/10^7)\} \tag{8.3b}$$

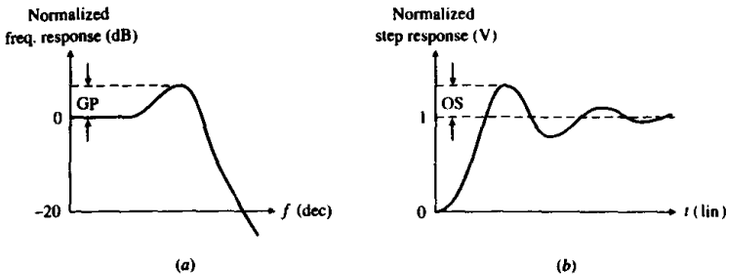
(*a*) To find GM we need to know $f_{-180°}$. The figure indicates that 1 MHz $\le f_{-180°} \le$ 10 MHz. Start out with 5 MHz, as an initial estimate, then use Eq. (8.3*b*) to find the actual value by trial and error. Letting $f = 5$ MHz in Eq. (8.3*b*) yields $\measuredangle T(j5 \times 10^6) = -195.3°$. This is too large, so try $f = 3$ MHz. This gives $\measuredangle T(j3 \times 10^6) = -178.3°$, which is too small. After a few more trials we find that $\measuredangle T = -180°$ for $f = 3.16$ MHz. Then, Eq. (8.3*a*) gives $|T(j3.16 \times 10^6)| = 91.04 \times 10^{-3}$. Finally, Eq. (8.1) gives GM = 20.82 dB.

(*b*) To find ϕ_m, we need to know f_x. The figure provides the initial estimate $f = 1$ MHz. Substituting into Eq. (8.3*a*) gives $|T(j10^6)| = 0.7036$, which is too small. So, try $f = 700$ kHz; this yields $|T(j700 \times 10^3)| = 1.167$, which is too large. After a few more iterations we find that $|T| = 1$ for $f = 784$ kHz. Then, Eq. (8.3*b*) gives $\measuredangle T(j784 \times 10^3) = -132.6°$, and Eq. (8.2) gives $\phi_m = 47.4°$.

(*c*) For $\phi_m = 60°$, we want $|T(jf_{-120°})| = 1$. Using Eq. (8.3*b*) we find, by trial and error, $f_{-120°} = 512$ kHz. The value of the denominator of Eq. (8.3*a*) at this frequency is 5760. Clearly, for $|T|$ to be unity at this frequency, its dc value T_0 must be lowered from 10^4 to 5760.

Peaking and Ringing

The presence of peaking in the frequency domain is usually accompanied by ringing in the time domain, and vice versa. As illustrated in Fig. 8.2, the two effects are quantified in terms of the *gain peaking GP*, in decibels, and the *overshoot OS*, in percentage. Both effects are absent in first-order systems since it takes a complex pole pair to produce them. For a second-order all-pole system, peaking occurs for $Q > 1/\sqrt{2}$, and ringing for $\zeta < 1$, where the *quality factor* Q and the *damping ratio* ζ are related as $Q = 1/2\zeta$, or $\zeta = 1/2Q$. Second-order systems are well documented



(*a*) (*b*)

FIGURE 8.2
Illustrating gain peaking GP and overshoot OS.

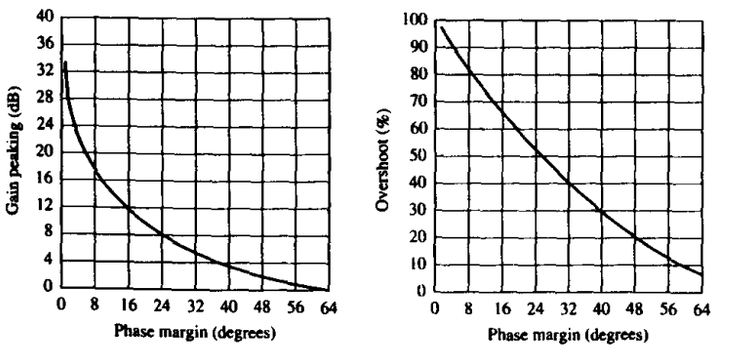
in the literature,[2] where it is found that

$$\text{GP} = 20\log_{10}\frac{2Q^2}{\sqrt{4Q^2-1}} \qquad \text{for } Q > 1/\sqrt{2} \tag{8.4}$$

$$\text{OS}(\%) = 100\exp\frac{-\pi\zeta}{\sqrt{1-\zeta^2}} \qquad \text{for } \zeta < 1 \tag{8.5}$$

$$\phi_m = \cos^{-1}\left(\sqrt{4\zeta^4+1} - 2\zeta^2\right) = \cos^{-1}\left(\sqrt{1+1/4Q^4} - 1/2Q^2\right) \tag{8.6}$$

Combining these equations yields the graphs of Fig. 8.3, which relate peaking and ringing to the phase margin. We observe that peaking occurs for $\phi_m \le \cos^{-1}(\sqrt{2}-1) = 65.5°$, and ringing for $\phi_m \le \cos^{-1}(\sqrt{5}-1) = 76.3°$. It is also worth keeping



(*a*) (*b*)

FIGURE 8.3
GP and OS as functions of ϕ_m for a second-order all-pole system.

in mind the following frequently encountered values of GP (ϕ_m) and OS (ϕ_m):

$$\text{GP}(60^\circ) \cong 0.3 \text{ dB} \qquad \text{OS}(60^\circ) \cong 8.8\%$$

$$\text{GP}(45^\circ) \cong 2.4 \text{ dB} \qquad \text{OS}(45^\circ) \cong 23\%$$

Depending on the case, a closed-loop response may have a single pole, a pole pair, or a higher number of poles. Mercifully, the response of higher-order circuits is often dominated by a single pole pair, so the graphs of Fig. 8.3 provide a good starting point for a great many circuits of practical interest.

The Rate of Closure (ROC)

We are now ready to develop a quick means for assessing stability from magnitude Bode plots for *minimum-phase systems*, that is, for systems having no roots in the right half of the s plane. To this end, let us first study the plots of Fig. 8.4, which pertain to the single-root function $H(jf) = (1 + jf/f_0)^{\pm 1}$, where -1 holds for a pole frequency, and $+1$ for a zero. Denoting the slope of $|H|$ as Slope($|H|$), we observe that for $f \le f_0/10$, Slope($|H|$) $\to$ 0 dB/dec and $\sphericalangle H \to 0^\circ$; for $f \ge 10f_0$, Slope($|H|$) $\to \pm 20$ dB/dec and $\sphericalangle H \to \pm 90^\circ$; for $f = f_0$, Slope($|H|$) $\to \pm 10$ dB/dec and $\sphericalangle H \to \pm 45^\circ$. We can empirically derive phase (in degrees) from slope (in decibels per decade) as

$$\sphericalangle H \cong 4.5 \times \text{Slope}(|H|) \tag{8.7}$$

This correlation holds also if $H(s)$ has more than one root, provided the roots are *real, negative,* and *well separated,* say, at least a decade apart.

Next, suppose both $|a|$ and $|1/\beta|$ have been graphed. Observe the slopes of the two curves at the crossover frequency f_x, and call the magnitude of their difference the *rate of closure,*

$$\text{ROC} = |\text{Slope}(|a|) - \text{Slope}(|1/\beta|)|_{f=f_x} \tag{8.8}$$

Considering that $\sphericalangle T(jf_x) = \sphericalangle a(jf_x) - \sphericalangle \beta^{-1}(jf_x)$, we can use the ROC to

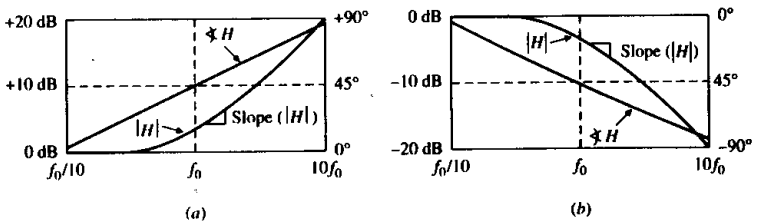


FIGURE 8.4
Graphical illustration of the relationship $\sphericalangle H \cong 4.5 \times \text{Slope}(|H|)$ for (a) a zero and (b) a pole.

estimate ϕ_m via Eq. (8.7). The following cases arise so frequently that it is worth keeping them in mind.

$$\text{ROC} \cong 20 \text{ dB/dec} \Rightarrow \phi_m \cong 90^\circ \tag{8.9a}$$

$$\text{ROC} \cong 30 \text{ dB/dec} \Rightarrow \phi_m \cong 45^\circ \tag{8.9b}$$

$$\text{ROC} \cong 40 \text{ dB/dec} \Rightarrow \phi_m \cong 0^\circ \tag{8.9c}$$

$$\text{ROC} > 40 \text{ dB/dec} \Rightarrow \phi_m < 0^\circ \tag{8.9d}$$

We shall also make frequent use of the property that for any two frequencies located within a region of constant slope of $\pm n20$ dB/dec, we have

$$|H(jf_1)|/|H(jf_2)| = (f_1/f_2)^{\pm n} \tag{8.10}$$

For instance, in the region of constant GBP of an op amp, we get the familiar result $|a(jf_1)|/|a(jf_2)| = (f_1/f_2)^{-1} = f_2/f_1$.

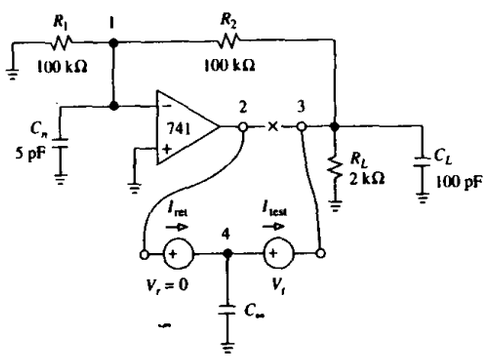
Finding T Using PSpice

PSpice is a powerful tool for finding T, especially when complex transistor-level or macromodel-level circuits are involved. A convenient method, developed by S. Rosenstark,[3] requires that we break the loop, inject a test signal in the forward direction, and perform two measurements at the return end, namely, the measurement of the open-circuit voltage V_{ret} and the short-circuit current I_{ret}. Then, we calculate

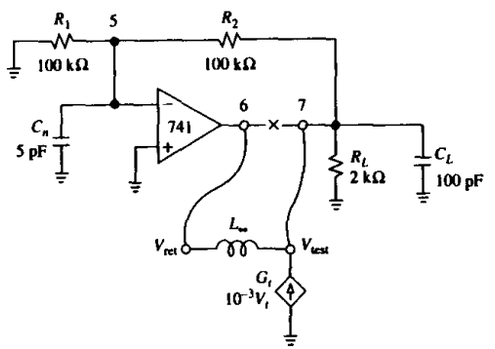
$$T = \frac{-1}{1/T_{\text{oc}} + 1/T_{\text{sc}}} \tag{8.11}$$

where $T_{\text{oc}} = V_{\text{ret}}/V_{\text{test}}$ and $T_{\text{sc}} = I_{\text{ret}}/I_{\text{test}}$, V_{test} and I_{test} being the voltage and current at the point of test-signal injection. The advantage of this method is that we can break the loop at any point we wish, without having to worry about the termination issues raised in Section 1.7.

The procedure is illustrated in Fig. 8.5 for a 741 op amp with $\beta = 0.5$. The circuit includes also R_L and C_L to model a typical output load, and C_n to model the stray capacitance of the inverting-input interconnections. Though we have chosen to break the loop at the output of the op amp, we could have broken it at any other point, such as at the inverting-input pin (see Problem 8.8). The only constraint is that as we break the loop we must maintain dc continuity for PSpice to perform the dc bias analysis. In Fig. 8.5a we use the source V_t to inject a test signal, a conveniently large shunt capacitance C_∞ to establish an ac short at the return end, and the source V_r to sense the short-circuit return current. In Fig. 8.5b we use the source G_t to inject a test signal, and a conveniently large series inductance L_∞ to maintain dc continuity



(a)



(b)

FIGURE 8.5
PSpice circuits to find T_{sc} and T_{oc}.

while providing an ac open. The PSpice circuit file uses the 741 Byle macromodel as follows.

```
Plotting the Loop Gain T:
.lib eval.lib
VCC 10 0 dc 15V
VEE 11 0 dc -15V
*Circuit to find Tsc:
R1sc 0 1 100k
R2sc 1 3 100k
Cnsc 1 0 5pF
RLsc 3 0 2k
CLsc 3 0 100pF
XOAsc 0 1 10 11 2 ua741
Vr 2 4 dc 0V
Vt 4 3 ac 1V
C00 4 0 1MegF
*Circuit to find Toc:
R1oc 0 5 100k
R2oc 5 7 100k
Cnoc 5 0 5pF
RLoc 7 0 2k
CLoc 7 0 100pF
XOAoc 0 5 10 11 6 ua741
L00 6 7 1MegH
Gt 0 7 4 3 1m
.ac dec 10 1Hz 10MegHz
.probe ;Tsc = I(Vr)/I(Vt), Toc = V(6)/V(7)
.end
```


The results of the simulation are shown in Fig. 8.6. Using the cursor facility of the Probe postprocessor, we find $f_x \cong 390$ kHz and $\measuredangle T(jf_x) \cong -134°$, indicating a phase margin $\phi_m \cong 46°$.

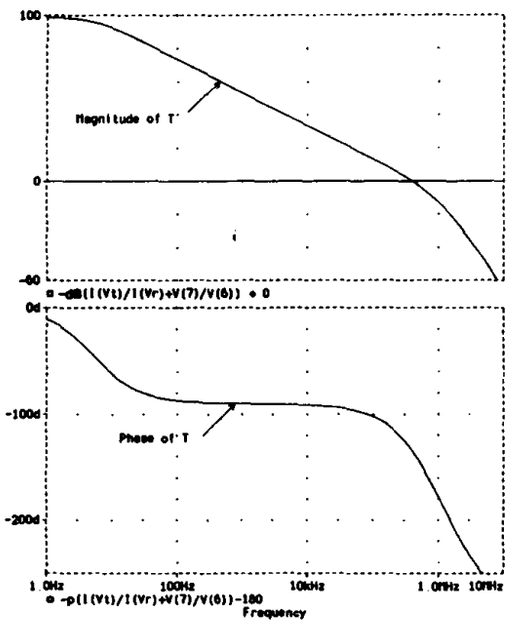


FIGURE 8.6
Bode plots of T for the op amp circuit of Fig. 8.5.

8.2 STABILITY IN CONSTANT-GBP OP AMP CIRCUITS

Op amps with a constant GBP are said to be *unconditionally stable* because with frequency-independent feedback, or $\sphericalangle\beta = 0$, they are stable for any $\beta \leq 1$ V/V. Since we now have $\sphericalangle T = \sphericalangle(a\beta) = \sphericalangle a$, and $\sphericalangle a(jf_x) \cong -90°$, these circuits enjoy $\phi_m = 180° + \sphericalangle a(jf_x) \cong 180° - 90° = 90°$. Look at Figs. 6.5*b* and 6.7*b* to appreciate the unconditional stability of the noninverting and inverting amplifiers: in both cases the rate of closure is ROC = 20 dB/dec.

As the transition frequency f_t is approached, constant-GBP op amps exhibit additional phase lag due to higher-order poles. Typically, $\sphericalangle a(jf_t) \cong -120°$, so $60° \leq \phi_m \leq 90°$, depending on the value of β. The circuit with the lowest phase margin is the *voltage follower*, for which $\beta = 1$ V/V and $f_x = f_t$. We observe that an op amp that has been stabilized for voltage-follower operation will be stable also as an *inverting integrator*, since the latter has $\beta(jf_x) = 1$ V/V. Look at Fig. 6.25*b* to convince yourself.

Feedback Pole

If the feedback network includes reactive elements, either intentional or parasitic, stability may no longer be unconditional, and suitable measures may have to be taken to raise ϕ_m. Of special concern is the case of a single feedback pole, or

$$\beta(jf) = \frac{\beta_0}{1 + jf/f_p} \tag{8.12}$$

where β_0 is the dc value of the feedback factor. Note that a pole (or a zero) of β becomes a zero (or a pole) for $1/\beta$. Since we are going to be working with $1/\beta$ rather than β, we find it more appropriate to use the symbol f_z instead of f_p. (The reader is cautioned against confusing the two!)

The effect of a feedback pole is illustrated in Fig. 8.7 for the case $f_z \ll \beta_0 f_t$. At $f = f_x$ we have Slope ($|a|$) $\cong -20$ dB/dec and Slope ($|1/\beta|$) $\cong +20$ dB/dec, so ROC $\cong |-20 - (+20)| = 40$ dB/dec. By Eq. (8.9*c*), $\phi_m \cong 0°$, indicating a circuit on the verge of oscillation. We can gain additional insight by examining the error function $1/(1 + 1/T)$. Using the high-frequency approximation $a \cong f_t/jf$ and letting $1/T = (1/a) \times (1/\beta) = (jf/f_t) \times (1 + jf/f_z)/\beta_0$, we get, after straightforward algebra,

$$A(jf) = A_{\text{ideal}} \times \frac{1}{1 - (f/f_x)^2 + (jf/f_x)/Q} \tag{8.13a}$$

$$f_x = \sqrt{f_z \beta_0 f_t} \qquad Q = \sqrt{\beta_0 f_t / f_z} \tag{8.13b}$$

The error function coincides with the second-order low-pass function H_{LP} defined in Eq. (3.44). Its characteristic frequency f_x is visualized in Fig. 8.7 as the *geometric mean* of f_z and $\beta_0 f_t$. We also note that the lower f_z compared to $\beta_0 f_t$, the higher the Q and, hence, the more pronounced the peaking and ringing. We shall now investigate the most common examples of feedback poles, along with suitable stabilization techniques.

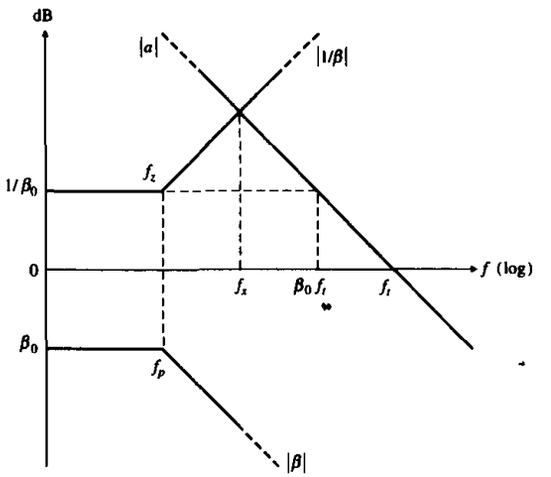


FIGURE 8.7
Illustrating the effect of a pole within the feedback loop of an internally compensated op amp.

The Differentiator Circuit

As we know, the differentiator of Fig. 8.8*a* gives, in the limit $a \to \infty$, $H_{\text{ideal}} = -(jf/f_0)$, where $f_0 = 1/2\pi RC$ is the *unity-gain frequency*. To find the actual transfer function $H(jf)$, we observe that $\beta = Z_C/(Z_C + R)$, $Z_C = 1/j2\pi fC$, where we have assumed $r_d = \infty$ and $r_o = 0$ for simplicity. Expanding gives $\beta(jf) =$

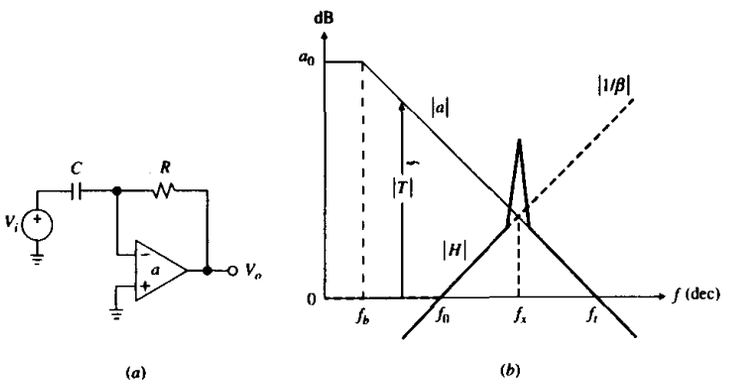


FIGURE 8.8
Uncompensated differentiator.

$1/(1 + jf/f_0)$. Applying Eq. (8.13) to the present case, we get

$$H(jf) = -(jf/f_0) \times H_{LP} \tag{8.14a}$$

$$f_x = \sqrt{f_0 f_t} \qquad Q = \sqrt{f_t/f_0} \tag{8.14b}$$

As depicted in Fig. 8.8*b*, the circuit exhibits an intolerable amount of peaking and is thus on the verge of oscillation.

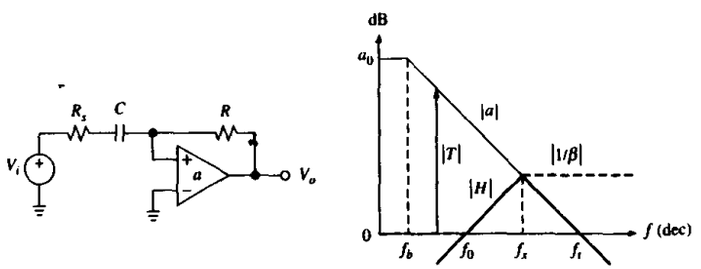
EXAMPLE 8.2. A 741 op amp differentiator has $R = 159\ \text{k}\Omega$ and $C = 10\ \text{nF}$. Find f_x, Q, and ϕ_m.

Solution. We have $f_0 = 1/(2\pi \times 159 \times 10^3 \times 10 \times 10^{-9}) = 10^2$ Hz, $f_x = (100 \times 10^6)^{1/2} = 10$ kHz, $Q = (10^6/10^2)^{1/2} = 100$, $\sphericalangle T(jf_x) = \sphericalangle a(jf_x) - \sphericalangle|1/\beta(jf_x)| = -\tan^{-1}(f_x/f_a) - \tan^{-1}(f_x/f_0) \cong -90° - \tan^{-1}(10^4/10^2) = -179.4°$, $\phi_m = 180° - 179.4° = 0.6°$.

A common way of stabilizing the differentiator is by adding a series resistance R_s as in Fig. 8.9*a*. At low frequencies R_s has little effect because $R_s \ll |Z_C|$. However, at high frequencies, where C acts as a short compared to R_s, the asymptotic value becomes $|1/\beta_\infty| = 1 + R/R_s$, indicating the creation of a break frequency past which the $|1/\beta|$ curve flattens out. If we position this breakpoint right on the $|a|$ curve, as in Fig. 8.9*b*, then we obtain ROC = 30 dB/dec, or $\phi_m = 45°$, by Eq. (8.9*b*). To find the required R_s, impose $1 + R/R_s = |a(jf_x)| = f_t/f_x = \sqrt{f_t/f_0} \gg 1$. This gives

$$R_s \cong R/\sqrt{f_t/f_0} \tag{8.15}$$

Thus, for $\phi_m = 45°$ in Example 8.2, use $R_s \cong 159/\sqrt{10^6/100} = 1.59\ \text{k}\Omega$. If a greater phase margin is desired, the second break frequency can be lowered further, but at the price of further reducing the frequency range of near-ideal differentiator behavior.



(*a*) (*b*)

FIGURE 8.9
Compensated differentiator.

Stray Input Capacitance Compensation

All practical op amps exhibit stray input capacitances. Of special concern is the net capacitance C_n of the inverting input toward ground,

$$C_n = C_d + C_c/2 + C_{ext} \tag{8.16}$$

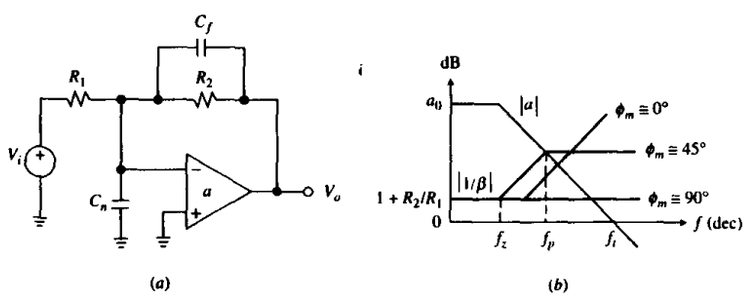
where C_d is the *differential capacitance* between the input pins; $C_c/2$ is the *common-mode capacitance* of each input to ground, so that when the inputs are tied together the net capacitance is the sum of the two; and C_{ext} is the *external parasitic capacitance* of components, leads, sockets, and printed-circuit traces associated with the inverting input node. Typically, each of the above components is on the order of a few picofarads.

As in the case of the differentiator, C_n creates a feedback pole whose phase lag erodes ϕ_m. A common way of counteracting this lag is by using a feedback capacitance C_f to create feedback phase lead. This is illustrated in Fig. 8.10*a* for the inverting case. Assuming $r_d = \infty$ and $r_o = 0$, we have $1/\beta = 1 + Z_2/Z_1$, where $Z_1 = R_1 \parallel (1/j2\pi f C_n)$ and $Z_2 = R_2 \parallel (1/j2\pi f C_f)$. Expanding, we get

$$\frac{1}{\beta} = \left(1 + \frac{R_2}{R_1}\right)\frac{1 + jf/f_z}{1 + jf/f_p} \tag{8.17}$$

where $f_z = 1/[2\pi(R_1 \parallel R_2)(C_n + C_f)]$ and $f_p = 1/2\pi R_2 C_f$.

In the absence of C_f we have $1/\beta = (1 + R_2/R_1)\{1 + jf[2\pi(R_1 \parallel R_2)C_n]\}$, indicating that the $|1/\beta|$ curve bends upward. If its break frequency is located well below the crossover frequency, we have ROC $\cong$ 40 dB/dec, or a circuit on the verge of oscillation. This situation corresponds to the curve $\phi_m \cong 0$ in Fig. 8.10*b*.



(*a*) (*b*)

FIGURE 8.10
Stray input capacitance compensation.

Inserting C_f creates a second breakpoint at f_p beyond which the $|1/\beta|$ flattens out toward the high-frequency asymptote $1/\beta_\infty = 1 + Z_{C_f}/Z_{C_n} = 1 + C_n/C_f$. By properly positioning this second breakpoint we can increase ϕ_m. For $\phi_m \cong 45°$ we place f_p right on the $|a|$ curve, so $f_p = \beta_\infty f_t$. Rewriting as $1/2\pi R_2 C_f = f_t/(1 +$

C_n/C_f) gives

$$C_f = (1 + \sqrt{1 + 8\pi R_2 C_n f_t})/4\pi R_2 f_t \qquad \text{for } \phi_m \cong 45° \tag{8.18a}$$

Alternatively, we can compensate for $\phi_m = 90°$. In this case we place f_p right on top of f_z so as to cause a pole-zero cancellation. This makes the $|1/\beta|$ curve flat throughout, or $1/\beta_\infty = |1/\beta_0|$. Rewriting as $1 + C_n/C_f = 1 + R_2/R_1$ yields

$$C_f = (R_1/R_2)C_n \qquad \text{for } \phi_m = 90° \tag{8.18b}$$

Moreover, the crossover frequency is $\beta_\infty f_t = \beta_0 f_t = f_t/(1 + R_2/R_1)$. This technique, also called *neutral compensation*, is similar to oscilloscope probe compensation.

We observe that the introduction of C_f yields, in the limit $a \to \infty$, $A_{\text{ideal}} = -Z_2/R_1 = (-R_2/R_1)/(1 + jf/f_p)$; that is, A_{ideal} is frequency-dependent with a pole frequency at $f = f_p$. Moreover, the error function $1/(1 + 1/T)$ has a pole frequency at the crossover frequency $\beta_\infty f_t$. Hence, the actual gain $A(jf) = A_{\text{ideal}}/(1 + 1/T)$ has a pole-frequency pair, namely, f_p and $\beta_\infty f_t$.

EXAMPLE 8.3. In Fig. 8.10*a* let $R_1 = R_2 = 30$ kΩ, and $C_{\text{ext}} = 3$ pF. Moreover, let the op amp have GBP = 20 MHz, $C_d = 7$ pF, and $C_c/2 = 6$ pF. (*a*) Find ϕ_m with C_f absent. (*b*) Find C_f for $\phi_m \cong 90°$. (*c*) Find $A(jf)$ after compensation. (*d*) Verify with PSpice.

Solution.

(*a*) We have $1 + R_2/R_1 = 2$, $C_n = 7 + 6 + 3 = 16$ pF, $f_z = 1/(2\pi \times 15 \times 10^3 \times 16 \times 10^{-12}) = 663$ kHz, and $1/\beta = 2[1 + jf/(663\text{ kHz})]$. Using Eq. (8.13*b*) we find $Q = 3.88$, and using Eq. (8.6) we find $\phi_m = 14.7°$—not a very convincing margin.

(*b*) Use $C_f = (30/30)16 = 16$ pF.

(*c*) We have $f_p = 1/2\pi R_2 C_f = 332$ kHz and $\beta_\infty f_t = (1/2)20 = 10$ MHz, so

$$A(jf) = \frac{-1}{[1 + jf/(332\text{ kHz})][1 + jf/(10\text{ MHz})]}\ \text{V/V}$$

(*d*) With reference to Fig. 8.11, we write the following file.

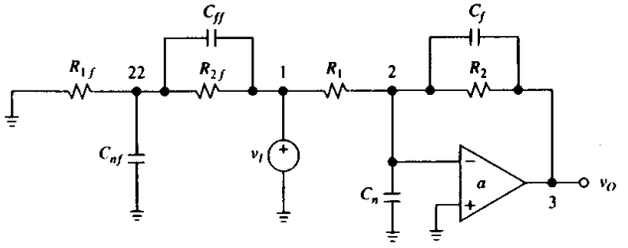


FIGURE 8.11
PSpice circuit of Example 8.3.


```
Stray input capacitance compensation:
vI 1 0 ac 1V pulse (0 1V 0 1ns 1ns 4us 8us)
R1 1 2 30k
Cn 2 0 16pF
R2 2 3 30k
Cf 2 3 16pF
ea0 5 0 0 2 1Meg ;a0 = 1 V/uV
Req 5 6 1Meg
Ceq 6 0 7.958nF ;fb = 20 Hz
eout 3 0 6 0 1 ;output buffer
*Circuit to plot 1/beta:
R2f 1 22 30k
Cff 1 22 16pF
R1f 22 0 30k
Cnf 22 0 16pF
.ac dec 50 100kHz 100MegHz
.tran 10ns 4us 0ns 10ns
.probe ;a=V(3)/V(0,2), 1/beta=V(1)/V(22), A=V(3)/V(1); vO(t)=v(3)
.end
```

The results of the simulation, shown in Fig. 8.12, confirm the stabilizing effect of C_f as well as the closed-loop pole frequencies of 332 kHz and 10 MHz.

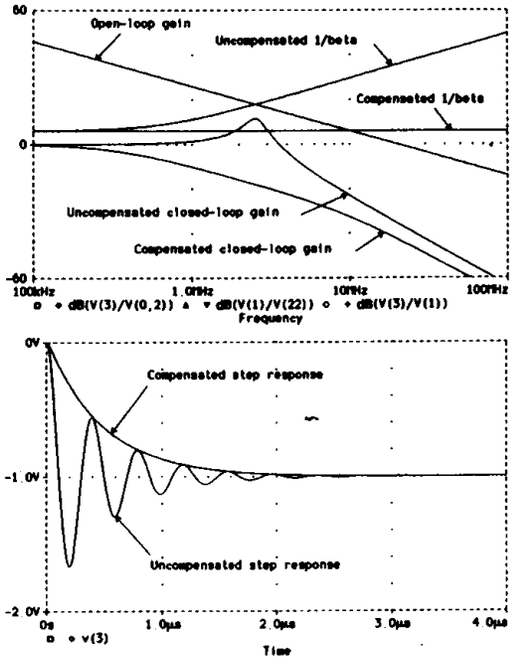


FIGURE 8.12
Frequency and transient responses of the circuit of Fig. 8.11.

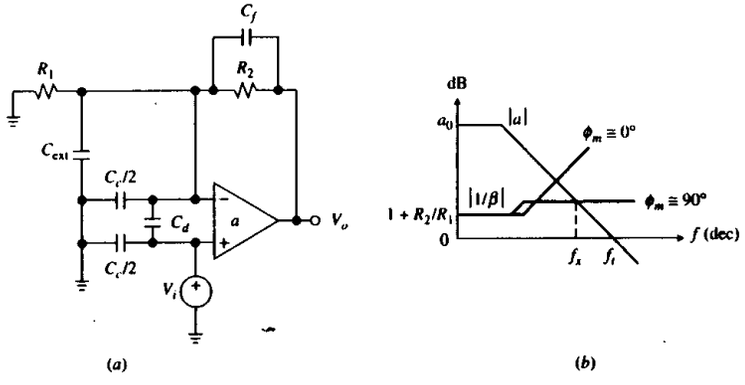


FIGURE 8.13
Stray input capacitance compensation for the noninverting configuration.

We now turn to the noninverting configuration[4] of Fig. 8.13*a*, where the various stray input capacitances have been shown explicitly. We observe that the overall capacitance C_n is still given by Eq. (8.16). However, the portion $C_1 = C_c/2 + C_{ext}$ is now in parallel with R_1, so we have $A_{ideal} = 1 + Z_2/Z_1$, $Z_1 = R_1 \parallel (1/j2\pi f C_1)$, $Z_2 = R_2 \parallel (1/j2\pi f C_f)$. We can make A_{ideal} frequency-independent by using

$$C_f = (R_1/R_2)(C_c/2 + C_{ext}) \tag{8.19}$$

The effect of C_f is shown in Fig. 8.13*b*. The actual gain is now $A(jf) \cong (1 + R_2/R_1)/(1 + jf/f_x)$, $f_x = \beta_\infty f_t = f_t/(1 + C_n/C_f)$.

EXAMPLE 8.4. Stabilize the circuit of Fig. 8.13*a* if the data are the same as in Example 8.3. Hence, find $A(jf)$.

Solution. We have $C_f = (30/30)(6 + 3) = 9$ pF, $f_x = 10^7/(1 + 16/9) = 7.2$ MHz, and

$$A(jf) \cong \frac{2}{1 + jf/(7.2\text{ MHz})} \text{ V/V}$$

With careful component layout and wiring, C_{ext} can be minimized but not altogether eliminated. Consequently, it is always a good practice to include a small feedback capacitance C_f in the range of a few picofarads to combat the effect of C_n as given in Eq. (8.16).

Capacitive-Load Isolation

There are applications in which the external load is heavily capacitive. Sample-and-hold amplifiers and peak detectors are typical examples. When an op amp drives a coaxial cable, it is the distributed cable capacitance that makes the load capacitive. Capacitive loading is shown in Fig. 8.14*a*, which pertains to both the inverting and the noninverting amplifier: for the former we lift node A off ground and apply the input source there, and for the latter we lift B and use it as the input node.

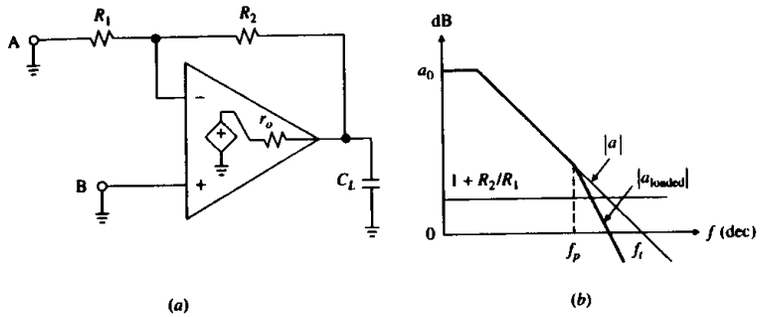


FIGURE 8.14
Capacitive loading.

The capacitance C_L forms a pole with the open-loop output resistance r_o. Ignoring loading by the feedback network, the loaded gain can be expressed as

$$a_{loaded} \cong a \frac{1}{1 + jf/f_p}$$

where $f_p = 1/2\pi r_o C_L$. As shown in Fig. 8.14*b*, the effect of the pole is to increase the ROC and thus invite instability. Looked at from another viewpoint, C_L will tend to resonate with the equivalent inductance L_{eq} of the closed-loop output impedance Z_o investigated in Section 6.3. Hence, intolerable peaking and ringing may ensue.

The popular cure depicted in Fig. 8.15 uses a small series resistance R_s to decouple the amplifier output from C_L, and a small feedback capacitance C_f to provide a high-frequency bypass around C_L as well as to combat the effect of any stray input capacitance C_n. It is possible to specify the compensation network so that the phase lead introduced by C_f exactly neutralizes the phase lag due to C_L. The design equations for neutral compensation are[5]

$$R_s = (R_1/R_2)r_o \qquad C_f = (1 + R_1/R_2)^2 (r_o/R_2) C_L \tag{8.20a}$$

and the closed-loop bandwidth is $f_B \cong 1/2\pi R_2 C_f$. In the case of voltage-follower

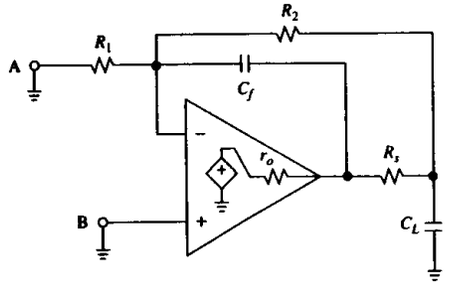


FIGURE 8.15
Stabilizing a capacitively loaded op amp circuit.

operation, where $R_1 = \infty$ and $R_2 = 0$, a convenient alternative is provided by the design equations[6]

$$R_s = 30r_o \qquad C_f = \sqrt{C_L/18\pi r_o \beta f_t} \tag{8.20b}$$

where f_t is the transition frequency of the op amp and $\beta = 1$ V/V for the voltage follower. The closed-loop bandwidth is now $f_B \cong \sqrt{\beta f_t/18\pi r_o C_L}$.

EXAMPLE 8.5. (*a*) Assuming the op amp of Fig. 8.14*a* has GBP = 10 MHz and $r_o = 100\,\Omega$, specify component values for operation as an inverting amplifier with $A_0 = -2$ V/V and $C_L = 5$ nF. (*b*) Find $A(jf)$.

Solution.

(*a*) For $A_0 = -2$ V/V, use $R_1 = 10\,\text{k}\Omega$ and $R_2 = 20\,\text{k}\Omega$, and insert the input source at node *A*. Then, Eq. (8.20*a*) yields $R_s = 50\,\Omega$ and $C_f \cong 56$ pF.

(*b*) We have $f_{-3\text{dB}} = 1/2\pi R_2 C_f \cong 140$ kHz. An additional breakpoint occurs at $f_x = \beta \times \text{GBP} = (1/3)10^7 = 3.33$ MHz. Consequently,

$$A(jf) = \frac{-2}{[1 + jf/(140 \times 10^3)][1 + jf/(3.33 \times 10^6)]} \text{ V/V}$$

We observe that since R_s is inside the feedback loop, its presence does not degrade dc accuracy appreciably. However, R_s should be kept suitably small to avoid excessive output-swing reduction and excessive slew-rate degradation. In a practical op amp the open-loop output impedance tends to behave inductively at high frequencies, so the above equations provide only initial estimates for R_s and C_f. The optimum values must be found empirically once the circuit has been assembled in the lab.[6]

An alternative way of stabilizing a capacitively loaded amplifier is via the input-lag method, to be discussed in Section 8.4. The need to drive capacitive loads arises frequently enough to warrant the design of special op amps with provisions for automatic capacitive-load compensation. The AD817 (Analog Devices) and LT1360 (Linear Technology) op amps are designed to drive unlimited capacitive loads. Special internal circuitry senses the amount of loading and adjusts the open-loop response to maintain an adequate phase margin regardless of the load. The process, completely transparent to the user, is most effective when the load is not fixed or is ill-defined, as in the case of unterminated coaxial cable loads.

Other Sources of Instability

In circuitry incorporating high-gain amplifiers such as op amps and voltage comparators, the specter of instability arises in a number of subtle ways unless proper circuit design and construction rules are followed.[7–10] Two common causes of instability are *poor grounding* and *inadequate power-supply filtering*. Both problems stem from the distributed impedances of the supply and ground busses, which can provide spurious feedback paths around the high-gain device and compromise its stability.

In general, to minimize the ground-bus impedance, it is good practice to use a ground plane, especially in audio and wideband applications. To reduce grounding problems further, it is good practice to provide two separate ground busses: a *signal-ground* bus to provide a return path for critical circuits—such as signal sources, feedback networks, and precision voltage references—and a *power-ground* bus to provide a return path for less critical circuits, such as high-current loads and digital circuits. Every effort is made to keep both dc and ac currents on the signal-ground bus *small* in order to render this bus essentially equipotential. To avoid perturbing this equipotential condition, the two busses are joined only at one point of the circuit.

Spurious feedback paths can also form through the power-supply busses. Because of nonzero bus impedances, any change in supply currents brought about by a load current change will induce a corresponding voltage change across the op amp supply pins. Due to finite PSRR, this change will in turn be felt at the input, thus providing an indirect feedback path. To break this path, each supply voltage must be bypassed with a 0.01-μF to 0.1-μF decoupling capacitor, in the manner already depicted in Fig. 1.36. The best results are obtained with low ESR and ESL ceramic chip capacitors, preferably surface-mounted. For this cure to be effective, the lead lengths must be kept short and the capacitors must be mounted as close as possible to the op amp pins. Likewise, the elements of the feedback network must be mounted close to the inverting-input pin in order to minimize the stray capacitance C_{ext} in Eq. (8.16). Manufacturers often provide evaluation boards to guide the user in the proper construction of the circuit.

8.3 INTERNAL FREQUENCY COMPENSATION

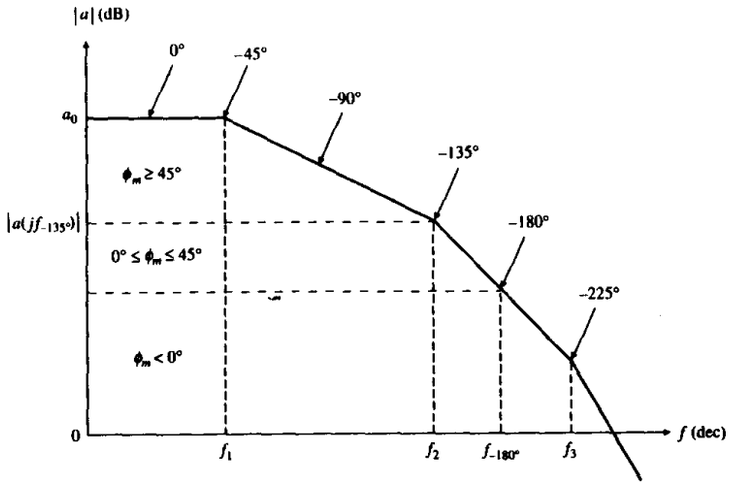
If we were to remove the 30-pF capacitor from the 741 op amp, we would end up with an uncompensated device. Such a device has indeed been marketed as the 748 op amp for those users who prefer custom compensation. Another highly popular uncompensated contemporary is the 301 op amp.

With the low-frequency dominant pole removed, an uncompensated op amp exhibits much higher bandwidth, but also much greater phase shift due to various high-frequency poles and zeros. Such a device is unstable in most applications, so efforts must be made to stabilize it. The overall response of an uncompensated op amp is the result of its individual internal-stage responses, and can be rather complex. For illustration purposes, however, the following three-pole approximation is generally satisfactory,

$$a(jf) = \frac{a_0}{(1 + jf/f_1)(1 + jf/f_2)(1 + jf/f_3)} \tag{8.21}$$

The magnitude plot of Fig. 8.16 (top) shows also important phase values, which have been associated with slope using Eq. (8.7). Note that GBP is constant only for $f_1 < f < f_2$.

Suppose we apply *frequency-independent feedback* around such an op amp. With this type of feedback the $1/\beta$ curve is flat, so we can visualize the $|T|$ curve as the $|a|$ curve, but with the $|1/\beta|$ line as the new 0-dB axis. As long as $1/\beta \geq |a(jf_{-135°})|$, the rate of closure is ROC $\leq$ 30 dB/dec, indicating a phase margin $\phi_m \geq 45°$. For $|a(jf_{-135°})| \geq 1/\beta \geq |a(jf_{-180°})|$ we have 30 dB/dec $\leq$ ROC $\leq$ 40 dB/dec, or



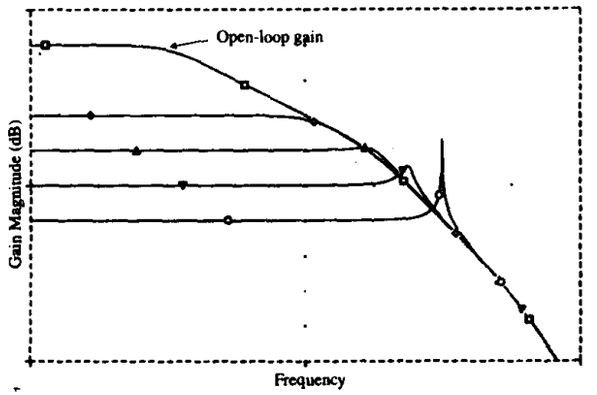


FIGURE 8.16
A three-pole open-loop response, showing a correspondence between phase shift and slope.

$45° \geq \phi_m \geq 0°$, indicating an inadequate degree of stability. Finally, for $1/\beta \leq |a(jf_{-180°})|$ we have ROC $\geq$ 40 dB/dec, or $\phi_m < 0$, indicating oscillatory behavior. Figure 8.16 (bottom) illustrates how peaking increases as we reduce $1/\beta$.

It is apparent that uncompensated op amps provide adequate phase margins only in high-gain applications. For instance, we must have $1/\beta \geq |a(jf_{-135°})|$ for $\phi_m \geq 45°$. To accommodate lower closed-loop gains, frequency compensation is needed. This is achieved by modifying either the open-loop response $a(jf)$ (internal compensation), or the feedback factor $\beta(jf)$ (external compensation), or a combination of both, as in decompensated amplifiers (see Section 8.4).

EXAMPLE 8.6. The μA702, the first monolithic op amp, had[11] $a_0 = 3600$ V/V, $f_1 = 1$ MHz, $f_2 = 4$ MHz, and $f_3 = 40$ MHz. Find (*a*) $|a(jf_{-135°})|$, and (*b*) $|a(jf_{-180°})|$.

Solution.

(*a*) Start out with the estimate $f_{-135°} = 4$ MHz. Then, use the trial-and-error technique of Example 8.1 to find $f_{-135°} = 4.78$ MHz, and $|a(jf_{-135°})| \cong 470$ V/V. An uncompensated 702 circuit is stable with $\phi_m = 45°$ only for $|1/\beta| \geq 470$ V/V.

(*b*) Similarly, $|a(jf_{-180°})| = |a(j14.3 \text{ MHz})| = 63.7$ V/V, indicating that for $|1/\beta| \leq 63.7$ V/V the circuit oscillates.

Figure 8.17 shows a three-pole op amp model that we shall use as the basis of our discussion as well as PSpice simulations.

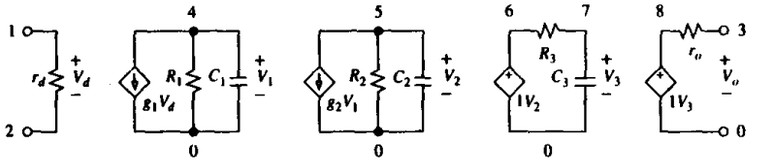


FIGURE 8.17
Three-pole op amp model, consisting of two transconductance stages and a voltage buffer.

Dominant-Pole Compensation

The objective of this method is the deliberate creation of a pole at a sufficiently low frequency f_d to ensure a rolloff rate of -20 dB/dec all the way up to the crossover frequency f_x. Figure 8.18 provides a graphical means for finding f_d. First, we draw the $|1/\beta|$ curve corresponding to the required closed-loop gain. Next, we locate point X corresponding to the desired f_x. For $\phi_m = 45°$, let $f_x = f_1$. From X we draw a line with a slope of -20 dB/dec until it intercepts the dc gain asymptote at point D.

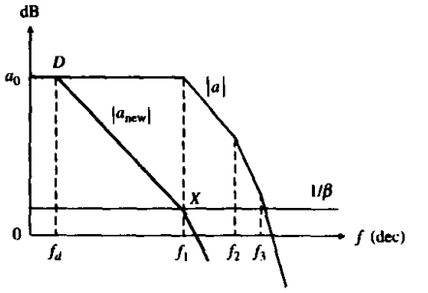


FIGURE 8.18
Dominant-pole compensation.

The abscissa of D is f_d. By the constancy of the GBP we have $a_0 f_d = (1/\beta) f_x$, or

$$f_d = \frac{f_x}{\beta a_0} \tag{8.22}$$

It is apparent that dominant-pole compensation causes a drastic gain reduction above f_d. But, this is the price we are paying for stability!

EXAMPLE 8.7. Find f_d to make the μA702 op amp of Example 8.6 unconditionally stable with $\phi_m = 45°$.

Solution. After creating the new pole frequency we have

$$a_{new}(jf) = \frac{1}{1 + jf/f_d} a(jf)$$

with $a(jf)$ as in Eq. (8.21). For $\phi_m = 45°$ we want $\sphericalangle a_{new}(jf_x) = -135°$. But, $\sphericalangle a_{new}(jf_x) = -\tan^{-1}(f_x/f_d) + \sphericalangle a(jf_x)$, or $-135° \cong -90° + \sphericalangle a(jf_x)$, indicating that we need $\sphericalangle a(jf_x) = -45°$. By trial and error we find that $\sphericalangle a = -45°$ at $f = 683$ kHz, where $|a| = 2930$ V/V. Imposing $1 = 2930/\sqrt{1 + (683 \times 10^3/f_d)^2}$ gives $f_d = 233$ Hz.

Shunt-Capacitance Compensation

The above discussion assumes that a fourth pole is added to the open-loop response, and that the existing poles are unaffected by this procedure. For the purpose of maximizing bandwidth, it is more efficient to rearrange the existing poles rather than create a new one. Specifically, if we decrease f_1 until f_x coincides with f_2, as in Fig. 8.19*b*, then the open-loop bandwidth will be improved by the factor f_2/f_1 compared to Fig. 8.18. A pole frequency is decreased by adding capacitance to the internal node causing it. Referring to Fig. 8.17, we observe that the equivalent resistance and capacitance of node V_1 form a low-pass function with the pole frequency $f_1 = 1/2\pi R_1 C_1$. If we deliberately add an external capacitance C_c as shown for the first-stage model of Fig. 8.19*a*, then f_1 is changed to $f_{1(new)} = 1/2\pi R_1 (C_1 + C_c)$.

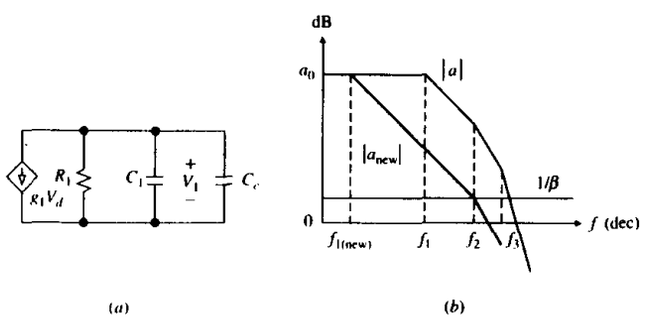


FIGURE 8.19
Dominant-pole compensation using a shunt capacitance C_c.

Rewriting Eq. (8.22) as $f_{1(new)} = f_2/\beta a_0$ gives, for $f_{1(new)} \ll f_1$,

$$C_c \cong \frac{\beta a_0}{2\pi R_1 f_2} \tag{8.23}$$

If the 741 op amp of Fig. 5.1 were not already compensated, a proper place to connect the shunt capacitance would be between the base of Q_5 and the negative-supply rail. Note that adding shunt capacitance to a node usually affects also the other pole frequencies,[11] a feature not explicitly conveyed by the simplified model of Fig. 8.17. Consequently, it may be necessary to calculate or measure the new value of f_2 and perform a few iterations to find the correct value of C_c.

EXAMPLE 8.8. In the op amp model of Fig. 8.17 let $r_d = 1$ MΩ, $g_1 = 2$ mA/V, $R_1 = 100$ kΩ, $g_2 = 10$ mA/V, $R_2 = 50$ kΩ, and $r_0 = 100$ Ω. (*a*) If the open-loop response has three pole frequencies at $f_1 = 100$ kHz, $f_2 = 1$ MHz, and $f_3 = 10$ MHz, find the dominant pole f_d and shunt capacitance C_c needed for operation as a voltage follower with $\phi_m = 45°$. (*b*) Repeat, but for operation as a unity-gain inverting amplifier.

Solution.

(*a*) By inspection, $a_0 = g_1 R_1 g_2 R_2 = 10^5$ V/V, and $C_1 = 1/2\pi R_1 f_1 = 15.9$ pF. For $\beta = 1$ V/V we get $f_{1(new)} = f_2/\beta a_0 = 10$ Hz and $C_c = 159$ nF.
(*b*) Now $\beta = 0.5$ V/V, so $f_{1(new)} = 20$ Hz and $C_c = 79.6$ nF.

Miller Compensation

Given the low-frequency nature of the dominant pole, the value of the shunt capacitance C_c tends to be too large for monolithic fabrication. As mentioned in Chapters 5 and 6, this drawback is overcome by placing C_c in the feedback path of one of the internal stages to take advantage of the multiplicative action of the Miller effect for capacitance. Luckily, another unexpected benefit accrues from this connection, namely, *pole splitting*.[11,12]

In Fig. 8.20*a*, C_c has been placed in the feedback path of the second stage, which, for the 741 op amp, is the Darlington stage depicted in Fig. 5.1. In the absence of C_c,

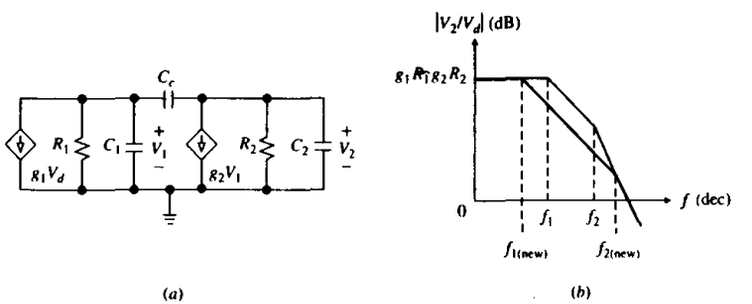


FIGURE 8.20
Miller compensation and pole splitting.

the circuit provides the pole frequency $f_1 = 1/2\pi R_1 C_1$ at the input, and the pole frequency $f_2 = 1/2\pi R_2 C_2$ at the output. With C_c present, a detailed ac analysis[12] (see Problem 8.30) yields

$$\frac{V_2}{V_d} \cong g_1 R_1 g_2 R_2 \frac{1 - jf/f_z}{(1 + jf/f_{1(\text{new})})(1 + jf/f_{2(\text{new})})} \tag{8.24}$$

where $f_z = g_2/2\pi C_c$, and

$$f_{1(\text{new})} \cong \frac{1}{2\pi R_1 g_2 R_2 C_c} \qquad f_{2(\text{new})} \cong \frac{g_2 C_c}{2\pi(C_1 C_2 + C_c C_1 + C_c C_2)} \tag{8.25}$$

Equation (8.24) reveals the presence of a *positive* real zero at $s = 2\pi f_z$, thus providing an example of a circuit that is not a minimum-phase system. This zero stems from direct signal transmission through C_c to the output, and its effect is to reduce ϕ_m. However, in bipolar op amps f_z is usually high enough to warrant approximating $1 - jf/f_z \cong 1$ over the useful frequency range.

Equation (8.25) indicates that increasing C_c lowers $f_{1(\text{new})}$ and raises $f_{2(\text{new})}$, causing the poles to split apart. *Pole splitting*, depicted in Fig. 8.20*b*, is highly beneficial since the shift in f_2 eases the amount of shift required of f_1, thus allowing for a wider bandwidth. We also note that the dominant-pole frequency is due to the familiar Miller-multiplied capacitance $g_2 R_2 C_c$, which combines with the input node resistance R_1 to form $f_{1(\text{new})}$.

EXAMPLE 8.9. Repeat (*a*) and (*b*) of Example 8.8, but using a feedback capacitance C_c. (*c*) Use PSpice to compare the two compensations for the voltage-follower case.

Solution.

(*a*) $C_1 = 15.9$ pF, $C_2 = 1/2\pi R_2 f_2 = 3.18$ pF. To find $f_{1(\text{new})}$ we need to know $f_{2(\text{new})}$. Assume $C_c \gg C_2$, so we can estimate $f_{2(\text{new})} \cong g_2/[2\pi(C_1 + C_2)] \cong 83$ MHz. Since this is much higher than f_3, which is 10 MHz, we impose $f_x = f_3 = 10$ MHz for $\phi_m \cong 45°$. Then, $f_{1(\text{new})} = f_3/\beta a_0 = 100$ Hz, which gives $C_c = 1/2\pi R_1 g_2 R_2 f_{1(\text{new})} = 31.8$ pF. By Eq. (8.25), $f_{2(\text{new})} \cong 77$ MHz; moreover, $f_z = g_2/2\pi C_c = 50$ MHz, confirming that both f_z and $f_{2(\text{new})}$ are well above f_x. It can be shown (see Problem 8.31) that the actual values of f_x and ϕ_m are 7.9 MHz and 36.7°.

(*b*) Now $\beta = 0.5$ V/V, so $f_{1(\text{new})} = 200$ Hz, $C_c = 15.9$ pF, and $f_{2(\text{new})} \cong 71$ MHz.

(*c*) Referring to Fig. 8.17, we write the following circuit file for the uncompensated device.

```
Dominant-pole compensation:
*a0 = 100 V/mV, f1 = 100 kHz, f2 = 1 MHz, f3 = 10 MHz
rd 1 2 1Meg
g1 4 0 1 2 2m
R1 4 0 100k
C1 4 0 15.92pF
g2 5 0 4 0 10m
R2 5 0 50k
C2 5 0 3.183pF
e3 6 0 5 0 1
R3 6 7 10k
C3 7 0 1.592pF
```



```
eO 8 0 7 0 1
ro 8 3 100
vi 1 0 ac 1 pulse (0 1V 0 10ns 10ns 2us 4us)
Rf 2 3 1k
.ac dec 10 1Hz 100MegHz
.tran 0.1us 2us
.probe ;a = V(3)/V(1,2), vO(t) = v(3)
.end
```

To compensate with a shunt capacitance C_c we add the statement

```
Cc 4 0 159nF
```

whereas to compensate with a feedback capacitance C_c we add

```
Cc 4 5 31.8pF
```

The results of the simulation are shown in Fig. 8.21.

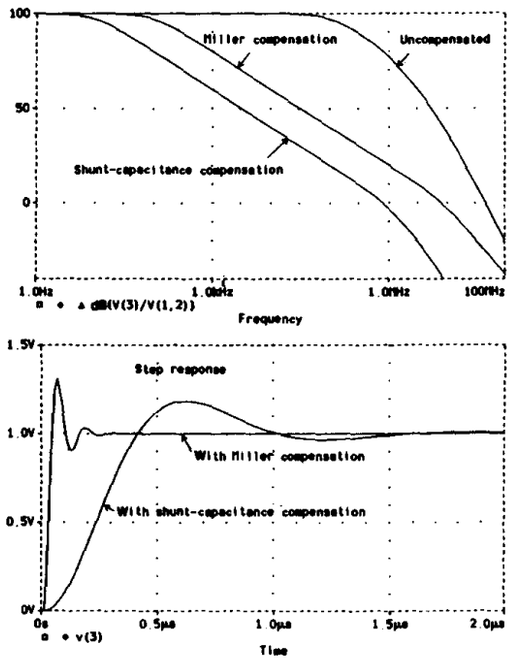


FIGURE 8.21
Frequency and transient responses for Example 8.9.

Unconditionally stable op amps are compensated for $\beta = 1$ V/V. Since this requires the lowest dominant-pole value and, hence, the largest C_c, these op amps are of necessity compensated conservatively. When used with $\beta < 1$ V/V, they tend to be wasteful in terms of bandwidth and slew rate since a smaller value of C_c would suffice. Custom compensation may then prove a better alternative.

Pole-Zero Compensation

An alternative dominant-pole compensation technique is *pole-zero cancellation*. This technique, shown for the first-stage model of Fig. 8.22*a*, uses a capacitance $C_c \gg C_1$ to significantly lower the first-pole frequency f_1, and a resistance $R_c \ll R_1$ to create a zero frequency that is used to cancel the second-pole frequency f_2. The compensated response is then dominated by the lowered first-pole frequency up to f_3, which, for $\phi_m = 45°$, becomes the new crossover frequency. To see how this comes about, note that the transfer function is now $V_1/V_d = -g_1[R_1 \| (1/j2\pi f C_1) \| (R_c + 1/j2\pi f C_c)]$. After expanding (see Problem 8.33), we get, for $C_c \gg C_1$ and $R_c \ll R_1$,

$$\frac{V_1}{V_d} \cong (-g_1 R_1) \frac{1 + jf/f_z}{(1 + jf/f_{1(\text{new})})(1 + jf/f_4)} \tag{8.26}$$

$$f_{1(\text{new})} \cong \frac{1}{2\pi R_1 C_c} \qquad f_z = \frac{1}{2\pi R_c C_c} \qquad f_4 \cong \frac{1}{2\pi R_c C_1} \tag{8.27}$$

In the absence of R_c and C_c we have $V_1/V_d = 1/(1 + jf/f_1)$, $f_1 = 1/2\pi R_1 C_1$. Inserting R_c and C_c lowers the first-pole frequency to $f_{1(\text{new})} \ll f_1$, creates a zero frequency at $f_z \gg f_{1(\text{new})}$, and creates an additional pole frequency at $f_4 \gg f_z$. If we specify the compensation network so that $f_z = f_2$, then we have a zero-pole cancellation and Eq. (8.21) becomes

$$a_{\text{new}}(jf) = \frac{a_0}{(1 + jf/f_{1(\text{new})})(1 + jf/f_3)(1 + jf/f_4)}$$

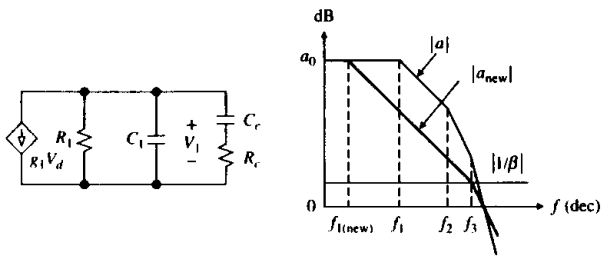


FIGURE 8.22
Pole-zero compensation.

For $\phi_m = 45°$ we let $f_x = f_3$. Then, rewriting Eq. (8.22) as $f_{1(\text{new})} = f_3/\beta a_0$, and noting that $f_{1(\text{new})} \ll f_1 < f_2$, we get

$$C_c \cong \frac{\beta a_0}{2\pi R_1 f_3} \tag{8.28a}$$

Moreover, imposing $f_z = f_2$ yields

$$R_c = 1/2\pi C_c f_2 \tag{8.28b}$$

Comparing Eq. (8.28*a*) with Eq. (8.23) reveals a bandwidth improvement by the factor f_3/f_2 with respect to the shunt-capacitance method.

EXAMPLE 8.10. Use the pole-zero method to compensate the op amp of Example 8.8 for $\phi_m = 45°$ and $\beta = 1$.

Solution. $C_c = 10^5/(2\pi \times 10^5 \times 10^7) = 15.9$ nF, $R_c = 1/(2\pi \times 15.9 \times 10^{-9} \times 10^6) = 10\ \Omega$. Note, incidentally, that $f_4 \cong 1$ GHz, thus justifying our choice of f_3 as the crossover frequency.

Feedforward Compensation

In a multistage amplifier the overall phase shift at f_x is the result of its individual-stage phase contributions. Usually there is one stage that acts as a bandwidth bottleneck by contributing a substantial amount of phase shift. Feedforward compensation creates a high-frequency bypass around this bottleneck stage to suppress its phase contribution in the vicinity of f_x and thus increase the phase margin.

The principle is illustrated in Fig. 8.23*a*, where the overall gain a of the uncompensated amplifier is expressed as the product of the gain a_1 of the bottleneck stage and the gain a_2 of the remaining stages lumped together. The bypass around

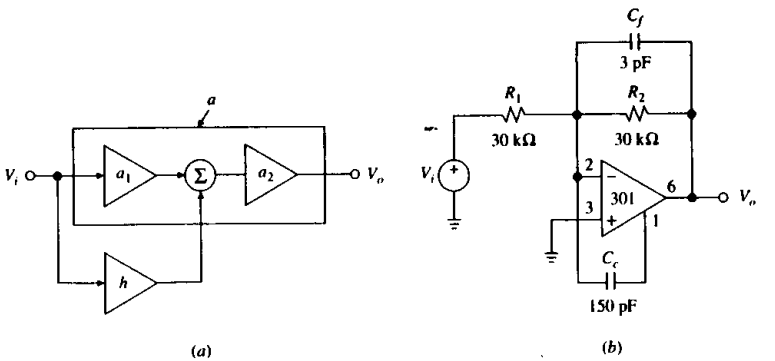


FIGURE 8.23
Feedforward compensation and implementation example.

the bottleneck stage is a high-pass function of the type

$$h(jf) = \frac{jf/f_0}{1 + jf/f_0}$$

so that

$$a_{new}(jf) = [a_1(jf) + h(jf)]a_2(jf)$$

At low frequencies, where $|h| \ll |a_1|$, we have $a_{new} \cong a_1 a_2 = a$, indicating that the high-gain advantages of the uncompensated response still hold there. However, at high frequencies, where $|a_1| \ll |h|$, we now have $a_{new} \cong a_2$, indicating a wider bandwidth as well as a lower phase shift because the dynamics are now controlled by a_2 alone.

Problems may arise[1,13] in the frequency region where a_{new} makes its transition from $a_1 a_2$ to a_2. If $\sphericalangle a_{new}$ approaches $-180°$ before the transition, excessive ringing may develop. Furthermore, a phase shift of $-180°$ at the transition causes signal cancellation at the summing node, thus creating a notch in the compensated response.

Feedforward compensation is implemented with a capacitive bypass around the bottleneck stage. This is shown in Fig. 8.22*b* for the case of the 301 op amp.[14] In this device the bandwidth bottleneck is the input stage because of the presence of lateral *pnp* transistors, whose frequency characteristics are notoriously poor. Connecting C_c between the inverting input (pin 2) and the input to the second stage (pin 1) bypasses the input stage by creating a high-pass function with $f_0 = 1/2\pi R_{eq} C_c$, where R_{eq} is the equivalent resistance seen by C_c.

Since only signals at the inverting input are transmitted to the second stage, feedforward compensation provides a much lower bandwidth for signals applied to the noninverting input. Consequently, this compensation is worthwhile only in inverting applications. Note also the presence of the feedback capacitance C_f to combat the effect of stray capacitance at the inverting input.

8.4 EXTERNAL FREQUENCY COMPENSATION

In this section we examine compensation techniques that stabilize a circuit by modifying its feedback factor $\beta(jf)$.

Reducing the Loop Gain

This method[1] shifts the $|1/\beta|$ curve upward until it intercepts the $|a|$ curve at $f = f_{-135}$, where $\phi_m = 45°$ (or further up for $\phi_m > 45°$). This shift is obtained by connecting a resistance R_c across the inputs, as in Fig. 8.24*a*. The circuit shown can be either an inverting or a noninverting amplifier, depending on whether we insert the input source at node A or B.

Assuming $r_d = \infty$ and $r_o = 0$ for simplicity, it is readily seen that

$$\frac{1}{\beta} = 1 + \frac{R_2}{(R_1 \parallel R_c)} = 1 + \frac{R_2}{R_1} + \frac{R_2}{R_c} \tag{8.29}$$

By choosing R_c suitably small, we can move the $1/\beta$ curve up until $1/\beta = |a(jf_2)|$,

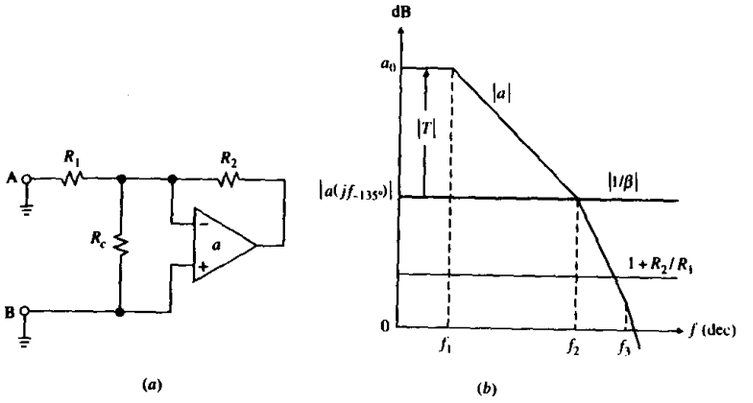


FIGURE 8.24
Frequency compensation via loop-gain reduction.

where $\phi_m = 45°$. This is shown in Fig. 8.24*b*. Solving for R_c yields

$$R_c = \frac{R_2}{|a(jf_2)| - (1 + R_2/R_1)} \tag{8.30}$$

If $\phi_m \neq 45°$ is desired, then replace f_2 with $f_{\phi_m - 180°}$, where ϕ_m is the desired phase margin, and $f_{\phi_m - 180°}$ is the frequency at which $\sphericalangle a = \phi_m - 180°$.

It should be pointed out that the presence of R_c does not affect A_{ideal} in the relation $A = A_{ideal}/(1 + 1/T)$; R_c only reduces T, resulting in a larger gain error. Moreover, the much increased dc noise gain may result in an intolerable dc output error E_O. Again, these are the prices we are paying for stability!

EXAMPLE 8.11. An op amp with $a_0 = 10^5$ V/V, $f_1 = 10$ kHz, $f_2 = 3$ MHz, and $f_3 = 30$ MHz is to be used as an inverting amplifier with $R_1 = 10\,k\Omega$ and $R_2 = 100\,k\Omega$. Find (*a*) R_c for $\phi_m \cong 45°$, (*b*) the dc gain error, (*c*) the dc output error E_O if the total input dc error is $E_I = 1$ mV, and (*d*) the closed-loop -3-dB frequency.

Solution.

(*a*) We calculate $|a(jf_2)| = 234.5$ V/V. Then, Eq. (8.30) gives $R_c = 447.4\,\Omega$ (use $430\,\Omega$).
(*b*) Letting $R_c = 430\,\Omega$ in Eq. (8.29) gives $1/\beta \cong 244$ V/V. Then, $a_0\beta = 10^5/244 \cong 410$, indicating a dc gain error $\epsilon_0 \cong -100/a_0\beta = -0.24\%$.
(*c*) $E_O = (1/\beta)E_I = 244 \times 1 = 244$ mV, quite an error!
(*d*) $f_{-3\,dB} = f_2 = 3$ MHz.

Input-Lag Compensation

The high dc noise-gain drawback of the previous method is overcome[1] by placing a capacitance C_c in series with R_c, as in Fig. 8.25*a*. At high frequencies, where C_c acts as a short compared to R_c, the $|1/\beta|$ curve is unchanged compared to

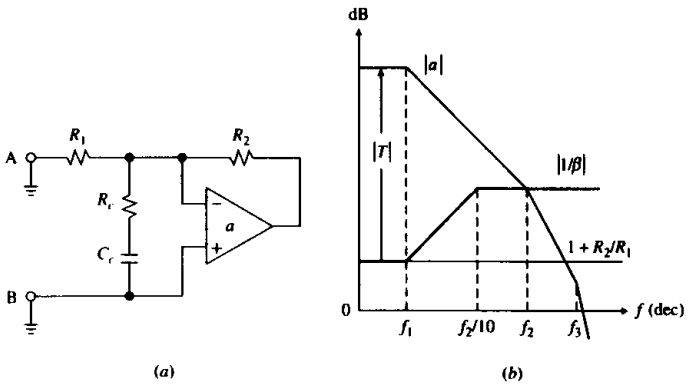


FIGURE 8.25
Input-lag compensation.

Eq. (8.29). However, at low frequencies, where C_c acts as an open, we now have $|1/\beta_0| = 1 + R_2/R_1$. Since this is much lower than the high-frequency value, we now have a much higher dc loop gain and a much lower dc output error.

To avoid degrading ϕ_m, it is good practice[1] to position the second breakpoint of the $|1/\beta|$ curve about a decade below f_2. To find the required value of C_c, we observe that at this breakpoint we have $|Z_{C_c}| = R_c$, or $1/(2\pi C_c f_2/10) = R_c$. Solving gives

$$C_c = \frac{5}{\pi R_c f_2} \tag{8.31}$$

where R_c is given in Eq. (8.30). Again, if $\phi_m \neq 45°$ is desired, replace f_2 with $f_{\phi_m - 180°}$.

EXAMPLE 8.12. (*a*)–(*d*) Repeat Example 8.11, but using input-lag compensation. (*e*) Estimate the actual value of ϕ_m after compensation. (*f*) Confirm with PSpice.

Solution.

(*a*) We have $R_c = 447.4\ \Omega$ (use 430 Ω) and $C_c = 5/(\pi 447.4 \times 3 \times 10^6) = 1.186$ nF (use 1.2 nF).
(*b*) The dc noise gain is now $1/\beta_0 = 1 + R_2/R_1 = 11$ V/V, and $a_0\beta_0 = 10^5/11 = 9091$. Hence, $\epsilon_0 \cong -100/9091 = -0.011\%$.
(*c*) $E_0 = 11E_I = 11$ mV—quite an improvement!
(*d*) $f_{-3\,\text{dB}} = 3$ MHz, as before.
(*e*) As we approach the crossover frequency, $1/\beta$ behaves like a high-pass function, so $1/\beta(jf) \cong 244(jf/0.1f_2)/(1 + jf/0.1f_2)$, with $0.1f_2 = 300$ kHz. The loop gain $T = a\beta$ is then

$$T = \frac{410[1 + jf/(3 \times 10^5)]}{[1 + jf/10^4][1 + jf/(3 \times 10^6)][1 + jf/(3 \times 10^7)][jf/(3 \times 10^5)]}$$

Following Example 8.1, we find that $|T| = 1$ for $f = 2.94$ MHz, where $\angle T = -145.6°$. Thus, $\phi_m = 34.4°$, a reasonable value. If desired, it can be increased by reducing R_c and raising C_c.

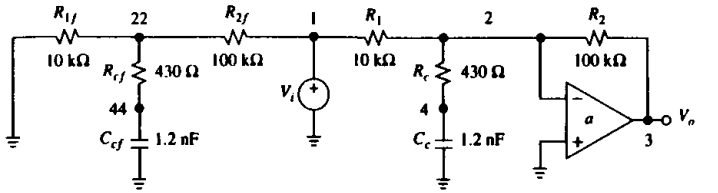


FIGURE 8.26
PSpice circuit of Example 8.12.

(*f*) With reference to Fig. 8.26, we write the following file.

```
Input-lag compensation:
Vi 1 0 ac 1V
*Main circuit:
R1 1 2 10k
R2 2 3 100k
Rc 2 4 430
Cc 4 0 1.2nF
*a0 = 100V/mV, f1 = 10kHz, f2 = 3MHz, f3 = 30MHz:
ea 3 0 Laplace {V(0,2)} = {1E5/((1+s/628E2)*(1+s/188E5)*(1+s/188E6))}
*Circuit to plot 1/beta:
R2f 1 22 100k
R1f 22 0 10k
Rcf 22 44 430
Ccf 44 0 1.2nF
.ac dec 10 1kHz 100MegHz
.probe ;a = V(3)/V(0,2), 1/beta = V(1)/V(22), A = V(3)/V(1)
.end
```

The results of the simulation are shown in Fig. 8.27.

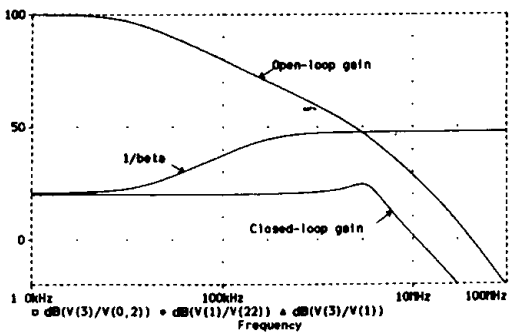


FIGURE 8.27
Frequency plots for the circuit of Fig. 8.26.

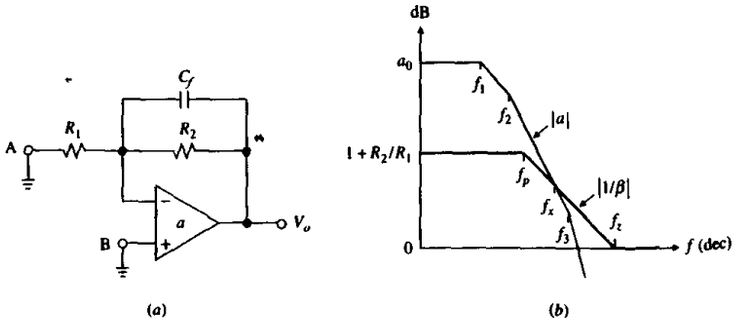
Compared with internal compensation, the input-lag method allows for higher slew rates as the op amp is spared from having to charge or discharge any internal compensating capacitance. The capacitance is now connected between the inputs, so the voltage changes it experiences tend to be very small. However, the settling-time improvement stemming from a higher slew rate is counterbalanced by a long settling tail[15] due to the presence of a pole-zero doublet at f_z and f_p.

A notorious disadvantage of this method is increased high-frequency noise, since the noise-gain curve is raised significantly in the vicinity of the crossover frequency f_x. Another disadvantage is a much lower closed-loop differential input impedance Z_d, since z_d is now in parallel with $Z_c = R_c + 1/j2\pi f C_c$, and Z_c is much smaller than z_d. Though this is inconsequential in inverting configurations, it may cause intolerable high-frequency input loading and feedthrough in noninverting configurations.

Input-lag compensation is nevertheless popular. It is also used in connection with constant-GBP op amps as an alternative to the capacitive-load isolation technique discussed in Section 8.2. We still apply Eqs. (8.30) and (8.31), but with f_2 replaced by $f_p = 1/2\pi r_o C_L$. An additional application of the input-lag method is the stabilization of decompensated op amps, discussed at the end of this section.

Feedback-Lead Compensation

This technique[1] uses a feedback capacitance C_f to create phase lead in the feedback path. This lead is designed to occur in the vicinity of the crossover frequency f_x, which is where ϕ_m needs to be boosted. Alternatively, we can view this method as a reshaping of the $|1/\beta|$ curve near f_x to reduce the rate of closure ROC. Referring to Fig. 8.28*a* and assuming $r_d = \infty$ and $r_o = 0$, we have $1/\beta = 1 + Z_2/R_1$,



(*a*) (*b*)

FIGURE 8.28
Feedback-lead compensation.

$Z_2 = R_2 \parallel (1/j2\pi f C_f)$. Expanding, we can write

$$\frac{1}{\beta(jf)} = \left(1 + \frac{R_2}{R_1}\right)\frac{1 + jf/f_z}{1 + jf/f_p} \tag{8.32}$$

where $f_p = 1/2\pi R_2 C_f$ and $f_z = (1 + R_2/R_1) f_p$. As depicted in Fig. 8.28*b*, $|1/\beta|$ has the low- and high-frequency asymptotes $|1/\beta_0| = 1 + R_2/R_1$ and $|1/\beta_\infty| = 0$ dB, and two breakpoints at f_p and f_z.

The phase lag provided by $1/\beta(jf)$ is maximum[1] at the geometric mean of f_p and f_z, so the optimum value of C_f is the one that makes this mean coincide with the crossover frequency, or $f_x = \sqrt{f_p f_z} = f_p\sqrt{1 + R_2/R_1}$. Under such a condition we have $|a(jf_x)| = \sqrt{1 + R_2/R_1}$, which can be used to find f_x via trial and error. Once f_x is known, we find $C_f = 1/2\pi R_2 f_p$, or

$$C_f = \frac{\sqrt{1 + R_2/R_1}}{2\pi R_2 f_x} \tag{8.33}$$

The closed-loop bandwidth is $1/2\pi R_2 C_f$. Moreover, C_f helps combat the effect of the inverting-input stray capacitance C_n.

One can readily verify that at the geometric mean of f_p and f_z we have $\measuredangle(1/\beta) = 90° - 2\tan^{-1}\sqrt{1 + R_2/R_1}$, so the larger the value of $1 + R_2/R_1$, the greater the contribution of $1/\beta$ to ϕ_m. For example, with $1 + R_2/R_1 = 10$ we get $\measuredangle(1/\beta) = 90° - 2\tan^{-1}\sqrt{10} \cong -55°$, which yields $\measuredangle T = \measuredangle a - (-55°) = \measuredangle a + 55°$. We observe that for this compensation scheme to work with a given ϕ_m, the open-loop gain must satisfy $\measuredangle a(jf_x) \geq \phi_m - 90° - 2\tan^{-1}\sqrt{1 + R_2/R_1}$.

EXAMPLE 8.13. (*a*) Using an op amp with $a_0 = 10^5$ V/V, $f_1 = 1$ kHz, $f_2 = 100$ kHz, and $f_3 = 5$ MHz, design a noninverting amplifier with $A_0 = 20$ V/V. Hence, verify that the circuit needs compensation. (*b*) Stabilize it with the feedback-lead method, and find ϕ_m. (*c*) Find the closed-loop bandwidth.

Solution.

(*a*) For $A_0 = 20$ V/V use $R_1 = 1.05$ kΩ and $R_2 = 20.0$ kΩ. Then $\beta_0 = 1/20$ V/V, and $a_0\beta_0 = 10^5/20 = 5000$. Thus, without compensation we have

$$T(jf) = \frac{5000}{[1 + jf/10^3][1 + jf/10^5][1 + jf/(5 \times 10^6)]}$$

Using trial and error as in Example 8.1, we find that $|T| = 1$ for $f = 700$ kHz, and that $\measuredangle T(j700\text{ kHz}) = -179.8°$. So, $\phi_m = 0.2°$, indicating a circuit in bad need of compensation.

(*b*) Using again trial and error we find that $|a| = \sqrt{20}$ V/V for $f = 1.46$ MHz, and $\measuredangle a(j1.46\text{ MHz}) = -192.3°$. Letting $f_x = 1.46$ MHz in Eq. (8.33) yields $C_f = 24.3$ pF. Moreover, $\phi_m = 180° + \measuredangle a - (90° - 2\tan^{-1}\sqrt{20}) = 180° + (-192.3°) - (90° - 2 \times 77.4°) = 52.5°$.

(*c*) $f_{-3\text{dB}} = 1/2\pi R_2 C_f = 327$ kHz.

We observe that feedback-lead compensation does not enjoy the slew-rate advantages of input-lag compensation; however, it provides better filtering capabilities

for internally generated noise. These are some of the factors the user needs to consider when deciding which method is best for a given application.

Decompensated Op Amps

These op amps are compensated for unconditional stability only when used with $1/\beta$ above a specified value, such as $1/\beta \geq (1/\beta)_{\min} = 5$ V/V, or $\beta \leq \beta_{\max} = 0.2$ V/V. Consequently, they provide a constant GBP only for $|a| \geq (1/\beta)_{\min}$. Being less conservatively compensated, decompensated op amps offer higher GBPs and SRs. For instance, the fully compensated LF356 op amp uses $C_c \cong 10$ pF to provide GBP = 5 MHz and SR = 12 V/μs for any $|a| \geq 1$ V/V. The LF357, its decompensated version, uses $C_c \cong 3$ pF to provide GBP = 20 MHz and SR = 50 V/μs, but only for $|a| \geq 5$ V/V.

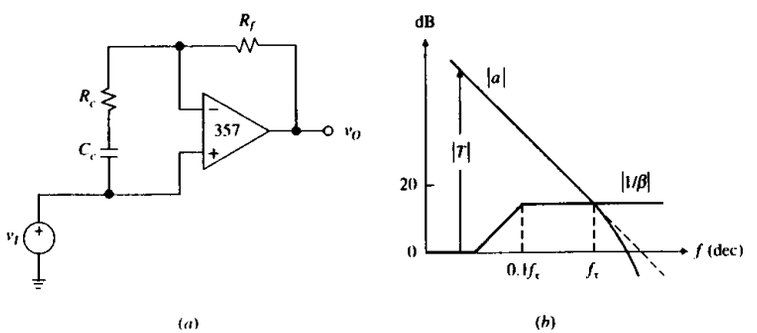
We observe that the constraint $1/\beta \geq (1/\beta)_{\min}$ need be satisfied only in the vicinity of the crossover frequency; elsewhere we can shape the $1/\beta$ curve as we please. For instance, we can use input-lag compensation to operate a decompensated op amp at values of $1/\beta$ below $(1/\beta)_{\min}$ while retaining the high-speed advantages of decompensation. To this end, we still use Eqs. (8.30) and (8.31), but with $|a(jf_2)|$ replaced by $(1/\beta)_{\min}$, f_2 replaced by $\beta_{\max} \times$ GBP, and R_2 replaced by R_f.

EXAMPLE 8.14. Figure 8.29 shows a common way of configuring a decompensated op amp as a voltage follower. It is apparent that at low frequencies, where C_c acts as an open circuit, we have $A_0 = 1$ V/V. (*a*) Given that the 357 op amp is compensated for $(1/\beta)_{\min} = 5$ V/V, specify suitable components to stabilize the circuit. (*b*) Find $A(jf)$.

Solution.

(*a*) By Eq. (8.30), $R_c = R_f/(5 - 1 - R_f/\infty) = R_f/4$. Let $R_c = 3$ kΩ and $R_f = 12$ kΩ. Also, $f_x \cong \beta_{\max} \times \text{GBP} = (1/5) \times 20 = 4$ MHz, so $C_c = 5/(\pi \times 3 \times 10^3 \times 4 \times 10^6) \cong 133$ pF (use 130 pF).

(*b*) $A(jf) \cong 1/[1 + jf/(4\text{ MHz})]$ V/V.



(*a*) (*b*)

FIGURE 8.29
Configuring a decompensated op amp as a unity-gain voltage follower.

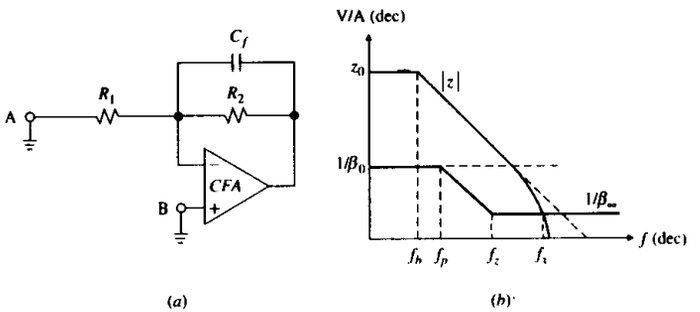
8.5 STABILITY IN CFA CIRCUITS[16]

The open-loop response $z(jf)$ of a current-feedback amplifier (CFA) is dominated by a single pole only over a designated frequency band. Beyond this band, higher-order roots come into play, which increase the overall phase shift. When frequency-independent feedback is applied around a CFA, the latter will offer unconditional stability with a specified phase margin ϕ_m only as long as $1/\beta \geq (1/\beta)_{\min} = |z(jf_{\phi_m - 180^\circ})|$, where $f_{\phi_m - 180^\circ}$ is the frequency at which $\sphericalangle z = \phi_m - 180^\circ$. Lowering the $1/\beta$ curve below $(1/\beta)_{\min}$ would increase the phase shift, thus eroding ϕ_m and inviting instability. This behavior is similar to that of decompensated op amps. The value of $(1/\beta)_{\min}$ can be found from the data-sheet plots of $|z(jf)|$ and $\sphericalangle z(jf)$. As with voltage-feedback amplifiers (VFAs), instability in CFA circuits may also stem from feedback phase lag due to external reactive elements.

Effect of Feedback Capacitance

To investigate the effect of feedback capacitance, refer to Fig. 8.30*a*. At low frequencies, C_f acts as an open circuit, so we can apply Eq. (6.58) and write $1/\beta_0 = R_2 + r_n(1 + R_2/R_1)$. At high frequencies, R_2 is shorted out by C_f, so $1/\beta_\infty = 1/\beta_0|_{R_2 \to 0} = r_n$. Since $1/\beta_\infty \ll 1/\beta_0$, the crossover frequency f_x is pushed into the region of greater phase shift, as shown in Fig. 8.30*b*. If this shift reaches -180°, the circuit will oscillate.

We thus conclude that *direct capacitive feedback must be avoided in CFA circuits*. In particular, the familiar inverting or Miller integrator is not amenable to CFA implementation, unless suitable measures are taken to stabilize it (see Problem 8.44). However, the noninverting or Deboo integrator is acceptable because β in the vicinity of f_x is still controlled by the resistance in the negative-feedback path. Likewise, we can readily use CFAs in those filter configurations that do not employ any direct capacitance between the output and the inverting input, such as *KRC* filters.



(*a*) (*b*)

FIGURE 8.30
A large feedback capacitance C_f tends to destabilize a CFA circuit.

Stray Input Capacitance Compensation

In Fig. 8.31*a* C_n appears in parallel with R_1. Replacing R_1 with $R_1 \parallel (1/j2\pi f C_n)$ in Eq. (6.58) yields, after minor algebra,

$$\frac{1}{\beta} = \frac{1}{\beta_0}(1 + jf/f_z) \tag{8.34a}$$

$$\frac{1}{\beta_0} = R_2 + r_n\left(1 + \frac{R_2}{R_1}\right) \qquad f_z = \frac{1}{2\pi(R_1 \parallel R_2 \parallel r_n)C_n} \tag{8.34b}$$

As shown in Fig. 8.31*b*, the $1/\beta$ curve starts to rise at f_z, and if C_n is sufficiently large to make $f_z < f_x$, the circuit will become unstable.

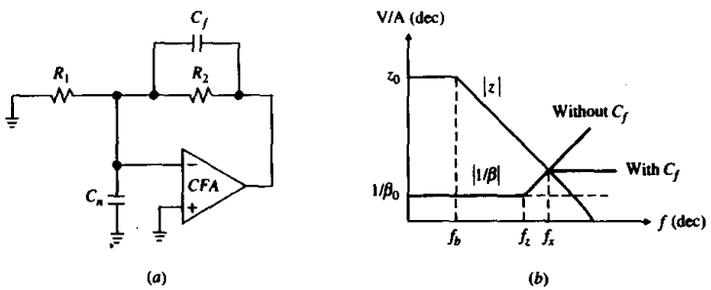


FIGURE 8.31
Input stray capacitance compensation in CFA circuits.

Like a VFA, a CFA is stabilized by counteracting the effect of C_n with a small feedback capacitance C_f. Together with R_2, C_f creates a pole frequency for $1/\beta$ at $f_p = 1/2\pi R_2 C_f$. For $\phi_m = 45°$, impose $f_p = f_x$. We observe that f_x is the geometric mean of f_z and $\beta_0 z_0 f_b$. Letting $1/2\pi R_2 C_f = \sqrt{\beta_0 z_0 f_b f_z}$ and solving, we get

$$C_f = \sqrt{r_n C_n / 2\pi R_2 z_0 f_b} \tag{8.35}$$

A typical application is when a CFA is used in conjunction with a current-output DAC to perform fast *I-V* conversion, and the stray capacitance is the combined result of the DAC output capacitance and the CFA input capacitance.

EXAMPLE 8.15. A current-output DAC is fed to a CFA having $z_0 = 750\ \text{k}\Omega$, $f_b = 200\ \text{kHz}$, and $r_n = 50\ \Omega$. Assuming $R_2 = 1.5\ \text{k}\Omega$ and $C_n = 100\ \text{pF}$, find C_f for $\phi_m = 45°$. Verify with PSpice.

Solution. $C_f = \sqrt{50 \times 100 \times 10^{-12}/(2\pi \times 1.5 \times 10^3 \times 1.5 \times 10^{11})} = 1.88\ \text{pF}$. This value can be increased for a greater phase margin, but this will also reduce the bandwidth of the *I-V* converter.

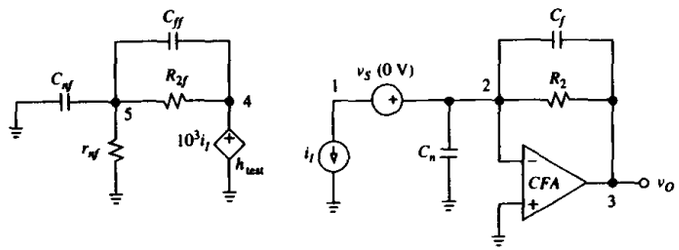


FIGURE 8.32
PSpice circuit of Example 8.15.

Referring to Fig. 8.32 and using the CFA subcircuit of Example 6.17, we write the following circuit file.

```
I-V converter using a CFA:
.subckt CFA vP vM vO
ein 1 0 vP 0 1
rn 1 2 50
vS 2 vM dc 0
fCFA 0 3 vS 1
Req 3 0 750k
Ceq 3 0 1.061pF
eout vO 0 3 0 1
.ends CFA
*Main circuit:
iI 1 0 ac 1mA pulse(0 1mA 0 0.1ns 0.1ns 50ns 100ns)
vS 2 1 dc 0
Cn 2 0 100pF
R2 2 3 1.5k
Cf 2 3 1.88pF
X1 0 2 3 CFA
*Circuit to plot 1/beta:
htest 4 0 vs 1k
R2f 4 5 1.5k
Cff 4 5 1.88pF
Cnf 5 0 100pF
rnf 5 0 50
*Circuit to plot z:
X2 4 6 7 CFA
Rs 6 0 100
RL 7 0 1Meg
.ac dec 100 1MegHz 1GHz
.tran 1ns 50ns
.probe ;A = V(3)/I(Vs), z = V(7)/I(Rs), 1/beta = V(4)/I(rnf), vO = v(3)
.end
```

The results of the simulation are shown in Fig. 8.33.

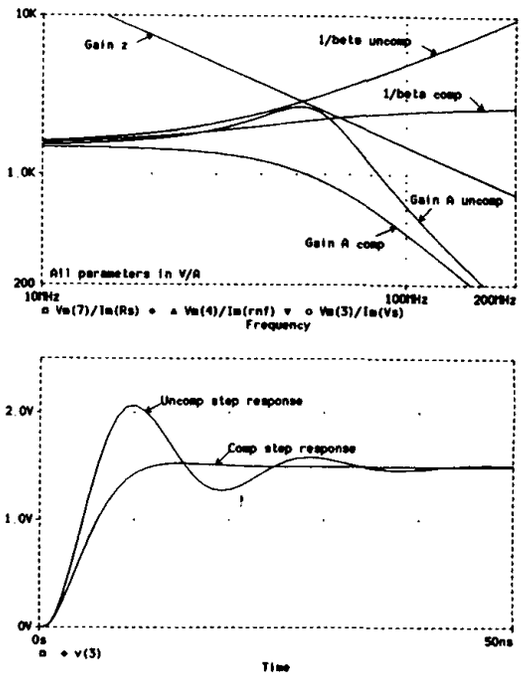


FIGURE 8.33
Frequency and transient responses of the circuit of Fig. 8.32.

8.6 COMPOSITE AMPLIFIERS

Two or more op amps can be combined to achieve improved overall performance.[17] The designer need be aware that when an op amp is placed within the feedback loop of another, stability problems may arise. In the following we shall designate the gains of the individual op amps as a_1 and a_2, and the gain of the composite device as a.

Increasing the Loop Gain

Two op amps, usually from a dual-op-amp package, can be connected in cascade to create a composite amplifier with a gain $a = a_1 a_2$ much higher than the individual gains a_1 and a_2. We expect the composite device to provide a much greater loop gain, and thus a much lower gain error. However, if we denote the individual unity-gain frequencies as f_{t1} and f_{t2}, we observe that at high frequencies, where $a = a_1 a_2 \cong (f_{t1}/jf)(f_{t2}/jf) = -f_{t1} f_{t2}/f^2$, the phase shift of the composite response approaches $-180°$, thus requiring frequency compensation.

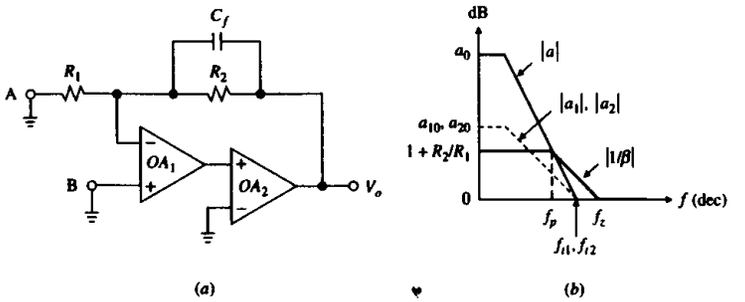


FIGURE 8.34
Composite amplifier with feedback-lead compensation.

In applications with sufficiently high closed-loop dc gains, the composite amplifier can be stabilized via the feedback-lead method[18] shown in Fig. 8.34*a*. As usual, the circuit can be either an inverting or a noninverting amplifier, depending on whether we insert the input source at node A or B. The decibel plot of $|a|$ is obtained by adding together the individual decibel plots of $|a_1|$ and $|a_2|$. This is illustrated in Fig. 8.34*b* for the case of matched op amps, or $a_1 = a_2$.

As we know, the $1/\beta$ curve has a pole frequency at $f_p = 1/2\pi R_2 C_f$ and a zero frequency at $f_z = (1 + R_2/R_1) f_p$. For ROC = 30 dB/dec, or $\phi_m = 45°$, we place f_p right on the $|a|$ curve. This yields $1 + R_2/R_1 = |a(jf_p)| = f_{t1} f_{t2}/f_p^2$. Solving for f_p and then letting $C_f = 1/2\pi R_2 f_p$ gives

$$C_f = \sqrt{(1 + R_2/R_1)/f_{t1} f_{t2}}/2\pi R_2 \tag{8.36}$$

The closed-loop bandwidth is $f_B = f_p$. It can be shown (see Problem 8.46) that increasing C_f by the factor $(1 + R_2/R_1)^{1/4}$ will make the crossover frequency f_x coincide with the geometric mean $\sqrt{f_p f_z}$ and thus maximize ϕ_m; however, this will also decrease the closed-loop bandwidth in proportion.

EXAMPLE 8.16. (*a*) The circuit of Fig. 8.34*a* is to be used as a noninverting amplifier with $R_1 = 1$ kΩ and $R_2 = 99$ k. (*a*) Assuming op amps of the 741 type, find C_f for $\phi_m = 45°$. Then compare ϕ_m, T_0, and f_B with the case of a single-op-amp realization. (*b*) Find C_f for the maximum phase margin. What are the resulting values of ϕ_m and f_p? (*c*) What happens if C_f is increased above the value found in (*b*)?

Solution.

(*a*) Insert the input source at node B. Letting $f_{t1} = f_{t2} = 1$ MHz in Eq. (8.36) gives $C_f = 16.1$ pF for $\phi_m = 45°$. Moreover, $T_0 = a_0^2/100 = 4 \times 10^8$, and $f_B = f_p = 100$ kHz. Had a single op amp been used, then $\phi_m = 90°$, $T_0 = a_0/100 = 2 \times 10^3$, and $f_B = 10^6/100 = 10$ kHz.

(*b*) $C_f = (100)^{1/4} \times 16.1 = 50.8$ pF, $f_p = 31.62$ kHz, $\phi_m = 180° + \sphericalangle a - \sphericalangle(1/\beta) \cong 180° - 180° - [\tan^{-1}(f_x/f_z) - \tan^{-1}(f_x/f_p)] = -(\tan^{-1} 0.1 - \tan^{-1} 10) = 78.6°$.

(*c*) Increasing C_f above 50.8 pF will reduce ϕ_m until eventually $\phi_m \to 0°$, indicating that overcompensation is detrimental.

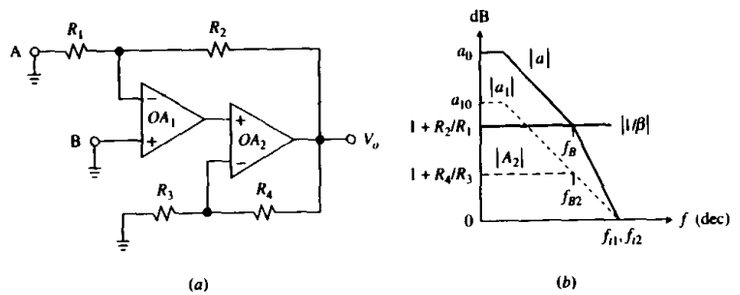


FIGURE 8.35
Composite amplifier with compensation provided by OA_2.

In Fig. 8.34 we have stabilized the composite amplifier by acting on its feedback network. An alternative[19] type of compensation is by controlling the pole of the second op amp using local feedback, in the manner depicted in Fig. 8.35. The composite response $a = a_1 A_2$ has the dc gain $a_0 = a_{01}(1 + R_4/R_3)$, and two pole frequencies at f_{b1} and at $f_{B2} = f_{t2}/(1 + R_4/R_3)$. Without the second amplifier, the closed-loop bandwidth would be $f_{B1} = f_{t1}/(1+R_2/R_1)$. With the second amplifier in place, the bandwidth is expanded to $f_B = (1+R_4/R_3)f_{B1} = f_{t1}(1+R_4/R_3)/(1 + R_2/R_1)$. It is apparent that if we align f_B and f_{B2}, then ROC = 30 dB/dec, or $\phi_m = 45°$. Thus, imposing $f_{t1}(1 + R_4/R_3)/(1 + R_2/R_1) = f_{t2}/(1 + R_4/R_3)$ yields

$$1 + R_4/R_3 = \sqrt{(f_{t2}/f_{t1})(1 + R_2/R_1)} \tag{8.37}$$

We observe that for the benefits of using OA_2 to be significant the application must call for a sufficiently high closed-loop gain.

EXAMPLE 8.17. (*a*) Assuming op amps of the 741 type in the circuit of Fig. 8.35*a*, specify suitable components for operation as an inverting amplifier with a dc gain of −100 V/V. Compare with a single-op-amp realization.

Solution. Insert the input source at node A and let $R_1 = 1\,\text{k}\Omega$ and $R_2 = 100\,\text{k}\Omega$. Then, $R_4/R_3 = \sqrt{101} - 1 = 9.05$. Pick $R_3 = 2\,\text{k}\Omega$ and $R_4 = 18\,\text{k}\Omega$. The dc loop gain is $T_0 = a_{10}(1 + R_4/R_3)/(1 + R_2/R_1) \cong 2 \times 10^4$, and the closed-loop bandwidth is $f_B \cong f_t/10 = 100\,\text{kHz}$. If only one op amp had been used, then $\phi_m \cong 90°$, $T_0 \cong 2 \times 10^3$ and $f_B \cong 10\,\text{kHz}$, indicating an order-of-magnitude improvement brought about by the second op amp.

Optimizing dc and ac Characteristics

There are applications in which it is desirable to combine the dc characteristics of a low-offset, low-noise device, such as a bipolar voltage-feedback amplifier (VFA), with the dynamics of a high-speed device, such as a current-feedback amplifier (CFA). The two sets of technologically conflicting specifications can be met with a composite amplifier. In the topology of Fig. 8.36*a* we use a CFA with local feedback

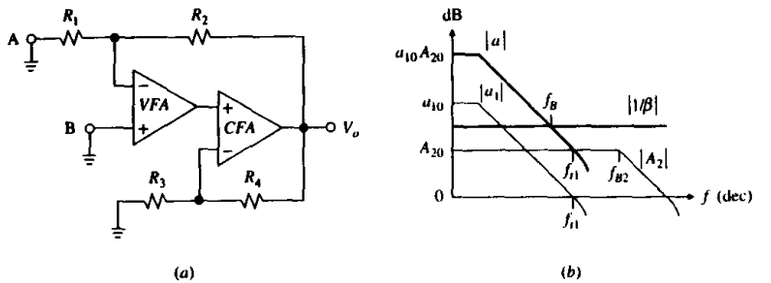


FIGURE 8.36
VFA-CFA composite amplifier.

to shift the $|a_1|_{\text{dB}}$ curve upward by the amount $|A_2|_{\text{dB}}$, and thus improve the dc loop gain by the same amount. As long as $f_{B2} \gg f_{t1}$, the phase shift due to the pole frequency at $f = f_{B2}$ will be insignificant at $f = f_{t1}$, indicating that we can operate the VFA with a feedback factor of unity, or at the maximum bandwidth f_{t1}. Imposing

$$1 + R_4/R_3 = 1 + R_2/R_1 \tag{8.38}$$

will maximize also the closed-loop bandwidth f_B of the composite device, which is now $f_B = f_{t1}$.

The composite topology offers important advantages other than bandwidth. Since the CFA is operated within the feedback loop of the VFA, its generally poorer input dc and noise characteristics become insignificant when referred to the input of the composite device, where they are divided by a_1. Moreover, with most of the signal swing being provided by the CFA, the slew-rate requirements of the VFA are significantly relaxed, thus ensuring high full-power bandwidth (FPB) capabilities for the composite device. Finally, since the VFA is spared from having to drive the output load, self-heating effects such as thermal feedback become insignificant, so the composite device retains optimum input-drift characteristics.

There are practical limitations to the amount of closed-loop gain achievable with a CFA. Even so, it pays to use a CFA as part of a composite amplifier. For instance, suppose we need an overall dc gain $A_0 = 10^3$ V/V, but using a CFA having only $A_{20} = 50$ V/V. Clearly, the VFA will now have to operate with a gain of $A_0/50 = 20$ V/V and a bandwidth $f_{t1}/20$. This is still 50 times better than if the VFA were to operate alone, not to mention the slew-rate and thermal-drift advantages.

In the arrangement of Fig. 8.36*a* the composite bandwidth is set by the VFA, so the amplification provided by the CFA above this band is in effect wasted. The alternative topology of Fig. 8.37 exploits the dynamics of OA_2 to their fullest extent by allowing it to participate directly in the feedback mode, but only at high frequencies. The circuit works as follows.

At dc, where the capacitances act as opens, the circuit reduces to that of Fig. 8.34*a*, so $a_0 = a_{10}a_{20}$. Clearly, the dc characteristics are set by OA_1, which provides OA_2 with whatever drive is needed to force $V_n \to V_{OS1}$. Moreover, any gross bias current at the inverting input of OA_2 is prevented from disturbing node V_n because of the dc blocking action by C_2.

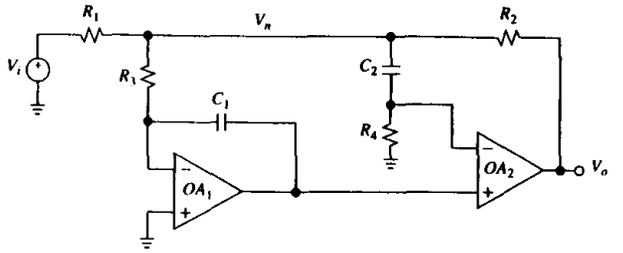


FIGURE 8.37
Composite amplifier enjoying the dc characteristics of OA_1 and the ac characteristics of OA_2.

As we increase the operating frequency, we witness a gradual decrease in OA_1's gain $A_1 = -1/(jf/f_1)$, $f_1 = 1/2\pi R_3 C_1$, while the crossover network $C_2 R_4$ gradually changes the mode of operation of OA_2 from open-loop to closed-loop. Above the crossover network frequency $f_2 = 1/2\pi R_4 C_2$ we can write $V_o \cong a_2(A_1 V_n - V_n)$, or

$$V_o \cong -\frac{a_{20}}{1 + jf/f_{b2}} \frac{1 + jf/f_1}{jf/f_1} V_n$$

It is apparent that if we impose $f_1 = f_{b2}$, or $R_3 C_1 = 1/2\pi f_{b2}$, then we obtain a *pole-zero cancellation* and $V_o = -aV_n$, $a = a_{20}/(jf/f_1) = a_{20} f_{b2}/jf \cong a_2$, indicating that the high-frequency dynamics are fully controlled by OA_2.

In a practical realization the zero-pole cancellation is difficult to maintain because f_{b2} is an ill-defined parameter. Consequently, in response to an input step, the composite device will not completely stabilize until the integrator loop has settled to its final value. The resulting settling tail may be of concern in certain applications.

Improving Phase Accuracy

As we know, a single-pole amplifier exhibits an error function of the type $1/(1 + 1/T) = 1/(1 + jf/f_B)$, whose phase error is $\epsilon_\phi = -\tan^{-1}(f/f_B)$, or $\epsilon_\phi \cong -f/f_B$ for $f \ll f_B$. This error is intolerable in applications requiring high phase accuracy. In the composite arrangement[20] of Fig. 8.38, OA_2 provides active feedback around OA_1 to maintain a low phase error over a much wider bandwidth than in the uncompensated case. This is similar to the active compensation of integrators of Section 6.5.

To analyze the circuit, let $\beta = R_1/(R_1 + R_2)$ and $\alpha = R_3/(R_3 + R_4)$. We note that OA_2 is a noninverting amplifier with gain $A_2 = (1/\beta)/(1 + jf/\beta f_{t2})$. Consequently, the feedback factor around OA_1 is $\beta_1 = \beta \times A_2 \times \alpha = \alpha/(1 + jf/\beta f_{t2})$.

The closed-loop gain of the composite device is $A = A_1 = a_1/(1 + a_1\beta_1)$, where we are using the fact that OA_1 too is operating in the noninverting mode. Substituting $a_1 \cong f_{t1}/jf$ and $\beta_1 = \alpha/(1 + jf/\beta f_{t2})$, and letting $f_{t1} = f_{t2} = f_t$, we obtain, for $\alpha = \beta$,

$$A(jf) = A_0 \frac{1 + jf/f_B}{1 + jf/f_B - (f/f_B)^2} \tag{8.39}$$

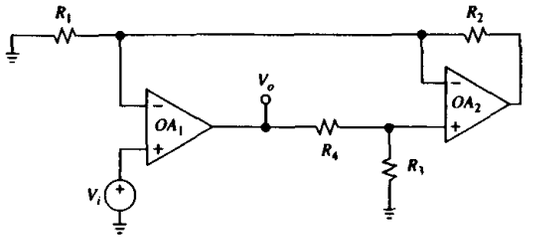


FIGURE 8.38
Composite amplifier with high phase accuracy.

where $A_0 = 1 + R_2/R_1$ and $f_B = f_t/A_0$. As discussed in Section 6.5, this error function offers the advantage of a very small phase error, namely, $\epsilon_\phi = -\tan^{-1}(f/f_B)^3$, or $\epsilon_\phi \cong -(f/f_B)^3$ for $f \ll f_B$.

Figure 8.39 (top) shows the results of the PSpice simulation of a composite amplifier with $A_0 = 10$ V/V using a matched pair of 10-MHz op amps, so that

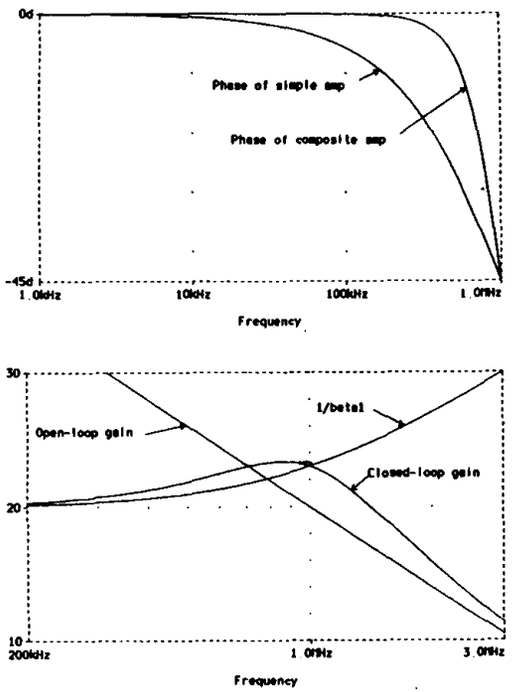


FIGURE 8.39
Frequency plots of the circuit of Fig. 8.38.

$f_B = 1$ MHz. For instance, at 1/10 of f_B, or 100 kHz, the composite circuit gives $\epsilon_\phi = -0.057°$, which is far better than $\epsilon_\phi = -5.7°$ for a single-op-amp realization.

The stability situation, shown in Fig. 8.39 (bottom), reveals a rise in the $|1/\beta_1|$ curve because of the feedback pole introduced by OA_2 at $f = \beta f_{t2}$. This frequency is high enough not to compromise the stability of OA_1, yet low enough to cause a certain amount of gain peaking: this is the price we are paying for the dramatic improvement in the phase-error characteristic!

PROBLEMS

8.1 The stability problem

8.1 An op amp with $a_0 = 10^3$ V/V and two pole frequencies at $f_1 = 100$ kHz and $f_2 = 2$ MHz is connected as a unity-gain voltage follower. Find ϕ_m, ζ, Q, GP, OS, and $A(jf)$. Would you use this circuit?

8.2 An amplifier has three identical pole frequencies so that $a(jf) = a_0/(1 + jf/f_1)^3$, and is placed in a negative-feedback loop with a frequency-independent feedback factor β. Find an expression for $f_{-180°}$ as well as the corresponding value of T.

8.3 (*a*) Verify that a circuit with a dc loop gain $T_0 = 10^2$ and three pole frequencies at $f_1 = 100$ kHz, $f_2 = 1$ MHz, and $f_3 = 2$ MHz is unstable. (*b*) One way of stabilizing it is by reducing T_0. Find the value to which T_0 must be reduced for $\phi_m = 45°$. (*c*) Another way of stabilizing it is by rearranging one or more of its poles. Find the value to which f_1 must be reduced for $\phi_m = 45°$. (*d*) Repeat parts (*b*) and (*c*), but for $\phi_m = 60°$.

8.4 An amplifier with $a(jf) = 10^5(1 + jf/10^4)/[(1 + jf/10) \times (1 + jf/10^3)]$ V/V is placed in a negative-feedback loop with frequency-independent β. (*a*) Find the range of values of β for which $\phi_m \geq 45°$. (*b*) Repeat, but for $\phi_m \geq 60°$. (*c*) Find the value of β that minimizes ϕ_m. What is $\phi_{m(\min)}$?

8.5 Two negative-feedback systems are compared at some frequency f_1. If it is found that the first has $T(jf_1) = 10\angle -180°$ and the second has $T(jf_1) = 10\angle -90°$, which system enjoys the smaller magnitude error? The smaller phase error?

8.6 The response of a negative-feedback circuit with $\beta = 0.1$ V/V is observed with the oscilloscope. For a 1-V input step, the output exhibits an overshoot of 12.6% and a final value of 9 V. Moreover, with an ac input, the phase difference between output and input reaches 90° for $f = 10$ kHz. Assuming a 2-pole error amplifier, find its open-loop response.

8.7 As mentioned, the rate-of-closure considerations hold only for minimum-phase systems. Verify by comparing the Bode plots of the minimum-phase function $H(s) = (1 + s/2\pi 10^3)/[(1 + s/2\pi 10)(1 + s/2\pi 10^2)]$ with those of the function $H(s) = (1 - s/2\pi 10^3)/[(1 + s/2\pi 10)(1 + s/2\pi 10^2)]$, which is similar to the former, except that its zero is located in the right half of the complex plane.

8.8 Repeat the PSpice simulation of the circuit of Fig. 8.5, but for the case in which the loop is broken at the inverting-input pin. Hence, compare the results with Fig. 8.6.

8.9 Assuming ideal op amp, derive an expression for the loop gain of the equal-component *KRC* filter of Example 3.8. Hence, discuss the stability of the circuit. What is its gain margin?

8.2 Stability of constant-GBP op amp circuits

8.10 The response of an unconditionally stable op amp can be approximated with a dominant pole frequency f_1 and a single high-frequency pole f_2 to account for the phase shift due to its higher-order roots. (*a*) Assuming $a_0 = 10^5$ V/V, $f_1 = 10$ Hz, and $\beta = 1$ V/V, find the actual bandwidth f_B and phase margin ϕ_m if $f_2 = 1$ MHz. (*b*) Find f_2 for $\phi_m = 60°$; what is the value of f_B? (*c*) Repeat (*b*), but for $\phi_m = 45°$.

8.11 An op amp with $a(jf) = 10^5/(1 + jf/10)$ is placed in a negative-feedback loop with $\beta(jf) = \beta_0/(1 + jf/10^5)^2$. Find the values of β_0 corresponding to (*a*) the onset of oscillatory behavior, (*b*) $\phi_m = 45°$, and (*c*) GM = 20 dB.

8.12 A Howland current pump is implemented with a constant-GBP op amp and four identical resistances. Using rate-of-closure reasoning, show that as long as the load is resistive or capacitive the circuit is stable, but can become unstable if the load is inductive. How would you compensate it?

8.13 Specify R_s in the differentiator of Example 8.2 for $\phi_m = 60°$. Hence, derive an expression for $H(jf)$. What is the value of Q?

8.14 An alternative frequency compensation method for the differentiator of Fig. 8.8*a* is by means of a suitable feedback capacitance C_f in parallel with R. Assuming $C = 10$ nF, $R = 78.7$ kΩ, and GBP = 1 MHz, specify C_f for $\phi_m = 45°$.

8.15 The noninverting differentiator of Fig. P3.2 uses an op amp with GBP = 1 MHz. If $R = 78.7$ kΩ and $C = 10$ nF, verify that the circuit needs compensation. How would you stabilize it?

8.16 (*a*) Show that the circuit of Fig. 8.10*a* gives $A = -R_2/R_1 \times H_{LP}$, where H_{LP} is the standard second-order low-pass response defined in Eq. (3.44) with $f_0 = \sqrt{\beta_0 f_t f_z}$ and $Q = \sqrt{\beta_0 f_t/f_z}/(1 + \beta_0 f_t/f_p)$. (*b*) Find Q in the circuit of Example 8.3 before compensation. (*c*) Compensate the circuit for $\phi_m = 45°$, and find Q after compensation.

8.17 In the circuit of Example 8.3 find C_f for $\phi_m = 60°$; hence, exploit Problem 8.16 to find $A(jf)$, GP, and OS.

8.18 An alternative way of stabilizing a circuit against stray input capacitance C_n is by scaling down all resistances to raise f_z until $f_z \geq f_x$. (*a*) Scale the resistances of the circuit of Example 8.3 so that with $C_f = 0$ the circuit yields $\phi_m = 45°$. (*b*) Repeat, but for $\phi_m = 60°$. (*c*) What is the main advantage and disadvantage of this technique?

8.19 The high-sensitivity *I-V* converter of Fig. 2.2 uses $R = 1$ MΩ, $R_1 = 1$ kΩ, $R_2 = 10$ kΩ, and the LF351 JFET-input op amp, which has GBP = 4 MHz. (*a*) Assuming an overall input stray capacitance $C_n = 10$ pF, show that the circuit does not have enough phase margin. (*b*) Find a capacitance C_f that, when connected between the output and the inverting input, will provide neutral compensation. What is the closed-loop bandwidth of the compensated circuit?

8.20 Using the op amp data of Example 8.5, find the maximum C_L that can be connected to the output of the circuit of Fig. 8.14*a* and still allow for $\phi_m \geq 45°$ if (*a*) $R_1 = R_2 = 20$ kΩ, (*b*) $R_1 = 2$ kΩ, $R_2 = 18$ kΩ, (*c*) $R_1 = \infty$, $R_2 = 0$. (*d*) Repeat (*c*), but for $\phi_m \geq 60°$.

8.21 Using PSpice, check the frequency and transient response of the circuit of (*a*) Example 8.4 and (*b*) Example 8.5.

8.22 Using the op amp data of Example 8.5, design an amplifier with $A_0 = +10$ V/V, under the constraint that the sum of all resistances be 200 kΩ, and that it be capable of driving a 10-nF load. Then use PSpice to verify its frequency and transient responses.

8.23 Modify the circuit of Example 8.5 for unity-gain voltage-follower operation. Then use PSpice to find GP and OS.

8.24 Assuming constant-GBP op amps, use linearized Bode plots to investigate the stability of (*a*) the wideband band-pass filter of Fig. 3.11, (*b*) the multiple-feedback low-pass filter of Fig. 3.32, and (*c*) the -*KRC* low-pass filter of Problem 3.27.

8.25 (*a*) Assuming the op amp has a constant GBP of 1 MHz, discuss the stability of the multiple-feedback band-pass filter of Fig. 3.31, and verify with PSpice. (*b*) Repeat, but for the -*KRC* band-pass filter of Problem 3.28 for the case $R_1 = R_2 = 1.607$ kΩ, $kR_2 = 1.445$ MΩ, and $C_1 = C_2 = 3.3$ nF.

8.3 Internal frequency compensation

8.26 Find f_d to stabilize the $\mu A702$ op amp of Example 8.6 for a noninverting gain of 10 V/V with (*a*) $\phi_m = 60°$, (*b*) GM = 12 dB, (*c*) GP = 2 dB, (*d*) OS = 5%.

8.27 A voltage comparator is a high-gain amplifier intended for open-loop operation. Figure P8.27 shows a way of configuring such a device as a voltage follower. (*a*) Assuming a two-pole device with $a_0 = 10^3$ V/V, $f_1 = 1$ MHz, and $f_2 = 10$ MHz, use rate-of-closure reasoning to show that the circuit can be stabilized by making the product RC sufficiently large. (*b*) Assuming a FET-input device, specify R and C for $\phi_m = 45°$. (*c*) Estimate the small-signal bandwidth.

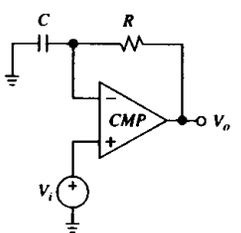


FIGURE P8.27

8.28 An amplifier has $a_0 = 10^4$ V/V, a dominant-pole frequency $f_1 = 1$ kHz, and an adjustable higher-order pole frequency f_2. Find β and f_2 for a maximally flat closed-loop response with a dc gain of 60 dB. What is the −3-dB frequency?

8.29 In Fig. P8.29 three CMOS inverters are cascaded to create a rudimentary op amp, which, in turn, is configured as an ac-coupled inverting amplifier with a closed-loop gain of −100 V/V. (*a*) Assuming $a_1 = a_2 = a_3 = -10^2/(1 + jf/10^5)$, show that with $R_c = C_c = 0$ the circuit is unstable. (*b*) Specify suitable values for R_c and C_c to provide dominant-pole stabilization with $\phi_m = 45°$.

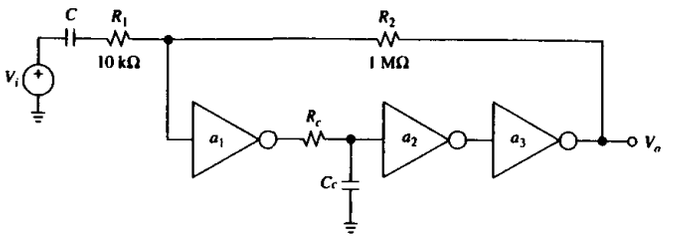


FIGURE P8.29

8.30 Referring to Fig. 8.20*a*, apply KCL at nodes V_1 and V_2, and then eliminate V_1 to find an expression for the transfer function V_2/V_d. Hence, prove Eqs. (8.24) and (8.25). *Hint:* Given two characteristic frequencies f_1 and f_2 such that $f_1 \ll f_2$, you can approximate $(1 + jf/f_1)(1 + jf/f_2) \cong 1 + jf/f_1 - f^2/f_1 f_2$.

8.31 For the op amp of Example 8.9*a* calculate the actual values of f_x and ϕ_m after compensation. Then verify that the effect of the zero f_z is to *reduce* the phase margin by 9°.

8.32 (*a*) An op amp has a dominant pole at $s = -2\pi f_1$, and two additional poles at $s = -2\pi f_2$ and $s = -2\pi f_3$, $f_3 = 10 \times$GBP. Show that for $\phi_m \geq 60°$ we must have $f_2 \geq 2.2 \times$GBP. (*b*) An op amp has a dominant pole at $s = -2\pi f_1$, a second pole at $s = -2\pi f_2$, and a zero at $s = +2\pi f_z$, $f_z = 10 \times$ GBP. Show that for $\phi_m \geq 45°$ we must have $f_2 \geq 1.2 \times$ GBP.

8.33 Prove Eqs. (8.26) and (8.27). Use the hint of Problem 8.30.

8.34 Use PSpice to verify the pole-zero compensation scheme of Example 8.10. Show both the frequency and transient responses.

8.4 External frequency compensation

8.35 The op amp of Example 8.11 is configured as a unity-gain inverting amplifier with two 100-kΩ resistances. Use input-lag compensation to stabilize it for $\phi_m = 45°$. Hence, find $A(jf)$.

8.36 In Fig. P8.36 let $R_1 = R_2 = R_4 = 100$ kΩ, $R_3 = 10$ kΩ, and let the op amp have $a_0 = 10^5$ V/V, $f_1 = 10$ kHz, $f_2 = 200$ kHz, and $f_3 = 2$ MHz. (*a*) Verify that the circuit is unstable. (*b*) Use input-lag compensation to stabilize it for $\phi_m = 45°$. (*c*) Find the closed-loop bandwidth after compensation.

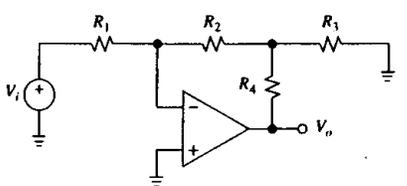


FIGURE P8.36

8.37 Use the input-lag technique to compensate the capacitively loaded amplifier of Example 8.5.

8.38 The OPA637 op amp of Fig. P8.38 is a decompensated amplifier with SR = 135 V/μs and GBP = 80 MHz for $1/\beta \geq 5$ V/V. Since the op amp is not compensated for unity-gain stability, the integrator shown would be unstable. (*a*) Show that the circuit can be stabilized by connecting a compensation capacitance C_c as shown, and find a suitable value for C_c for $\phi_m = 45°$. (*b*) Obtain an expression for $H(jf)$ after compensation and indicate the frequency range over which the circuit behaves reasonably well as an integrator.

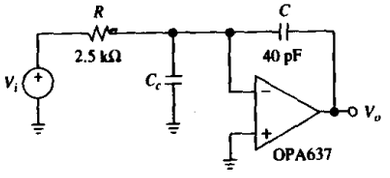


FIGURE P8.38

8.39 An op amp with GBP = 6 MHz and $r_o = 30\ \Omega$ is to operate as a unity-gain voltage follower with an output load of 5 nF. Design an input-lag network to stabilize it. Then verify its frequency and transient responses via PSpice.

8.40 Using a decompensated op amp with GBP = 80 MHz and $\beta_{max} = 0.2$ V/V, design a unity-gain inverting amplifier, and find $A(jf)$.

8.41 Using an LF357 decompensated op amp, which has GBP = 20 MHz and $\beta_{max} = 0.2$ V/V, design an I-V converter with a sensitivity of 0.1 V/μA under the following constraints: (*a*) no compensation capacitances are allowed, and (*b*) the closed-loop bandwidth must be maximized. Then find an expression for $A(jf)$.

8.42 An op amp with $a_0 = 10^6$ V/V and two coincident pole frequencies $f_1 = f_2 = 10$ Hz is configured as an inverting amplifier with $R_1 = 1\,k\Omega$ and $R_2 = 20\,k\Omega$. (*a*) Use feedback-lead compensation to stabilize it for $\phi_m = 45°$; then find $A(jf)$. (*b*) Find the value of C_f that will maximize ϕ_m; next find ϕ_m as well as the corresponding closed-loop bandwidth.

8.43 The wideband band-pass filter of Example 3.5 is implemented with an op amp having $a_0 = 10^5$ V/V and two pole frequencies $f_1 = 10$ Hz and $f_2 = 2$ MHz. Sketch the Bode plots of $|a|$ and $|1/\beta|$ in the vicinity of f_x and find ϕ_m.

8.5 Stability in CFA circuits

8.44 The CFA integrator of Fig. P8.44 uses a series resistance R_2 between the summing junction and the inverting-input pin to ensure $1/\beta \geq (1/\beta)_{min}$ over frequency and thus avoid instability problems. (*a*) Investigate the stability of the circuit using Bode plots. (*b*) Assuming the CFA parameters of Problem 6.57, specify suitable components for $f_0 = 1$ MHz. (*c*) List possible disadvantages of this circuit.

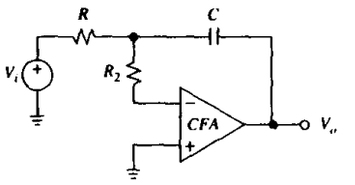


FIGURE P8.44

8.45 The CFA of Problem 6.57 is to be used to design a Butterworth band-pass filter with $f_0 = 10$ MHz and $H_{0BP} = 0$ db, and two alternatives are being considered, namely, the multiple-feedback and the *KRC* designs. Which configuration are you choosing, and why? Show the final circuit.

8.46 (*a*) Show that without C_f the CFA I-V converter of Fig. 8.32 yields $V_o/I_i = R_2 H_{LP}$, where H_{LP} is the standard second-order low-pass response defined in Eq. (3.44) with $f_0 = (z_0 f_b/2\pi r_n R_2 C_n)^{1/2}$ and $Q = z_0 f_b/(r_n + R_2) f_0$. (*b*) Predict the GP and OS for the circuit of Example 8.15 before compensation.

8.47 A certain CFA has $r_n = 50\ \Omega$ and an open-loop dc gain of 1 V/μA, and its frequency response can be approximated with two pole frequencies, one at 100 kHz and the other at 100 MHz. The CFA is to be used as a unity-gain voltage follower. (*a*) Find the feedback resistance needed for a phase margin of 45°; what is the closed-loop bandwidth? (*b*) Repeat, but for a 60° margin.

8.6 Composite amplifiers

8.48 (*a*) With reference to the circuit of Fig. 8.34*a*, show that ϕ_m is maximized for $C_f = (1 + R_2/R_1)^{3/4}/[2\pi R_2 (f_{t1} f_{t2})^{1/2}]$. (*b*) Show that for $\phi_{m(max)} \geq 45°$ we must have $1 + R_2/R_1 \geq \tan^2 67.5° = 5.8$. (*c*) Assuming 741 op amps, specify suitable component values for operation as an inverting amplifier with $A_0 = -10$ V/V and maximum phase margin. Hence, find the actual values of ϕ_m and $A(jf)$.

8.49 (*a*) Compare the circuit of Example 8.16 with a circuit implemented by cascading two amplifiers with individual dc gains $A_{10} = A_{20} = \sqrt{|A_0|}$ V/V. (*b*) Repeat, but for the circuit of Example 8.17.

8.50 An alternative to Eq. (8.37) is $1 + R_4/R_3 = \sqrt{(1 + R_2/R_1)/2}$, where we have assumed $f_{t1} = f_{t2}$. (*a*) Verify that this alternative yields $\phi_m \cong 65°$. (*b*) Apply it to the design of a composite amplifier with dc gain $A_0 = -50$ V/V. (*c*) Assuming $f_{t1} = f_{t2} = 4.5$ MHz, find $A(jf)$.

8.51 In the composite amplifier of Fig. 8.37 assume OA_1 has $a_{10} = 100$ V/mV, $f_{t1} = 1$ MHz, $V_{OS1} \cong 0$, and $I_{B1} \cong 0$, and OA_2 has $a_{20} = 25$ V/mV, $f_{t2} = 500$ MHz, $V_{OS2} = 5$ mV, and $I_{B2} = 20\ \mu$A. Specify suitable components for $A_0 = -10$ V/V, under the constraint $f_2 = 0.1 f_1$. What is the output dc error E_O and the closed-loop bandwidth f_B?

8.52 For the circuit of Problem 8.51 find the total rms output noise E_{no} if $e_{n1} = 2\ \text{nV}/\sqrt{\text{Hz}}$, $i_{n1} = 0.5\ \text{pA}/\sqrt{\text{Hz}}$, $e_{n2} = 5\ \text{nV}/\sqrt{\text{Hz}}$, and $i_{n2} = 5\ \text{pA}/\sqrt{\text{Hz}}$. Ignore $1/f$ noise. Can you reduce E_{no}?

8.53 (*a*) Find ϕ_m, GP, and OS for the composite amplifier of Fig. 8.38. (*b*) Find its 1° phase-error bandwidth, and compare it with that of a single-op-amp realization with the same value of A_0, as well as with that of the cascade realization of two amplifiers with individual dc gains $\sqrt{A_0}$.

8.54 The active-compensation scheme of Fig. P8.54 (see *IEEE Trans. Circuits Syst.*, vol. CAS-26, Feb. 1979, pp. 112–117) works for both the inverting and the noninverting mode of operation of OA_1. Show that $V_o = [(1/\beta)V_2 + (1 - 1/\beta)V_1]/(1 + 1/T)$, $1/(1 + 1/T) = (1 + jf/\beta_2 f_{t2})/(1 + jf/\beta f_{t1} - f^2/\beta f_{t1}\beta_2 f_{t2})$, $\beta = R_1/(R_1 + R_2)$, $\beta_2 = R_3/(R_3 + R_4)$.

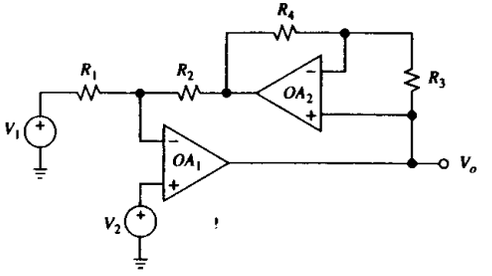


FIGURE P8.54

8.55 Apply the scheme of Problem 8.54 to the design of a high-phase-accuracy (*a*) voltage follower, (*b*) I-V converter with a sensitivity of 10 V/mA, and (*c*) difference amplifier with a dc gain of 100 V/V. Assume matched op amps with $f_t = 10$ MHz.

REFERENCES

1. J. K. Roberge, *Operational Amplifiers: Theory and Practice*, John Wiley & Sons, New York, 1975.
2. R. C. Dorf, *Modern Control Systems*, Addison-Wesley, Reading, MA, 1967.
3. S. Rosenstark, *Feedback Amplifier Principles*, Macmillan, New York, 1986.
4. J. G. Graeme, "Phase Compensation Counteracts Op Amp Input Capacitance," *EDN*, January 6, 1994, pp. 97–104.
5. S. Franco, "Simple Techniques Provide Compensation for Capacitive Loads," *EDN*, June 8, 1989, pp. 147–149.
6. J. Graeme, "Phase Compensation Extends Op Amp Stability and Speed," *EDN*, September 16, 1991, pp. 181–192.
7. J. Williams, "High-Speed Amplifier Techniques," Application Note AN-47, *Linear Applications Handbook Volume II*, Linear Technology, Milpitas, CA, 1993.
8. A. P. Brokaw, "An IC Amplifiers User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change," Application Note AN-202, *Applications Reference Manual*, Analog Devices, Norwood, MA, 1993.
9. A. P. Brokaw, "Analog Signal Handling for High Speed and Accuracy," Application Note AN-342, *Applications Reference Manual*, Analog Devices, Norwood, MA, 1993.
10. J.-H. Broeders, M. Meywes, and B. Baker, "Noise and Interference," *1996 Design Seminar*, Burr-Brown, Tucson, AZ, 1996.
11. P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 3d ed., John Wiley & Sons, New York, 1993.
12. J. E. Solomon, "The Monolithic Operational Amplifier: A Tutorial Study," *IEEE J. Solid-State Circuits*, vol. SC-9, Dec. 1974, pp. 314–332.
13. J. G. Graeme, G. E. Tobey, and L. P. Huelsman, *Operational Amplifiers: Design and Applications*, McGraw-Hill, New York, 1971.
14. R. J. Widlar, "Feedforward Compensation Speeds Op Amp," Linear Brief LB-2, *Linear Applications Handbook*, National Semiconductor, Santa Clara, CA, 1994.
15. J. Dostál, *Operational Amplifiers*, 2d ed., Butterworth-Heinemann, Stoneham, MA, 1993.
16. Based on the author's article "Current-Feedback Amplifiers Benefit High-Speed Designs," *EDN*, January 5, 1989, pp. 161–172. ©Cahners Publishing Company, 1997, a Div. of Reed Elsevier Inc.
17. J. Williams, "Composite Amplifiers," Application Note AN-21, *Linear Applications Handbook Volume I*, Linear Technology, Milpitas, CA, 1990.
18. J. Graeme, "Phase Compensation Perks Up Composite Amplifiers," *Electronic Design*, August 19, 1993, pp. 64–78.
19. J. Graeme, "Composite Amplifier Hikes Precision and Speed," *Electronic Design Analog Applications Issue*, June 24, 1993, pp. 30–38.
20. J. Wong, "Active Feedback Improves Amplifier Phase Accuracy," *EDN*, September 17, 1987.

9

NONLINEAR CIRCUITS

All circuits encountered so far are designed to behave linearly. Linearity is achieved by (*a*) using negative feedback to force the op amp to operate within its linear region and (*b*) implementing the feedback network with linear elements.

Using a high-gain amplifier with positive feedback, or even with no feedback at all, causes the device to operate primarily in saturation. This bistable behavior is highly nonlinear and forms the basis of voltage-comparator and Schmitt-trigger circuits.

Nonlinear behavior can also be achieved by implementing the feedback network with nonlinear elements, such as diodes and analog switches. Common examples include precision rectifiers, peak detectors, and sample-and-hold amplifiers. Another class of nonlinear circuits exploits the predictable exponential characteristic of the BJT to achieve a variety of nonlinear transfer characteristics, such as logarithmic amplification and analog multiplication. This category of nonlinear circuits will be investigated in Chapter 13.

9.1 VOLTAGE COMPARATORS

The function of a voltage comparator is to compare the voltage v_P at one of its inputs against the voltage v_N at the other, and output either a low voltage V_{OL} or a high voltage V_{OH} according to

$$v_O = V_{OL} \quad \text{for } v_P < v_N \tag{9.1a}$$

$$v_O = V_{OH} \quad \text{for } v_P > v_N \tag{9.1b}$$

As shown in Fig. 9.1*a*, the symbolism used for comparators is the same as for op amps. We observe that while v_P and v_N are *analog* variables because they can assume a continuum of values, v_O is a *binary* variable because it can assume only one of two values, V_{OL} or V_{OH}. It is fair to view the comparator as a one-bit analog-to-digital converter.

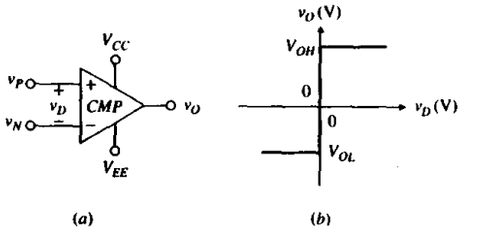


FIGURE 9.1
Voltage-comparator symbolism and ideal VTC. (All node voltages are referenced to ground.)

Introducing the differential input voltage $v_D = v_P - v_N$, the above equations can also be expressed as $v_O = V_{OL}$ for $v_D < 0$ V, and $v_O = V_{OH}$ for $v_D > 0$ V. The voltage transfer curve (VTC), shown in Fig. 9.1*b*, is a nonlinear curve. At the origin, the curve is a vertical segment, indicating an infinite gain there, or $v_O/v_D = \infty$. A practical comparator can only approximate this idealized VTC, with actual gains being typically in the range from 10^3 to 10^6 V/V. Away from the origin, the VTC consists of two horizontal lines positioned at $v_O = V_{OL}$ and $v_O = V_{OH}$. These levels need not necessarily be symmetric, though symmetry may be desirable in certain applications. All that matters is that the two levels be sufficiently far apart to make their distinction reliable. For example, digital applications require $V_{OL} \cong 0$ V and $V_{OH} \cong 5$ V.

The Response Time

In high-speed applications it is of interest to know how rapidly a comparator responds as the input state changes from $v_P < v_N$ to $v_P > v_N$, and vice versa. Comparator speed is characterized in terms of the *response time*, also called the *propagation delay* t_{PD}, defined as the time it takes for the output to accomplish 50% of its transition in response to a predetermined voltage step at the input. Figure 9.2 illustrates the setup