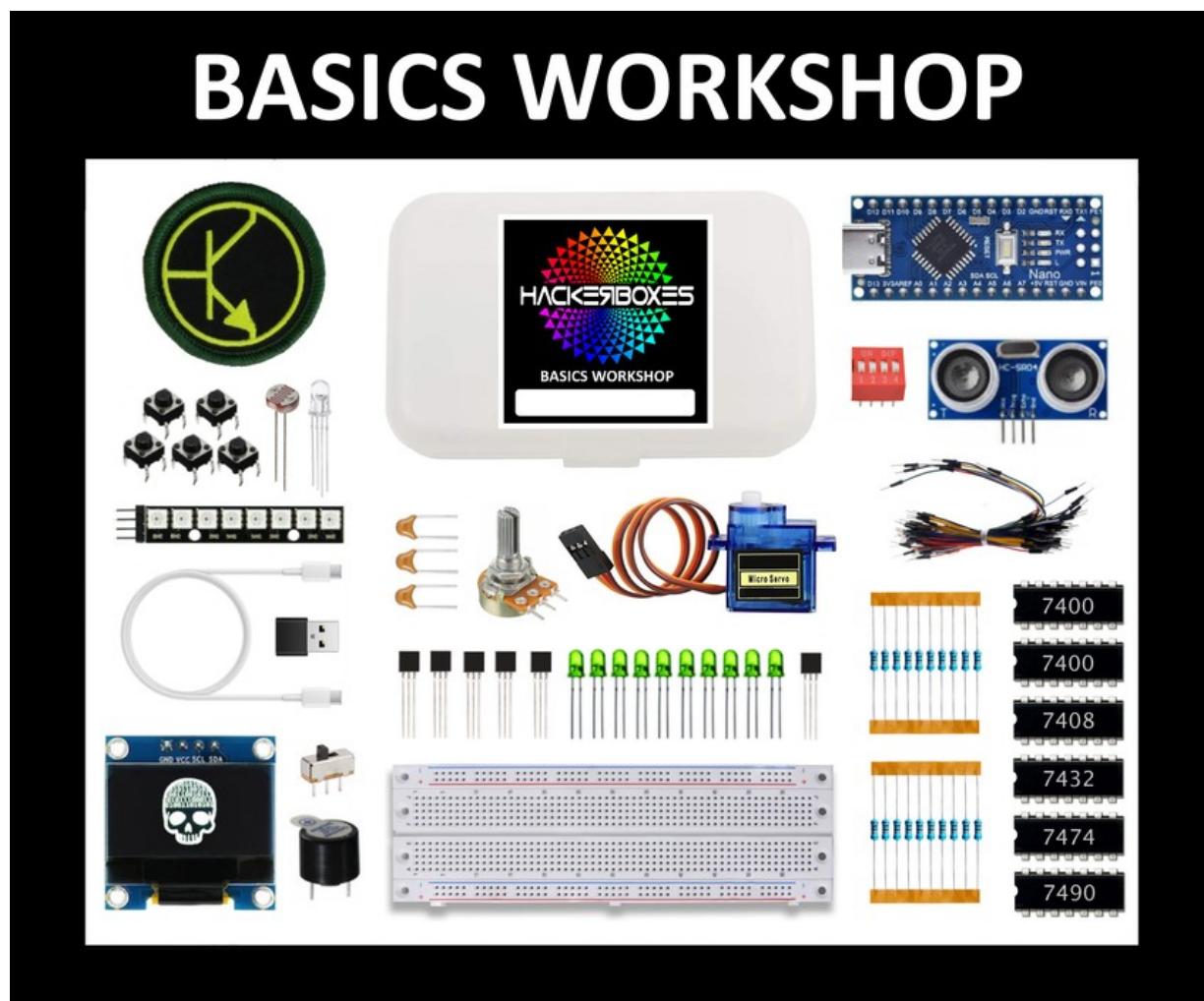


# HackerBox Basics Workshop

By [HackerBoxes](#) in [CircuitsElectronics](#)





## Introduction: HackerBox Basics Workshop



The HackerBox Basics Workshop provides an enlightening introduction to electronics suitable for ages 10-110. No soldering required. The electronic components and modules were carefully selected to work along with the included solderless breadboard using jumper wire connections. The HackerBox Basics Workshop is perfect for self-study or classroom use in schools, business, scouts, makerspaces, or other training scenarios. Accordingly, the workshop is [available for purchase here](#) in single units or class packs of ten.

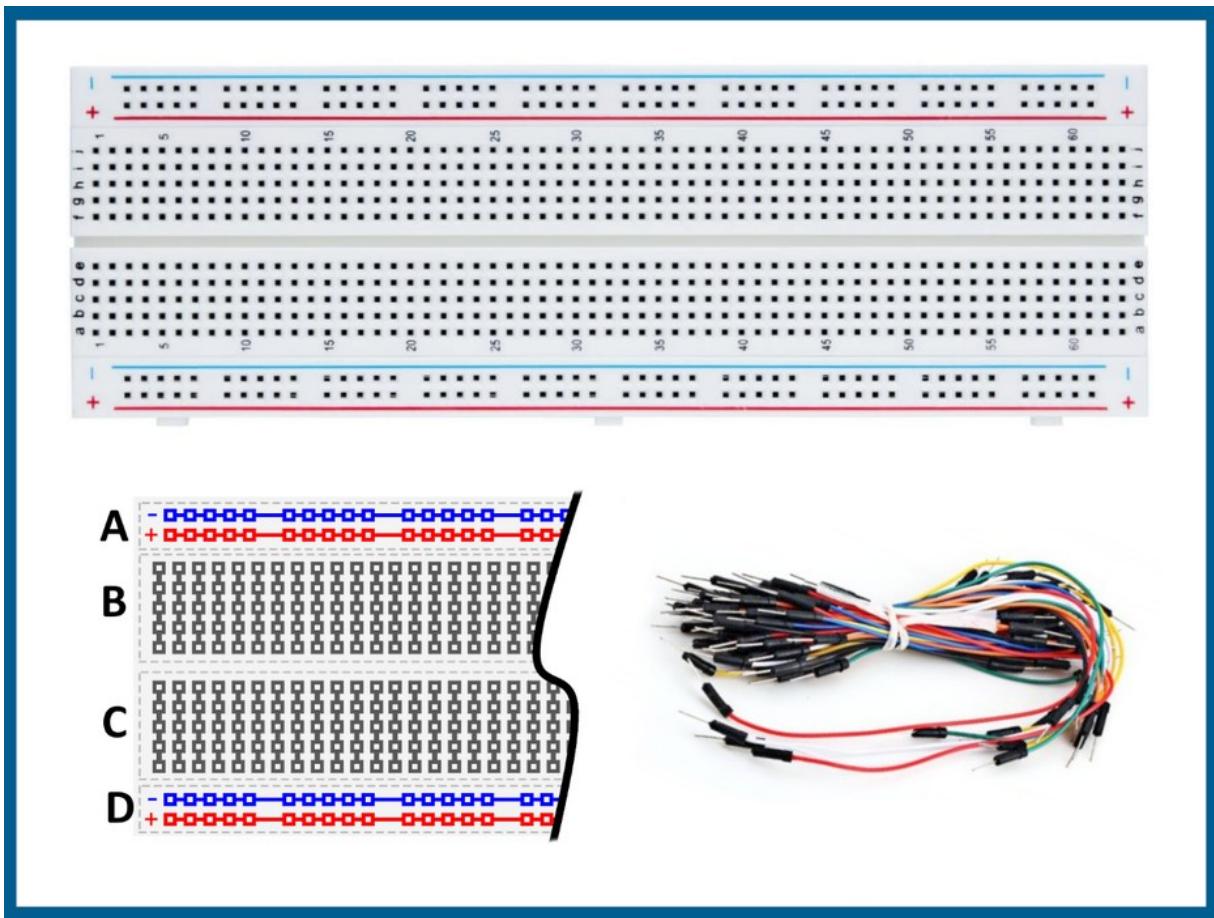
# Supplies

This material covers introductory electronics in fifty topics and hands-on experiments. This journey, which we call *Electrons to A.I.*, starts with fundamental electricity, visits semiconductor transistors, digital logic, data storage, sensors, controllers, computer programs, and arrives at embedded computing devices capable of machine learning and artificial intelligence. The *Electrons to A.I.* educational programming spans the following subject matter:

1. Solderless Breadboards
2. Electron Flow
3. Control Electron Flow with a Switch
4. Control Electron Flow with a Pushbutton
5. Microcontrollers
6. Set Up The Arduino Nano
7. Control Electron Flow with Program Code
8. Looping and Timers
9. Program Output to Serial Monitor
10. Program Input from a Pushbutton
11. Digital Versus Analog
12. Analog Input from a Potentiometer
13. Measuring Voltage
14. Voltage Dividers
15. Resistor Structures
16. Ohm's Law
17. Adjusting Light Brightness
18. Light Sensors
19. Temperature Sensors
20. Program Control Flow
21. Storing Data in Arrays
22. Generating Sound
23. Measure Distance
24. Electromechanical Motion
25. Controlling Servo Motors
26. Displaying Graphics and Text
27. Full Color LEDs
28. Serial Addressable LEDs
29. Measuring Capacitance
30. Capacitor Structures
31. Electron Flow through Diodes
32. Transistors
33. Transistors as Switches
34. Digital Logic
35. Logic Gates from Transistors
36. Integrated Logic Chips
37. XOR Gates from NAND Gates

- 38. Combining Logic Gates
- 39. Storing Information
- 40. NAND Gate Flip-Flops
- 41. D Flip-Flop Integrated Circuit
- 42. Binary Counter
- 43. Computer Architecture
- 44. Assembly Language and Machine Code
- 45. Instruction Cycle
- 46. Algorithms and Heuristics
- 47. Machine Learning
- 48. Artificial Neural Networks
- 49. Embedded Neural Networks
- 50. Artificial Intelligence

# Step 1: Solderless Breadboards



Solderless breadboards are the fastest and easiest way to prototype and experiment with electronic circuits and systems.

The drawing illustrates the four areas of the typical solderless breadboard.

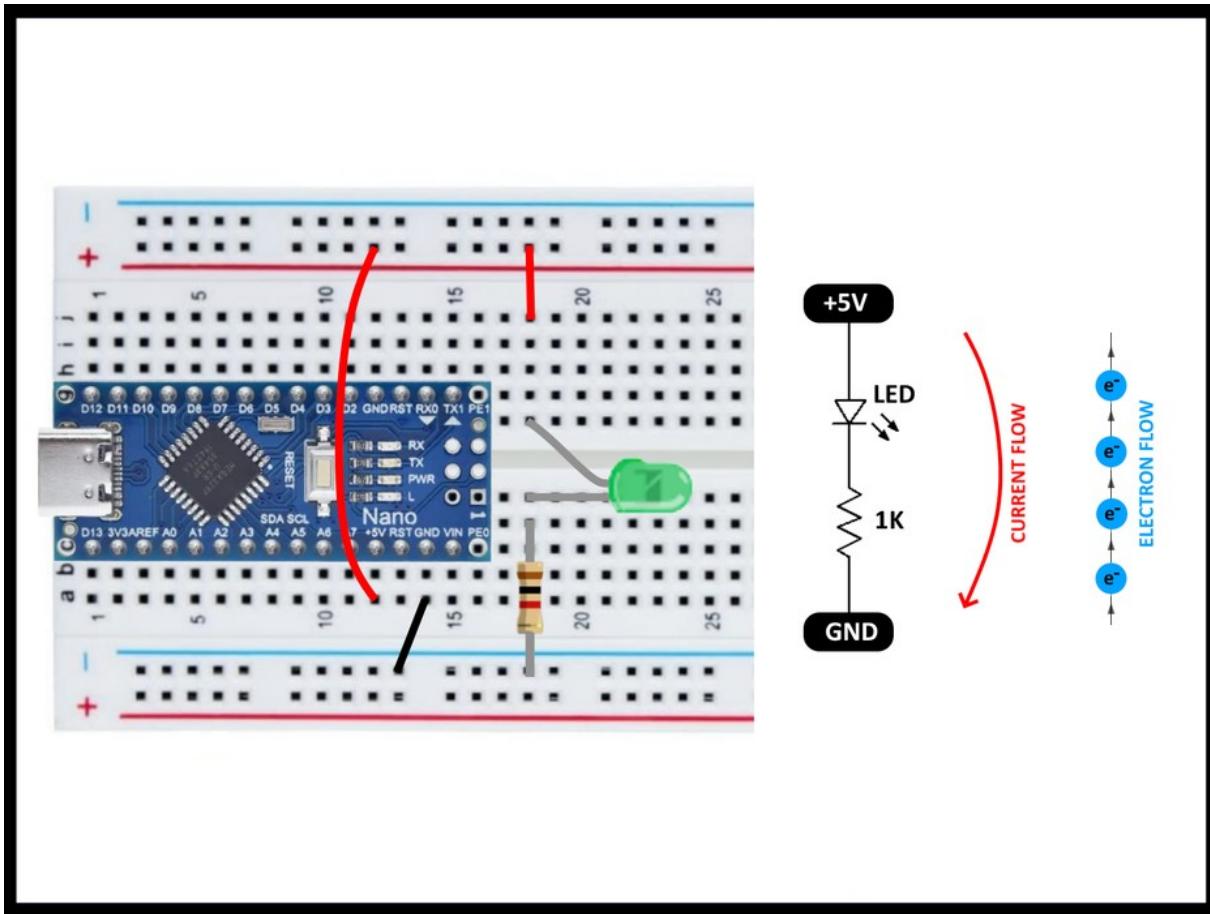
**Areas A and D** are "power rails" generally used to conduct the plus and minus voltages for your power supply across the entire length of the board. For example, the blue lines might be grounded (ZERO VOLTS) and the red lines might be connected to the +5V power supply line.

**Areas B and C** are "terminal strips" generally used to connect the pins of various circuit components. Each vertical column of five pins are connected together in the same way that the long horizontal rows of the power rails are connected together. Note that Area B is separated from Area C by a gap of exactly the distance between the two rows of pins on a standard DIP Chip. Accordingly, the terminal strips of Area B and those of Area C are not connected to one another.

**Jumper Wires** having pins or stripped wires on each end may be used to connect between the terminal strips as needed. The jumpers may also be used to connect the power rails into the terminal strip areas where needed.

For additional background on solderless breadboards, have a look at this [tutorial](#) from Sparkfun.

## Step 2: Electron Flow



The Arduino Nano module is a microcontroller device with a USB-C connector. There is a lot of interesting circuitry on the Arduino Nano, which we will get to in due time. For now, we are only using the Arduino Nano as a mechanism for connecting 5V power from USB to our breadboard.

Once the Arduino Nano is inserted into the solderless breadboard as shown, the white USB-C to USB-C cable can be connected to the Arduino Nano. The other end of the cable can be connected to your PC (or USB hub) assuming there is an open USB-C port. If instead there is only a USB-A port available, there is a black/silver USB-C to USB-A adapter inside the plastic box of components.

Once power, a tiny red LED on the Arduino Nano will flash. We can ignore that for now.

Disconnect the USB power cable while assembling the circuit shown.

Let's examine the components and connections of the circuit...

The red "+" power rail across the top of the breadboard is connected to the +5V pin of the Arduino Nano by the longer red jumper wire.

The blue "-" power rail across the bottoms of the breadboard is connected to a GND pin of the Arduino Nano by the short black jumper wire.

The shorter red jumper wire connects the +5V power rail to the green LED. Note that the LED has a long pin and a short pin. The long pin must connect to the +5V power rail.

The short pin of the green led is connected to a 1K Ohm resistor.

The other end of the resistor is connected to the GND power rail.

These connections implement the circuit shown in the schematic to the right of the solderless breadboard.

One pin of the green LED is connected to the +5V power rail. The other pin of the green LED is connected (via the 1K resistor) to the GND power rail. Accordingly, there will be a potential difference between +5V rail and the GND rail across the LED. This difference will attract electrons from the GND rail to the +5V rail. Opposites attract, so the negative electrons (all electrons are negatively charged) are pulled towards the +5V direction.

Why exactly are we talking about [electrons](#)? Atoms make up everything and those atoms have electrons floating around them. Some of those electrons can be made to move. The electrons move more easily from metal atoms than from atoms of insulating material. Thus metals can conduct electricity (electrons). What that means is when a voltage (also called a potential difference) is applied across a conductor (like metal wire), some electrons in the conductor are drawn from the negative side of the voltage to the positive side of the voltage.

Electrons get sucked from the ground power rail, through the green LED, and towards the +5V rail. When the electrons flow through the LED, it glows with light.

## Current Affairs

It is worth committing to memory that while electric current is the flow of electrons, the convention for specifying the direction of current flow is in the opposite direction of the flow of the electrons. Electrons flow negative to positive but "Conventional Current" flows positive to negative. Just accept it, or read under the heading "conventions" on the Wikipedia page for [electric current](#) to learn more.

## Identifying Resistors

The Basics Workshop includes 1K and 10K resistors. How can we tell them apart?

The 1K resistors can be:

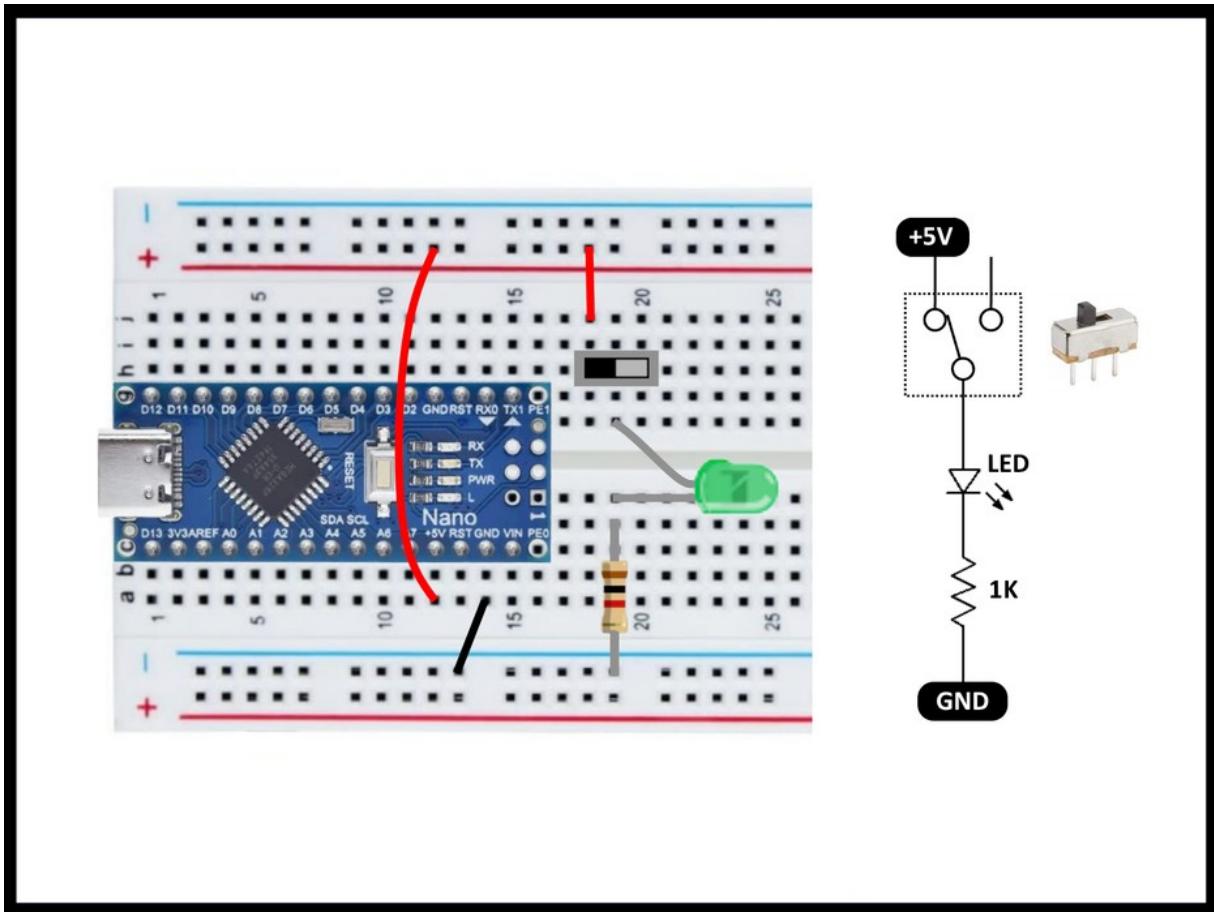
1. Beige with stripes colored: brown, black, red ( $1\_0\_00 = 1\text{K Ohms}$ ), or
2. Blue with stripes colored: brown, black, black, brown ( $1\_0\_0\_0 = 1\text{K ohms}$ )

The 10K resistors can be:

1. Beige with stripes colored: brown, black, orange ( $1\_0\_000 = 10\text{K Ohms}$ ), or
2. Blue with stripes colored: brown, black, black, red ( $1\_0\_0\_00 = 10\text{K ohms}$ )

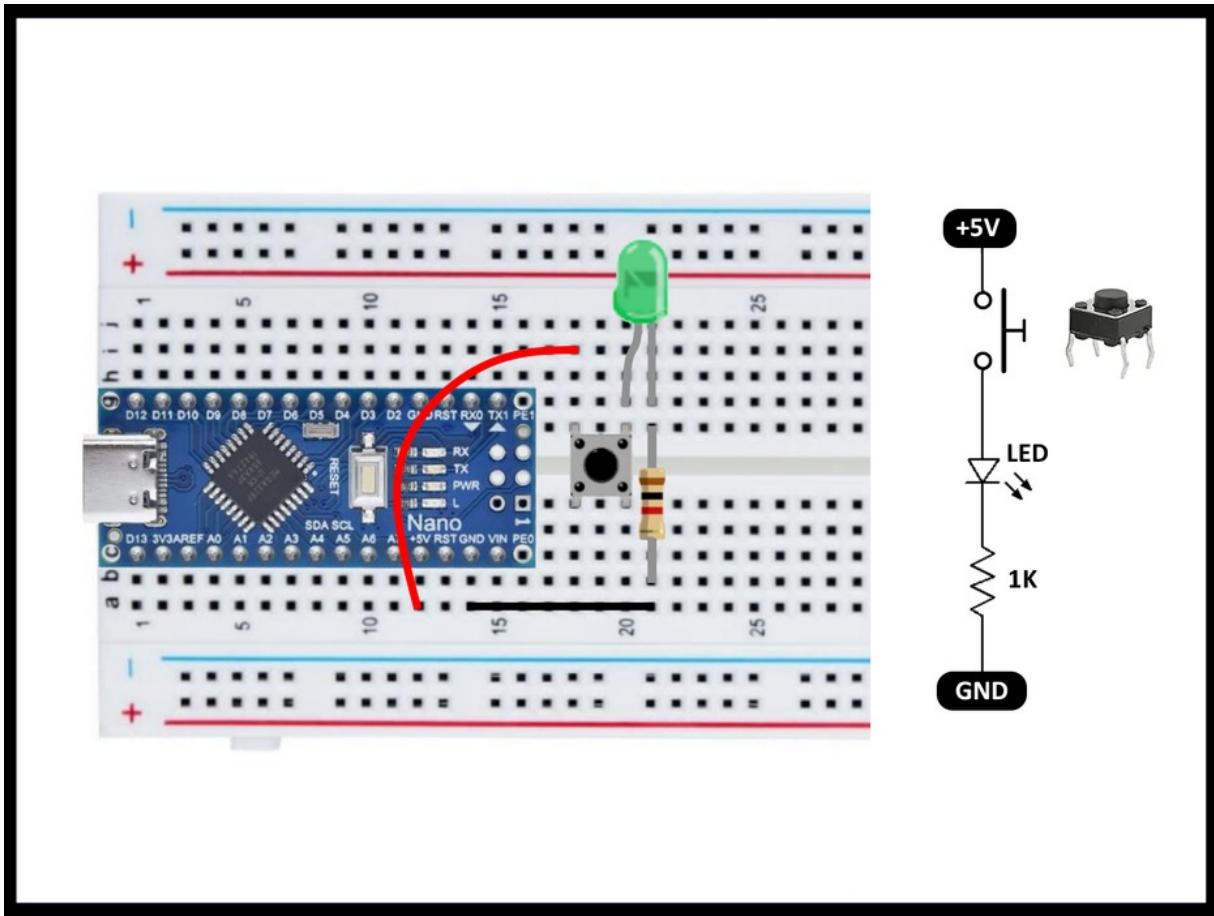
Resistor [color code calculator](#).

## Step 3: Control Electron Flow With a Switch



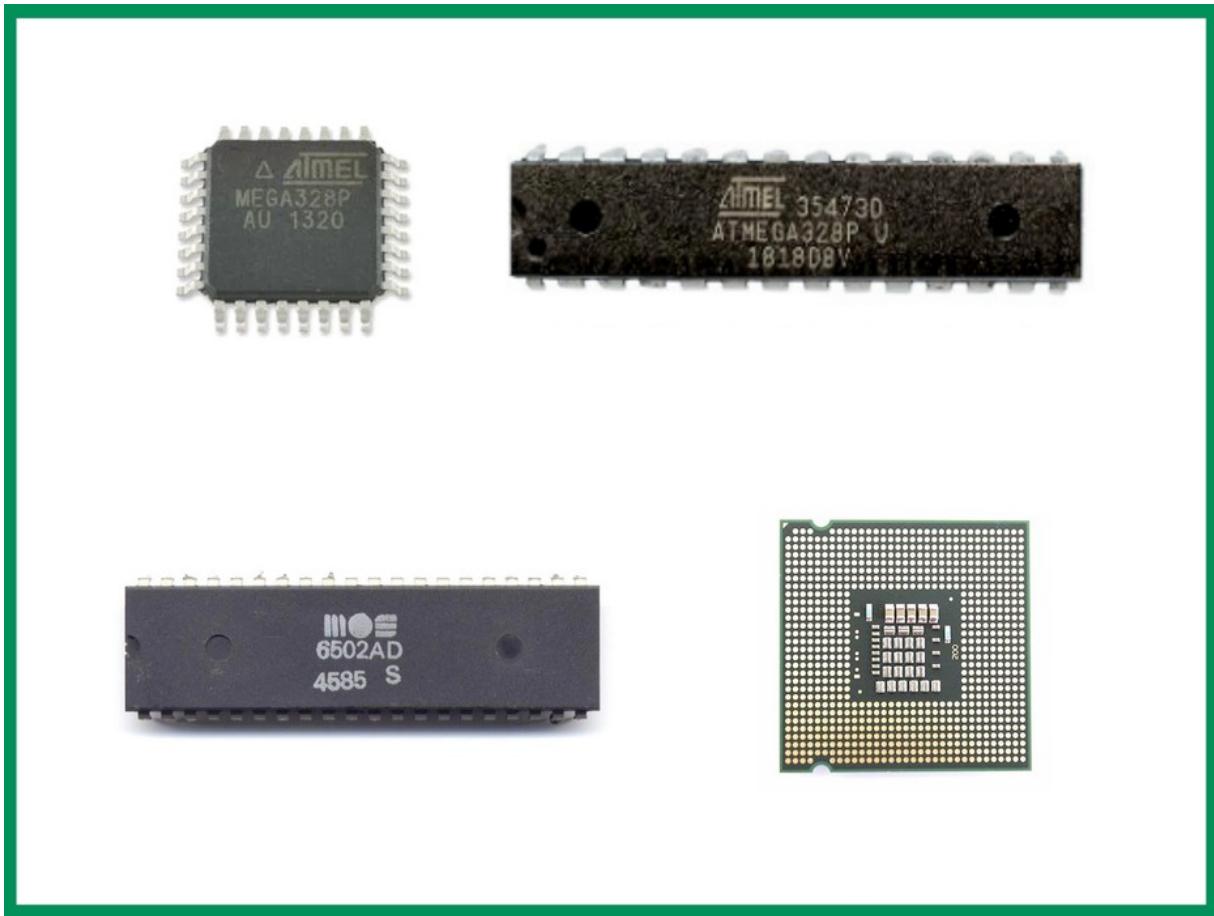
Our circuit can be updated with the addition of an ON-OFF slide switch. The switch can turn the flow of electrons on and off so that the LED is illuminated or not illuminated.

## Step 4: Control Electron Flow With a Pushbutton



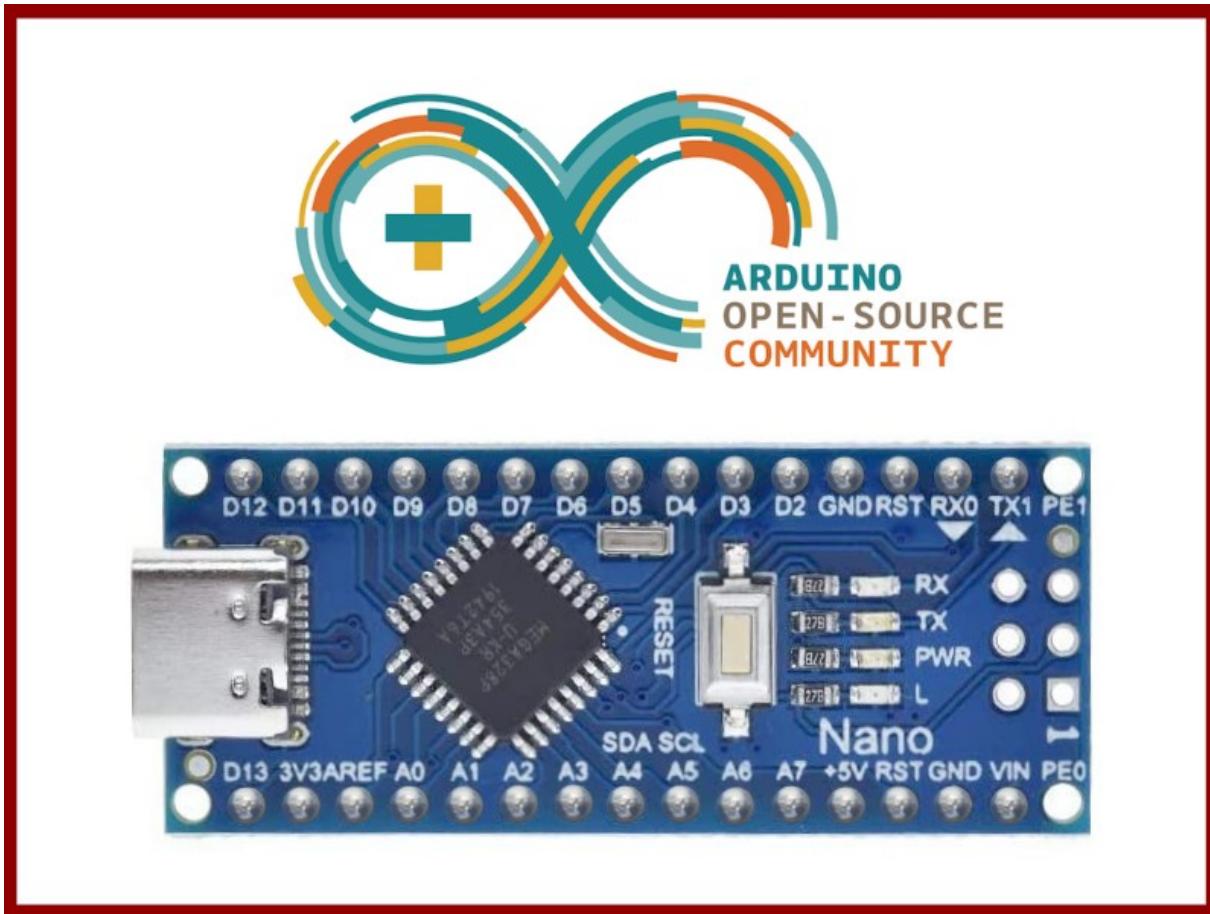
Replacing the slide switch with a momentary pushbutton allow the flow of electronics to occur when the pushbutton is pressed. The flow of electronics is blocked when the button is released opening the circuit.

## Step 5: Microcontrollers



A microcontroller or microcontroller unit (MCU) is a small computer on a single integrated circuit (IC) chip. A microcontroller contains one or more CPUs (processor cores) along with memory and programmable input/output peripherals. Program memory in the form of flash memory and/or ROM is also often included on chip, as well as a small amount of RAM. Microcontrollers are designed for embedded applications, in contrast to the microprocessors used in personal computers or other general purpose applications consisting of various discrete chips. Modern MCUs often integrate one or more advanced peripheral blocks such as graphics processing units (GPU), Wi-Fi modules, or coprocessors. ([wikipedia](#))

## Step 6: Set Up the Arduino Nano



The microcontroller we'll be working with here is the ATmega328P, which is part of the Arduino Nano module that we've already placed on the solderless breadboard.

The software we will use to program and interface with the Arduino Nano is called the Arduino IDE. Let's [download and install it now](#).

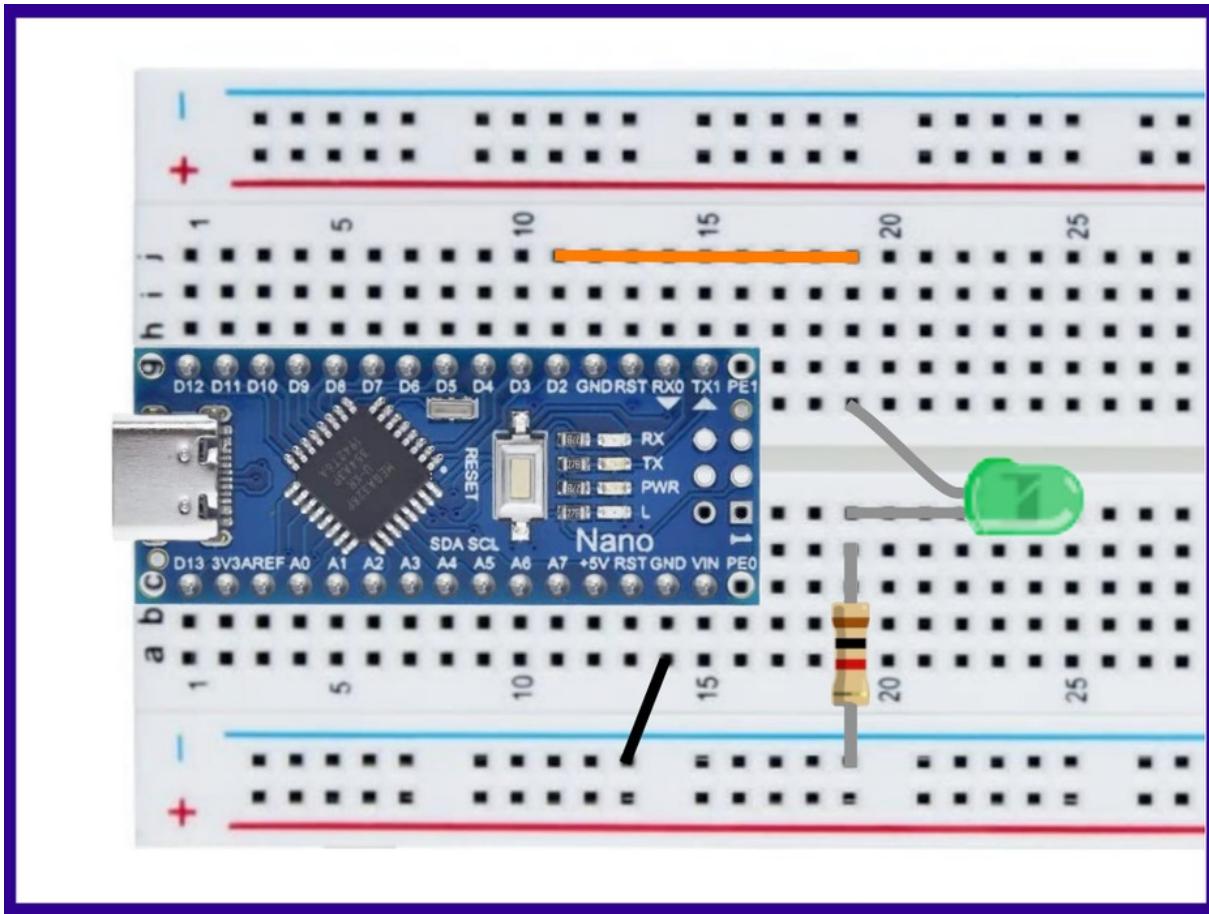
1. Connect the Arduino Nano to a USB port of your computer
2. Run the Arduino IDE
3. In the IDE, select Tools > Board > Arduino Nano
4. Also select Tools > Processor > ATmega328P (Old Bootloader)
5. Also select Tools > Port > (the USB port connected to the Nano)

Troubleshooting:

If there are multiple USB ports to select from, you can do a little test. One of the ports will disappear from the list when you unplug the USB cable from the Nano and then navigate back into the Tools dropdown menu again. That one that disappears is the port connected to the Nano.

If there are no USB ports to select (or at least there is no port that disappears when unplugged), you may need to install a driver for the USB chip on the Nano module. This chip is the CH340 which have a driver included in most modern operating systems, but there is more information [here](#) if you need it.

## Step 7: Control Electron Flow With Program Code



Disconnect the power from the Arduino Nano (unplug the USB cable) and wire up the circuit shown here. This circuit is exactly like the one used in Step 2 with one important distinction. The wire connecting to the long pin of the green LED connects to the MCU I/O pin D2 instead of connecting to +5V.

Pin D2 is an INPUT/OUTPUT (I/O) pin which means that the MCU can input or output signals through it. In order to operate the LED, the pin will be used as an output. More specifically, a digital output. A digital output can only be set to HIGH (5V) or LOW (GND).

You can probably guess that when Pin D2 is set to HIGH (5V) the green LED will be illuminated as it was in Step 2. When Pin D2 is set to LOW (GND) the green LED will not be illuminated. This is a lot like using a switch but instead of having to flip the switch on or off, the LED will now be under program control.

So let's write a program. Select File > New in the IDE. In a new, empty sketch there are two empty functions: `setup()` and `loop()`.

Inside setup() type:

```
pinMode(2, OUTPUT);
```

This tells the chip that we will use ARDUINO PIN 2 as an output from the chip.

Inside loop() type:

```
digitalWrite(2, HIGH);
```

This tells the chip to output a HIGH value (5V) to ARDUINO PIN 2.

Click the arrow above the code window to compile the code and upload the program into the Arduino Nano board. The first time you compile a new program, the IDE will ask you to select the folder you want it saved to and also to give it a file name.

During download, the small LEDs on the Arduino Nano module will flicker briefly. Finally the green LED, which you have wired to the D2 pin will light up and glow steady. Congratulations! You just wrote and uploaded your first microcontroller program.

You may have noticed that the tiny red LED on the Arduino Nano has stopped flashing. That is because the program that was flashing the LED has been replaced with your new program that turns on pin D2 and lights up the LED attached thereto.

Change the word HIGH in your program to LOW and then upload the program again. As may seem obvious, this will turn the LED off.

## Step 8: Looping and Timers

The diagram shows a code snippet for an Arduino sketch. It starts with a macro definition `#define ledPin 2`. This is annotated with a yellow arrow pointing to it and the text "The LED is connected to I/O pin #2". The sketch then defines a `setup()` function which sets the pin mode to output using `pinMode(ledPin,OUTPUT)`. This is annotated with a yellow arrow and the text "Use pin #2 as an output". The sketch also defines a `loop()` function. Inside the `loop()` function, the LED is turned on with `digitalWrite(ledPin,HIGH)`, annotated with a red arrow and the text "Put 5V (HIGH) on pin #2". It then waits with `delay(1000)`, annotated with a red arrow and the text "wait one second". The LED is then turned off with `digitalWrite(ledPin,LOW)`, annotated with a red arrow and the text "Put 0V (LOW) on pin #2". It waits again with `delay(1000)`, annotated with a red arrow and the text "wait one second". A large orange oval encloses the entire `loop()` function, with an arrow pointing back to the start of the loop and the text "Loop around, doing it forever!".

```
#define ledPin 2

void setup()
{
    pinMode(ledPin,OUTPUT);
}

void loop()
{
    digitalWrite(ledPin,HIGH); // Put 5V (HIGH) on pin #2
    delay(1000); // wait one second
    digitalWrite(ledPin,LOW); // Put 0V (LOW) on pin #2
    delay(1000); // wait one second
}
```

Let's try a more complicated program. Clean up the program from the last step to look exactly like the one in the image here.

First, we'll define a macro `ledPin` as 2 to represent the I/O pin 2 (aka D2) that the green LED is wired up to.

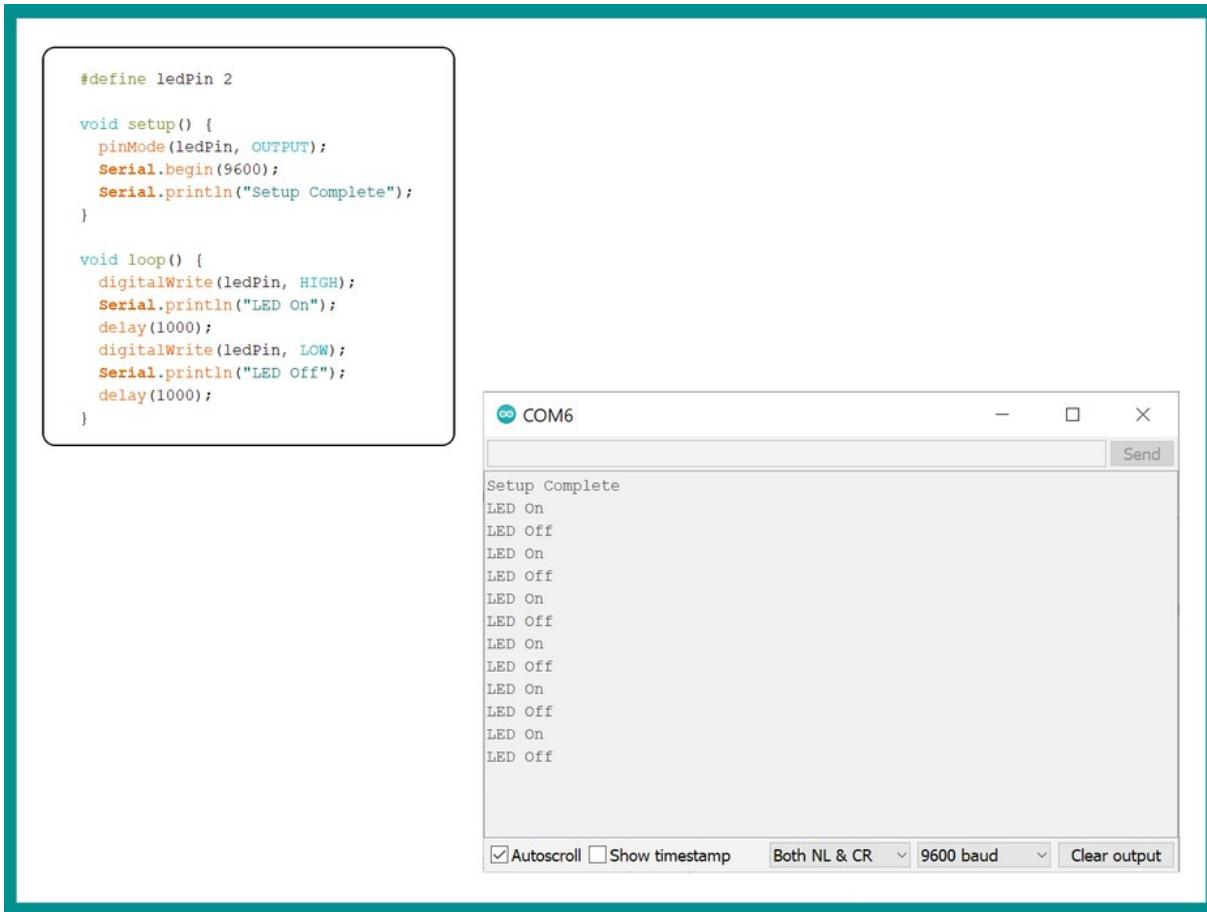
The `loop()` function loops around forever and ever. In each pass, the LED is turned on, we wait for a delay of 1s (1,000 milliseconds), the LED is turned off, we wait for a delay of 1s, and then we loop around and do it again.

Once you test out this code on the Nano, play around with changing the delay parameters from 1,000 to 100, or 500, or 2,000. Remember these delays are a number of milliseconds.

Note that the two delay numbers do not need to be the same. Try setting the LED on for 200 and then off for 2,000. Does the LED flash pattern match what you expect from your program.

Change both delays back to 1,000 and then also change the ledPin value from 2 to 13. The tiny red LED on the Arduino that was originally flashing when we first powered the module is attached to pin D13, so this final change returns the Arduino Nano to how we found it - with the tiny red LED slowly flashing on and off.

## Step 9: Program Output to Serial Monitor



The image shows the Arduino IDE interface. On the left, there is a code editor window containing the following sketch:

```
#define ledPin 2

void setup() {
  pinMode(ledPin, OUTPUT);
  Serial.begin(9600);
  Serial.println("Setup Complete");
}

void loop() {
  digitalWrite(ledPin, HIGH);
  Serial.println("LED On");
  delay(1000);
  digitalWrite(ledPin, LOW);
  Serial.println("LED Off");
  delay(1000);
}
```

On the right, there is a Serial Monitor window titled "COM6". The monitor displays the following text:

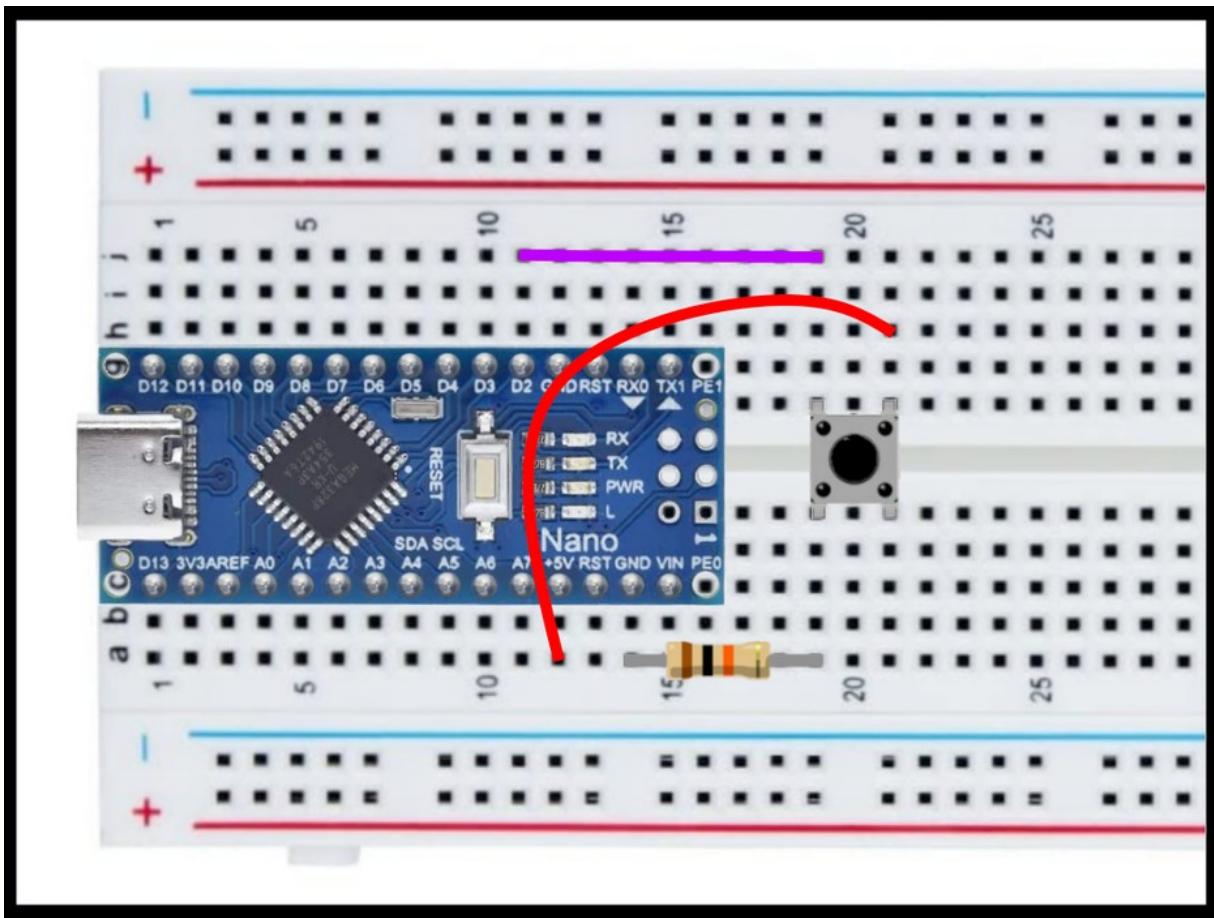
```
Setup Complete
LED On
LED Off
```

At the bottom of the Serial Monitor window, there are several configuration options:

- Autoscroll
- Show timestamp
- Both NL & CR
- 9600 baud
- Clear output

Update the code to reflect what is shown in the image. Note that the setup and LED state change are now also output to the serial port. Program the Nano and then open Tools > Serial Monitor to see the output over the MCU's serial port. Printing output to the serial port can be useful for simple program debugging.

## Step 10: Read Program Input From a Pushbutton



Wire the button and a 10K resistor to the Nano as shown. See the below *ReadButton.ino* sketch file and program it to the Arduino Nano. Again open the Serial Monitor to view the output printed over the Nano's serial port.

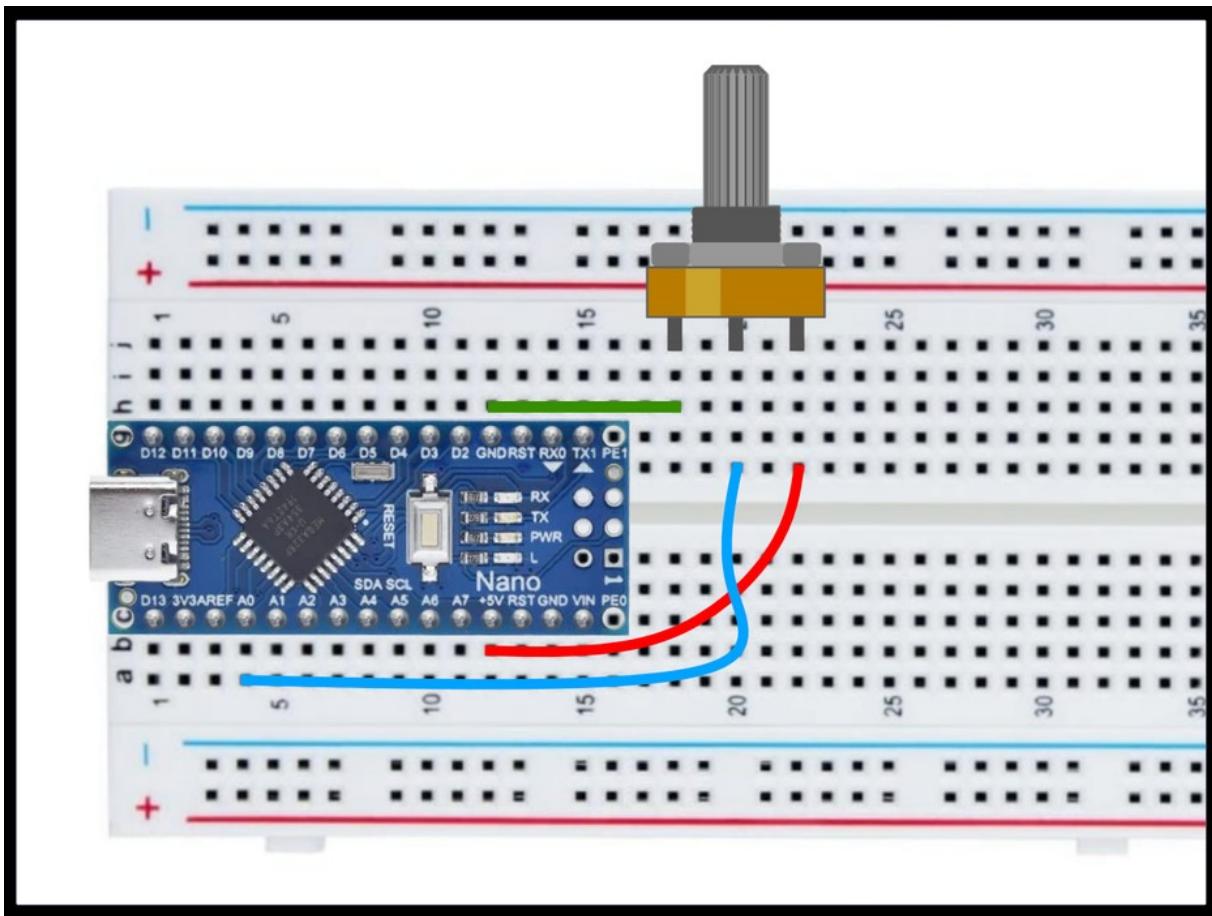
## Step 11: Digital Vs. Analog



On and off signals - switch on and off - button pressed or not - LED on or off are DIGITAL they are only on or off - one or zero.

Analog signals (like the state of a light dimmer knob) can take on many values besides simply on and off - one and zero. Of course, values in a computer are only digital (ones and zeros) so analog values from the real world are still stored and processed within a computer as digital numbers. Those numbers just have a wider range of values other than just high and low (one and zero).

## Step 12: Reading Analog Input From a Potentiometer



Wire the potentiometer (viable resistor) to the Nano as shown. See the below *ReadAnalog.ino* sketch file and program it to the Arduino Nano.

Open Tools > Serial Monitor

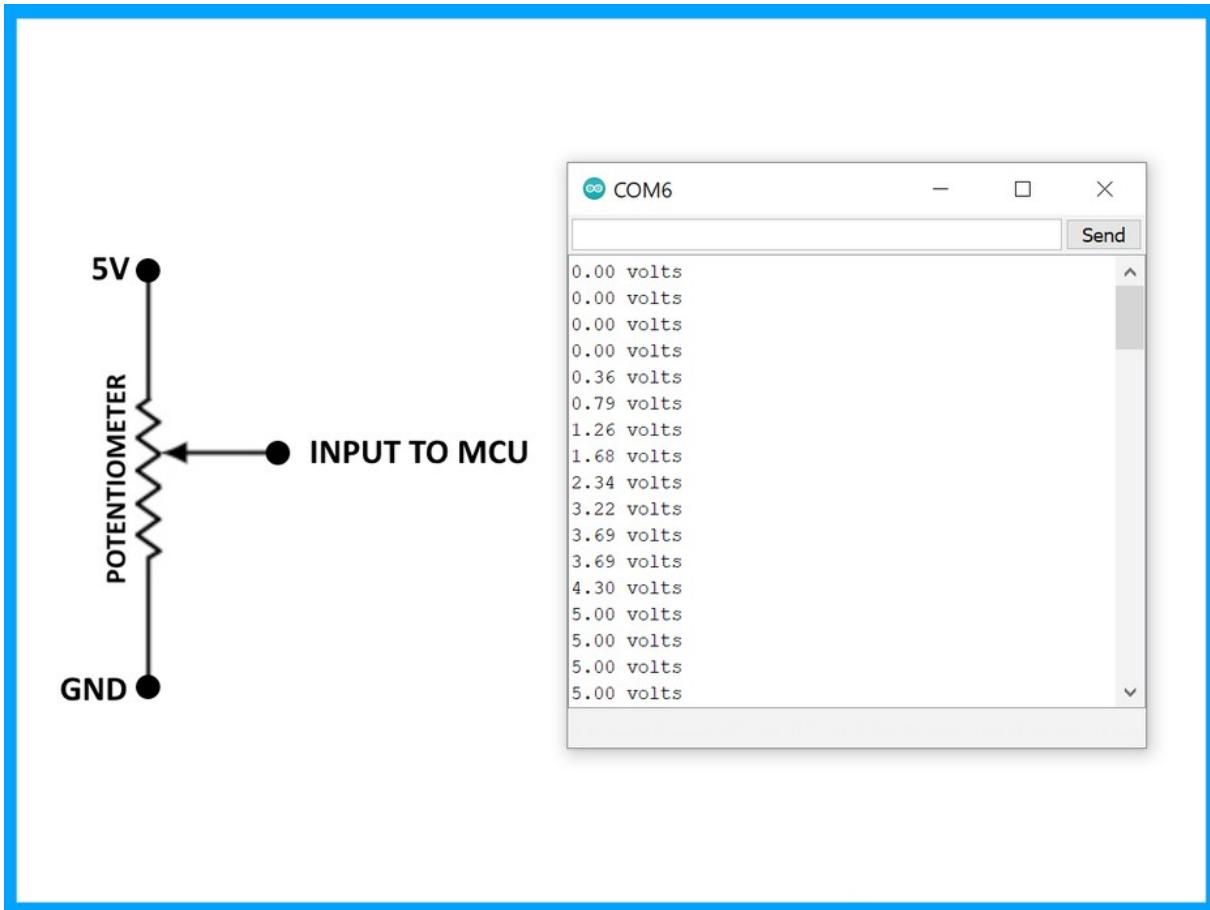
Slowly turn the potentiometer to see the values change in the serial monitor

Close the serial monitor

Open Tools > Serial Plotter

Slowly turn the potentiometer to see the plot trace change in the serial plotter

## Step 13: Measuring Voltage



Reading analog values is quite interesting because it is how we get real world data into the MCU. Reading when a button is open or closed (one or zero) is one thing, but reading a range of different values allows our program to "know" much more interesting signals than simply on and off. For example, these interesting signals may represent sounds, light, images, radio, and so forth.

Note that the values from the previous *ReadAnalog.ino* sketch range from 0 at one end of the potentiometer to 1023 when the potentiometer is turned all the way to the other end. What do these values mean?

The analog values from the potentiometer enter the MCU through an analog-to-digital converter (ADC). The ADC is actually reading the voltage at the input pin. The ADC represents the voltage using ten bits. Ten bits can hold two to the power of ten (1024) different values. Accordingly, the ADC represents the input voltage as a number between 0 and 1023.

The ADC value 0 (lowest value) represents 0 volts at the input pin. The ADC value 1023 (highest value) represents 5V at the input pin. Generalizing this conversion

scale to any ADC value, we can see that the ADC value may be multiplied by (5/1023) to convert the ADC value to voltage. That scaling factor of (5/1023) maps the 0-1023 input values to 0-5 volts.

Download the attached *ReadVoltage.ino* sketch file and program it to the Arduino Nano.

Open Tools > Serial Monitor

Slowly turn the potentiometer to see the values change in the serial monitor. Note that the range of displayed values is now 0.00 to 5.00 volts.

Let's look more closely at the sketch. It is very close to our last sketch with a couple of interesting changes...

The variable *analogValue* is still declared as type *int*, or an integer number. It will only take on values of whole numbers between 0 and 1023. In other words, *analogValue* will never be 1.5 or 2.7.

In contrast, the variable *voltage* is declared as type *float*, or a floating point number. It can take on decimal values. This is important because the integer read into the *analogValue* variable will not necessarily remain a whole number once it is multiplied by the scaling factor of (5/1023).

Look at the function call to output the numerical value *voltage* to the serial monitor. It is not *println* (print a line) like last time. Instead it is *print* (print a string). Then, the following line *Serial.print(" volts")* is used to append a space and the word *volts* after the number. Since the number output did not end the line (it was *print*, not *println*) the space and the word *volts* will be on the same line as the number. However, since the function call to *println* to outputs the space-volts string, it does end the line. This allows the next number printed to begin on its own new line.

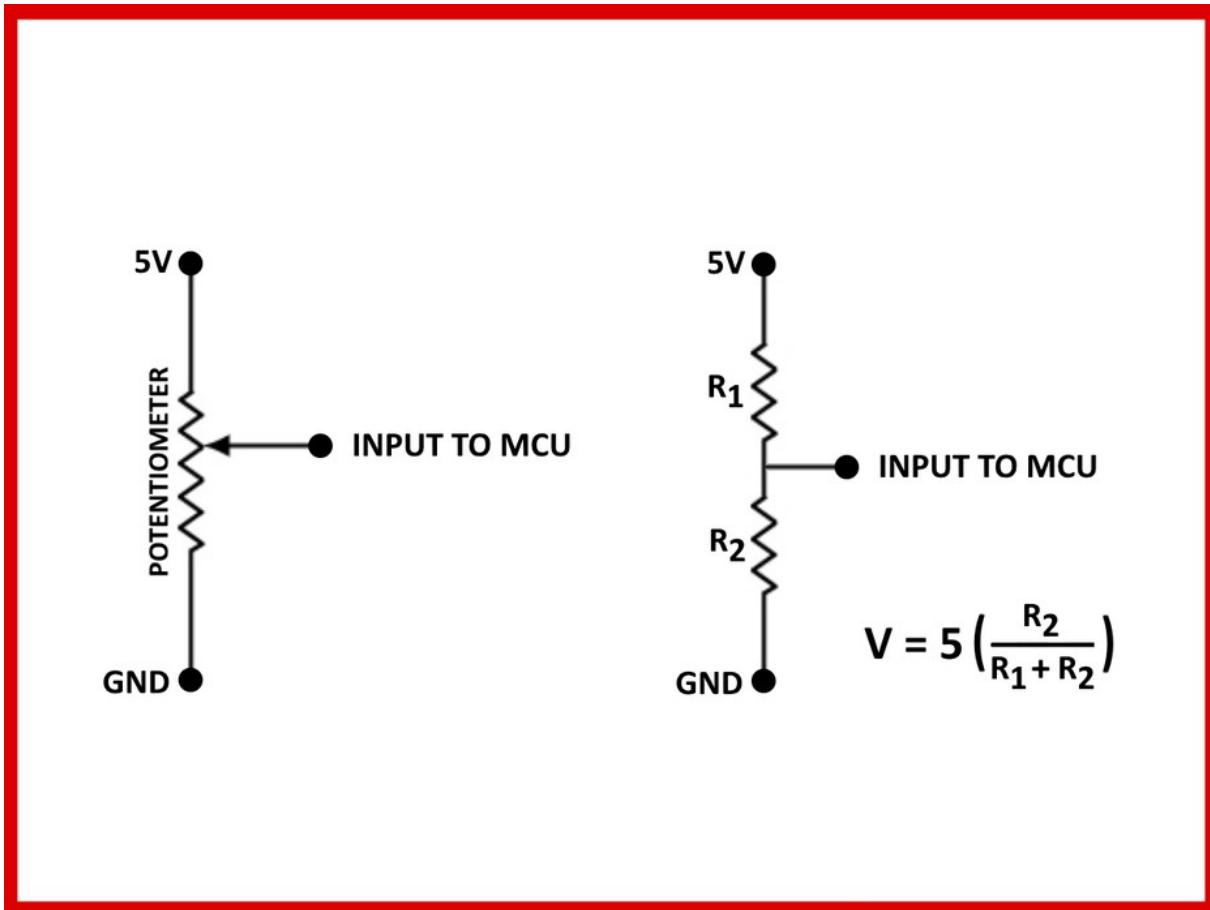
The subtleties of output formatting in computer programs are simple but complicated. They show us the multitude of actions that we take for granted when writing or typing. Our brains have just learned to do many things automatically, such as moving the pencil to the next line or hitting return at the end of a line. We must be more explicit about such things when writing computer programs.

```
# ReadVoltage.ino

void setup() {
    pinMode(A0, INPUT);
    Serial.begin(9600);
    Serial.println("Setup Complete");
}

void loop() {
    int analogValue = analogRead(A0);
    float voltage = analogValue * (5.0 / 1023.0);
    Serial.print(voltage);
    Serial.println(" volts");
    delay(250);
}
```

## Step 14: Voltage Dividers



The potentiometer we've been using has a total resistance of 10K ohms (10,000 ohms). As the schematic symbol implies, the potentiometer is actually a long 10K resistor connected between the two outer pins of the potentiometer. The center pin of the potentiometer connects to a wiper that sweeps across the length of the resistor as the shaft is rotated. The wiper effectively splits the resistor into two resistor portions that are connected in the middle at the center pin such that  $R_1 + R_2 = 10K$ . The allocation of the total 10K resistance between  $R_1$  and  $R_2$  is changed by rotating the shaft of the potentiometer.

If the potentiometer shaft is adjusted to its center point,  $R_1 = R_2 = 5K$ . This will equally divide the total voltage. The total 5V will be divided in half and the ADC will see 2.5V at the input pin.

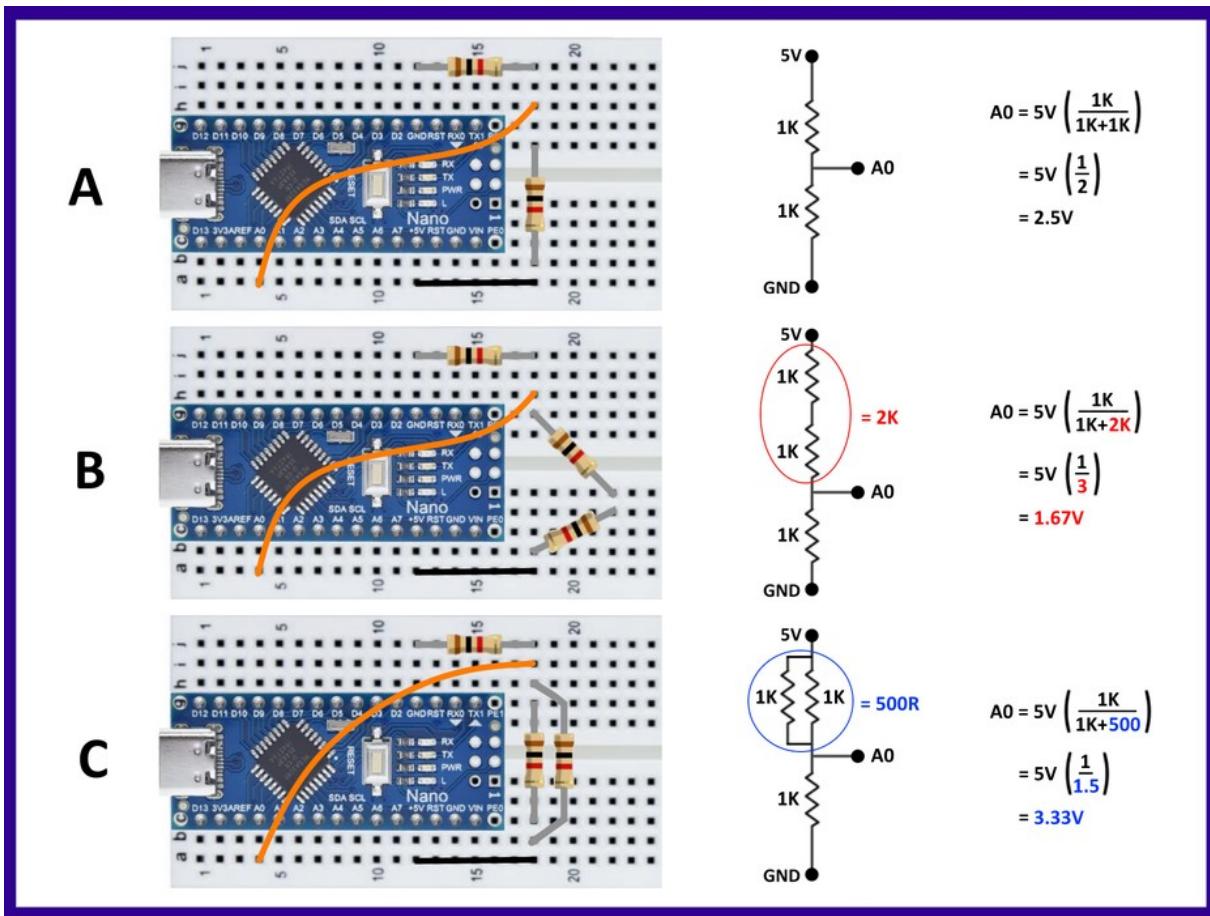
This structure of two resistances with an output tapped between the resistances is common and very useful. It even has a special name: **voltage divider**. The two resistances of a voltage divider can be the two portions of a potentiometer, two separate resistor components, or various other resistive loads. An example voltage

divider we will use later will have one resistor and one sensor that changes its resistance based on whatever it is sensing.

The formula shown in the image illustrates how the values of the two resistances R1 and R2 determine how the total voltage (5V in this case) gets "divided" to create the output voltage being measured. Don't worry too much about all of the math for now, you will encounter this structure again and again and it will eventually click into place.

Useful trick: The value of an unknown resistor can be determined by creating a voltage divider including the unknown resistor and a known resistor. The ADC is then used to measure the voltage output from the voltage divider. The measured voltage is plugged into the formula allowing us to calculate the unknown resistance.

## Step 15: Resistor Structures



**Case A:** If we remove the potentiometer and replace it with two equal 1K resistors R1 and R2, the division of total voltage will be exactly half (2.5V) just as when we set the potentiometer to its midpoint creating two equal R1 and R2 resistive portions. Set this up on the breadboard and try it out. The *ReadVoltage.ino* sketch file is still useful for this experiment.

**Case B:** Replace the 1K resistor R1 from Case A (that's the resistor between A0 and 5V) with a 2K resistor to establish the illustrated voltage divider ratio. But wait, we don't have a 2K resistor! Luckily, resistances add up in series, so two 1K resistors placed in series are equivalent to one 2K resistor. Set this up on the breadboard and try it out.

**Case C:** Replace the 1K resistor R1 from Case A (that's the resistor between A0 and 5V) with a 0.5K (500 ohm) resistor to establish the illustrated voltage divider ratio. But wait, we don't have a 500 ohm resistor! Luckily, two equal resistors become half of the original resistance when arranged in parallel. Two 1K resistors placed in parallel are equivalent to one 500 ohm resistor. This "parallel halving" can be conceptualized as

twice the current passing through two parallel pipes (or resistors) than would pass through only one of them. The effective doubling of pipe width in the parallel structure cuts the resistance in half.

Techniques using various resistor configurations (also called resistor networks) are useful to modify voltage levels and bend electricity to our will.

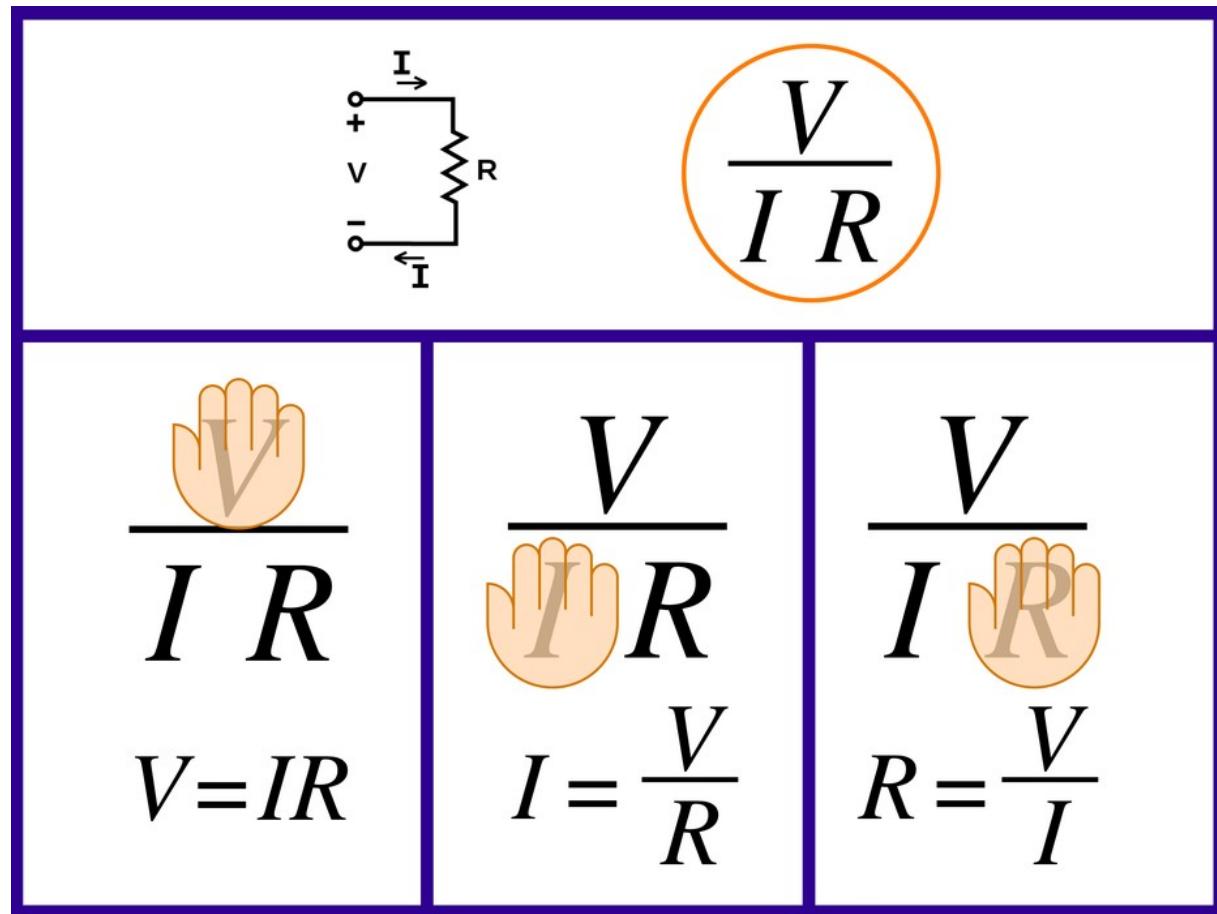
**Some questions to ponder:**

What is the equivalent resistance of THREE parallel 1K resistors?

What is the equivalent resistance of a 1M (one million) resistor in series with a 0.1 ohm resistor? Are both resistors really necessary? Would such a structure ever be found in a commercial product?

What is the equivalent resistance of a 1K resistor in parallel with a 10K resistor?  
Warning: This one is tricky. It will probably require a little research if you want to attempt the challenge, but the payoff is that you will also discover the theory behind why the two parallel 1K resistors in Case C above combine to form a 500 ohm resistor.

## Step 16: Ohm's Law



A lot of attention is paid to voltage, current, and resistance because the three quantities are related in a simple, reliable way. Let's dig deeper...

**Voltage (V)** is the difference in electric potential energy between two points. To make an analogy, when talking about mass, gravitational potential can be thought of as how high something has been raised off the ground and thus how much energy it has to release when it falls to the ground. Similarly, a charge at 5V potential has more energy to expend getting to 0V (ground) than does a charge at only 2V. Voltage is sometimes called "electrical pressure" because it is a bit like water pressure. To give the tap water in your house pressure as it flows out of the faucet, water is often pumped uphill to a water tower. The higher the tower (gravitational potential above the ground), the more pressure or the harder water can push through the pipe. Similarly, the more voltage (electrical potential raised above ground), the harder the electrons can push through the wires.

**Electrical Current (I)** is very similar to the notion of water current in a river or a pipe. Current is how much stuff (electrons in this case) flow through per unit time. For

example, gallons-per-minute of water or charges-per-second of electricity.

**Resistance (R)** can be thought of as the “tightness” of the pipe. The narrower the pipe is (higher resistance), the less current flows through for a given potential (voltage). You can make more current flow through a pipe by pushing it harder (higher voltage) or opening the pipe up (less resistance).

The relationship between these three qualities is formalized as **Ohm's Law**:

$$V = I \times R$$

where voltage (V in volts) equals current (I in amperes) times resistance (R in ohms).

If you are not a fan of algebra, a useful mnemonic tool is illustrated here. Starting with the "V over IR" expression in the orange circle, we can simply over the parameter we'd like to know and the remaining two parameters display the necessary calculation to find the desired parameter.

How much current flowed through our 10K potentiometer when it was connected between 5V and Ground?

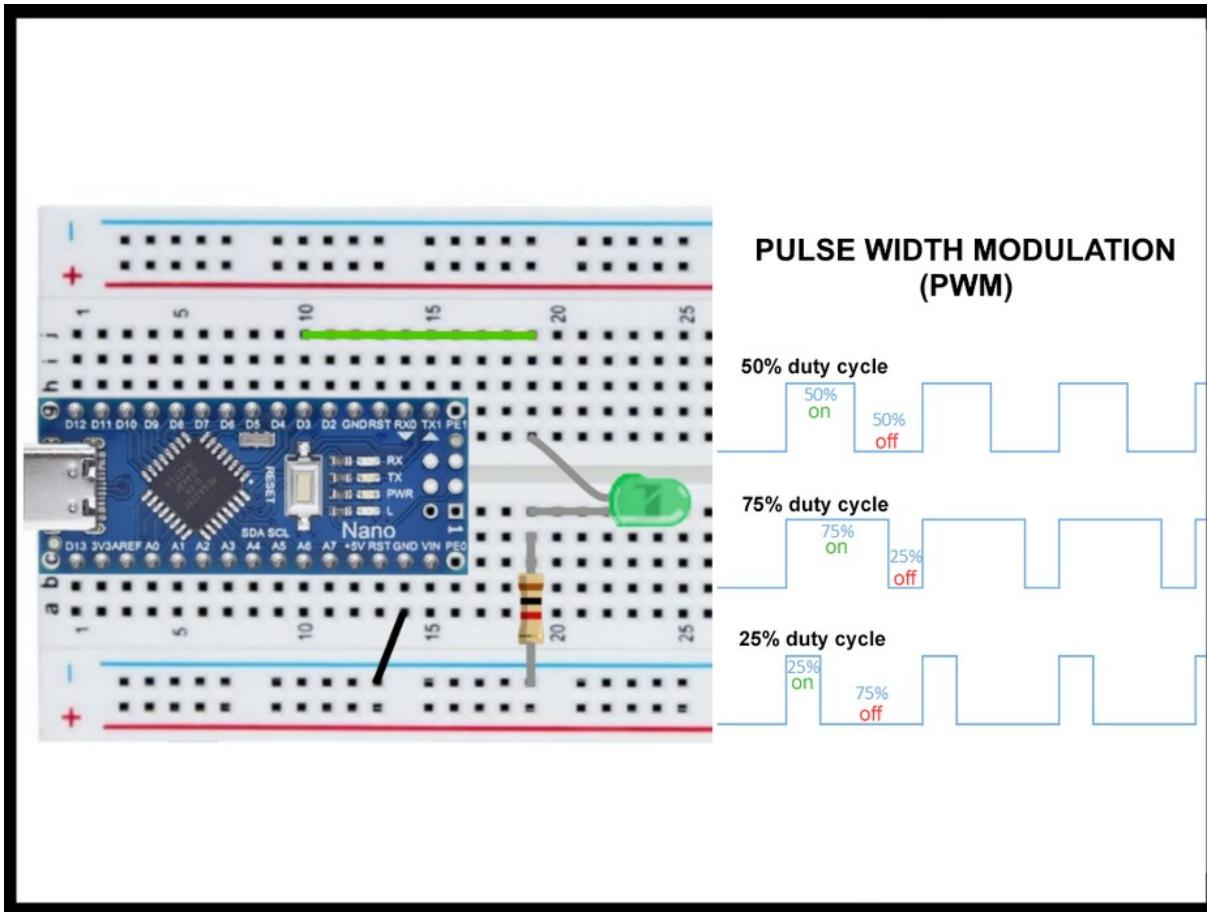
$$5V = \text{Current} \times 10,000 \text{ ohms}$$

$$\text{Current (I)} = 5 / 10,000 = 0.0005 \text{ A} = 0.5 \text{ mA}$$

This may seem very small, but keep in mind that the pins of a digital silicon chip (like our MCU) really do not like to supply (or sink) a lot of current. This is part of why we've been placing a "current limiting resistor" in series whenever connecting an LED to the MCU.

Note that the same amount of current flowing through the long 10K resistor of the potentiometer also flows through each of the potentiometer's resistive portions R1 and R2. This is due to a generalization of the law of conservation of charge: "current in" generally equals "current out". The more water you drink, the more you will probably need to visit the restroom.

## Step 17: Adjusting Light Brightness



Build this circuit. It's the same one we used in Steps 7, 8, and 9 with one important difference. The MCU output is now set to pin number 3 instead of pin number 2. Why is that? Pin 2 does not support PWM but pin 3 does. We'll get to why that's important for this experiment.

You might think that we can just dim a light (or otherwise adjust its brightness) by changing the voltage on it. Well, that might be true in some cases, but LEDs conduct exponentially, so we can think of them as only being "all on" or "all off". Furthermore, our simple MCU does not have a DAC (digital to analog converter). Many MCUs do have DACs, but this one does not. Without a DAC, the MCU cannot actually make an analog value, but only on (5V) and off (0V).

If you download the *LEDdimmer.ino* sketch and have a look, you will notice the use of a function called *analogWrite()* even though there is no analog output on this MCU.

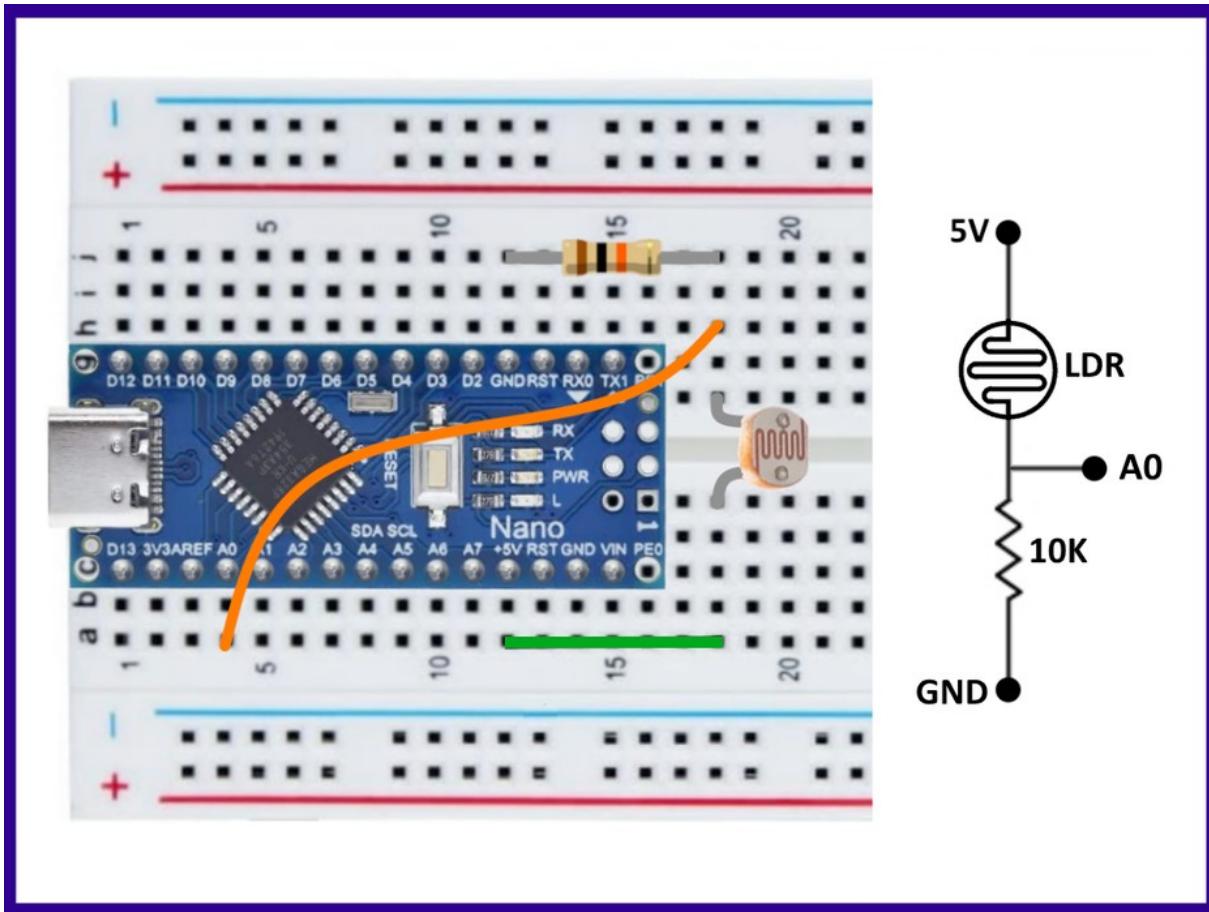
What is going on when we call *analogWrite()* is actually a trick that involves pulsing the output pin rapidly on and off. The duty cycle of this pulsing is what is adjusted to create what seems sort of like an analog signal. The output signal is only ever 0V or

5V (never actually analog) but the duty cycle specifies what percentage of time that the pulsing signal is high versus low. This technique is called **PWM (pulse width modulation)**. Example PWM waveforms are illustrated in the image.

The *analogWrite()* function can be called with the value 0 (pulsing always low or 0V), the value 255 (pulsing always high or 5V), or any value between to specify what amount of the time the pulsing is high. The *LEDdimmer.ino* code uses the values 50, 150, and 250 to generate three different levels of brightness for our green LED. Even though we cannot see it, the PWM is actually pulsing the LED on and off very rapidly.

Feel free to try out other values or patterns or values. How about wiring up the potentiometer, reading the potentiometer from pin A0, scaling the value read to the range of 0-255, and then using that scaled value to drive the LED IO pin 3. Go ahead and give it a shot!

## Step 18: Light Sensors

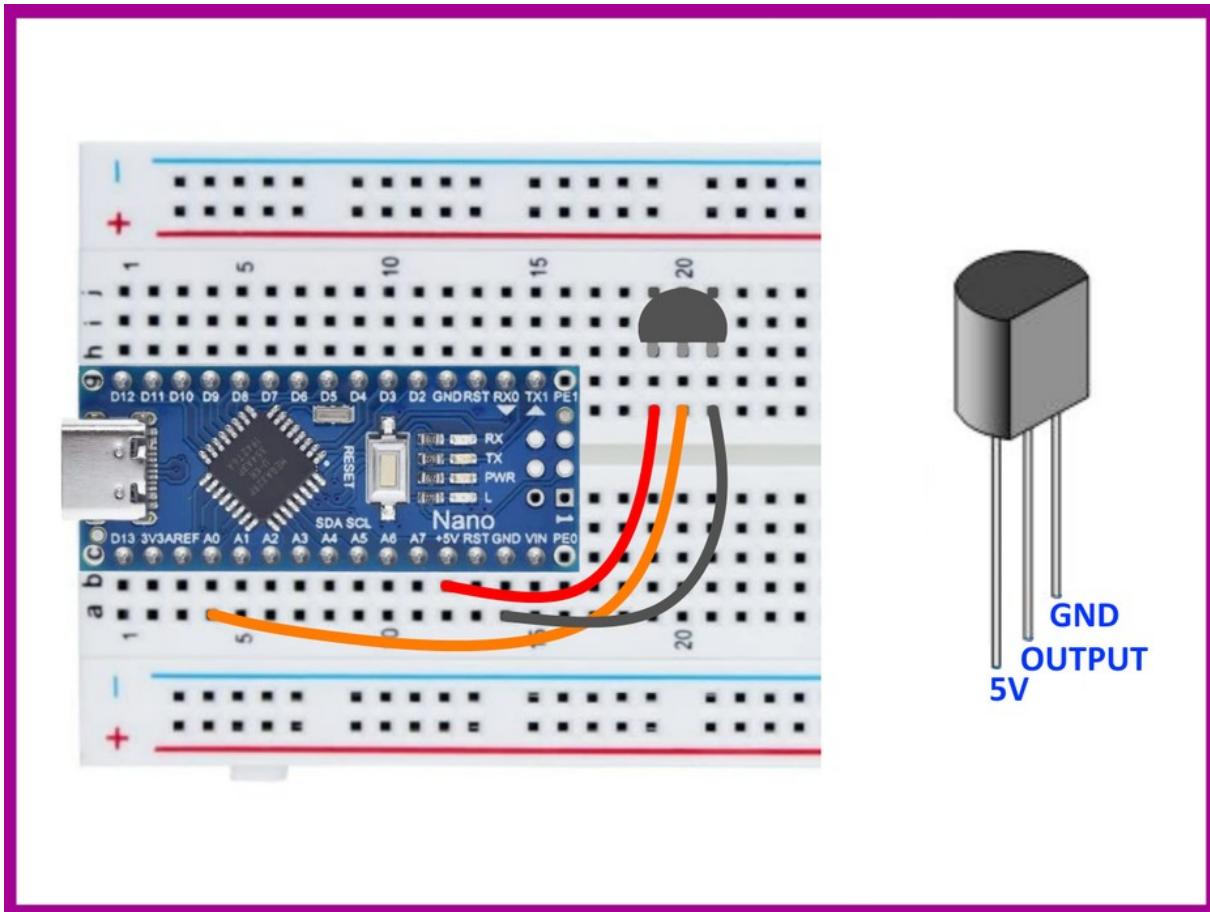


A common light sensor is a Photo Resistor, which is also known as a Photo Cell or Light Dependent Resistor (LDR). An LDR is a resistor with a resistance that decreases when brighter light shines upon its photosensitive surface.

Wire up the Photo Resistor and a 10K Ohm Resistor in a Voltage Divider structure as shown. Connect the output of the Voltage Divider to pin A0 of the Nano as shown. Use the *ReadVoltage.ino* sketch to read and display the output of the voltage divider. Open the Serial Monitor to view the output printed through the Nano's serial port. Notice now the voltage changes when the Photo Resistor is shielded from ambient light or when a brighter light shines upon it.

Can you figure out what will happen if you swap the LDR and the 10K resistor around so they are on different sides of the voltage divider? Give it a ponder and then try it out to test your theory.

## Step 19: Temperature Sensors



Wire up the TMP36GT9Z Temperature Sensor ([datasheet](#)) to the Nano as shown. Be careful to identify the correct component from the part number on the flat surface of the body. Also be careful to correctly orient the component according the flat surface of the body.

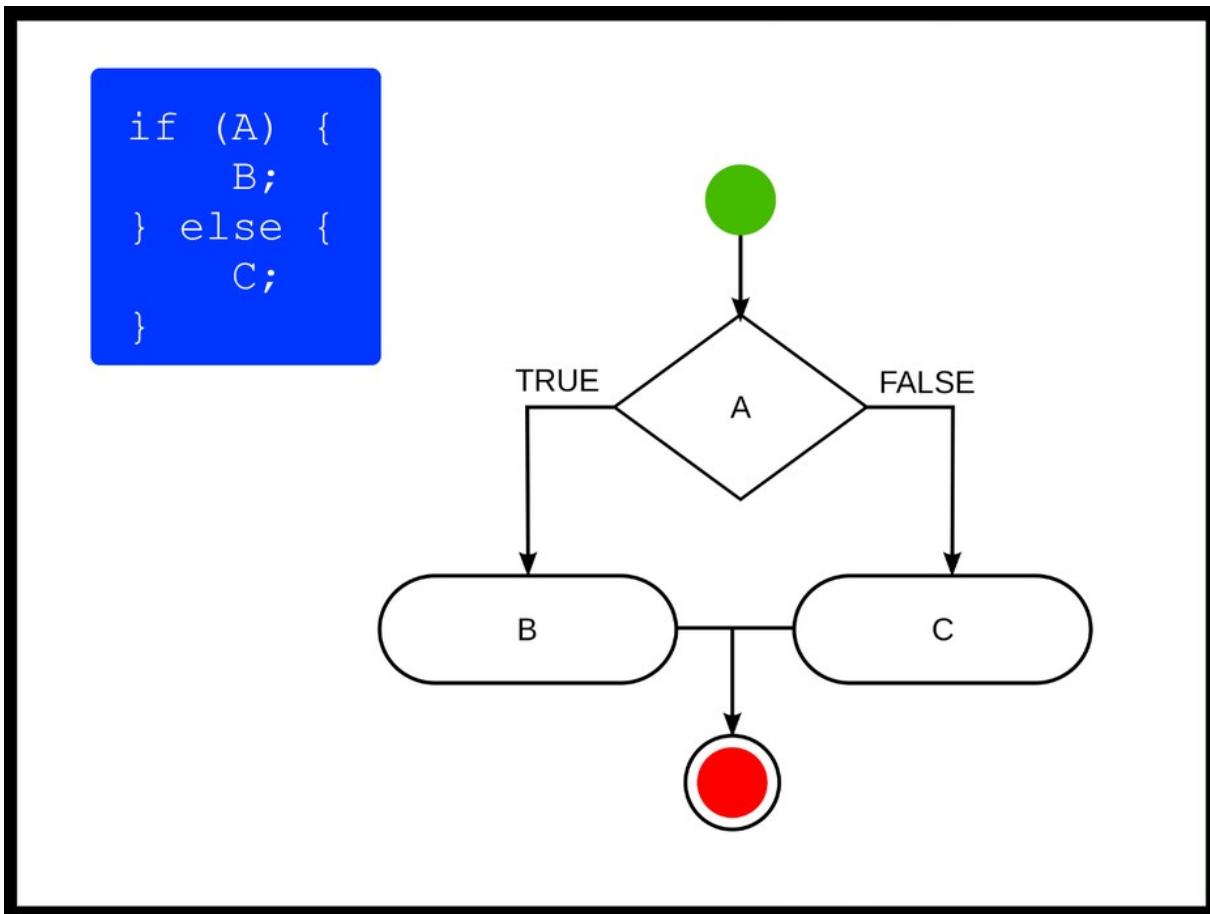
Download the attached *ReadTemp.ino* sketch file and program it to the Arduino Nano. Open the Serial Monitor to view the output printed over the Nano's serial port. You may notice that the measured temperature is close but not correct. Any variation is often due to the USB power supply voltage not being exactly 5.00V. Calibrating sensors against noise, power fluctuations, etc. is a common matter for careful attention in electronic design. For this education purpose, we will just accept that it is not perfect.

**Identifying the TMP36 Component:** Your parts kit includes SIX components that look like the one in the image. That "look" is called a TO-92 package component. TO-92 components generally have a small black body with one flat side and three leads extending from one end. TO-92 components are often automatically identified as

transistors. While some TO-92 packaged devices certainly may be transistors, not all of them are.

Of the SIX TO-92 components in the parts kit, ONE of them is the TMP36 Temperature Sensor and FIVE of them are 2N2222A Bipolar Transistors. Examining the flat surface of the component's body (perhaps with a magnifying lens) will reveal some very tiny printing that will indicate the difference between the TMP36 and 2N2222 devices.

## Step 20: Program Control Flow



Most of the program code we've looked at so far has simply used the `setup()` and `loop()` functions to control the flow of the program. Whatever we put in `setup()` happens once when the program starts. Whatever we put in `loop()` literally loops around and keeps happen for ever.

Looking at the `ReadButton.ino` sketch that we used earlier, you will see an if-else block. This is illustrated in the image above: If A is true, then do B. Otherwise (else) do C. Examine how that structure is used in the `ReadButton.ino` sketch to do different things when the button is pushed versus when the button is not pushed.

Sometimes we need more control. Let's consider some examples...

- sit and do nothing until an input is received
- keep doing something periodically until an input is received
- do something 10 times
- do something 10 times but stop if an input is received
- do something 10 times where each of those does something else four times
- receive a keyboard input and do different things based on which key was pressed

Download and run the *ControlFlow.ino* sketch attached here. The sketch demonstrates simple examples of the four most commonly used program control flow mechanisms: if, else, for, while. Carefully examine how they are used in the sketch.

More information on these four along with the other available control mechanisms (do...while, switch...case, return, break, continue, goto) can be studied in the Arduino Documentation under [Control Structure](#). Over time, you will encounter examples of these various forms. You will develop a feeling for which ones you like using for certain types of tasks. Many tasks can be accomplished just as well using two or three different control mechanisms, but some tasks lend themselves more to one specific type of control mechanism.

**Program Comments** (also called **inline documentation**) are important notes placed inside a program while writing it. They can tell others what the programmer was thinking when they wrote the program. They can also remind the programmer what is going on when they look at the code again later. Notice the comment block at the top of the *ControlFlow.ino* sketch demonstrating the use of // and /\*...\*/ structures for commenting your code. Commenting your code is more important than you might realize right now. Trust us... learn it, love it, do it.

## Step 21: Storing Data in Arrays

The screenshot shows the Arduino IDE interface. The top bar displays "DataArrays | Arduino 1.8.19". The menu bar includes "File", "Edit", "Sketch", "Tools", and "Help". Below the menu is a toolbar with icons for back, forward, file operations, and a search function. The main code editor window contains the following C++ code:

```
void setup() {
  Serial.begin(9600);
  Serial.println("Setup Complete");
}

void loop() {
  Serial.println("initialize an array of five integers:");
  Serial.println("int myArray[5] = {3, 4, 5, 6, 7}");
  int myArray[5] = {3, 4, 5, 6, 7};

  for (int c=0; c<5; c++){
    Serial.print("element ");
    Serial.print(c);
    Serial.print(" of myArray is ");
    Serial.println(myArray[c]);
  }

  Serial.println("The first element is index 0");
  Serial.println("The last element is index 4");
  Serial.println("There is no index 5");

  Serial.println(); //skip a line
  Serial.println("An array of characters is a string of text");
  Serial.println("char myString[]="my pet is a cat\"");
  char myString[]="my pet is a cat";
  Serial.println(myString);
  Serial.println("change element 12 from c to r");
  myString[12]='r';
  Serial.println(myString);

  while(1); //just wait forever
}
```

The serial monitor window on the right is titled "COM6" and shows the output of the sketch. It reads:

```
Setup Complete
initialize an array of five integers:
int myArray[5] = {3, 4, 5, 6, 7}
element 0 of myArray is 3
element 1 of myArray is 4
element 2 of myArray is 5
element 3 of myArray is 6
element 4 of myArray is 7
The first element is index 0
The last element is index 4
There is no index 5

An array of characters is a string of text
char myString[]="my pet is a cat"
my pet is a cat
change element 12 from c to r
my pet is a rat
```

At the bottom of the serial monitor, there are checkboxes for "Autoscroll" and "Show timestamp".

So far, we have used variables to store information. Variables have types like integer (int), character (char), or floating point (float).

Multiple pieces of related data can be stored in a collection called an array.

Each piece of data in the array is called an element and an index number is used to select the various elements. Just like a variable has a type, the elements of an array have types. In fact, all of the elements have the same type. So we say that it is an array of integers, or an array of characters, etc.

Download and run the *DataArrays.ino* sketch attached here. The sketch demonstrates a couple of examples of creating and using arrays. Carefully examine how they are used in the sketch.

First, an array of five integers is created (declared) and initialized:

```
int myArray[5] = {3, 4, 5, 6, 7};
```

Initializing means starting the array with its initial values preset. An array can also be created without initializing its values.

Examine how the for loop is used to index through the array named myArray. The index variable c counts from 0 to 4 to access each element of the array.

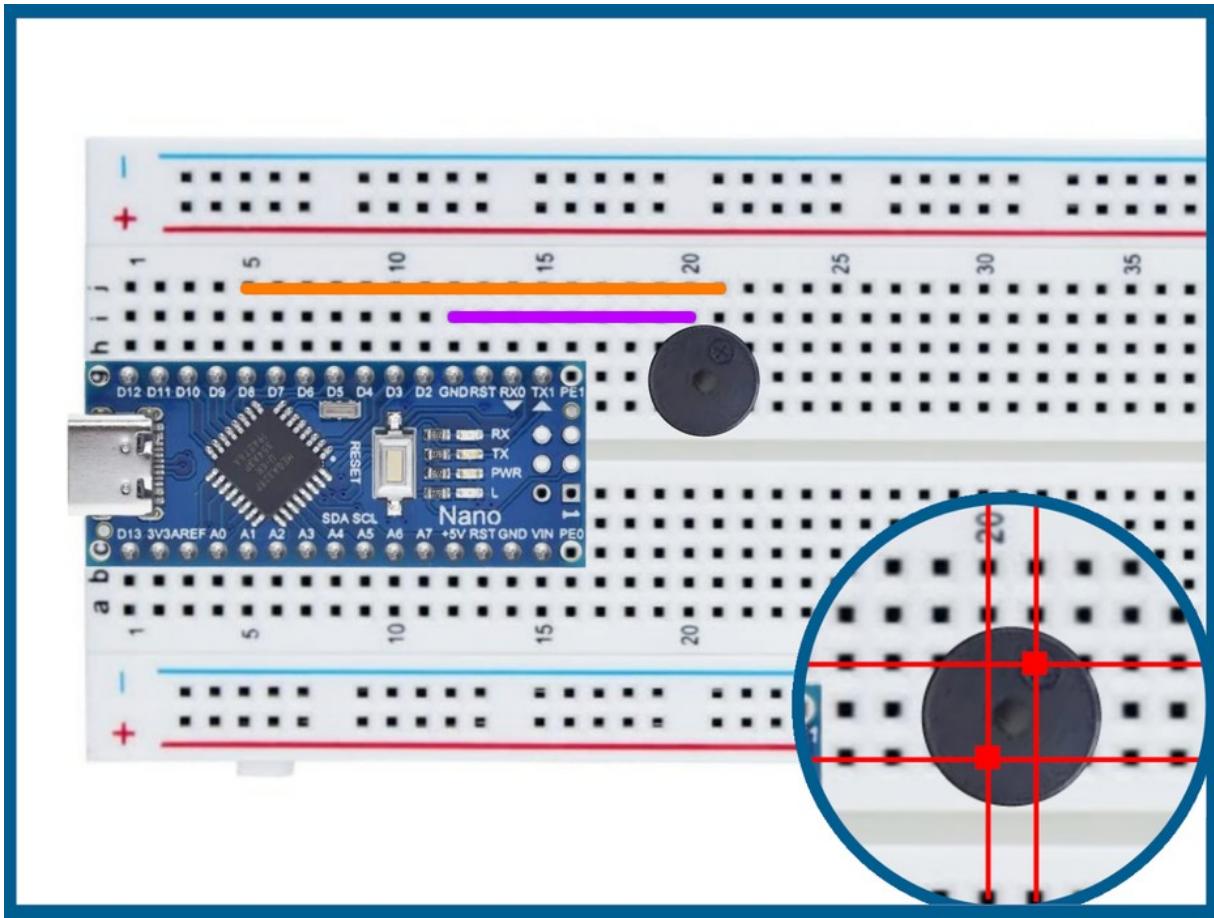
The second example shows how an array of characters can be used to store words. An array of characters is also called a [string](#), text string, or a string of characters.

Look at the last line of the loop() function:

```
while(1); //just wait forever
```

Since "1" is always true, this while() conditional will execute its contents forever. However, its contents are empty. There aren't even curly braces, just a semicolon. So "executing the contents of the while loop" really means "do nothing". Since "1" is always true, this simple line "does nothing" forever. Execution is just stuck right there (forever) so this line of code accomplishes "halting" the loop() function so that it doesn't keep looping. This is a simple trick that is worth remembering.

## Step 22: Generating Sound



Piezoelectric speakers (also known as piezo buzzers) generate sound using the piezoelectric effect. This is in contrast to the electromagnetic coils used to generate motion (vibrations) in a traditional speaker. Piezoelectric crystals physically deform slightly (compress or expand) when electricity is applied. Likewise, the crystals also build up electric charge in response to mechanical stress such as bending or squeezing.

The electrical deforming property of piezo crystals can be used to generate sound (vibrations). While that sounds is not high fidelity, it is very efficient. A piezo buzzer can be driven directly from an I/O pin without any amplifier circuitry.

Wire up the Piezo Buzzer to the Nano as shown. Since the pins of the buzzer do not have spacing that matches the solderless breadboard it is helpful to insert the buzzer at an angle as illustrated.

Download and run the *Sounds.ino* sketch attached here. The sketch demonstrates using the `tone()` command to generate sounds. The `tone()` can take three parameters:

```
tone(pin, frequency, duration)
```

The first parameter *pin* specifies which I/O pin the buzzer is connected to. The second parameter *frequency* specifies the frequency of the tone to generate, and the third parameter specifies for how long to generate it (in milliseconds).

After the five notes are played, there is a delay of four seconds before looping around to play the notes again.

## Using #define Preprocessor Directives

A `#define` is handled by the preprocessor before a program is even compiled. It simply replaces any instance of the first portion with the second portion. While it might seem like a variable, it is not. We cannot store anything in it or modify it at runtime. It doesn't even exist in the view of the compiler because it is handled as a preprocess. It is just a simple text replacement to make code easier to read and fixed values (such as constants and I/O pin numbers) easy to globally modify from one place.

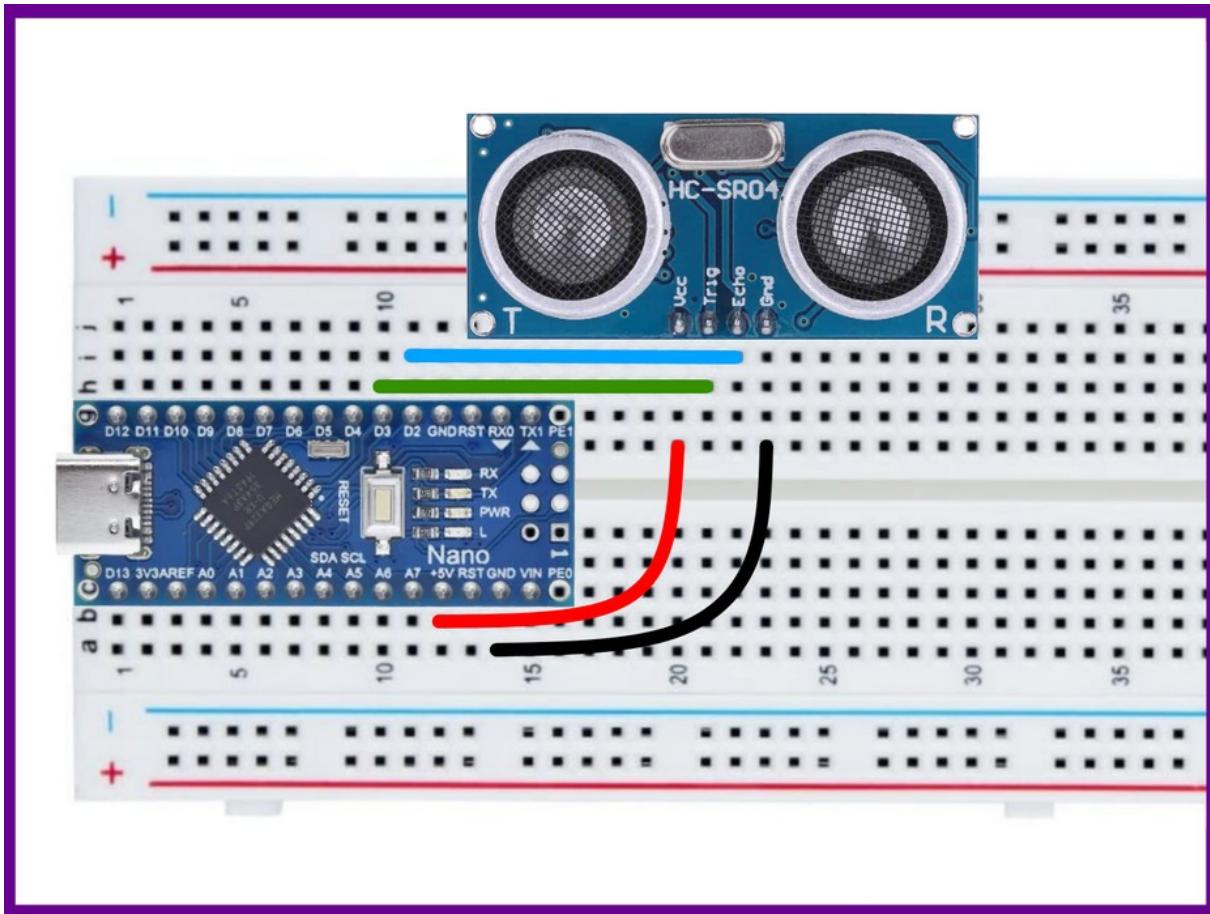
In the current example, five `#define` lines provide the frequencies (in Hz) for the notes to play:

```
#define NOTE_D7 2349  
#define NOTE_E7 2637  
#define NOTE_C7 2093  
#define NOTE_C6 1047  
#define NOTE_G6 1568
```

A few more `#define` lines specify the duration (in ms) for each note and the pause time that includes the note duration plus a little more to provide space between the notes. There is also a `#define` to represent the I/O where the buzzer is connected:

```
#define noteDuration 800  
#define notePause 900  
#define buzzerPin 8
```

## Step 23: Measuring Distance



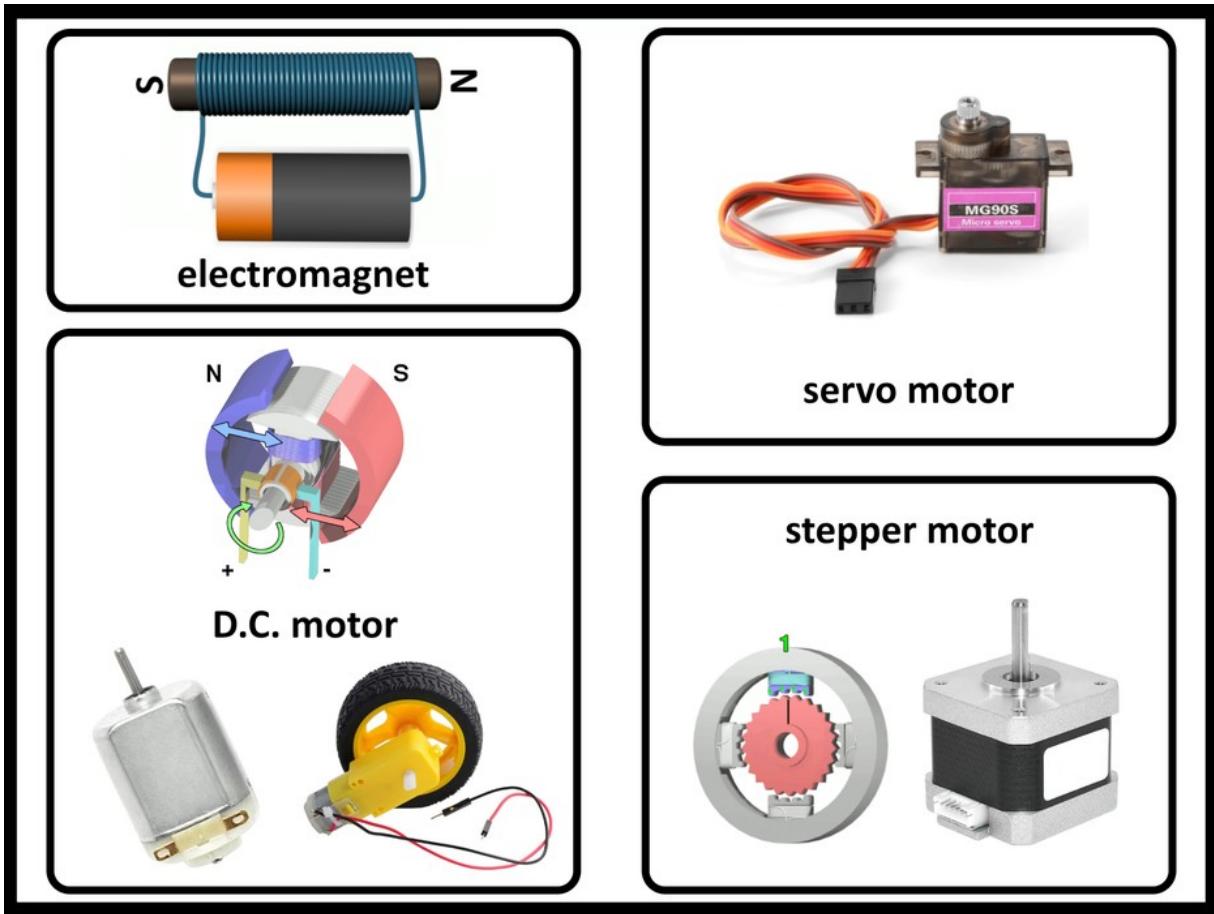
The HC-SR04 ultrasonic sensor module is like a bat. It includes a transmitter for radiating ultrasonic waves at 40kHz (40,000 Hz). The upper frequency limit of human hearing is around 20kHz so frequencies higher than that are called ultrasonic. The HC-SR04 module also includes a receiver to detect any ultrasonic waves that bounce back to it. The radiated ultrasonic waves propagate through the air and reflect off any surfaces they encounter. Some of the reflected waves bounce back to the module.

The microcontroller can measure the time between transmitting the waves and receiving the reflections. Comparing this echo time to the known speed of sound through air allows the microcontroller to calculate the distance from the sensor to the reflecting object.

Wire up the HC-SR04 ultrasonic sensor module to the Arduino Nano as shown. The trigger (trig) pin is used to tell the module to transmit its ultrasonic waves. The echo pin allows the module to tell the microcontroller when it detects the reflected (echo) of the ultrasonic waves.

Download and run the *Ultrasound.ino* sketch attached here. The sketch triggers a short pulse from the ultrasonic transmitter and then measures the amount of time for a reflected pulse to be detected at the ultrasonic receiver. Since that echo time is round-trip, it is divided by two to find the one-way trip duration. Finally, the one-way time is multiplied by the speed of sound to find the distance of the echo in centimeters. The distance is displayed on the serial monitor.

## Step 24: Electromechanical Motion



**Electromagnets** serve as the nexus between electricity and physical motion or movement.

An electromagnet is a type of magnet in which the magnetic field is produced by an electric current. Electromagnets generally have a wire wound into a coil around a core. When electrical current flows through the wire, such as from a battery, a magnetic field is created allowing the core to act much like a permanent magnet. However, the magnetic field disappears when the electrical current is not flowing through the wire.

The magnetic field can be turned on, off, or reversed using electricity. The magnetic field can be used to move (attract or repel) other physical objects or structures. Accordingly, physical motion can be generated, stopped, and reversed under electrical control.

**Direct current motors (DC motors)** are rotary motors that can be found in toys, tools, and appliances. The small, silver DC motor in the illustration is shown on its

own and as part of a yellow gearbox with an attached wheel. Such motors are often used in toys and hobby projects.

DC motors have an arrangement of coils (electromagnets) and permanent magnets that can convert electrical current into rotational motion. DC motors have structures that periodically change the direction of current in part of the motor thereby allowing the motion to spin around in a circle as the current changes.

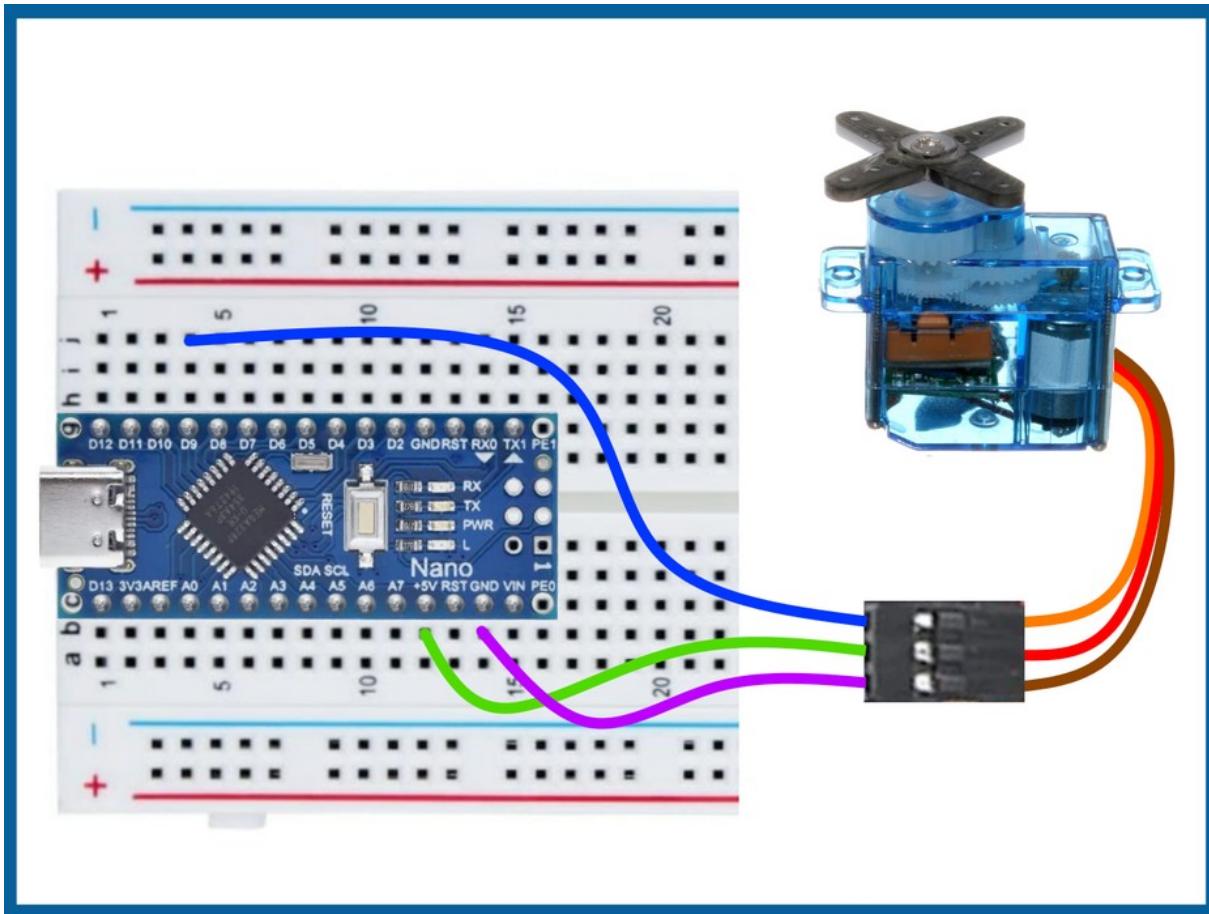
The diagram of a simple DC motor shows a stationary set of magnets around the outside called the stator. The diagram also shows windings of wire in the center forming electromagnets. This center can rotate and is called the rotor. The connections in front of the rotor cause the current flow to change as the motor spins and forms a structure called the commutator.

**Servo motors** are simple motors coupled to closed loop control mechanisms that are often built into each motor. The control mechanism includes a controller and a sensor for position feedback. A servo motor can usually turn automatically to any angle instructed by the controller. Servo motors are used in applications such as robotics, model planes, and CNC (computer numerical control) machinery common in manufacturing.

**Stepper motors** have multiple notched or toothed electromagnets arranged as a stator around a central rotor. Each full rotation of motion is divided into a number of equal steps related to the spacing of the notches or teeth in the electromagnets. The motor position can be commanded to move to one of these steps. The electromagnets are energized by a control circuit that is usually external to the stepper motor.

Unlike servo motors, stepper motors generally employ open-loop control. The motor itself does not incorporate a position sensor for feedback, so the motor does not "know" where it is. This state information must instead be collected and maintained by the control electronics connected to the stepper motor. Stepper motors in your scanner or printer usually have to move to one end of their motion range to reset their position every time the system is powered up. You are probably accustomed to hearing this startup process occur and now you know why.

## Step 25: Controlling Servo Motors



The Arduino IDE includes a built-in [Servo Library](#) capable of controlling multiple servo motors making careful use of timing mechanism within the microcontroller. The library can control 12 different servos using only one timer.

Wire up the servo motor to the Arduino Nano as shown using the wire harness built into the servo and three male-to-male jumper wires. The servo wiring harness has three color-coded lines: 5V, Ground, and Signal. As shown, the Signal line connects to I/O pin 9 of the Arduino Nano. Pulses on the Signal line instruct circuitry within the servo to move the motor shaft to different angular settings.

It is useful to push one of the included servo attachments onto the output gear of the servo to make movements of the servo easier to see.

Open the sketch:

File > Examples > Servo > Sweep

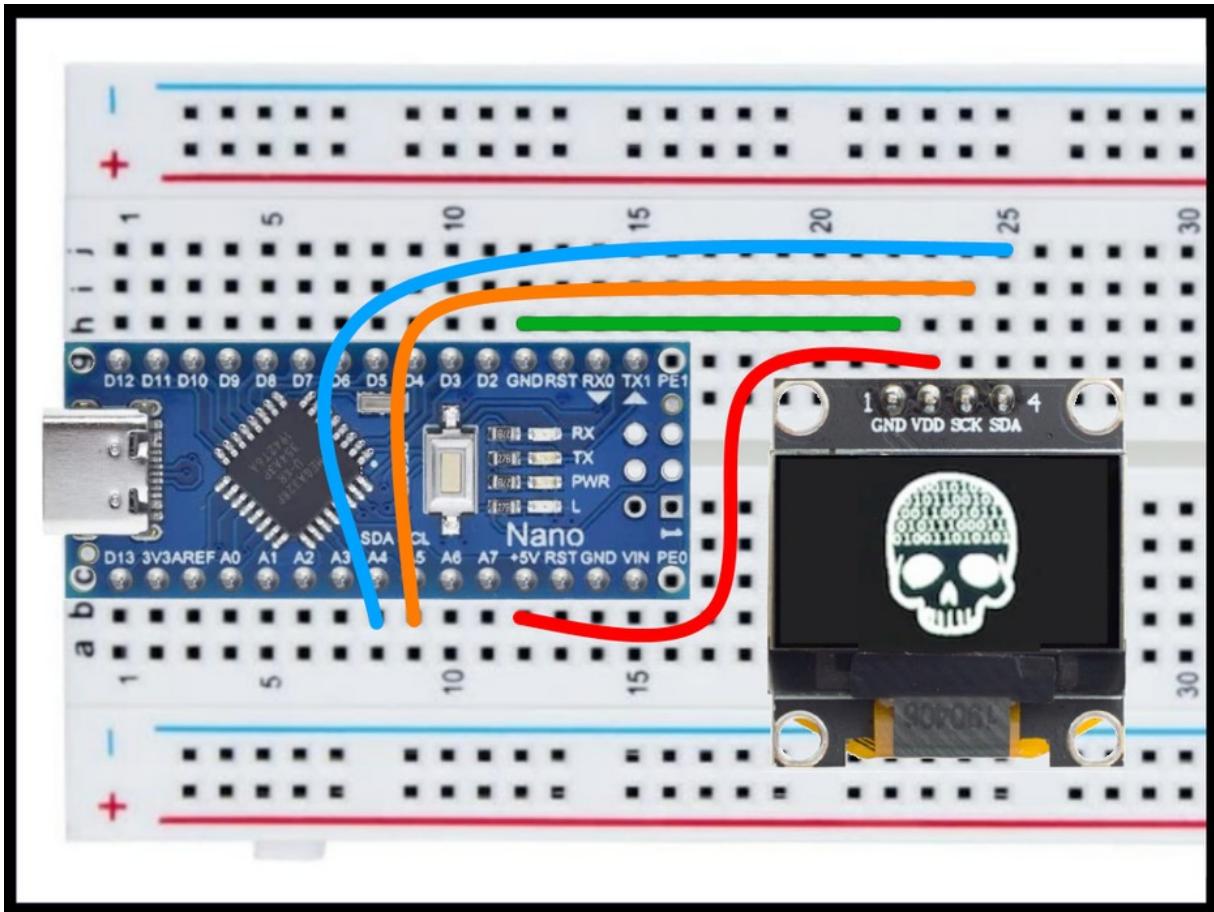
Download and run the sketch on the microcontroller. As you can probably guess from looking at the sketch code, it will sweep the shaft of the servo motor from 0 to 180 degrees and then back again.

What do you expect if you change the loop() function to contain only:

```
myservo.write(random(180));  
delay(5000);
```

How could this be used to replace rolling dice or using a "spinner" on a board game?

## Step 26: Displaying Graphics and Text



The OLED display module measures a tiny 0.96 inch but has a resolution of 128 X 64 pixels.

In addition to the pins for 5V Power (VDD) and GND, there are two pins for the IIC (inter-integrated circuit) bus. The IIC bus is also known as the [I2S bus](#). The two I2C bus pins are SCK (Serial Clock) and SDA (Serial Data). The four pins for the display should be wired to the Arduino Nano as shown.

In the last step, we used a built-in library for servos. Now it is time to pull in an external library. External libraries are extremely useful for adding additional functionality to the Arduino IDE and sketches that we build within the IDE.

The external library that we will install is the [Adafruit SSD1306 Library](#). The driver chip inside the OLED display module is an SSD1306 so this library is designed to allow your Arduino sketch to communicate with this driver chip.

In the Arduino IDE, navigate to **Tools > Manage Libraries**

In the window that pops up, enter SSD1306 in the search box. A few different libraries will come up in the search, so be sure to hit install under the entry for **Adafruit SSD1306**.

The installation process will ask if it should also install the dependency **Adafruit GFX Library**. Be sure to click to allow that Adafruit GFX dependency to also be installed. After this, your two new libraries will be installed into the Arduino IDE and ready to use.

Download and run the *OLEDtext.ino* sketch attached here. Notice that the sketch uses #include to invoke the new GFX and SSD1306 libraries through the Arduino IDE. Once the sketch runs as provided, try changing the settings for TextSize, cursor position, and the string being "printed" to the display.

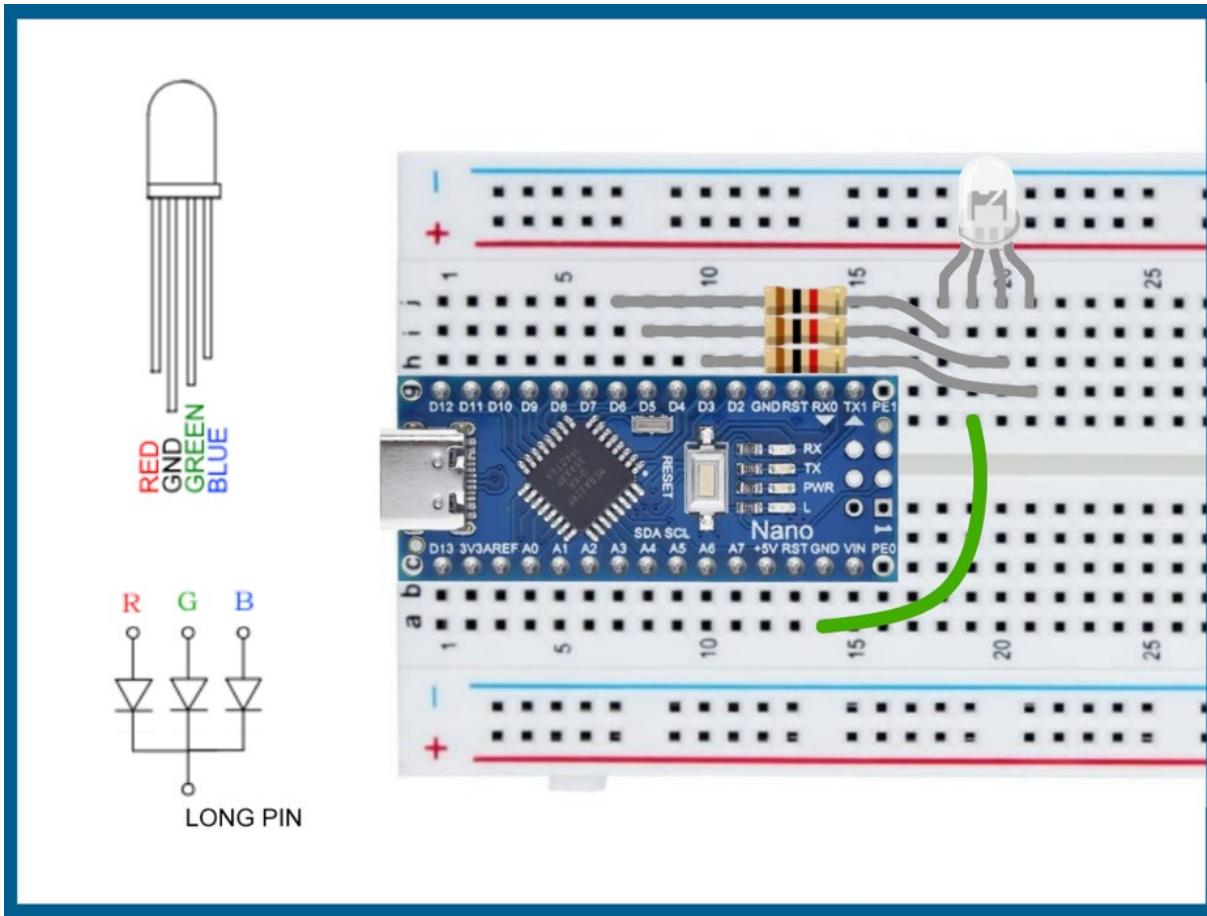
Libraries usually come with example programs for demonstrating use of the library. Give this one a try:

File > Examples > Adafruit SSD1306 > SSD1306\_128x64\_I2C

Once the sketch opens up, change the value in #define SCREEN\_ADDRESS from 0x3D to 0x3C

Run the sketch to see a nice variety of graphics and text display examples.

## Step 27: Full Color LEDs



The Common Cathode RGB LED is actually three LEDs inside of one package. The RGB stands for red, green, and blue. These are the colors of each of the three LEDs.

Recall from our earlier LED work that each LED (or any diode for that matter) has an anode terminal and a cathode terminal. The LED is forward biased, and can light up, when the higher voltage (for example +5V) is applied to the anode, and the lower voltage (for example GND) is applied to the cathode. For this reason, the anode and the cathode are often referred to as the positive and negative terminals respectively.

The three LEDs inside this one LED package have their cathode terminals connected together, which is why it is referred to as a "common cathode" arrangement. We will call this one shared cathode terminal the ground terminal for our purposes here.

The three separate anodes for the different colored internal LEDs can be driven with 5V to light up the individual LEDs as desired. Just as with the signal LEDs used earlier, a 1K resistor is placed inline with each of the three colored LEDs to limit the total current flowing through the LED.

Wire up the Common Cathode RGB LED and three 1K Resistors to the Arduino Nano as shown.

Download and run the *CommonCathodeRGB.ino* sketch attached here. The sketch uses PWM to achieve the desired brightness from each of the red, green, and blue LEDs allowing the three colors to mix together to create other colors as shown with in the sketch.

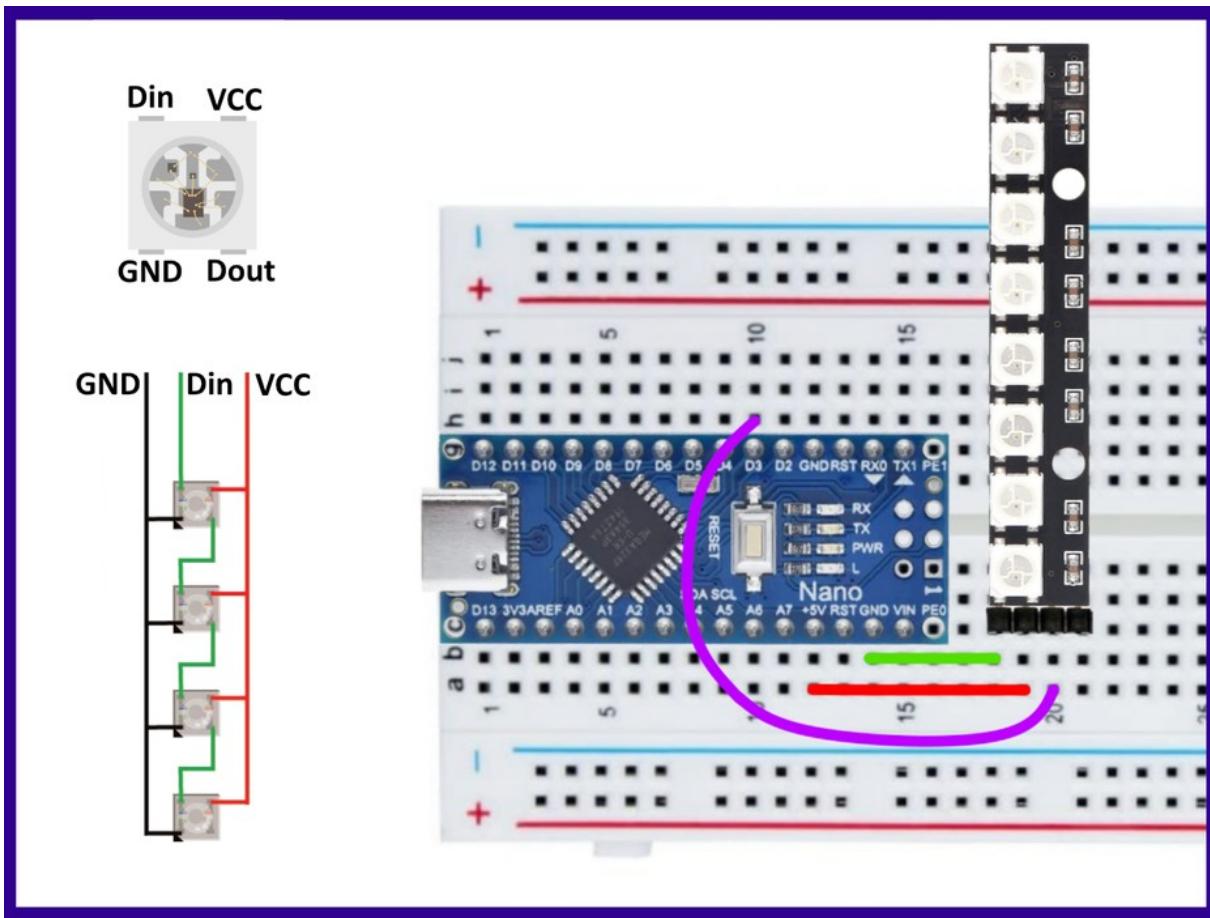
## Features of I/O Pins

Recall that PWM outputs are generated by the Arduino Nano using the [analogWrite\(\)](#) function. As shown in the function's documentation, only pins 3, 5, 6, 9, 10, and 11 of the Arduino Nano can be used for PWM. That is why pins 3, 5, and 6 are used in this experiment and pin 4 is not. It is important to check the features of specific I/O pins on an MCU when selecting which pins you will use for which purpose. You will learn that for different MCUs, certain pins may be I/O (both input and output) while some are input only and some are output only. Some pins may have specific I/O characteristics or bus applications. Some pins was be able to trigger interrupts while some may not. Some pins may have optional pull-up resistors, pull-down resistors, both, or neither. There are many options to check up on when it comes to micro controller I/O pins. Note that I/O pins are also sometimes called GPIO (general purpose I/O) pins.

## Quantity of I/O Pins

Since only pins 3, 5, 6, 9, 10, and 11 of the Arduino Nano can be used for PWM and the common cathode LED requires three of those to display full colors, only two such RGB LEDs can be driven by the Arduino Nano. In additional to what specific functionality each I/O pin may have, we also have to pay close attention to how many I/O pins there are in total and how we allocate them in our project. This often forces us to figure out tricks to get additional functionality from the MCU. For example, you probably see projects with far more than two RGB LEDs all the time. Next we will look at one of the more popular ways to get there.

## Step 28: Serial Addressable LEDs



One of the easiest techniques for controlling multiple RGB LEDs with one microcontroller involves serial, addressable LEDs. Certain examples of these are commonly referred to as NeoPixels or RGB Pixels.

While such a device is often called "an LED", each one actually contains 3 LEDs (one red, one blue, and one green) along with an embedded, or integrated, control circuit.

The control circuit of each device can be feed control information through one pin (data in or Din) and thus only requires one I/O pin from the microcontroller. The control information is sent from the microcontroller to the first addressable LED in a serial fashion, meaning one bit at a time - in a series. First, eight bits are sent defining the amount of green light to be emitted, then eight bits defining the amount of red light, and finally eight bits defining the amount of blue light. Those 24 bits are grabbed, or "latched", into the controller. Those 24 bits define a possible total of 16,777,216 (2 to the power of 24) different colors.

In addition to its *data in* pin, each RGB pixel also has a *data out* (or Dout) pin. The first pixel's Dout pin is daisy chained to the second pixels Din pin, and so forth until all

of the pixels are connected in a single chain. This structure allows the entire chain to be fed from a single I/O pin of the microcontroller. Once each RGB pixel latches the first 24 bits it receives, the control circuit outputs any additional bits on its Dout pin. From the Dout pin, the additional bits are sent along to next RGB pixel in the chain.

### **Wire up the Eight-Pixel Addressable RGB LED Module as shown**

The module includes eight daisy-chained WS2812Bs devices. You can read the ES2812B datasheet [from the manufacturer](#) if you wish.

### **Install the FastLED Library**

In the Arduino IDE, navigate to **Tools > Manage Libraries**

In the window that pops up, enter FastLED in the search box. A few different libraries will come up in the search, so be sure to hit install under the entry for FastLED by Daniel Garcia.

The FastLED library comes with some nice example programs. Load this one for now:

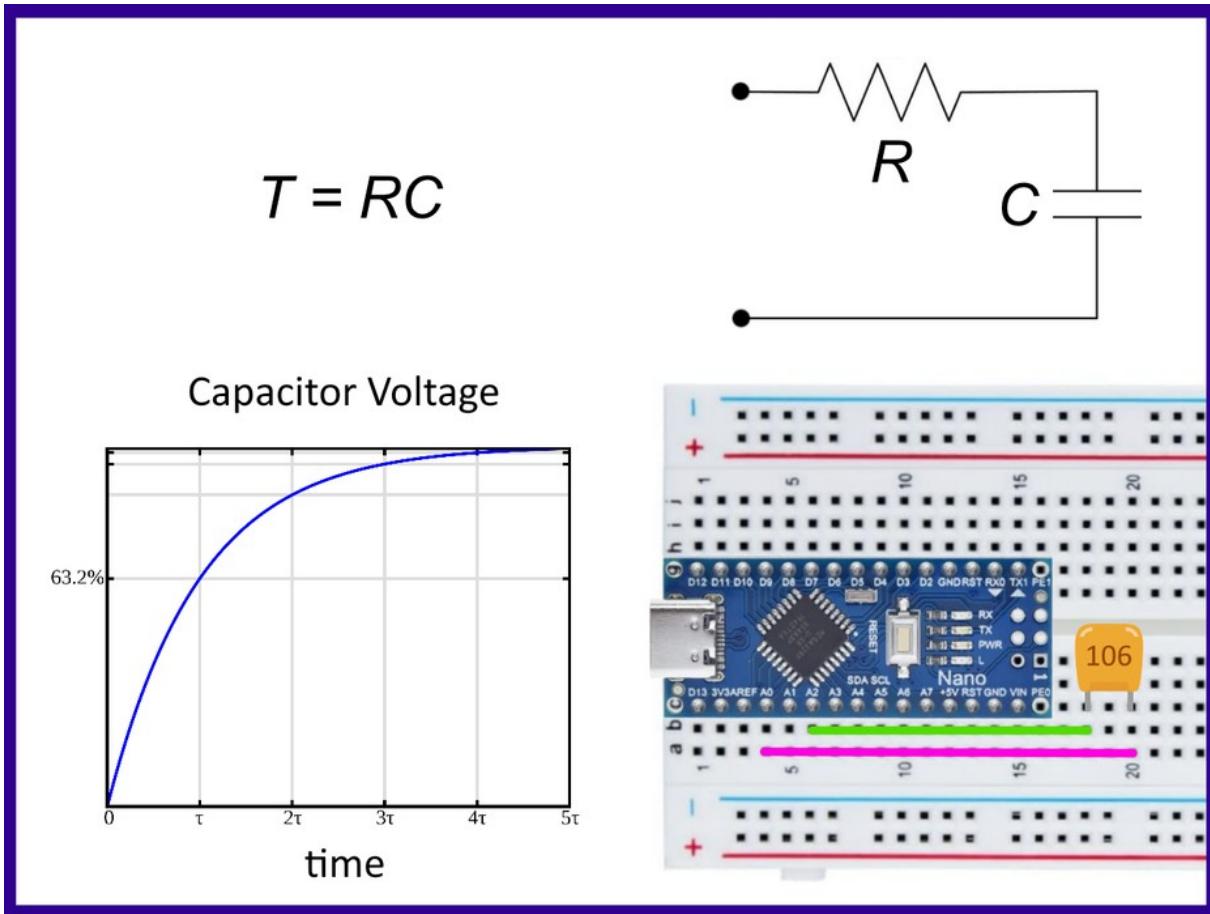
### **File > Examples > FastLED > DemoReel100**

Once the sketch opens, change two defines to match these:

```
#define LED_TYPE WS2812B  
#define NUM_LEDS 8
```

Run the sketch. After enjoying the results, play around with the sketch to see what fun can be had with these serial, addressable LEDs. As you can see, they are extremely versatile.

## Step 29: Measuring Capacitance



A capacitor is a two terminal device capable of storing energy in an electric field. A capacitor can be thought of as a very fast rechargeable battery where energy is stored in an electric field instead of as chemical energy. Since an electric field can be generated and discharged rapidly, the capacitor operates on a much faster time scale than a chemical battery.

The simplest structure for a capacitor is two parallel conductive plates. Between the plates, there is usually a nonconducting dielectric such as ceramic, glass, plastic, paper, mica, or air. Alluding to that parallel plate structure, the schematic symbol for a capacitor is two parallel lines.

The effect of a capacitor is known as capacitance and is measured in the unit Farads. One Farad is huge, so practical capacitors are usually measured in pico Farads (10 to the power of -12 Farads), nano Farads (10 to the power of -9 Farads), or micro Farads (10 to the power of -6 Farads).

We will measure a ceramic capacitor with marking "106" which equals a capacitance value of  $10\mu\text{F}$ . The marking represents a value in picofarads starting with two digits

"10" followed by the multiplier factor 6 (ten to the power of six) or 1,000,000. Giving us the value of  $10 * 1,000,000 \text{ pF}$  or  $10 \mu\text{F}$ .

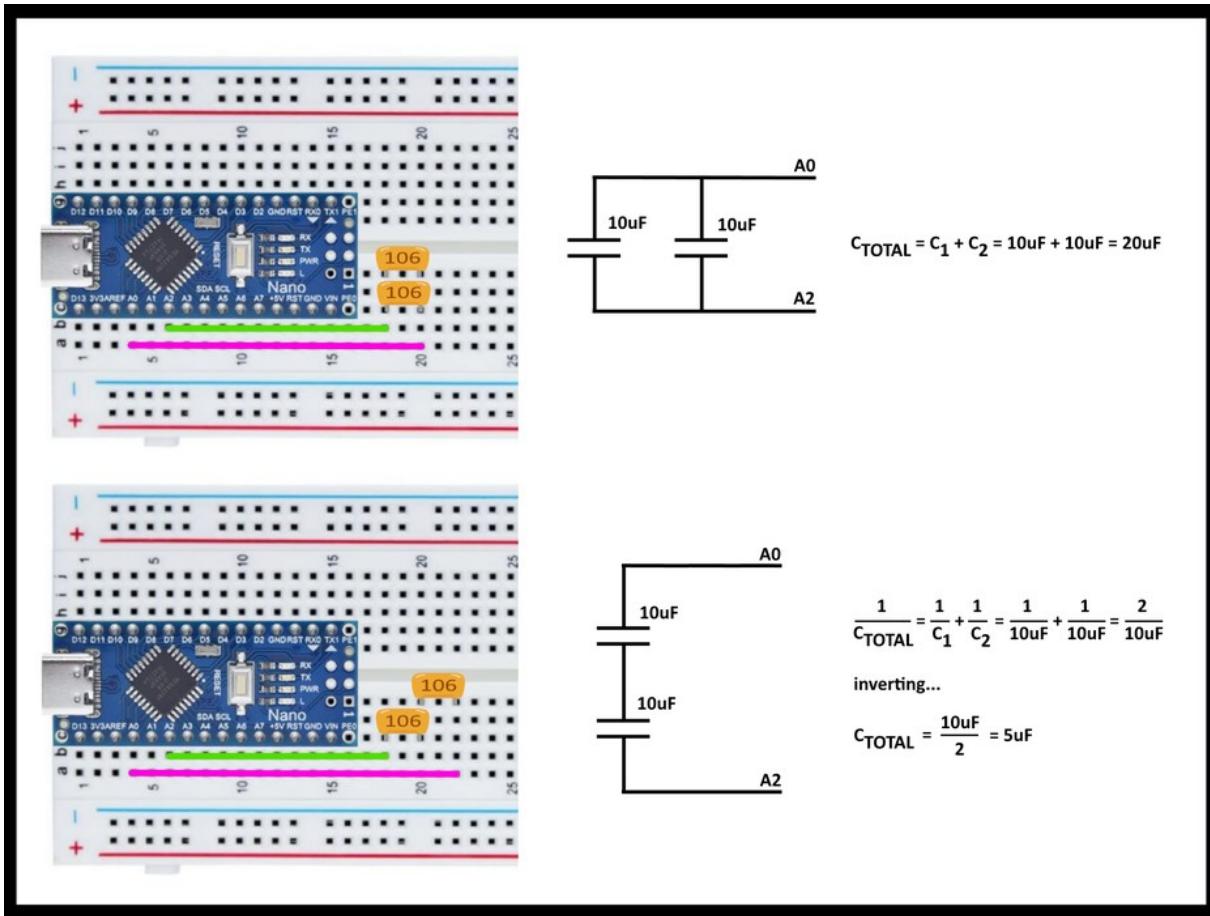
When a voltage is applied across a capacitor, the electric field within the capacitor is charged up and energy is stored with the capacitor. This energy can then be discharged (used up) out of the capacitor. How rapidly the capacitor charges or discharges can be used to calculate the value of the capacitor.

Microcontroller code can measure the time required for charging or discharging the capacitor to calculate the capacitance between two pins. Wire the  $10\mu\text{F}$  ceramic capacitor between pins A0 and A2 of the Nano as shown.

Download the attached *Capacitance.ino* sketch file and program it to the Arduino Nano. Open the Serial Monitor to view the output printed over the Nano's serial port. Notice how the capacitors marked as  $10\mu\text{F}$  capacitors will have measurements varying from about 8 to 11  $\mu\text{F}$ . This is normal for the type of capacitor we are working with.

How does this timing work? According to basic physics, it requires one *time constant* to charge a capacitor from zero up to 63.2% of the applied voltage. In this case, that would be 63.2% of 5V. But what is the *time constant*? It is just  $R*C$ , where R is the resistance of the circuit (in Ohms) and C is the capacitance (in Farads). It may look like there is no resistor in the circuit, but in fact the microcontroller's internal pullup resistor (having approximately 34.8 Ohms) is used to charge up the external capacitor. The code in the sketch is a little complicated, but you can certainly explore how the RC time constant and the known pullup resistance of the microcontroller are used to make the measurement calculations.

## Step 30: Capacitor Structures



Modify the previous capacitor circuit by combining two 10uF capacitors in parallel and then in series as shown here. In each instance, observe the output of the serial monitor to measure the equivalent capacitance of the combined capacitors. Remember that the capacitors are not exactly 10uF even though that is how they are marked.

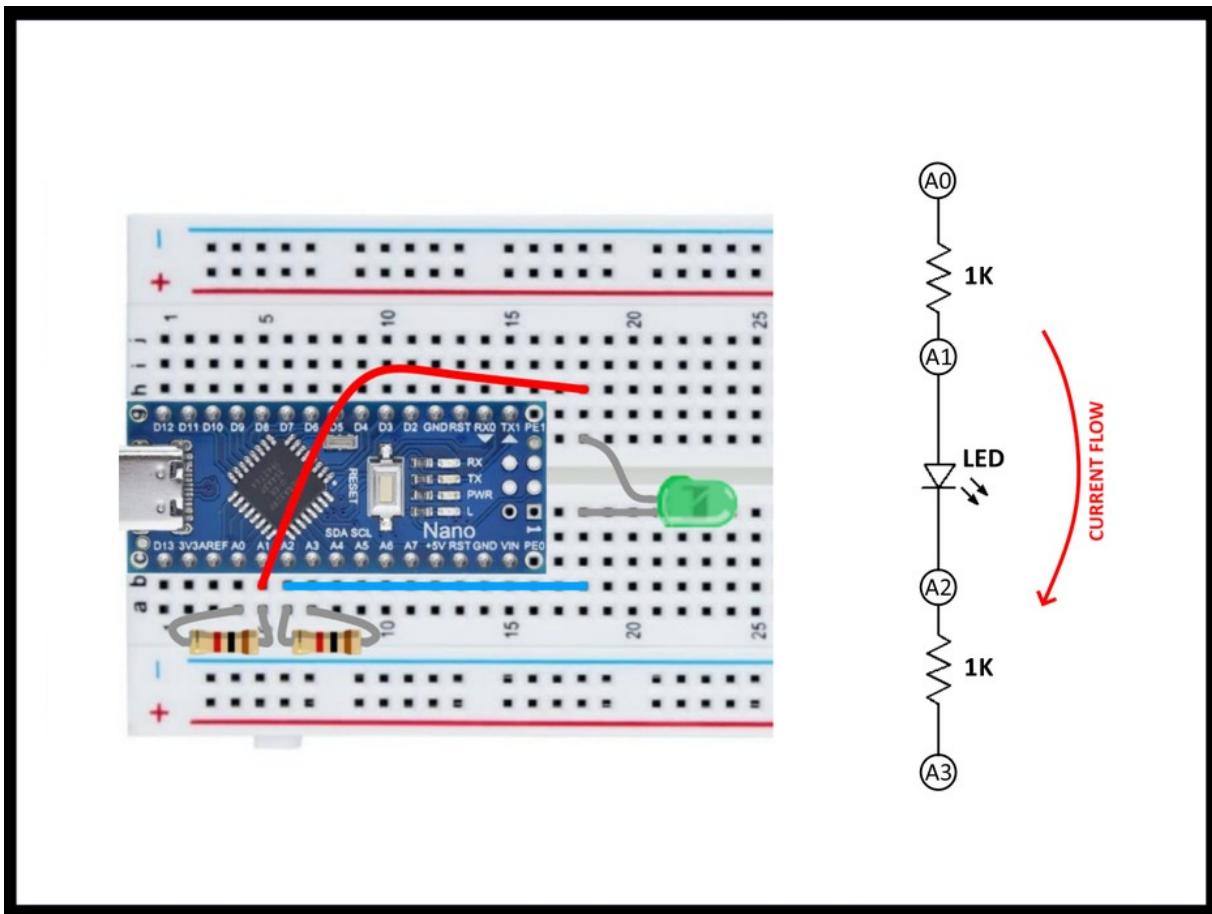
Revisit the results found in **Step 15: Resistor Structures**. Notice how resistors and capacitors combine in similar, but opposite, fashions. Serial resistors add together while parallel capacitors add together. The equivalent resistance of parallel resistors is the inverse of the sum of the inverse of the individual resistors. Similarly, the equivalent capacitance of series capacitors is the inverse of the sum of the inverse of the individual capacitors.

Consider delving deeper into capacitor structures by combining all three of the 10uF capacitors in different ways.

For an advanced exercise, measure the capacitance of each capacitor alone and then plug those actual individual capacitances into the parallel and serial equivalence

formulas to see how close the combined measurements are to theory.

## Step 31: Electron Flow Through Diodes



Semiconductor diodes are like one-way valves. They only allow current to flow in one direction, and not in the opposite direction. This is true for all types of Diodes, including LEDs (Light Emitting Diodes).

Wire up two 1K resistors and an LED as shown in the diagram.

Download the attached *DiodeTest.ino* sketch file and program it to the Arduino Nano. Open the Serial Monitor to view the output printed over the Nano's serial port.

With the LED wired as shown (long pin to A1 and short pin to A2), the serial monitor will indicate that current flows from A1 to A2 but current cannot flow from A2 to A1.

With the direction of the LED swapped, current will flow from A2 to A1, but not from A1 to A2.

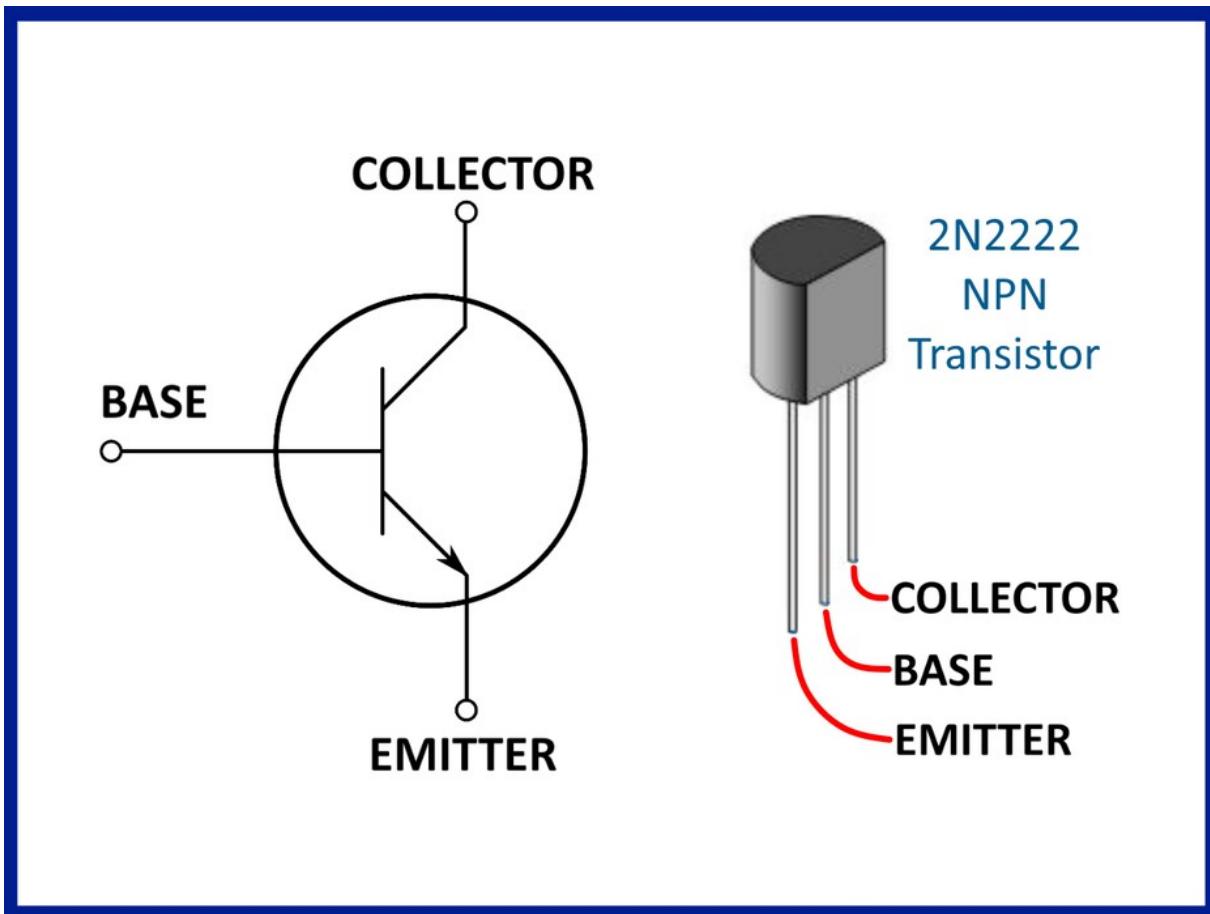
With the LED removed, current will not flow in either direction.

With A1 connected directly to A2, current will flow in both directions.

Carefully examining the sketch code will reveal how two additional pins (A0 and A3) are used to control 1K resistors connected (respectively) to A1 and A2. The first test in the code sets A3 to ground which means the 1K resistor connected to A2 is grounded (pulling low). Then the code configures A0 as an input meaning that A0 is not driving high or low, but instead is floating. With A0 floating, the resistor connected to A1 will not be pulled high or low. Pin A1 is however connected directly to 5V. So one side (A1) of the DUT (device under test) is set to 5V and the other side (A2) of the DUT has a 1K resistor to ground and can also be read as an analog input to the microcontroller.

Depending upon what is between A1 and A2, current will either not flow (keeping the original 5V difference between A1 and A2). However, if current is flowing through the DUT, it will also flow through the 1K resistor since they are in series. The voltage drop in the 1K resistor will make the difference between A1 and A2 less than 5V. Sensing this lower voltage difference allows the code to identify that current is flowing. This trickery probably starts out sounding a lot more complicated than it really is. Stepping through the measurement process several times or until everything clicks is a worthwhile undertaking if you're up for it.

## Step 32: Transistors

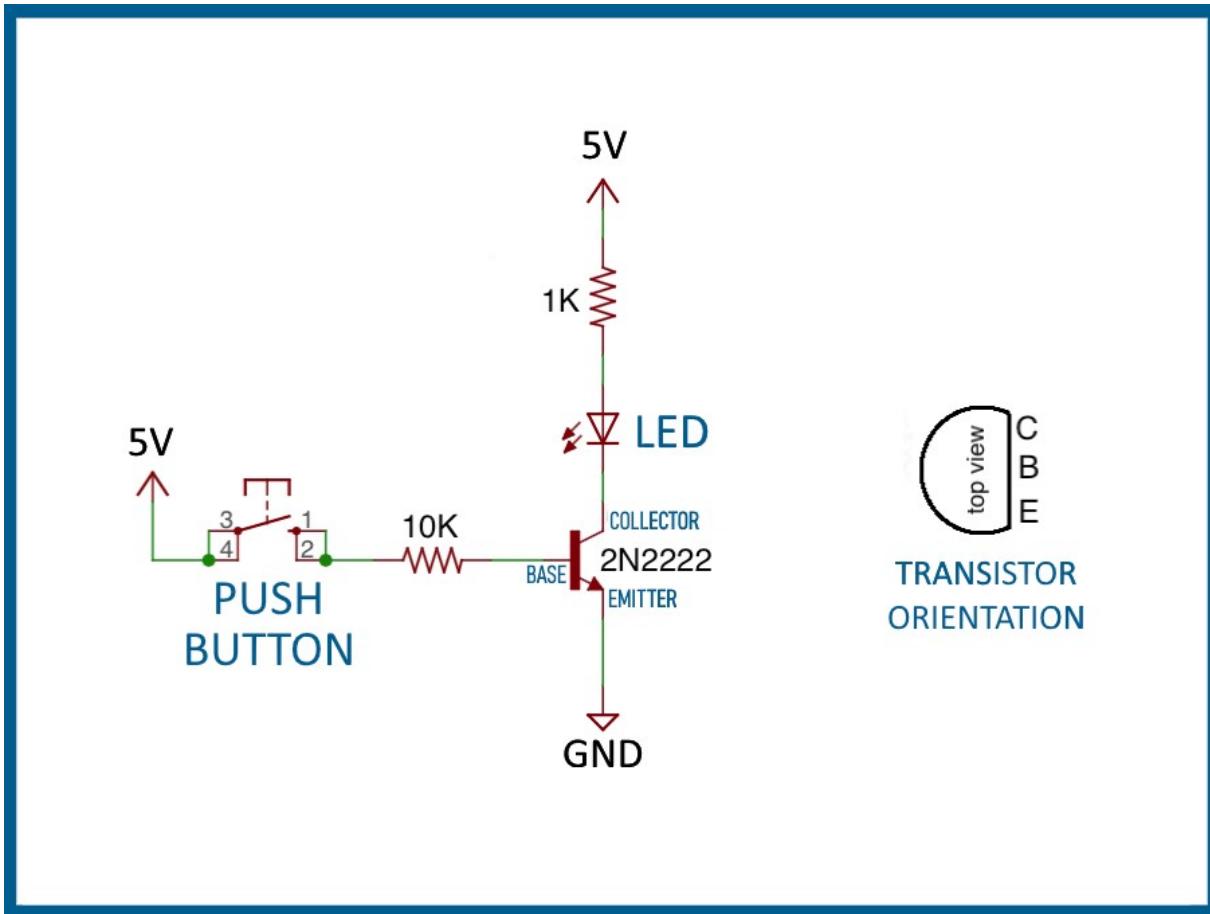


A transistor is a semiconductor device generally having three terminals. Transistors are capable of switching or amplifying electrical signals. An input signal at a first pair of the terminals can switch or amplify the signal passing through a second pair of terminals. We will be starting with [2N2222A NPN Bipolar Transistors](#). The three terminals of a bipolar transistor are called base, collector, and emitter.

In addition to NPN transistors, there are also PNP transistors. In addition to bipolar transistors, other common transistors include field effect transistors (FETs), metal oxide semiconductor FETs (MOSFETs), and complementary metal oxide semiconductor (CMOS) transistors. The three terminals of all these types of FETs are called gate, source, and drain.

Individual transistors, like the 2N2222, only have one transistor in a three-pin package, but modern electronic devices often pack many, many (even billions) of transistors into an integrated circuit.

## Step 33: Transistors As Switches



A 2N2222 transistor can be used as a switch. This circuit is very much like the earlier circuits, "Control Electron Flow With A Switch" and "Control Electron Flow With A Pushbutton". Instead of a mechanical switch or button, the collector-emitter path through the transistor is used to open and close the path for electron flow through the LED.

Build this circuit on the breadboard using one transistor, one push button, two resistors, and an LED.

When the button is closed, a 5V signal is applied between the base and the grounded emitter ( $V_{be} = 5V$ ). This "control signal" forces  $V_{ce}$  (the voltage from collector to emitter) to zero such that the transistor acts like a short or closed switch. This allows current to flow through the LED causing it to light up.

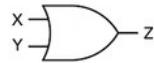
When the button is open,  $V_{be} = 0V$ , and the transistor acts like an open switch and current does not flow through the LED. The LED remains unlit. These two lit/unlit conditions show how the control signal at the base turns the transistor on and off like a switch. Notice that the LED draws current through the 1K resistor and not through

the 10K resistor. Only a very tiny amount of current comes through the 10K resistor to activate the transistor "switch". This illustrates how we can control a large amount of current with quite a small amount of current using a transistor as a switch.

This circuit can be called a buffer or pass-gate. From a logic (HIGH / LOW) perspective, the circuit's output matches (buffers, or passes) its input. The opposite logic element is called an inverter or NOT gate. The NOT gate outputs a 1 (HIGH) when its input is a 0 (LOW) and vice-versa, which implements logical negation. The NOT circuit is illustrated in Step 5 of the [HackerBox 0039 Box Guide](#).

## Step 34: Digital Logic

**OR**



$$Z = X + Y$$

Input	Input	Output
X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	1

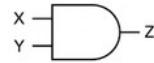
**NOR**



$$Z = \overline{X+Y}$$

Input	Input	Output
X	Y	Z
0	0	1
0	1	0
1	0	0
1	1	0

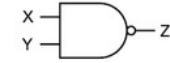
**AND**



$$Z = X \cdot Y$$

Input	Input	Output
X	Y	Z
0	0	0
0	1	0
1	0	0
1	1	1

**NAND**



$$Z = \overline{X \cdot Y}$$

Input	Input	Output
X	Y	Z
0	0	1
0	1	1
1	0	1
1	1	0

Many modern electronics systems are based on digital (also known as, binary or Boolean) logic.

Here we see four of the most common logical operators: OR, NOR, AND, NAND. Each one is shown in three different common representations: schematic symbol, Boolean logic expression, and truth table.

The output of the OR operator is true when either its first input is true OR its second input is true. The logical OR is an "inclusive OR" meaning that the output is true also when both inputs are true.

The output of the NOR operator is simply NOT OR, which is to say the logical opposite of the OR operator.

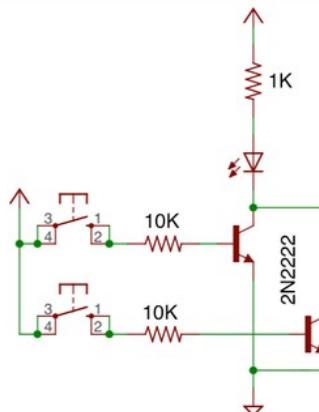
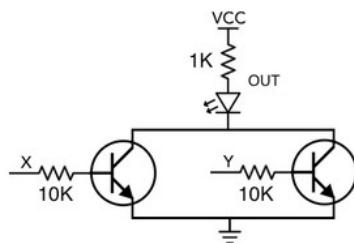
The output of the AND operator is true only when both its first input is true AND its second input is true.

The output of the NAND operator is simply NOT AND, which is to say the logical opposite of the AND operator.

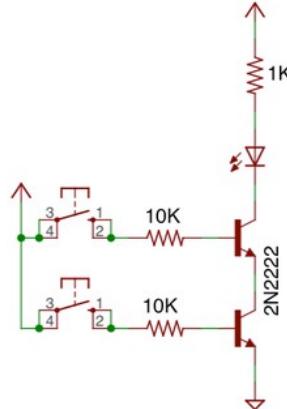
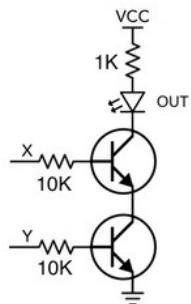
Two additional [logic operators](#) worth becoming familiar with are XOR and XNOR.

## Step 35: Logic Gates From Transistors

### OR GATE



### AND GATE



Electronic logic gates can be constructed from transistors. Each transistor acts as a switch as we saw in our last experiment.

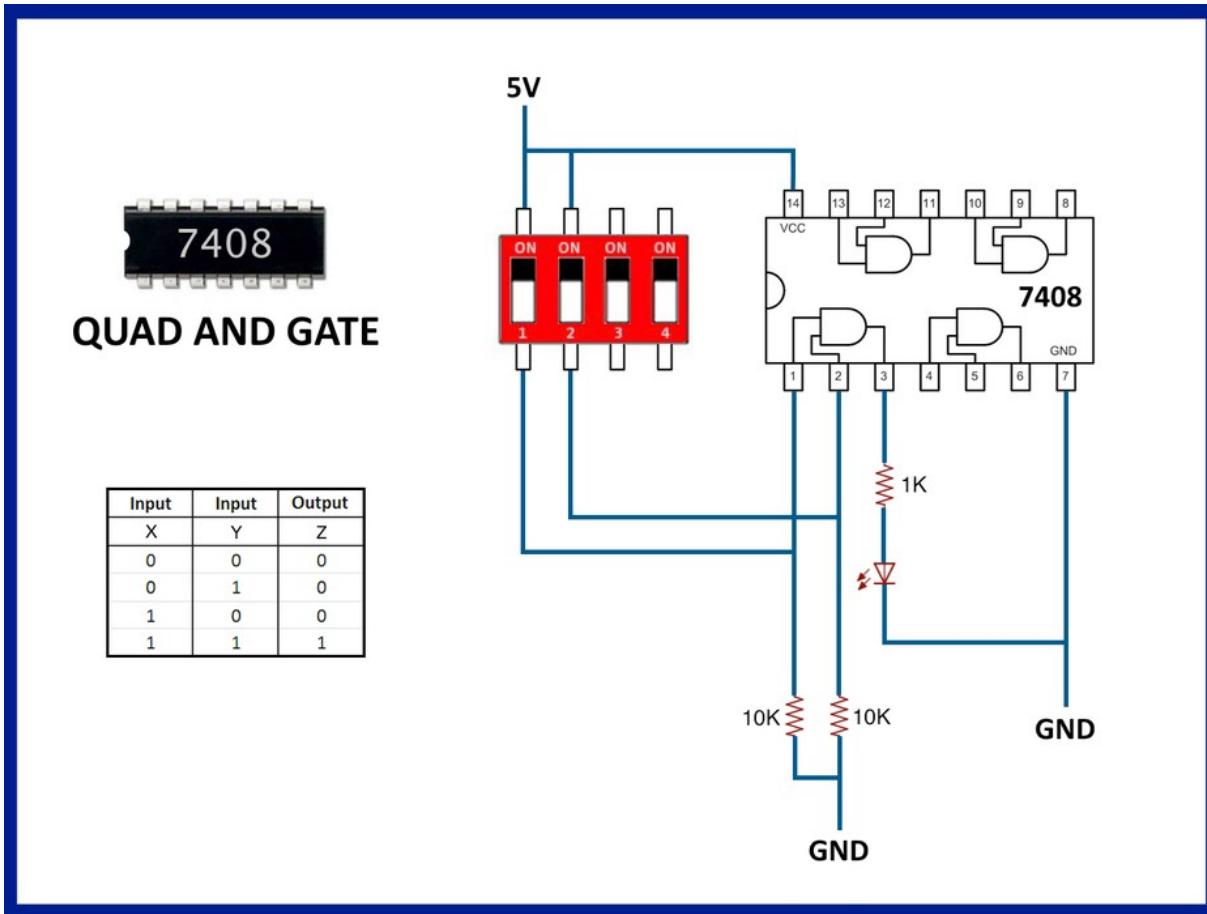
An OR GATE is formed from two transistor switches arranged in parallel. Given this parallel form, the gate is ON (or TRUE) when either the first input is ON (or TRUE) **OR** the second input is ON (or TRUE). In parallel, either transistor conducting will allow current to flow.

Build this circuit on the breadboard using two transistor, two push buttons (inputs), three resistors, and an LED (output). Compare its operations with the truth table for the logical OR operator.

An AND GATE is formed from two transistor switches arranged in series. Given this series form, the gate is ON (or TRUE) only when both the first input is ON (or TRUE) **AND** the second input is ON (or TRUE). In series, both transistors must conduct to allow current to flow.

Build this circuit on the breadboard using two transistor, two push buttons (inputs), three resistors, and an LED (output). Compare its operations with the truth table for the logical AND operator.

## Step 36: Integrated Logic Chips



An integrated circuit (commonly referred to as a chip) generally contains a large number of transistors integrated into a single device. There are integrated circuits for performing all manner of electronic feats including microprocessors, audio amplifiers, network interfaces, cryptographic engines, graphics processors, flash memory, and on and on.

In the 1960s, a whole series of digital integrated circuits became available with many of the initial chips implementing logic gates. For example, the 7408 chip is a Quad AND Gate, which means that the chip contains four individual AND logic gates as shown here. All of the gory details of the 7408 chip can be seen in its [datasheet](#) from Texas Instruments.

The illustrated circuit demonstrates the use of one of the AND gates within a 7408 chip. The circuit can be assembled on the breadboard using a 4-bit DIP switch (for the two inputs), three resistors, and an LED (for the output).

What are the resistors for?

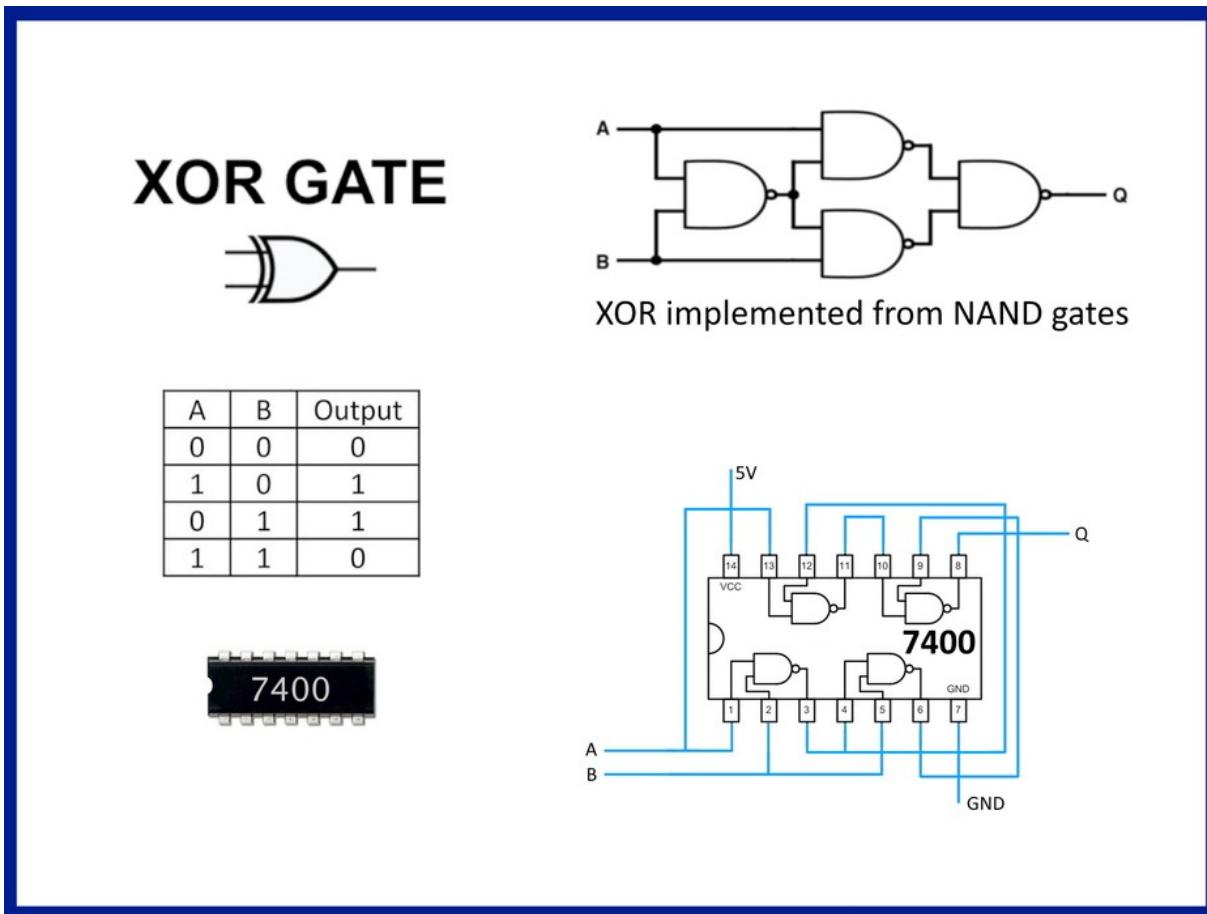
The 1K resistor is a current limiting resistor to keep the LED from drawing too much current. It is the same "current limiting" resistor application we've used in earlier experiments.

The two 10K resistors are "pull-down" resistors that gently set the logic inputs at pins 1 and 2 to low (or 0V) when the respective input switch is open. An open signal is also referred to as "floating" as it can float to any voltage level in a nondeterministic fashion. Since a floating input can take on many different values, it provides an unknown input, which is obviously not good. Gently pulling the line down to 0V makes each input zero instead of floating. Since 10K is a pretty high resistance (very unlike a direct short), we can think of that as gently pulling the voltage level. Then when the switch is closed, the line is very firmly (by a direct short) connected to high (or 5V) which easily overrides the gentle pull-down. So the 10K pull-down resistor lets a single switch provide both a HIGH and LOW input even though the switch is only really connected to HIGH (5V).

### Other Gates

Assemble similar demonstration circuits for an OR gate using the 7432 chip ([datasheet](#)) and for a NAND gate using the 7400 chip ([datasheet](#)). Verify the correct operation against the expected truth table for each logic operator.

## Step 37: XOR Implemented From NAND Gates



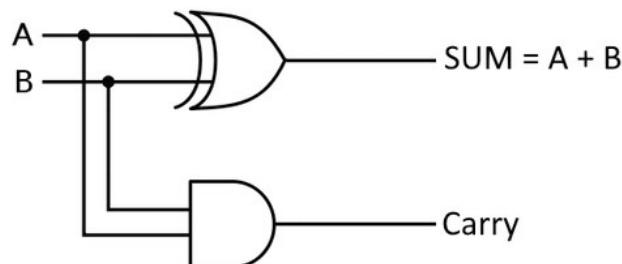
As mentioned earlier, the logical OR operation is an "inclusive OR" meaning that the output is true also when both inputs are true. The "exclusive OR" (or XOR) excludes the condition where both inputs are true. This is demonstrated in the truth table shown here.

The XOR logic can be implemented by combining all four of the NAND gates of a 7400 quad NAND chip ([datasheet](#)). The XOR circuit can be assembled on the breadboard in a very similar fashion to the previous AND gate circuit. A 4-bit DIP switch (for the two inputs A and B) and two 1K pull-down resistors feed input pins 1, 2, 5, and 13 as shown. A 1K resistor and an LED are connected at pin 8 to display the output (Q).

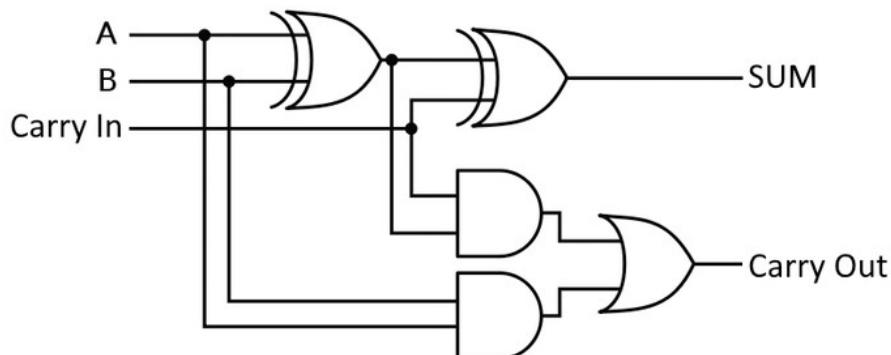
Note that we suggest 1K pull-down resistors here, not the 10K used in the AND circuit. Feel free to try it both ways, but you will likely find that 1K works better.

## Step 38: Combining Logic Gates

### HALF ADDER



### FULL ADDER



We've combined transistors to construct gates, now let's combine gates to do some math.

Combinational Logic generates outputs based only on the present inputs. In fact, combinational logic is sometimes referred to as time-independent logic because it has no memory. Later we will see how sequential logic can compute outputs based on present inputs and also on history.

Mathematical operations are generally combinational (memoryless or stateless). When you are multiplying two numbers together, it doesn't really matter what numbers you multiplied together yesterday or who won the last world cup.

#### Half Adder

The half adder illustrated here is quite simple. It only adds one bit to another bit (labeled A and B).

Consider the possible outcomes:

A	B	SUM
0	0	0
0	1	1
1	0	1
1	1	10

Notice that the lowest bit of the SUM is just an XOR and the higher bit is only high when both A and B are high.

We call the low bit SUM and generate it using one XOR gate.

We call the high bit CARRY and generate it using one AND gate.

Consider how we add two base ten (decimal) numbers. We need to use a carry when two digits sum up to 10 or more because the value overflows into the next higher digit. In base two (binary), we need to carry when two digits sum up to two or more, which is also 10 in binary. In binary the value two (written as 10) overflows into the next higher digit. Carrying is the same concept in base two as it is in base ten.

The half adder can be constructed on the breadboard in a similar fashion to the gate circuit exercises: Use the 4-bit DIP switch for the two inputs (A and B) along with two 1K pull-down resistors. Implement the XOR gate by combining all four NAND gates of the 7400 quad NAND chip. Use one AND gate of the 7408 chip. Finally, two LEDs, each with its own 1K current limiting resistor are used to display the SUM and Carry outputs. Remember to connect Vcc and GND of both chips to the 5V and GND power supply rails respectively.

## Full Adder

An obvious weakness of the half adder is that it can only add two bits so there is no way to add in the carry from the previous digit.

The full adder allows us to add  $A + B$  and also the carry bit from the previous (lower) digit. We can make an 8 bit adder by chaining 8 full adders together with the Carry Out from the lowest bit wired to the Carry In of the next higher bit and continuing this chaining from Carry Out to Carry In through all 8 adders. This method can be simply extended to make a 64 bit adder (or any other word size) by chaining 64 full adders.

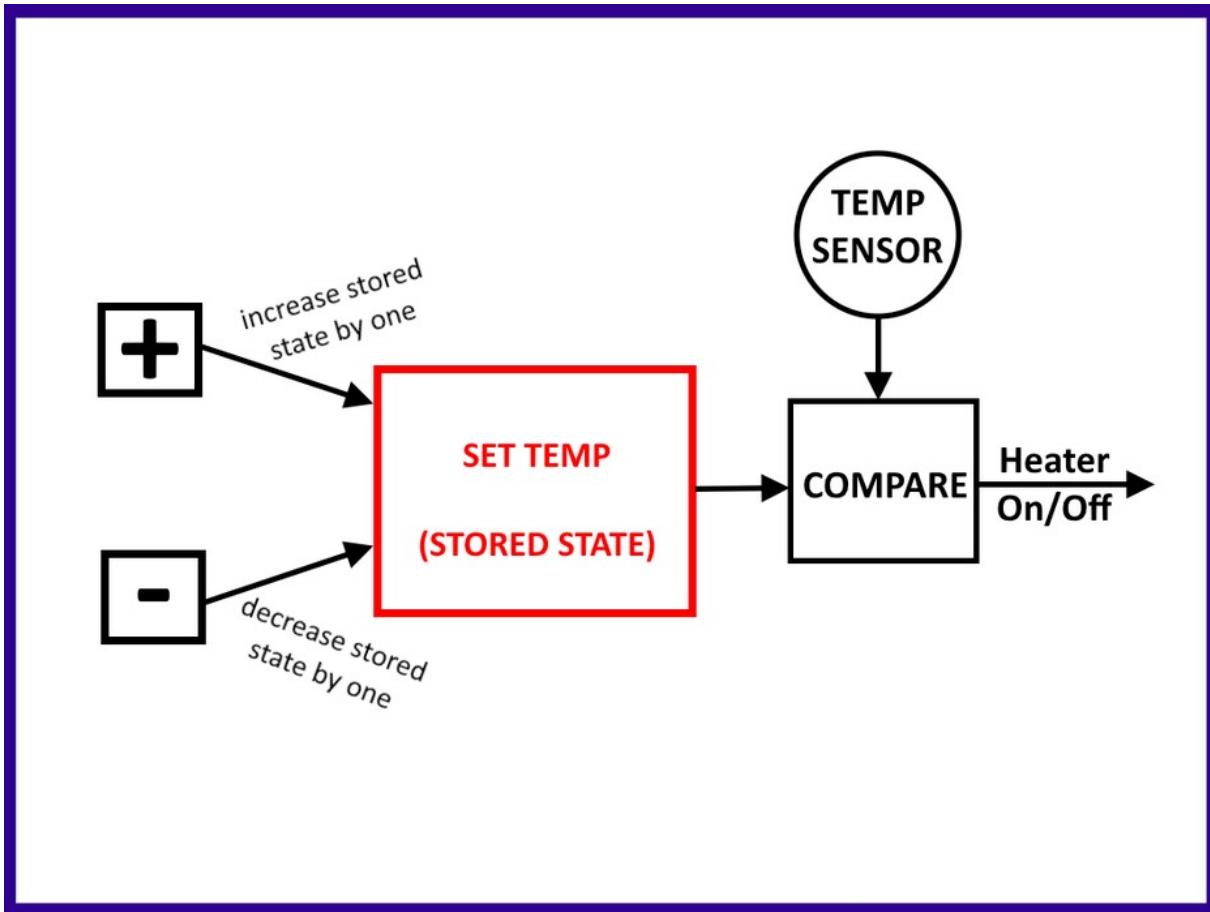
You can attempt to assemble the full adder on the breadboard using the two 7400 NAND chips to implement two XOR gates along with two AND gates from the 7408 chip and an OR gate from the 7432 chip.

Notice how this is getting a little messy. We will need a much higher level of integration to start doing very useful mathematics. It will use exactly the same gates as we've been working with, but just a whole lot more of them.

## Arithmetic Logic Unit (ALU)

In a computer CPU, the ALU is a combinational digital logic circuit that does math. Generally an ALU is given two sets of input bits that represent two numerical values along with some control bits indicating which mathematical operation to perform on the two inputs. The ALU then generates a set of output bits representing the result of the computation. The ALU includes the circuitry necessary to perform the computation on the input bits. For example, the adders that we've built would be used when the control bits indicate that an addition is to be performed.

## Step 39: Storing Information



Thus far, we have only seen logic circuits that compute an output based on the present inputs. When the inputs go away, the outputs change. This type of circuit is memoryless or stateless meaning that it has no memory and thus it cannot maintain state information. Making an analogy to switches, a momentary pushbutton does not "remember" that it was being pressed once it is released. Its state is lost because it has no memory. In contrast, a toggle switch (like a light switch) can "remember" when it is on or off without needing to be "held" in that state by the operator.

Logic circuits that can maintain state are called Sequential Logic. Sequential logic has memory and can generate outputs based on not only the present inputs, but past inputs, and even based on sequences of past inputs.

In the illustrated example, a simplified digital thermostat must maintain the state of its set temperature. The operator can adjust the set temperature up one degree by pressing the "+" button. If the set temperature was previously at 60 degrees, that maintained state information must be used by the circuit (along with the "+" input) to determine that the new set point must be 61 degrees. If the operator presses the "+"

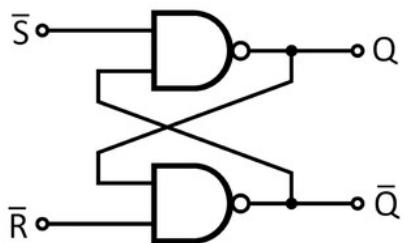
button again, the set point will increase to 62 degrees. This demonstrates that the state information represents the results from a sequence of past inputs.

Since we've already looked at computer code on a microcontroller, this issue of state information may seem overly simplistic or even obvious. The state of the thermostat can simply be placed in a variable within a computer program. However, a digital logic circuit does not have variables. In fact, when we store information in a variable within a computer program, the computer is actually leveraging an electronic storage element - a sequential circuit.

Just as the combinational logic gates we learned about were the basis of the mathematical operations in the ALU of a computer, the storage elements we will learn about are the basis of the registers and memory of the computer.

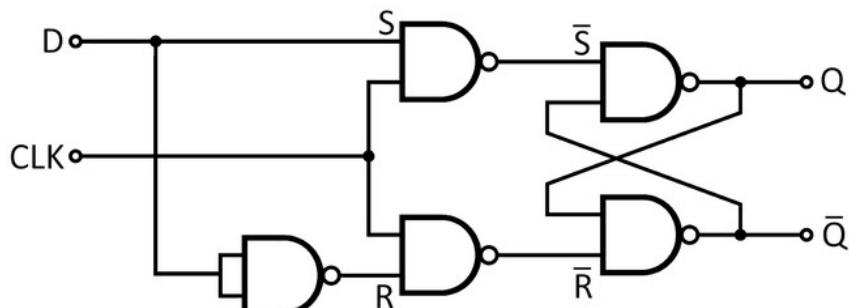
## Step 40: NAND Gate Flip-Flops

### SR Flip-Flop



S	R	$Q_{next}$	Action
0	0	Q	Hold state
0	1	0	Reset
1	0	1	Set
1	1	X	Not allowed

### D Flip-Flop



Clock	D	$Q_{next}$
Rising edge	0	0
Rising edge	1	1
Non-rising	X	Q

The basic electronic storage element is the **flip-flop**. Similar to how we combined NAND gates together to form an XOR gate, the same NAND gates (from the same 7400 quad NAND chip) can be combined to form flip-flops.

The simplest flip-flop is called the "set, reset flip-flop" or more typically the SR Flip-Flop. It only requires two NAND gates as shown here. The Q terminal is the output of the flip-flop and Q-Bar will always be the logical opposite of whatever Q is.

When the SR flip-flop is set ( $S = \text{HIGH}$ , meaning  $S\text{-Bar} = \text{LOW}$ ), the output ( $Q$ ) is set or HIGH. When the SR flip-flop is reset ( $R = \text{HIGH}$ , meaning  $R\text{-Bar} = \text{LOW}$ ), the output ( $Q$ ) is reset or LOW. When neither S or R are asserted (meaning they are both LOW or ZERO), the SR flip-flop is holding the output ( $Q$ ) meaning that  $Q$  does not change. Since  $Q$  does not change in this hold condition, the SR flip-flop can be said to be storing a bit in memory or maintaining state.

A more versatile type of flip-flop is the D Flip-Flop, which can be implemented using five NAND gates (requiring two 7400 quad NAND chip). The D flip-flop locks its input ( $D$ ) onto the output ( $Q$ ) whenever the clock transitions from low to high (called "on the

"rising edge"). When the clock signal is not rising, the output (Q) is maintained at the last value that was clocked-in without any care for what happens at the input (D). Again, the flip-flop can be said to be storing a bit in memory or maintaining state.

If you'd rather not wire up these examples on the breadboard, the digital logic simulator [Logic.ly](#) allows us to play with logic circuits right in a browser window. When the page first opens, you will see some samples to explore. One of them is a D flip-flop.

## Step 41: D Flip-Flop Integrated Circuit

### Dual D Flip-Flop Integrated Circuit



The diagram shows the internal circuit of the 7474 Dual D Flip-Flop integrated circuit. It consists of two D flip-flops, each with a data input (D), a clock input (CP), a set input (S), a clear input (C), and outputs Q and Q-bar. The 7474 chip has 14 pins. Pin 14 is V<sub>CC</sub>, pin 13 is C<sub>D2</sub>, pin 12 is D<sub>2</sub>, pin 11 is CP<sub>2</sub>, pin 10 is S<sub>D2</sub>, pin 9 is Q<sub>2</sub>, pin 8 is Q-bar<sub>2</sub>. Pins 1 through 7 are shared between the two halves: pin 1 is C<sub>D1</sub>, pin 2 is D<sub>1</sub>, pin 3 is CP<sub>1</sub>, pin 4 is S<sub>D1</sub>, pin 5 is Q<sub>1</sub>, pin 6 is Q-bar<sub>1</sub>, and pin 7 is GND.

Inputs				Outputs	
S <sub>D</sub>	C <sub>D</sub>	CP	D	Q	Q-bar
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	—	H	H	L
H	H	—	L	L	H
H	H	L	X	Q <sub>0</sub>	Q-bar <sub>0</sub>

NOTE: H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial;  
— = LOW-to-HIGH Clock Transition  
Q<sub>0</sub>(Q-bar<sub>0</sub>) = Previous Q(Q-bar) before LOW-to-HIGH Transition of Clock

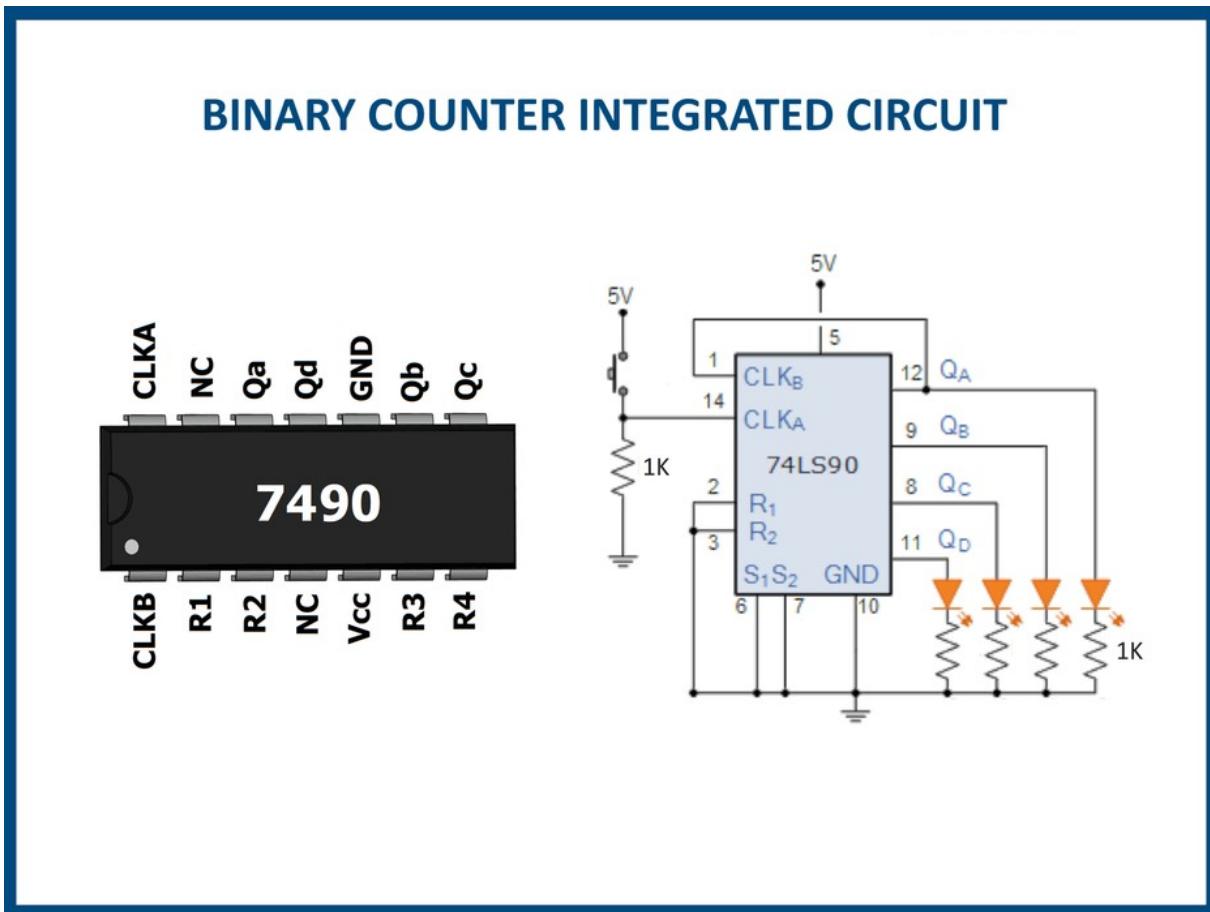
While it is useful to understand how to implement flip-flops from individual gates, flip-flops are also available ready-made in integrated circuits, such as the 7474 Dual D-Type Flip-Flop chip ([datasheet](#)).

The two flip-flops in the 7474 chip have the typical D-Type signals (D, CLK, Q, and Q-Bar). Note that CLK is called CP in this diagram. In addition to these signals, each flip-flop also has a set (S) and clear (C) signal. These are basically set and reset, so the flip-flops are D-type with additional SR-type features. Note, in the truth table, that when S and C are both disabled (both HIGH) then the flip-flop acts just as our earlier D-type flip-flop. Otherwise, set and clear (S and C) perform their expected set and reset functionality overriding the data (D) and clock (CP) inputs entirely.

Why did we say that S and C are disabled when they are both HIGH? That is because they are both active-low signals. This is indicated by the bar on their names and the little circle at the input point in the diagram. An active-low signal is active when it is LOW and inactive when it is HIGH, which is opposite the normal expectation.

To try out a flip-flop from the 7474, use an on-off slide switch on the D input, a momentary input on the clock (CP) input, the usual pull-up/pull-down resistors, an LED on the output (Q), and also tie set (S) and reset (C) directly to 5V (HIGH) to force them to inactive. Observe that D can be set to either value but that value value doesn't lock into the state/output (Q) until there is a rising edge on the clock (CP) line.

## Step 42: Binary Counter

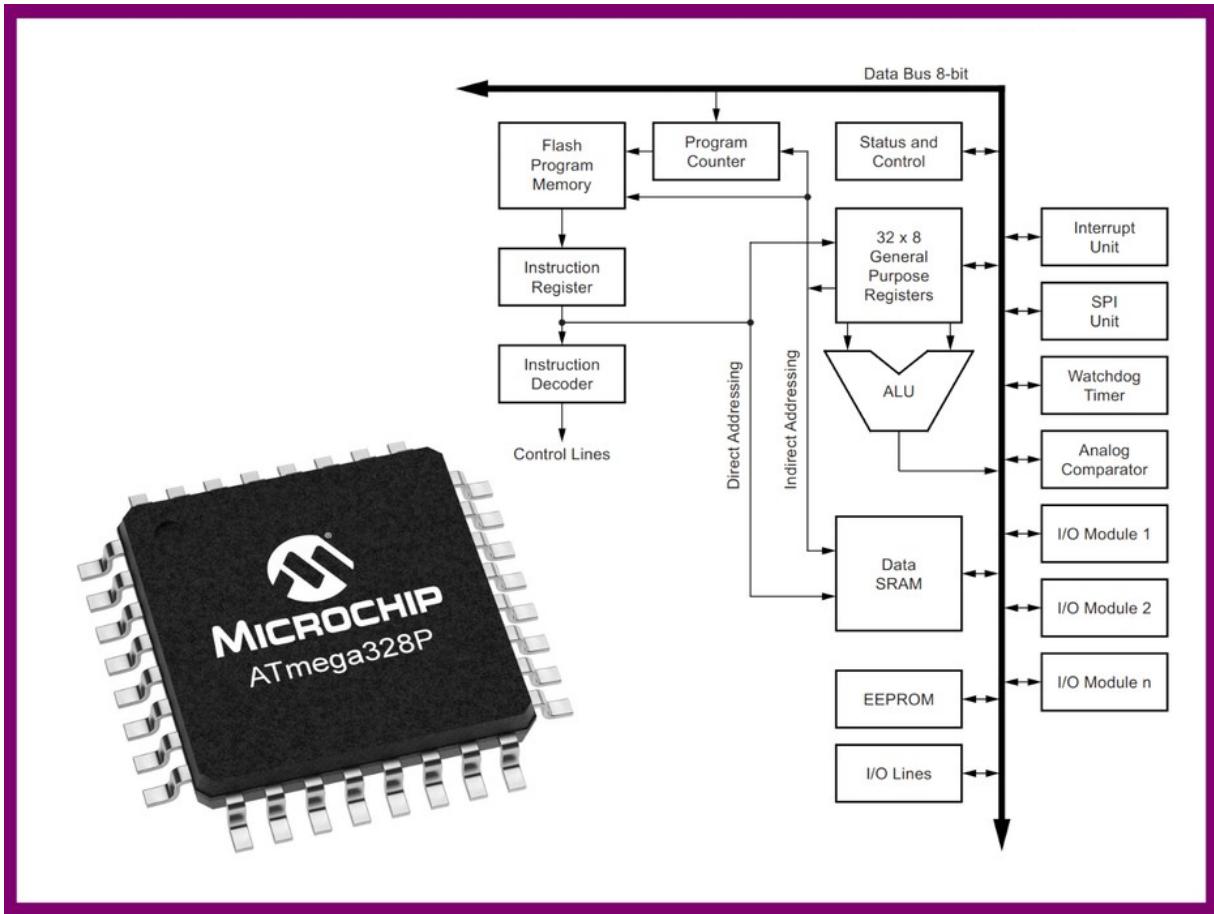


As discussed, the 7474 chip is a level of integration higher than a bunch of NAND gates. There are plenty of even more integrated chips that have multiple gates and multiple flip-flops. One such example is the 7490 Four-Bit Counter Chip ([datasheet](#)).

In the 7490, four bits of state Q<sub>a</sub>, Q<sub>b</sub>, Q<sub>c</sub>, and Q<sub>d</sub> are maintained (using flip-flops) and the binary value represented by this nibble (half of a byte) is incremented (counted up by one) every time the clock is pulsed. Assemble the 7490 circuit on the breadboard and give it a spin.

Approximately how many NAND gates would it takes to implement this four-bit counter? How many transistors would it take to implement those NAND gates? And 16 times that many to implement a 64 bit counter. It is quite easy to appreciate the power of successive integration.

## Step 43: Computer Architecture



Computer Architecture is an area of Computer Engineering concerned with the structures of computer processors. These structures include functional blocks, memories, buses, and control signals. The microarchitecture of a processor includes blocks and interconnections that implement the control path describing what the processor does and also the data path describing how data moves through the processor. The arithmetic logic unit (ALU) we've already discussed is an important example block of the architecture.

The instruction set architecture (ISA) specifies the instructions that the processor can execute and how they relate to the system's memory, data registers, and buses. A microprocessor generally includes a very small number of memory units called the registers. The instructions performed by the processor operate directly on these registers and then output results directly to the registers. The contents of the registers can be loaded in from the main memory or stored out to the main memory. The main memory is generally much, much larger than the register space (also called the register file).

The ATmega328P microcontroller chip that we are already familiar with has a RISC architecture 8-bit AVR processing core. The processor support 131 instructions that are mostly capable of executing in a single clock cycle. The processor includes a register file of 32 8-bit registers. According to the ATmega328P [datasheet](#):

The AVR uses a Harvard architecture – with separate memories and buses for program and data. Instructions in the program memory are executed with a single level pipelining. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This concept enables instructions to be executed in every clock cycle. The program memory is in-system reprogrammable flash memory.

The fast-access register file contains 32 8-bit general purpose working registers with a single clock cycle access time. This allows single-cycle arithmetic logic unit (ALU) operation. In a typical ALU operation, two operands are output from the register file, the operation is executed, and the result is stored back in the register file – in one clock cycle.

The ALU supports arithmetic and logic operations between registers or between a constant and a register. Single register operations can also be executed in the ALU. After an arithmetic operation, the status register is updated to reflect information about the result of the operation.

Program flow is provided by conditional and unconditional jump and call instructions, able to directly address the whole address space. Most AVR instructions have a single 16-bit word format. Every program memory address contains a 16-bit or 32-bit instruction. Program flash memory space is divided in two sections, the boot program section and the application program section. Both sections have dedicated lock bits for write and read/write protection.

## Step 44: Assembly Language and Machine Code

```
LDI R16, 0x43  
LDI R17, 0xD6  
LDI R18, 0x11  
LDI R19, 0x45
```

R16	0x43	R17	0xD6
R18	0x11	R19	0x45

```
ADD R17, R19  
ADC R16, R18
```

R16	0x55	R17	0x1B
-----	------	-----	------

From the 131 instructions that the AVR processor can execute, lets use just three of them to write a little program. We will use LDI (load immediate), ADC (add with carry), and ADD (add without carry).

Of the 32 8-bit registers inside the processor, we will be using four of them. They are called R16, R17, R18, and R19.

The program adds two 16-bit values together 0x43D6 and 0x1145. Since the registers are only 8 bits wide, each of those values will require two registers. The first four operations load the values that we want to add into the registers as shown by the four blocks in the center.

Next, the two lower bytes are added together using ADD and lastly the two higher bytes are added using ADC. When the higher bytes are added using "add with carry" any carry generated by adding the lower bytes is also added into the higher bytes.

While very close to the machine language used by the processor itself, assembly language is still reasonably readable by a human. A program called an assembler can

be used to convert assembly code into machine code, which in this case would be:

```
E4 03 ED 16 E1 21 E4 35 0F 13 1F 02
```

The machine code 0xE403 represents "load 0x43 into register 16", 0xED16 represents "load 0xD6 into register 17", and 0x1F02 represents "add register 16 and register 18 along with any carry from the most recent addition and put the results in register 16".

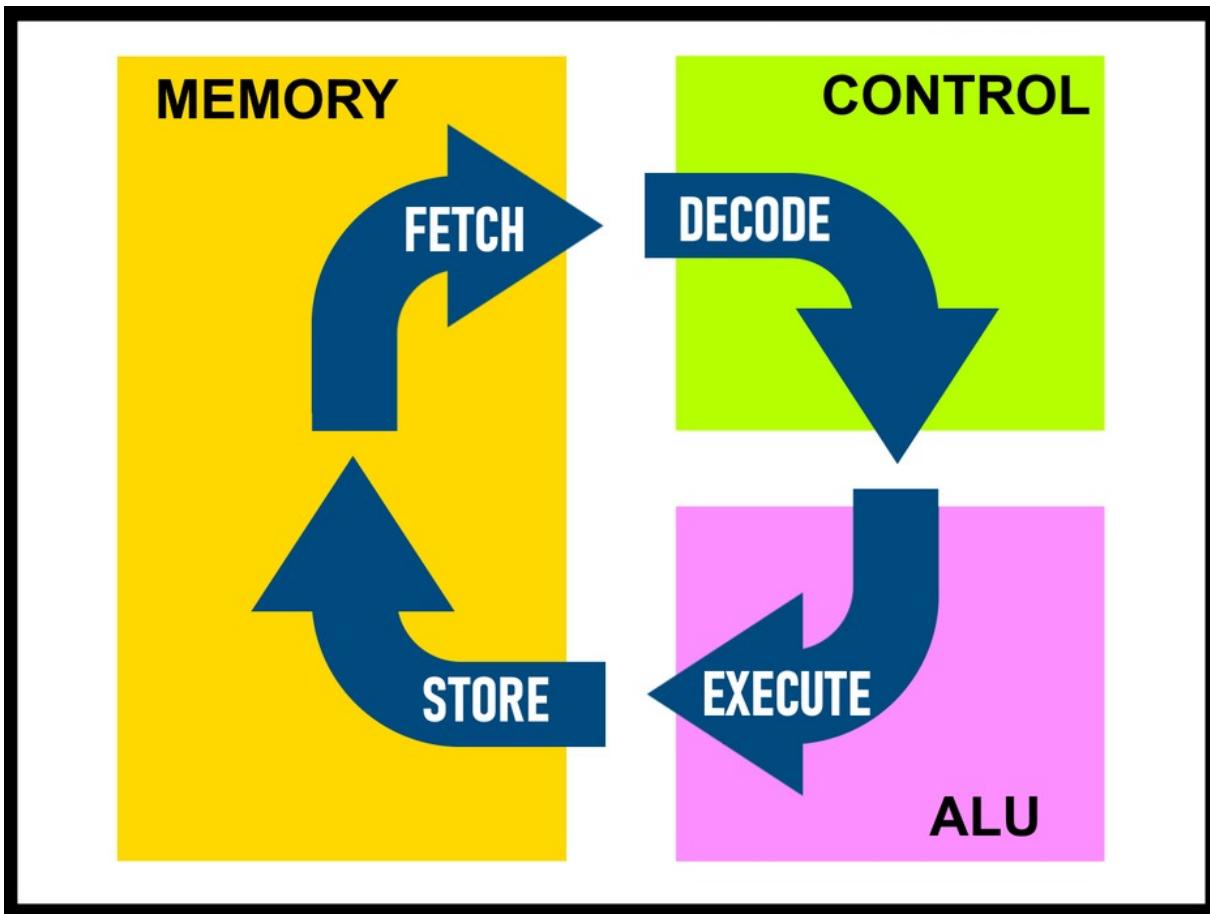
If you are very brave, you can precisely decipher the machine code using the [AVR Instruction Set Manual](#). For example, the LDI instruction is broken down on page 115.

This is quite messy, which is why assemblers were developed to allow humans to efficiently write programs using assembly language instead of machine code. Of course, higher level languages like C/C++, or Python allow us to simply write something like:

```
register int sum = 0x43D6 + 0x1145;
```

We've come a long way!

## Step 45: Instruction Cycle



The instruction cycle of a processor includes three stages: fetch, decode, and execute. We might also include store as a fourth stage or simply an implied stage.

It is useful to consider the blocks of the processor architecture while considering these stages.

**Fetch:** The program counter is a register that always contains the memory address of the current instruction being executed. That address gets pushed to the address bus to read the instruction from the main system memory into the instruction register. The program counter is incremented for use in the next cycle.

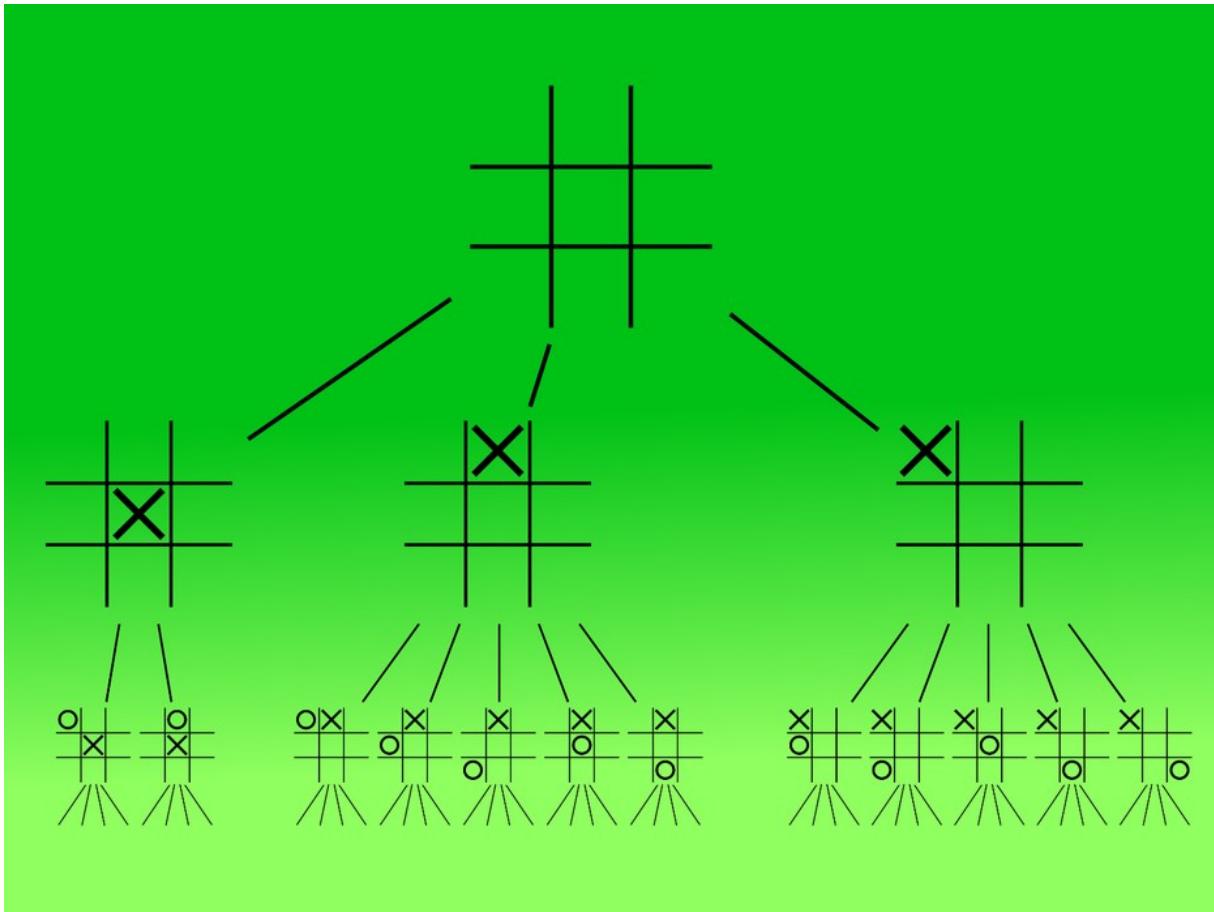
**Decode:** The instruction decoder parses the value in the instruction register to determine what the processor is being instructed to do. This is represented as control signals fed to other blocks within the processor.

**Execute:** The decoded instruction is carried out - generally by the ALU or as a memory operation.

(Store): A value may be stored from a register out to the main system memory.

The instruction cycle repeats forever.

## Step 46: Algorithms and Heuristics

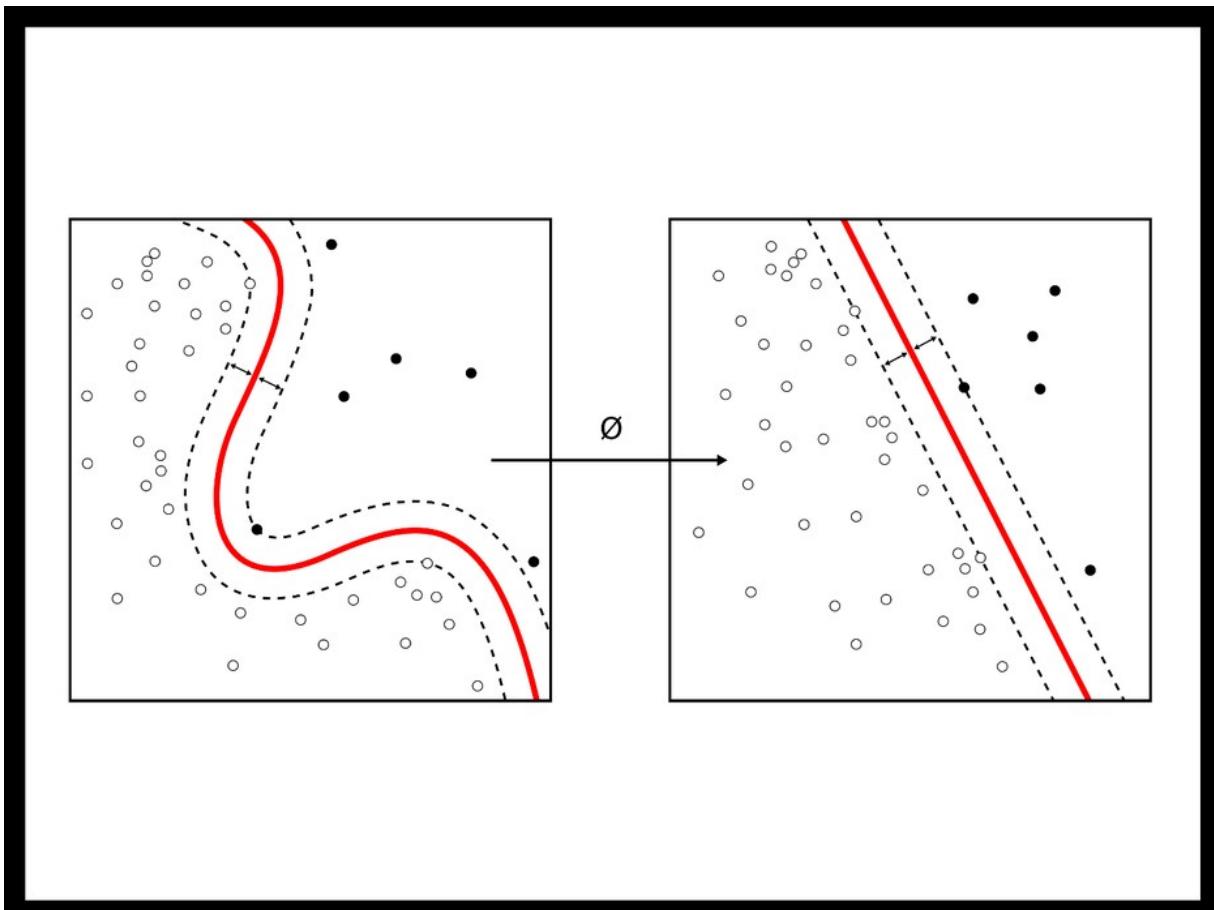


Algorithms, like programs we've encountered thus far, are specific sequences of steps or instructions to solve particular problems. The results of an algorithm are usually predictable and repeatable. Common algorithms in computer science include searching, sorting, graph traversal, game trees, and numerical algorithms such as root finding, integration, or transformations.

A heuristic approach, unlike an algorithmic solution, is generally an approximation or "best guess" to a problem that is often incompletely defined or too complex for timely exploration of a closed-form solutions. The results are usually neither predictable nor repeatable.

Using two examples from game-theory, an algorithm for tic-tac-toe would simply generate and explore all possible branches of the entire game tree. In contrast, a heuristic approach to playing chess might ignore (prune away) large portions of the game tree that do not roughly match certain characteristics of the present game. In the heuristic case, the entire tree is not searched, but the most likely portions are searched as a "best guess" approach.

## Step 47: Machine Learning



Machine Learning (ML) techniques allow machines to discover solutions to problems. Machine Learning is especially useful when a problem is hard to define or changes in real-time rendering the development of explicit human-programmed algorithms too static or costly.

ML approaches can be categorized into three types:

Supervised Learning: A training set provides the system with correct examples of inputs and outputs. The system develops a trained model capable to map the inputs to the outputs.

Unsupervised Learning: The system is given uncategorized input data and seeks to discover structure in the data. The discovered patterns may be useful on their own or may be used to establish a trained model.

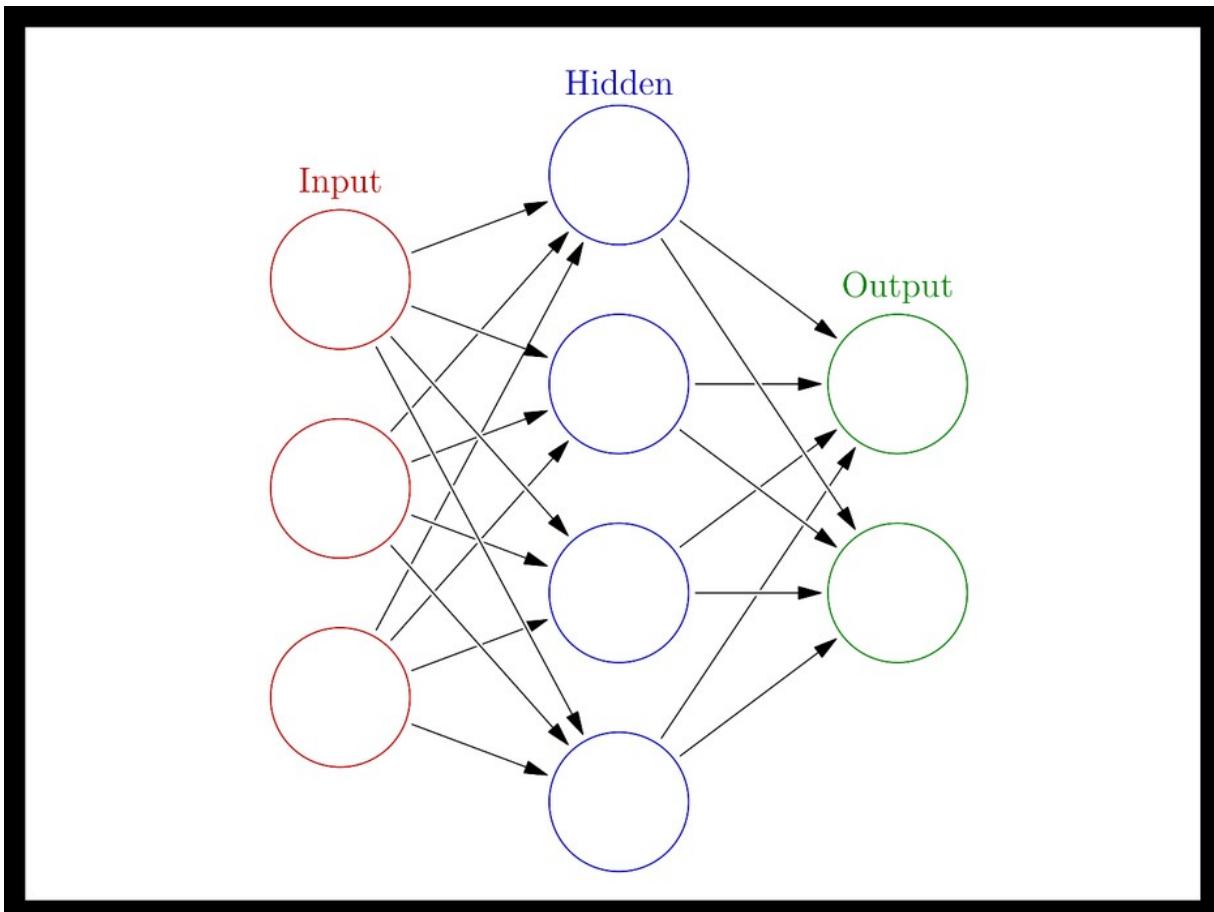
Reinforcement Learning: The system performs a task such as playing a game or picking stocks. The system's performance is reinforced (rewarded) for being successful and the system seeks to maximize obtaining rewards.

While ML is often associated with large data sets and hefty compute resources, however TinyML can run on tiny microcontrollers (such as our ATmega328P) with low power consumption. TinyML allows ML capabilities to be integrated into virtually any device.

This example of [Arduino Machine Learning](#) demonstrates how to train a TinyML model using an off-line python program that implements a classifier based on [decision tree learning](#).

The example then executes the trained model within an impressively lightweight Arduino sketch.

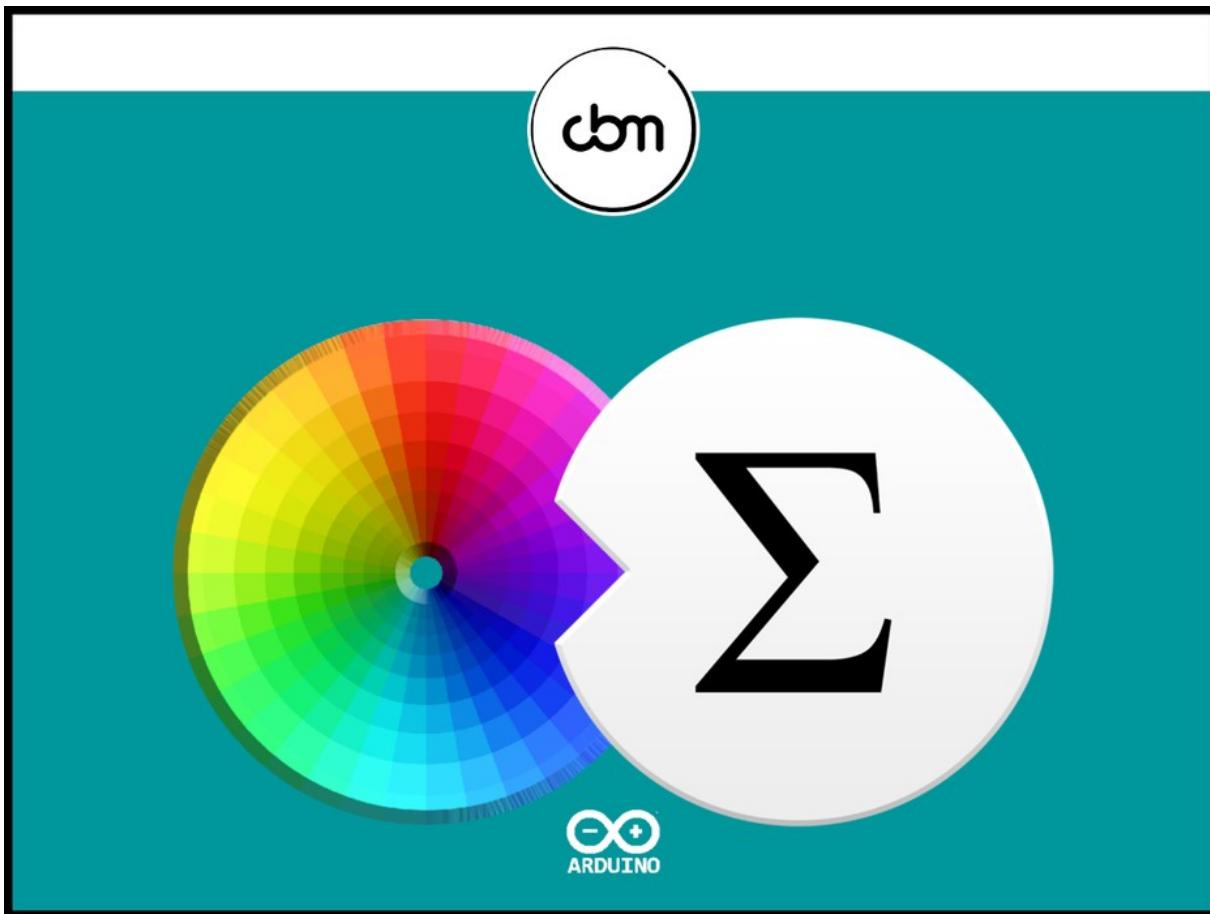
## Step 48: Artificial Neural Networks



Neural Networks, or more correctly artificial neural networks (ANNs) mimic the biological neuron structures of brains to implement specific types of machine learning. In ANNs, sets of artificial neurons are connected by weighted signals analogous to synaptic connections between biological neurons.

The output of each neuron is computed by a linear sum of its inputs. The connections between neurons have a weight that is established by the training of the network. The weight increases or decreases the strength of the connection. The neurons are generally aggregated into layers including a first layer (the input layer) and a final layer (the output layer). One or more layers between the input and output layers may be referred to as hidden layers.

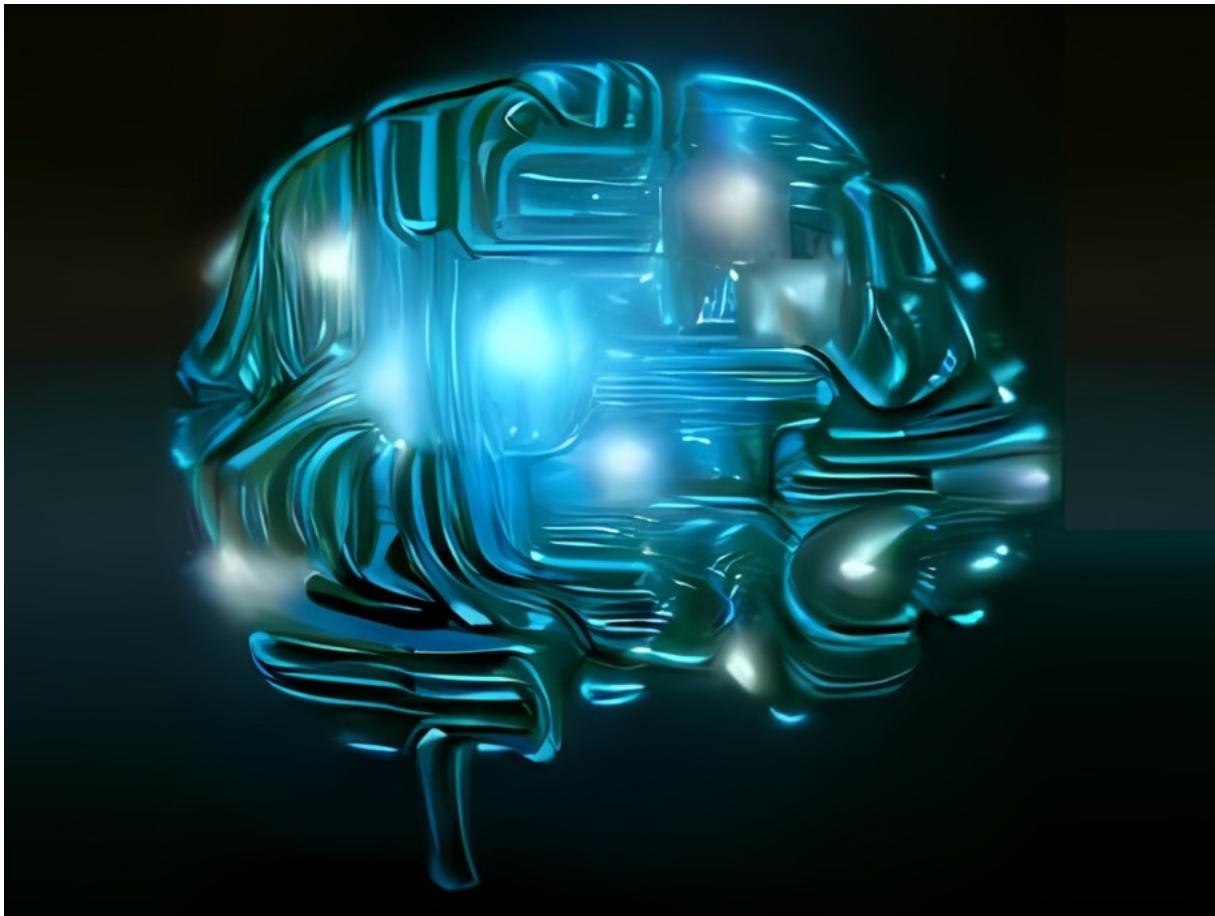
## Step 49: Embedded Neural Networks



Efficient implementations of ANNs can even be embedded into small microcontrollers. For example, the [Arduino Nuruona Library](#) from Caio Benatti Moretti allows Arduino boards to load Artificial Neural Network (ANN) structures and perform tasks such as pattern recognition (classification), non-linear regression, function approximation, and time-series prediction.

The ColorSesnor demo that comes with the library trains a neural network using the photo resistor to collect reflected light from the RGB LEDs. The trained network is capable of classifying colors as demonstrated by Moretti in this [blog entry](#).

## Step 50: Artificial Intelligence



Artificial Intelligence (AI) is a vast field comprising many different problem categories and at even more solution techniques.

A.I. was founded as an academic discipline in 1956 and has since moved through multiple cycles of optimism followed by disappointment and loss of funding. As of 2012, when deep learning surpassed previous AI techniques, there has been a vast increase in funding and interest. ([Wikipedia](#))

The A.I. technologies we have surveyed in this tutorial, including statistical learning, game trees, and neural networks, are surely just the tip of the iceberg.

**"The first ultra-intelligent machine is the last invention that man need ever make."**

- I.J. Good, A.I. Researcher, 1965

## Step 51: Hack the Planet



We hope you are enjoying the **HackerBox Basics Workshop**. To continue your adventure into electronics, computer technology, and hacker culture, visit [HackerBoxes.com](https://HackerBoxes.com) where you can find the [HackerBox Soldering Workshop](#), and [HackerBox Core Workshop](#). Together, these three workshops build towards increasingly advanced electronics projects, such as those found in the monthly HackerBox subscription boxes.

# Appendix A – Arduino Code

## Step 10 – ReadButton.ino

```
#define buttonPin 2

void setup() {
    pinMode(buttonPin, INPUT);
    Serial.begin(9600);
    Serial.println("Setup Complete");
}

void loop() {
    if (digitalRead(buttonPin))
        Serial.println("Button Pressed");
    else
        Serial.println("Button Not Pressed");
    delay(2000);
}
```

## Step 12 – ReadAnalog.ino

```
#define buttonPin 2

void setup() {
    pinMode(buttonPin, INPUT);
    Serial.begin(9600);
    Serial.println("Setup Complete");
}

void loop() {
    if (digitalRead(buttonPin))
        Serial.println("Button Pressed");
    else
        Serial.println("Button Not Pressed");
    delay(2000);
}
```

## **Step 13 – ReadVoltage.ino**

```
void setup() {  
    pinMode(A0, INPUT);  
    Serial.begin(9600);  
    Serial.println("Setup Complete");  
}  
  
void loop() {  
    int analogValue = analogRead(A0);  
    float voltage = analogValue * (5.0 / 1023.0);  
    Serial.print(voltage);  
    Serial.println(" volts");  
    delay(250);  
}
```

## **Step 17 – LEDdimmer.ino**

```
#define LEDpin 3  
  
void setup() {  
    pinMode(LEDpin, INPUT);  
}  
  
void loop() {  
    analogWrite(LEDpin, 250); // bright  
    delay(1000);  
    analogWrite(LEDpin, 150); // dim  
    delay(1000);  
    analogWrite(LEDpin, 50); // dimmer  
    delay(1000);  
}
```

## Step 19 – ReadTemp.ino

```
// Read Temperature Sensor TMP36GT9Z on Pin A0

void setup() {
    pinMode(A0, INPUT);
    Serial.begin(9600);
}

void loop() {
    int    analogValue = analogRead(A0);

    float volts = analogValue * (5.0 / 1023.0);
    float millivolts = volts * 1000;
    float tempC = (millivolts - 500) / 10;
    float tempF = (tempC * 1.8) + 32;

    Serial.print(tempC);
    Serial.print(" \u00b0"); // degree symbol
    Serial.print("C ");

    Serial.print(tempF);
    Serial.print(" \u00b0"); // degree symbol
    Serial.println("F");

    delay(1500);
}
```

## Step 20 – ControlFlow.ino

```
// anything after a double slash is a comment
// comments are not run in the program
// a comment documents what the program is doing as a
//           note to others or even you in the future
/* anything inside a pair of slash-stars is a comment */

void setup() {
    Serial.begin(9600);
}

void loop() {
    int i;

    i=0;
    if (i<1) {
        Serial.println("Yes, zero is less than one.");
    }

    if (i>1) {
        Serial.println("No! This line should never be reached.");
    } else {
        Serial.println("Yes, zero is not greater than one.");
    }

    Serial.println("Let's count to five using a for loop...");
    for (i=1; i < 6; i++) {
        Serial.println(i);
    }

    i=1;
    Serial.println("Let's count to five using a while loop...");
    while (i <= 5) {
        Serial.println(i);
        i++;
    }

    Serial.println("Let's get stuck in an infinite loop...");
    while (true); // true is always true
}
```

## Step 21 – DataArrays.ino

```
void setup() {
    Serial.begin(9600);
    Serial.println("Setup Complete");
}

void loop() {
    Serial.println("intialize an array of five integers:");
    Serial.println("int myArray[5] = {3, 4, 5, 6, 7}");
    int myArray[5] = {3, 4, 5, 6, 7};

    for (int c=0; c<5; c++){
        Serial.print("element ");
        Serial.print(c);
        Serial.print(" of myArray is ");
        Serial.println(myArray[c]);
    }

    Serial.println("The first element is index 0");
    Serial.println("The last element is index 4");
    Serial.println("There is no index 5");

    Serial.println(); //skip a line
    Serial.println("An array of characters is a string of text");
    Serial.println("char myString[]=\"my pet is a cat\"");
    char myString[]="my pet is a cat";
    Serial.println(myString);
    Serial.println("change element 12 from c to r");
    myString[12]='r';
    Serial.println(myString);

    while(1); //just wait forever
}
```

## Step 22 – Sounds.ino

```
#define NOTE_D7 2349
#define NOTE_E7 2637
#define NOTE_C7 2093
#define NOTE_C6 1047
#define NOTE_G6 1568

#define noteDuration 800
#define notePause 900

#define buzzerPin 8

void setup() {

}

void loop() {
    tone(buzzerPin, NOTE_D7, noteDuration);
    delay(notePause);
    noTone(buzzerPin);

    tone(buzzerPin, NOTE_E7, noteDuration);
    delay(notePause);
    noTone(buzzerPin);

    tone(buzzerPin, NOTE_C7, noteDuration);
    delay(notePause);
    noTone(buzzerPin);

    tone(buzzerPin, NOTE_C6, noteDuration);
    delay(notePause);
    noTone(buzzerPin);

    tone(buzzerPin, NOTE_G6, noteDuration);
    delay(notePause);
    noTone(buzzerPin);

    delay(4000); //wait 4 seconds = 4,000 ms
}
```

## Step 23 – Ultrasound.ino

```
#define echoPin 2
#define trigPin 3
#define SpeedOfSound 0.0343 // in cm-per-microsecond

void setup() {
    pinMode(echoPin, INPUT);
    pinMode(trigPin, OUTPUT);
    digitalWrite(trigPin, LOW);
    Serial.begin(9600);
}

void loop() {
    float echoTime, distance;

    digitalWrite(trigPin, HIGH);
    delayMicroseconds(10);
    digitalWrite(trigPin, LOW);

    echoTime = pulseIn(echoPin, HIGH);
    distance = (echoTime/2.0) * SpeedOfSound;
    Serial.print("distance in cm: ");
    Serial.println(distance);
    delay(200);
}
```

## Step 26 – OLEDtext.ino

```
#include <Wire.h>
#include <Adafruit_GFX.h>
#include <Adafruit_SSD1306.h>

#define SCREEN_WIDTH 128 // OLED display width, in pixels
#define SCREEN_HEIGHT 64 // OLED display height, in pixels

// Declaration for an SSD1306 display connected to I2C (SDA, SCL pins)
Adafruit_SSD1306 display(SCREEN_WIDTH, SCREEN_HEIGHT, &Wire, -1);

void setup() {
    Serial.begin(115200);

    if(!display.begin(SSD1306_SWITCHCAPVCC, 0x3C)) {
        Serial.println("SSD1306 allocation failed");
        while(1);
    }

    delay(2000);
    display.clearDisplay();
    display.setTextSize(2);
    display.setTextColor(WHITE);
    display.setCursor(10, 25);
    display.println("HACKERBOX");
    display.display();
    while(1);
}
```

## Step 27 – CommonCathodeRGB.ino

```
#define RED_LED_PIN      6
#define GREEN_LED_PIN    5
#define BLUE_LED_PIN     3

void setup() {
  pinMode(RED_LED_PIN, OUTPUT);
  pinMode(GREEN_LED_PIN, OUTPUT);
  pinMode(BLUE_LED_PIN, OUTPUT);
}

void loop() {
  RGB_LED(255, 0, 0);      // Red
  RGB_LED(0, 255, 0);      // Green
  RGB_LED(0, 0, 255);      // Blue
  RGB_LED(255, 255, 125); // Purple
  RGB_LED(0, 255, 255);   // Cyan
  RGB_LED(255, 0, 255);   // Magenta
  RGB_LED(255, 255, 0);   // Yellow
  RGB_LED(255, 255, 255); // White
}

void RGB_LED(int red_LED_value, int green_LED_value, int blue_LED_value)
{
  analogWrite(RED_LED_PIN, red_LED_value);
  analogWrite(GREEN_LED_PIN, green_LED_value);
  analogWrite(BLUE_LED_PIN, blue_LED_value);
  delay(2000);
}
```

## Step 29 – Capacitance.ino

```
// Simple Capacitance Meter
// For capacitors between 18 pF and 470 uF
// Results outputs to the Arduino Serial Monitor
//
// Sketch from Circuit Basics:
// https://www.circuitbasics.com/how-to-make-an-arduino-capacitance-meter/
///////////////////////////////
const int OUT_PIN = A2;
const int IN_PIN = A0;
const float IN_STRAY_CAP_TO_GND = 24.48;
const float IN_CAP_TO_GND = IN_STRAY_CAP_TO_GND;
const float R_PULLUP = 34.8;
const int MAX_ADC_VALUE = 1023;

void setup(){
    pinMode(OUT_PIN, OUTPUT);
    pinMode(IN_PIN, OUTPUT);
    Serial.begin(9600);
}

void loop(){
    pinMode(IN_PIN, INPUT);
    digitalWrite(OUT_PIN, HIGH);
    int val = analogRead(IN_PIN);
    digitalWrite(OUT_PIN, LOW);

    if (val < 1000){
        pinMode(IN_PIN, OUTPUT);

        float capacitance = (float)val * IN_CAP_TO_GND / (float)(MAX_ADC_VALUE - val);

        Serial.print(F("Capacitance Value = "));
        Serial.print(capacitance, 3);
        Serial.print(F(" pF ("));
        Serial.print(val);
        Serial.println(F(" )"));
    }

    else{
        pinMode(IN_PIN, OUTPUT);
        delay(1);
        pinMode(OUT_PIN, INPUT_PULLUP);
        unsigned long u1 = micros();
        unsigned long t;
        int digVal;

        do{
            digVal = digitalRead(OUT_PIN);
            unsigned long u2 = micros();
            t = u2 > u1 ? u2 - u1 : u1 - u2;
        } while ((digVal < 1) && (t < 400000L));
    }
}
```

```

pinMode(OUT_PIN, INPUT);
val = analogRead(OUT_PIN);
digitalWrite(IN_PIN, HIGH);
int dischargeTime = (int)(t / 1000L) * 5;
delay(dischargeTime);
pinMode(OUT_PIN, OUTPUT);
digitalWrite(OUT_PIN, LOW);
digitalWrite(IN_PIN, LOW);

float capacitance = -(float)t / R_PULLUP / log(1.0 - (float)val /
(float)MAX_ADC_VALUE);

Serial.print(F("Capacitance Value = "));
if (capacitance > 1000.0){
    Serial.print(capacitance / 1000.0, 2);
    Serial.print(F(" uF"));
}
else{
    Serial.print(capacitance, 2);
    Serial.print(F(" nF"));
}

Serial.print(F(" ("));
Serial.print(digVal == 1 ? F("Normal") : F("HighVal"));
Serial.print(F(", t= "));
Serial.print(t);
Serial.print(F(" us, ADC= "));
Serial.print(val);
Serial.println(F(")"));

}
while (millis() % 1000 != 0);
}

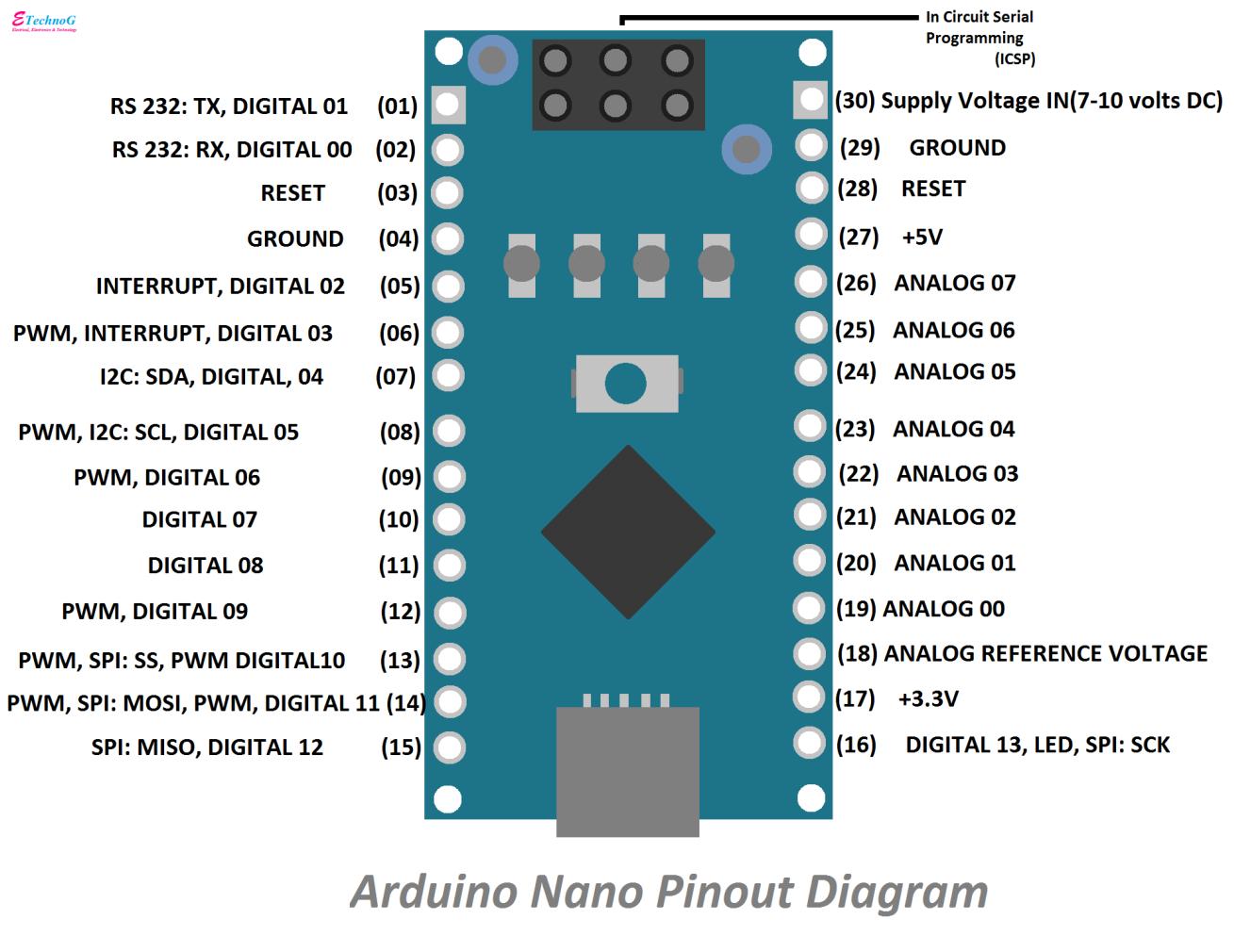
```

## Step 31 – DiodeTest.ino

```
//////////  
//  
// Measure direction of current flow between pins A1 and A2  
//  
// (Requires two 1K voltage sensing resistors)  
//  
//////////  
  
#define A1_R A0 //Pin A0 controls the 1K resistor on A1  
#define A2_R A3 //Pin A3 controls the 1K resistor on A2  
  
void setup() {  
    Serial.begin(9600);  
}  
  
void loop() {  
  
    float V1T02, V2T01;  
  
    // FIRST: measure the voltage between A1 to A2  
    // Connect A2 to GND through the 1K resistor at A3  
    pinMode(A2, INPUT);  
    pinMode(A2_R, OUTPUT);  
    digitalWrite(A2_R, 0);  
    // Connect A1 directly to 5V  
    pinMode(A1_R, INPUT);  
    pinMode(A1, OUTPUT);  
    digitalWrite(A1, 1);  
    // Read voltage at A2  
    delay(100);  
    V1T02 = 5-5*((float)analogRead(A2)/1023);  
    Serial.print("Voltage difference between A1 and A2: ");  
    Serial.print(V1T02);  
    if (V1T02 < 3)  
        Serial.println(" - current is flowing from A1 to A2");  
    else  
        Serial.println(" - current is not flowing from A1 to A2");  
  
    delay(3000);  
  
    // SECOND: measure the voltage between A2 to A1  
    // Connect A2 directly to 5V  
    pinMode(A2_R, INPUT);  
    pinMode(A2, OUTPUT);  
    digitalWrite(A2, 1);  
    // Connect A1 to GND through the 1K resistor at A0  
    pinMode(A1, INPUT);  
    pinMode(A1_R, OUTPUT);  
    digitalWrite(A1_R, 0);  
    // Read voltage at A1  
    delay(100);  
    V2T01 = 5-5*((float)analogRead(A1)/1023);  
    Serial.print("Voltage difference between A2 and A1: ");
```

```
Serial.print(V2T01);
if (V2T01 < 3)
    Serial.println(" - current is flowing from A2 to A1");
else
    Serial.println(" - current is not flowing from A2 to A1");

delay(3000);
}
```



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Component	Marking	Units
Resistors [R1]	[R1]	Ohm ( $\Omega$ , $k\Omega$ , or $M\Omega$ )
Capacitors [C1]	[C1]	Farad $\mu F$ or mF
Voltage Sources	BATT1	
BJTs	Q1	
Integrated Circuits	[C1] U1	
Operational Amplifiers	ADJ	
Logic Gates	NOT, NOR, XOR, XNOR	
Variable Resistors	[R1]	
Polarized Capacitors	C1	
Inductors	L1	
Batteries	BATT1	
n-Channel MOSFETs	Q1	
p-Channel MOSFETs	Q1	
Voltage Nodes	VCC, 5V, V+, GND, AGND	
Switches	SW1	
Diodes	D1	
LED		
Photodiode		
Schottky Diode		
Zener Diode		
DPDT		
SPST		
SP3T		
Variable Inductors	L1	
Potentiometer		
Microcontrollers	ATMEGA328P_PDI	
Power Supply	3V3	3.3v
Resistor	2.2K	2,200 $\Omega$
Transformer	T1	
Crystal	Y1	Hertz (Hz)
Inductor	L1	Henry ( $\mu H$ or mH)
Transistor (BJT)	Q1	
Integrated Circuit (IC)	IC1 U1	
Transformer		
Power Supply	Vcc	Use the spec sheet

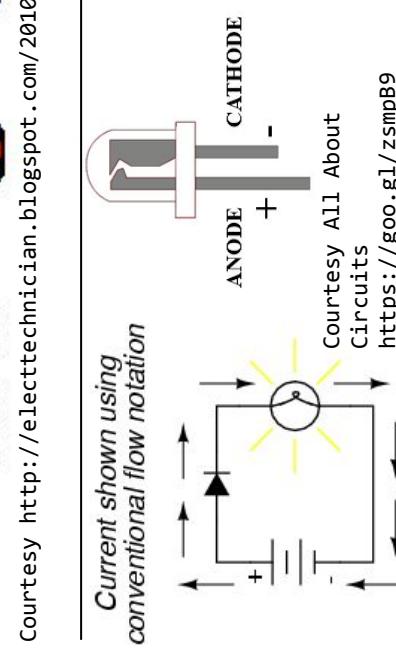
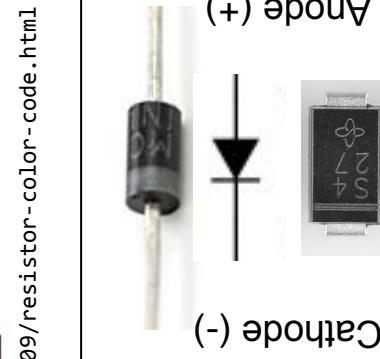
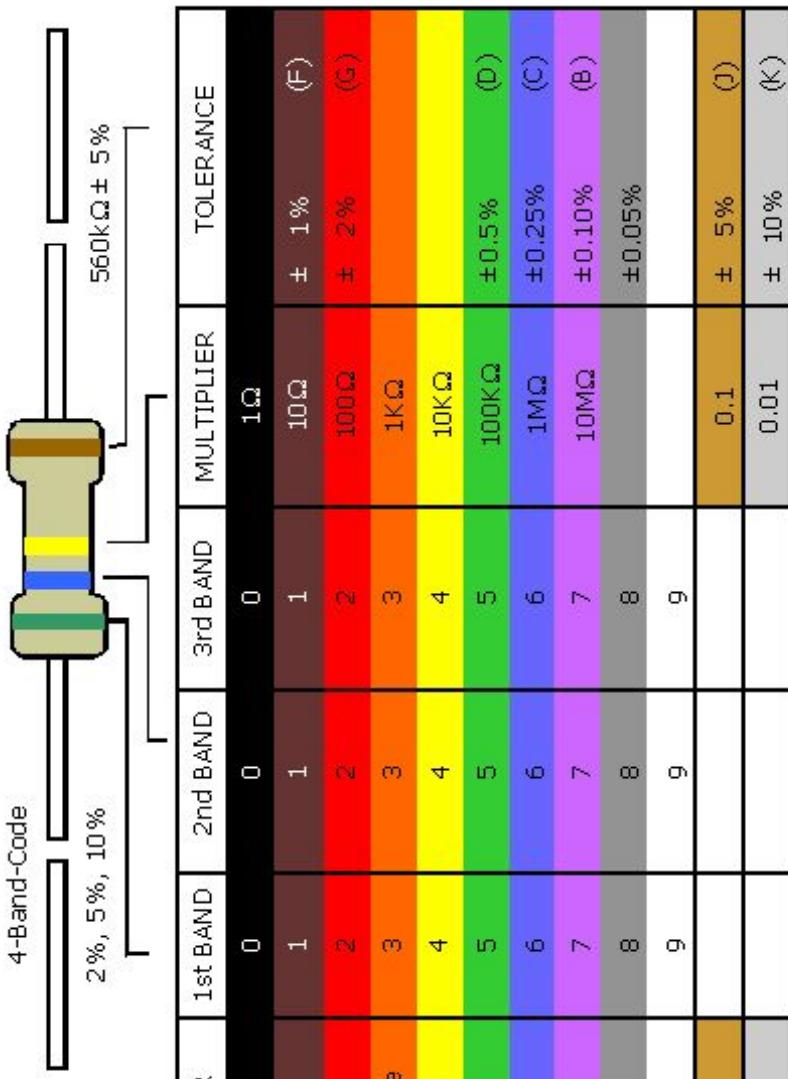
Component drawing  
courtesy SparkFun.





tera (T)	1,000,000,000,000
giga (G)	1,000,000,000
mega (M)	1,000,000
kilo (k)	1,000
hecto (h)	100
deca (da)	10
deci (d)	0.1
centi (c)	0.01
milli (m)	0.001
micro ( $\mu$ )	0.000 001
nano (n)	0.000 000 001
pico (p)	0.000 000 000 001

Courtesy  
<https://plainphysics.com/category/ordinary-physics/mechanics/si-units>

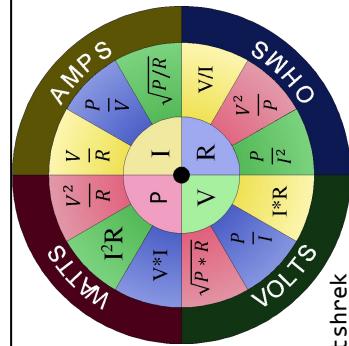


$$\underline{104} = 10 \times 10^4$$

Suffix with 4 Zeros

$$\underline{10000} \text{ pF}$$

Courtesy  
<https://learn.sparkfun.com/tutorials/capacitor-kit-identification-guide>



Courtesy  
<https://imgur.com/user/fatshrek>



## SNx400, SNx4LS00, and SNx4S00 Quadruple 2-Input Positive-NAND Gates

### 1 Features

- Package Options Include:
  - Plastic Small-Outline (D, NS, PS)
  - Shrink Small-Outline (DB)
  - Ceramic Flat (W)
  - Ceramic Chip Carriers (FK)
  - Standard Plastic (N)
  - Ceramic (J)
- Also Available as Dual 2-Input Positive-NAND Gate in Small-Outline (PS) Package
- Inputs Are TTL Compliant;  $V_{IH} = 2\text{ V}$  and  $V_{IL} = 0.8\text{ V}$
- Inputs Can Accept 3.3-V or 2.5-V Logic Inputs
- SN5400, SN54LS00, and SN54S00 are Characterized For Operation Over the Full Military Temperature Range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$

### 2 Applications

- AV Receivers
- Portable Audio Docks
- Blu-Ray Players
- Home Theater
- MP3 Players or Recorders
- Personal Digital Assistants (PDAs)

### 3 Description

The SNx4xx00 devices contain four independent, 2-input NAND gates. The devices perform the Boolean function  $Y = A \cdot B$  or  $Y = \bar{A} + B$  in positive logic.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LS00DB	SSOP (14)	6.20 mm × 5.30 mm
SN7400D, SN74LS00D, SN74S00D	SOIC (14)	8.65 mm × 3.91 mm
SN74LS00NSR	PDIP (14)	19.30 × 6.35 mm
SNJ5400J, SNJ54LS00J, SNJ54S00J	CDIP (14)	19.56 mm × 6.67 mm
SNJ5400W, SNJ54LS00W, SNJ54S00W	CFP (14)	9.21 mm × 5.97 mm
SN54LS00FK, SN54S00FK	LCCC (20)	8.89 mm × 8.89 mm
SN7400NS, SN74LS00NS, SN74S00NS	SO (14)	10.30 mm × 5.30 mm
SN7400PS, SN74LS00PS	SO (8)	6.20 mm × 5.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Logic Diagram, Each Gate (Positive Logic)



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

## Table of Contents

<b>1</b>	<b>Features .....</b>	<b>1</b>
<b>2</b>	<b>Applications .....</b>	<b>1</b>
<b>3</b>	<b>Description .....</b>	<b>1</b>
<b>4</b>	<b>Revision History.....</b>	<b>2</b>
<b>5</b>	<b>Pin Configuration and Functions .....</b>	<b>3</b>
<b>6</b>	<b>Specifications.....</b>	<b>4</b>
6.1	Absolute Maximum Ratings .....	4
6.2	ESD Ratings: SN74LS00 .....	4
6.3	Recommended Operating Conditions .....	4
6.4	Thermal Information .....	6
6.5	Electrical Characteristics: SNx400 .....	6
6.6	Electrical Characteristics: SNx4LS00 .....	6
6.7	Electrical Characteristics: SNx4S00 .....	6
6.8	Switching Characteristics: SNx400 .....	7
6.9	Switching Characteristics: SNx4LS00.....	7
6.10	Switching Characteristics: SNx4S00.....	7
6.11	Typical Characteristics .....	8
<b>7</b>	<b>Parameter Measurement Information .....</b>	<b>9</b>
7.1	Propagation Delays, Setup and Hold Times, and Pulse Width.....	9
<b>8</b>	<b>Detailed Description .....</b>	<b>10</b>
8.1	Overview .....	10
8.2	Functional Block Diagram .....	10
8.3	Feature Description.....	10
8.4	Device Functional Modes.....	10
<b>9</b>	<b>Application and Implementation .....</b>	<b>11</b>
9.1	Application Information.....	11
9.2	Typical Application .....	11
<b>10</b>	<b>Power Supply Recommendations .....</b>	<b>12</b>
<b>11</b>	<b>Layout.....</b>	<b>13</b>
11.1	Layout Guidelines .....	13
11.2	Layout Example .....	13
<b>12</b>	<b>Device and Documentation Support .....</b>	<b>14</b>
12.1	Documentation Support .....	14
12.2	Related Links .....	14
12.3	Receiving Notification of Documentation Updates	14
12.4	Community Resources.....	14
12.5	Trademarks .....	14
12.6	Electrostatic Discharge Caution.....	14
12.7	Glossary .....	14
<b>13</b>	<b>Mechanical, Packaging, and Orderable Information .....</b>	<b>15</b>

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

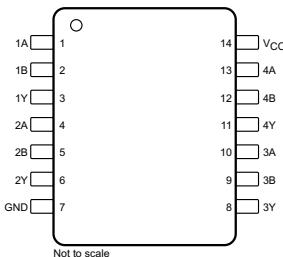
Changes from Revision C (November 2016) to Revision D	Page
• Changed <i>Typical Application Diagram</i> see <i>Application and Implementation</i> section.....	1

Changes from Revision B (October 2003) to Revision C	Page
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section.....	1
• Changed <i>Ordering Information</i> table to <i>Device Comparison Table</i> ; see <i>Package Option Addendum</i> at the end of the data sheet.....	1
• Changed Package thermal impedance, $R_{\theta,JA}$ , values in <i>Thermal Information</i> table From: 86°C/W To: 90.9°C/W (D), From: 96°C/W To: 102.8°C/W (DB), From: 80°C/W To: 54.8°C/W (N), and From: 76°C/W To: 89.7°C/W (NS).....	6

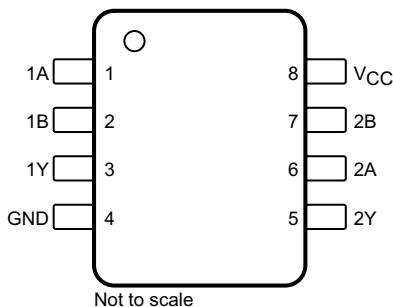
## 5 Pin Configuration and Functions

**SN5400 J, SN54xx00 J and W, SN74x00 D, N, and NS, or  
SN74LS00 D, DB, N, and NS Packages  
14-Pin CDIP, CFP, SOIC, PDIP, SO, or SSOP**

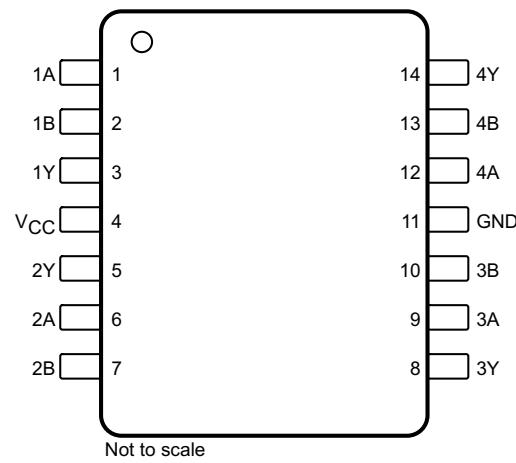
Top View



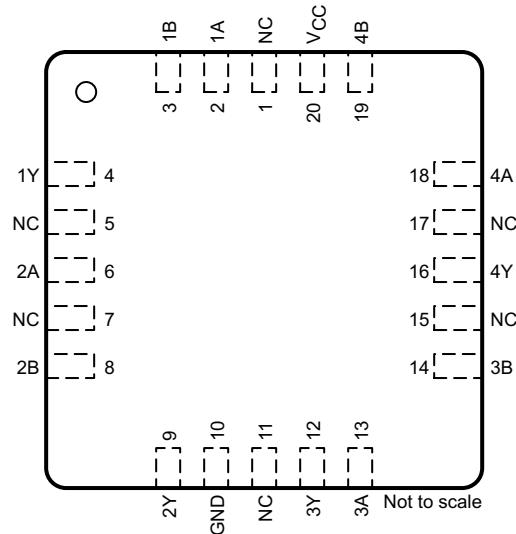
**SN5400 W Package  
14-Pin CFP  
Top View**



**SN74xx00 PS Package  
18-Pin SO  
Top View**



**SN54xx00 FK Package  
20-Pin LCCC  
Top View**



### Pin Functions

NAME	CDIP, CFP, SOIC, PDIP, SO, SSOP	PIN				I/O	DESCRIPTION
		SO (SN74xx00)	CFP (SN5400)	LCCC			
1A	1	1	1	2	I	Gate 1 input	
1B	2	2	2	3	I	Gate 1 input	
1Y	3	3	3	4	O	Gate 1 output	
2A	4	6	6	6	I	Gate 2 input	
2B	5	7	7	8	I	Gate 2 input	
2Y	6	5	5	9	O	Gate 2 output	
3A	10	—	9	13	I	Gate 3 input	
3B	9	—	10	14	I	Gate 3 input	

### Pin Functions (continued)

NAME	PIN				I/O	DESCRIPTION
	CDIP, CFP, SOIC, PDIP, SO, SSOP	SO (SN74xx00)	CFP (SN5400)	LCCC		
3Y	8	—	8	12	O	Gate 3 output
4A	13	—	12	18	I	Gate 4 input
4B	12	—	13	19	I	Gate 4 input
4Y	11	—	14	16	O	Gate 4 output
GND	7	4	11	10	—	Ground
NC	—	—	—	1, 5, 7, 11, 15, 17	—	No connect
V <sub>CC</sub>	14	8	4	20	—	Power supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage, V <sub>CC</sub> <sup>(2)</sup>		7		V
Input voltage	SNx400 and SNxS400	5.5		V
	SNx4LS00	7		
Junction temperature, T <sub>J</sub>		150		°C
Storage temperature, T <sub>stg</sub>		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Voltage values are with respect to network ground terminal.

### 6.2 ESD Ratings: SN74LS00

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance. ESD Tested on SN74LS00N package.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	SN54xx00	4.5	5	5.5	V
		SN74xx00	4.75	5	5.25	
V <sub>IH</sub>	High-level input voltage		2			V
V <sub>IL</sub>	Low-level input voltage	SNx400, SN7LS400, and SNx4S00			0.8	V
		SN54LS00			0.7	
I <sub>OH</sub>	High-level output current	SN5400, SN54LS00, and SN74LS00			-0.4	mA
		SNx4S00			-1	
I <sub>OL</sub>	Low-level output current	SNx400			16	mA
		SN5LS400			4	
		SN7LS400			8	
		SNx4S00			20	

## Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T <sub>A</sub>	Operating free-air temperature	SN54xx00		-55	125
		SN74xx00		0	70 °C

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)(2)</sup>		SN74LS00				UNIT
		D (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	
		14 PINS	14 PINS	14 PINS	14 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	90.9	102.8	54.8	89.7	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	51.9	53.3	42.1	48.1	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	48	53.4	34.8	50.1	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	18.6	16.5	26.9	16.7	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	47.8	52.9	34.7	49.8	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

(2) The package thermal impedance is calculated in accordance with JESD 51-7.

## 6.5 Electrical Characteristics: SNx400

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V <sub>IK</sub>	V <sub>CC</sub> = MIN and I <sub>I</sub> = -12 mA				-1.5	V
V <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8 V, and I <sub>OH</sub> = -0.4 mA		2.4	3.4		V
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, and I <sub>OL</sub> = 16 mA			0.2	0.4	V
I <sub>I</sub>	V <sub>CC</sub> = MAX and V <sub>I</sub> = 5.5 V				1	mA
I <sub>IH</sub>	V <sub>CC</sub> = MAX and V <sub>I</sub> = 2.4 V				40	µA
I <sub>IL</sub>	V <sub>CC</sub> = MAX and V <sub>I</sub> = 0.4 V				-1.6	mA
I <sub>OS</sub>	V <sub>CC</sub> = MAX	SN5400	-20	-55		mA
I <sub>CCH</sub>		SN7400	-18	-55		
I <sub>CCL</sub>	V <sub>CC</sub> = MAX and V <sub>I</sub> = 0 V			4	8	mA
	V <sub>CC</sub> = MAX and V <sub>I</sub> = 4.5 V			12	22	mA

## 6.6 Electrical Characteristics: SNx4LS00

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V <sub>IK</sub>	V <sub>CC</sub> = MIN and I <sub>I</sub> = -18 mA				-1.5	V
V <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, and I <sub>OH</sub> = -0.4 mA		2.5	3.4		V
V <sub>OL</sub>	V <sub>CC</sub> = MIN and V <sub>IH</sub> = 2 V	I <sub>OL</sub> = 4 mA		0.25	0.4	V
		I <sub>OL</sub> = 8 mA (SN74LS00)		0.35	0.5	
I <sub>I</sub>	V <sub>CC</sub> = MAX and V <sub>I</sub> = 7 V				0.1	mA
I <sub>IH</sub>	V <sub>CC</sub> = MAX and V <sub>I</sub> = 2.7 V				20	µA
I <sub>IL</sub>	V <sub>CC</sub> = MAX and V <sub>I</sub> = 0.4 V				-0.4	mA
I <sub>OS</sub>	V <sub>CC</sub> = MAX		-20	-100		mA
I <sub>CCH</sub>	V <sub>CC</sub> = MAX and V <sub>I</sub> = 0 V			0.8	1.6	mA
I <sub>CCL</sub>	V <sub>CC</sub> = MAX and V <sub>I</sub> = 4.5 V			2.4	4.4	mA

## 6.7 Electrical Characteristics: SNx4S00

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V <sub>IK</sub>	V <sub>CC</sub> = MIN and I <sub>I</sub> = -18 mA				-1.2	V
V <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8 V, and I <sub>OH</sub> = -1 mA		2.5	3.4		V
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, and I <sub>OL</sub> = 20 mA				0.5	V
I <sub>I</sub>	V <sub>CC</sub> = MAX and V <sub>I</sub> = 5.5 V				1	mA
I <sub>IH</sub>	V <sub>CC</sub> = MAX and V <sub>I</sub> = 2.7 V				50	µA
I <sub>IL</sub>	V <sub>CC</sub> = MAX and V <sub>I</sub> = 0.5 V				-2	mA

## Electrical Characteristics: SNx4S00 (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>OS</sub>	V <sub>CC</sub> = MAX	-40		-100	mA
I <sub>CCH</sub>	V <sub>CC</sub> = MAX and V <sub>I</sub> = 0 V		10	16	mA
I <sub>CCL</sub>	V <sub>CC</sub> = MAX and V <sub>I</sub> = 4.5 V		20	36	mA

## 6.8 Switching Characteristics: SNx400

V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C, and over operating free-air temperature range (unless otherwise noted). See [Figure 2](#).

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	A or B	Y	R <sub>L</sub> = 400 Ω and C <sub>L</sub> = 15 pF	11	22		ns
t <sub>PHL</sub>				7	15		

## 6.9 Switching Characteristics: SNx4LS00

V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C, and over operating free-air temperature range (unless otherwise noted). See [Figure 2](#).

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	A or B	Y	R <sub>L</sub> = 2 kΩ and C <sub>L</sub> = 15 pF	9	15		ns
t <sub>PHL</sub>				10	15		

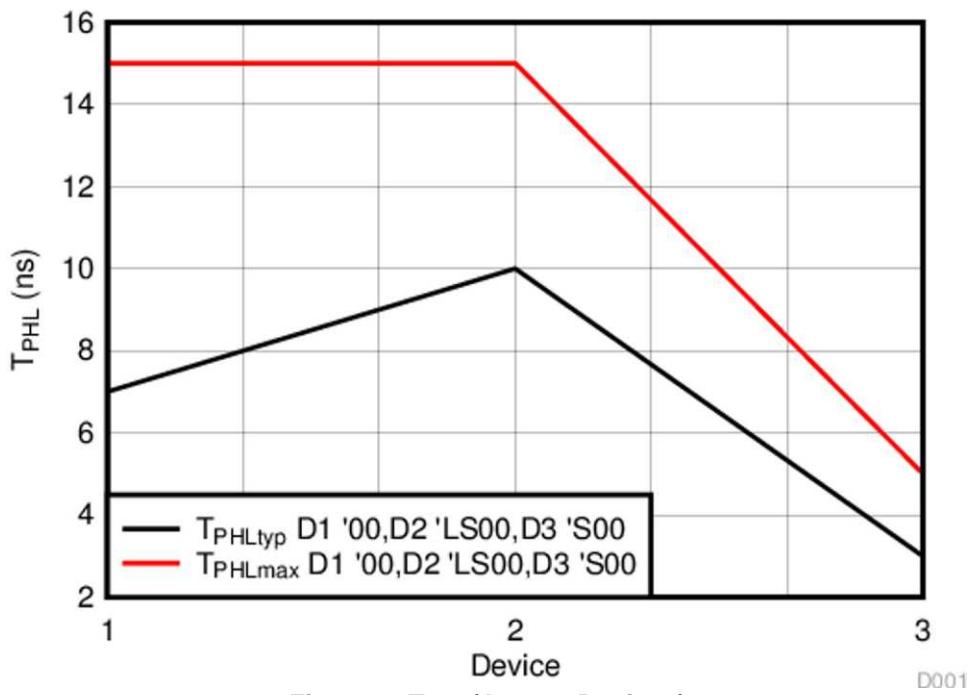
## 6.10 Switching Characteristics: SNx4S00

V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C, and over operating free-air temperature range (unless otherwise noted). See [Figure 2](#).

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	A or B	Y	R <sub>L</sub> = 280 Ω and C <sub>L</sub> = 15 pF	3	4.5		ns
			R <sub>L</sub> = 280 Ω and C <sub>L</sub> = 50 pF	4.5			
t <sub>PHL</sub>	A or B	Y	R <sub>L</sub> = 280 Ω and C <sub>L</sub> = 15 pF	3	5		ns
			R <sub>L</sub> = 280 Ω and C <sub>L</sub> = 50 pF	5			

## 6.11 Typical Characteristics

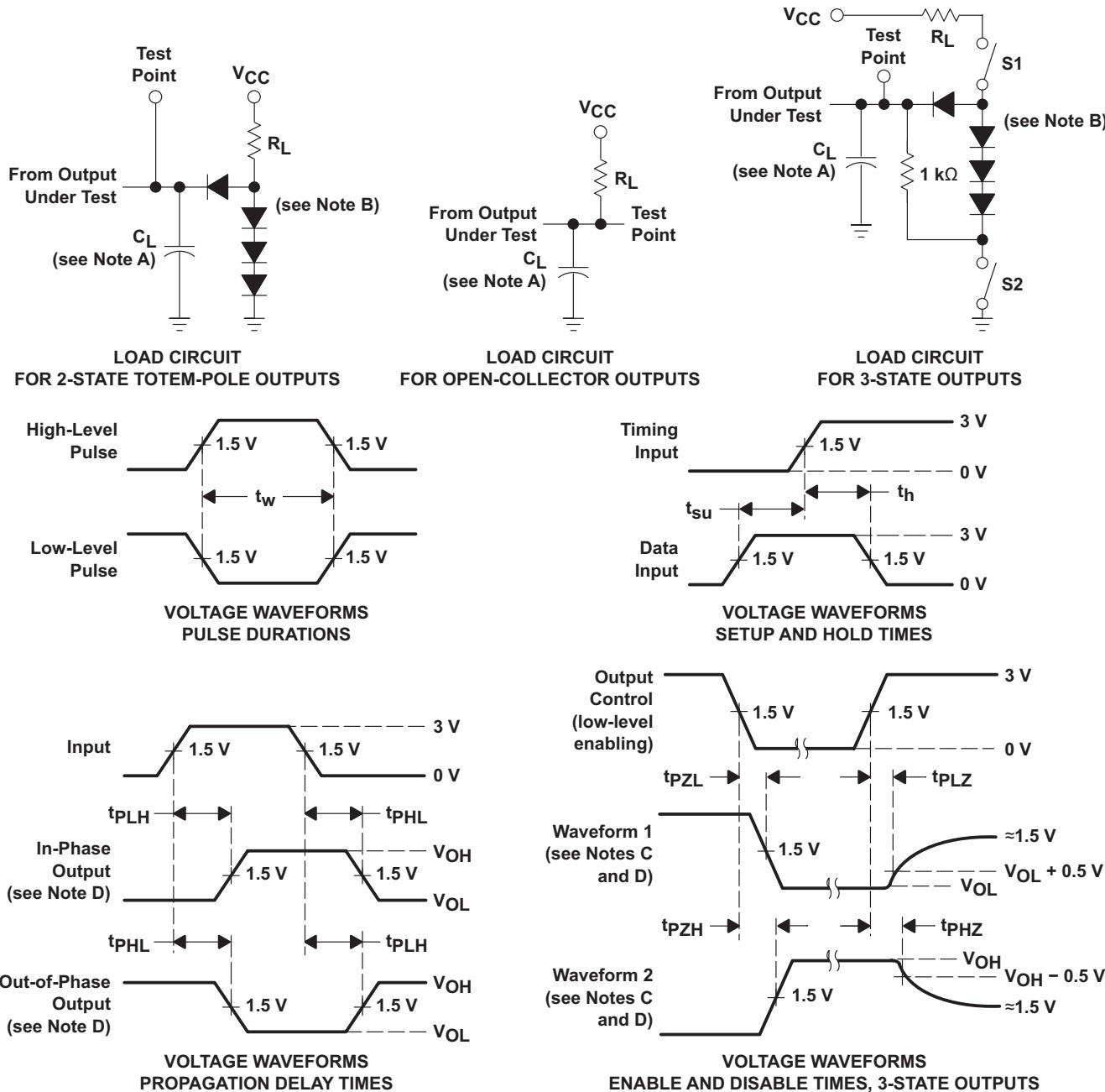
$C_L = 15 \text{ pF}$



**Figure 1.  $T_{PHL}$  (Across Devices)**

## 7 Parameter Measurement Information

### 7.1 Propagation Delays, Setup and Hold Times, and Pulse Width



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - All diodes are 1N3064 or equivalent.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - S1 and S2 are closed for  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_{PZH}$ , and  $t_{PLZ}$ ; S1 is open and S2 is closed for  $t_{PZH}$ ; S1 is closed and S2 is open for  $t_{PLZ}$ .
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O \approx 50 \Omega$ ;  $t_r$  and  $t_f \leq 7 \text{ ns}$  for Series 54/74 devices and  $t_r$  and  $t_f \leq 2.5 \text{ ns}$  for Series 54S/74S devices.
  - The outputs are measured one at a time with one input transition per measurement.

**Figure 2. Load Circuits and Voltage Waveforms**

## 8 Detailed Description

### 8.1 Overview

The SNx4xx00 devices are quadruple, 2-input NAND gates which perform the Boolean function  $Y = \overline{A} \cdot \overline{B}$  or  $Y = A + B$  in positive logic.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

The operating voltage of SN74xx00 is from 4.75-V to 5.25-V  $V_{CC}$ . The operating voltage of SN54xx00 is from 4.5-V to 5.5-V  $V_{CC}$ . The SN54xx00 devices are rated from  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  whereas SN74xx00 device are rated from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

### 8.4 Device Functional Modes

Table 1 lists the functions of the devices.

**Table 1. Functional Table (Each Gate)**

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

## 9 Application and Implementation

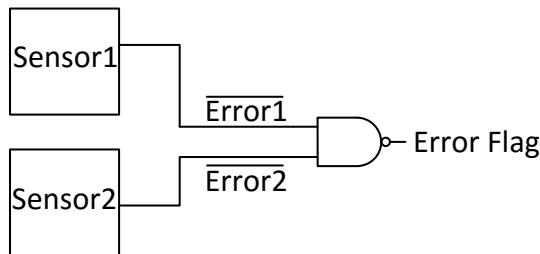
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The SNx4xx00 devices are quadruple, 2-input NAND gate. A typical application of NAND gate can be as an error indicator as shown in [Figure 3](#). If either of the sensor has an error, the error flag is high to indicate system error.

### 9.2 Typical Application



**Figure 3. Typical Application Diagram**

#### 9.2.1 Design Requirements

These devices use BJT technology and have unbalanced output drive with  $I_{OL}$  and  $I_{OH}$  specified as per the [Recommended Operating Conditions](#).

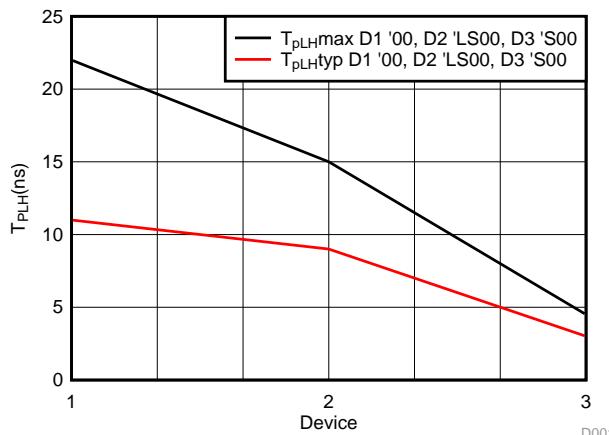
#### 9.2.2 Detailed Design Procedure

- Recommended Input Conditions:
  - The inputs are TTL compliant.
  - Because the base-emitter junction at the inputs breaks down, no voltage greater than 5.5 V must be applied to the inputs.
  - Specified high and low levels: See  $V_{IH}$  and  $V_{IL}$  in [Recommended Operating Conditions](#).
- Recommended Output Conditions:
  - No more than one output must be shorted at a time as per the [Electrical Characteristics: SNx400](#) for thermal stability and reliability.
  - For high-current applications, consider thermal characteristics of the package listed in [Thermal Information](#).

## Typical Application (continued)

### 9.2.3 Application Curve

$C_L = 15 \text{ pF}$



**Figure 4.  $T_{PLH}$  (Across Devices)**

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in *Recommended Operating Conditions* for each of the SNx4LS00, SNx4S00, and SNx400 devices.

Each  $V_{CC}$  pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply,  $0.1 \mu\text{F}$  is recommended; if there are multiple  $V_{CC}$  pins, then  $0.01 \mu\text{F}$  or  $0.022 \mu\text{F}$  is recommended for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A  $0.1 \mu\text{F}$  and a  $1 \mu\text{F}$  are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

When using multiple bit logic, devices inputs must never float.

Devices with multiple-emitter inputs (SN74 and SN74S series) need special care. Because no voltage greater than 5.5 V must be applied to the inputs (if exceeded, the base-emitter junction at the inputs breaks down), the inputs of these devices must be connected to the supply voltage,  $V_{CC}$ , through series resistor,  $R_S$  (see [Figure 5](#)). This resistor must be dimensioned such that the current flowing into the gate or gates, which results from overvoltage, does not exceed 1 mA. However, because the high-level input current of the circuits connected to the gate flows through this resistor, the resistor must be dimensioned so that the voltage drop across it still allows the required high level. [Equation 1](#) and [Equation 2](#) are for dimensioning resistor,  $R_S$ , and several inputs can be connected to a high level through a single resistor if the following conditions are met.

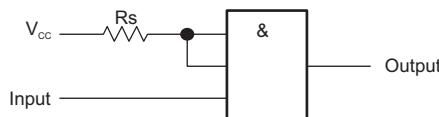
$$R_{S(\min)} \frac{V_{CCP} - 5.5 \text{ V}}{1 \text{ mA}} \quad (1)$$

$$R_{S(\max)} \frac{V_{CC(\min)} - 2.4 \text{ V}}{n I_{IH}} \quad (2)$$

where

- $n$  = number of inputs connected
- $I_{IH}$  = high input current (typical 40  $\mu\text{A}$ )
- $V_{CC(\min)}$  = minimum supply voltage,  $V_{CC}$
- $V_{CCP}$  = maximum peak voltage of the supply voltage,  $V_{CC}$  (about 7 V)

### 11.2 Layout Example



**Figure 5. Series Resistor Connected to Unused Inputs of Multiple-Emitter Transistors**

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

*Designing With Logic* (SDYA009)

### 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN5400	<a href="#">Click here</a>				
SN54LS00	<a href="#">Click here</a>				
SN54S00	<a href="#">Click here</a>				
SN7400	<a href="#">Click here</a>				
SN74LS00	<a href="#">Click here</a>				
SN74S00	<a href="#">Click here</a>				

### 12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.5 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 12.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.7 Glossary

[SLYZ022 — TI Glossary](#).

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
JM38510/00104BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/00104BCA	Samples
JM38510/00104BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/00104BDA	Samples
JM38510/07001BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/07001BCA	Samples
JM38510/07001BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/07001BDA	Samples
JM38510/30001B2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30001B2A	Samples
JM38510/30001BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30001BCA	Samples
JM38510/30001BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30001BDA	Samples
JM38510/30001SCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30001S CA	Samples
JM38510/30001SDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30001S DA	Samples
M38510/00104BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/00104BCA	Samples
M38510/00104BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/00104BDA	Samples
M38510/07001BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/07001BCA	Samples
M38510/07001BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/07001BDA	Samples
M38510/30001B2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30001B2A	Samples
M38510/30001BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30001BCA	Samples
M38510/30001BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30001BDA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
M38510/30001SCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30001S CA	Samples
M38510/30001SDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30001S DA	Samples
SN5400J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN5400J	Samples
SN54LS00J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS00J	Samples
SN54S00J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54S00J	Samples
SN7400D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7400	Samples
SN7400DG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7400	Samples
SN7400N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN7400N	Samples
SN7400NE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN7400N	Samples
SN74LS00DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS00	Samples
SN74LS00DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS00	Samples
SN74LS00N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS00N	Samples
SN74LS00NE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS00N	Samples
SN74LS00NS	OBsolete	SO	NS	14	TBD		Call TI	Call TI	0 to 70	74LS00	
SN74LS00NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS00	Samples
SN74LS00NSRG4	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS00	Samples
SN74LS00PSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS00	Samples
SN74S00D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	S00	Samples
SN74S00N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74S00N	Samples
SNJ5400J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ5400J	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ5400W	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ5400W	Samples
SNJ54LS00FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS00FK	Samples
SNJ54LS00J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS00J	Samples
SNJ54LS00W	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS00W	Samples
SNJ54S00FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54S00FK	Samples
SNJ54S00J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54S00J	Samples
SNJ54S00W	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54S00W	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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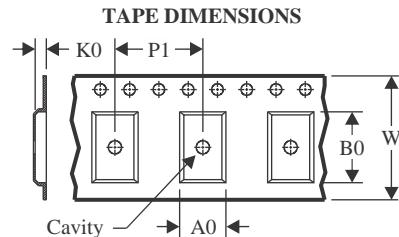
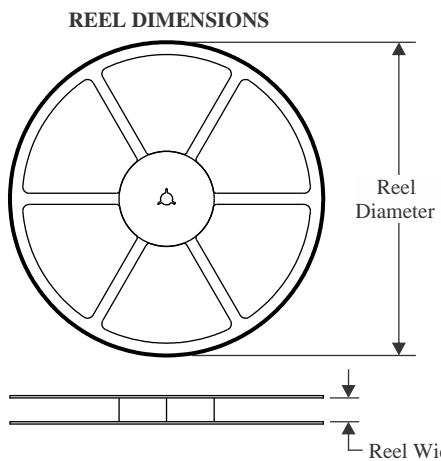
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN5400, SN54LS00, SN54LS00-SP, SN54S00, SN7400, SN74LS00, SN74S00 :**

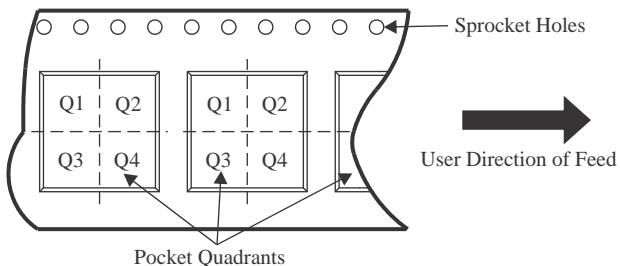
- Catalog : [SN7400](#), [SN74LS00](#), [SN54LS00](#), [SN74S00](#)
- Military : [SN5400](#), [SN54LS00](#), [SN54S00](#)
- Space : [SN54LS00-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

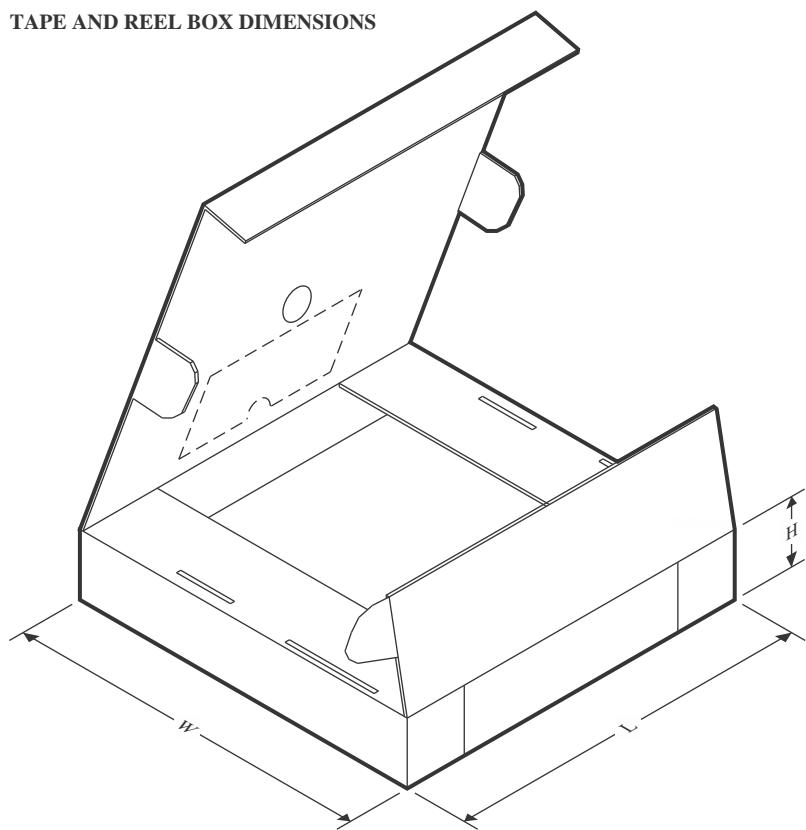
**TAPE AND REEL INFORMATION**

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

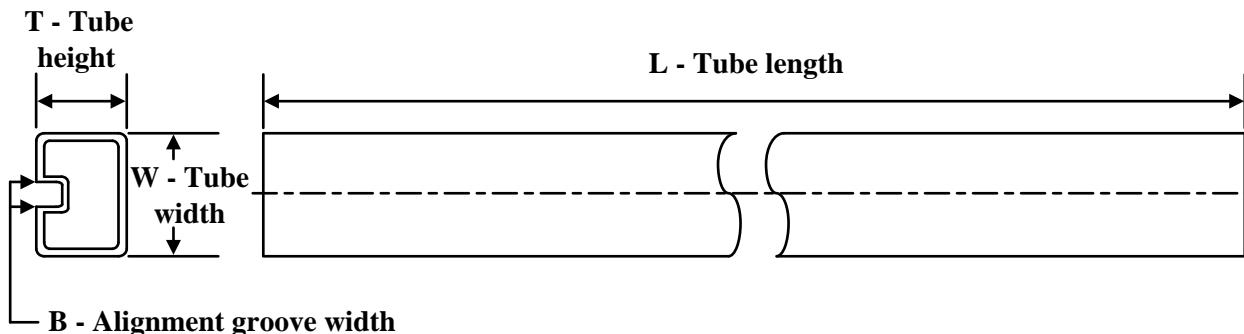
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS00DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LS00DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS00NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LS00PSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS00DBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74LS00DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LS00NSR	SO	NS	14	2000	356.0	356.0	35.0
SN74LS00PSR	SO	PS	8	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T ( $\mu$ m)	B (mm)
JM38510/00104BDA	W	CFP	14	25	506.98	26.16	6220	NA
JM38510/07001BDA	W	CFP	14	25	506.98	26.16	6220	NA
JM38510/30001BDA	W	CFP	14	25	506.98	26.16	6220	NA
JM38510/30001SDA	W	CFP	14	25	506.98	26.16	6220	NA
M38510/00104BDA	W	CFP	14	25	506.98	26.16	6220	NA
M38510/07001BDA	W	CFP	14	25	506.98	26.16	6220	NA
M38510/30001BDA	W	CFP	14	25	506.98	26.16	6220	NA
M38510/30001SDA	W	CFP	14	25	506.98	26.16	6220	NA
SN7400D	D	SOIC	14	50	506.6	8	3940	4.32
SN7400DG4	D	SOIC	14	50	506.6	8	3940	4.32
SN7400N	N	PDIP	14	25	506	13.97	11230	4.32
SN7400N	N	PDIP	14	25	506	13.97	11230	4.32
SN7400NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN7400NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS00N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS00N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS00NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS00NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74S00D	D	SOIC	14	50	506.6	8	3940	4.32
SN74S00N	N	PDIP	14	25	506	13.97	11230	4.32
SN74S00N	N	PDIP	14	25	506	13.97	11230	4.32
SNJ5400W	W	CFP	14	25	506.98	26.16	6220	NA
SNJ54LS00FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS00W	W	CFP	14	25	506.98	26.16	6220	NA
SNJ54S00FK	FK	LCCC	20	55	506.98	12.06	2030	NA

# GENERIC PACKAGE VIEW

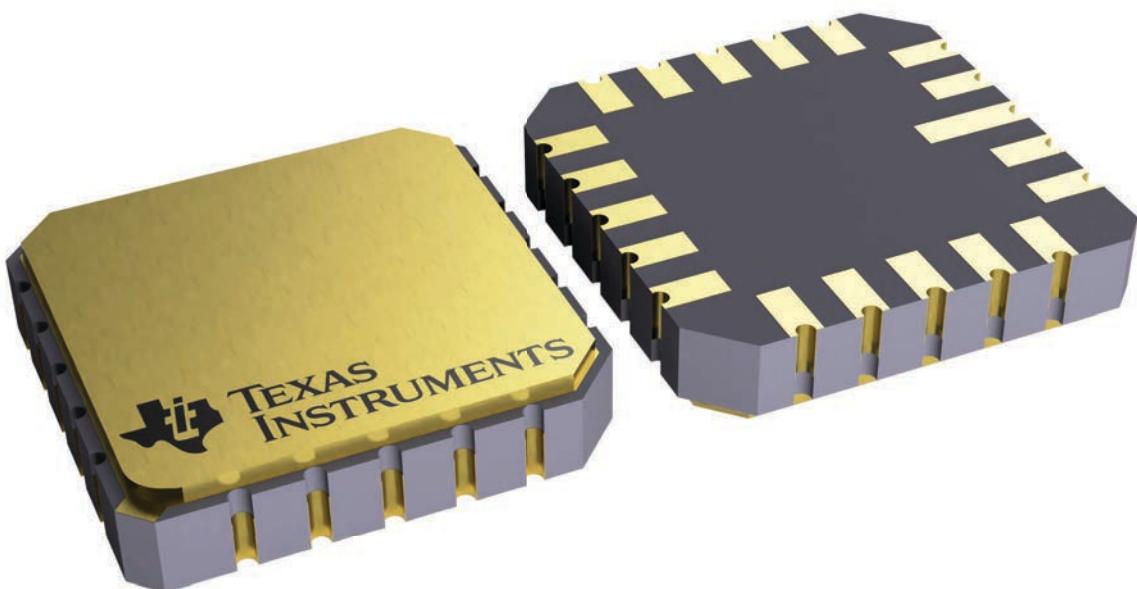
**FK 20**

**LCCC - 2.03 mm max height**

**8.89 x 8.89, 1.27 mm pitch**

**LEADLESS CERAMIC CHIP CARRIER**

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



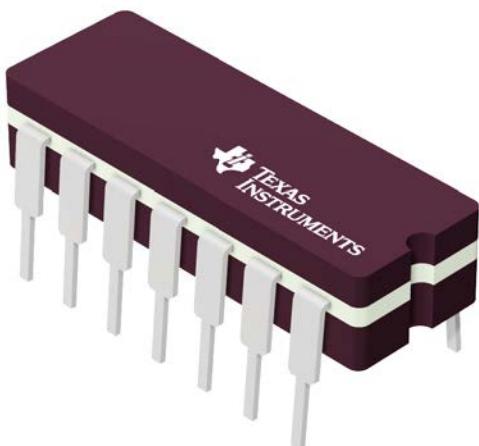
4229370VA\

# GENERIC PACKAGE VIEW

J 14

**CDIP - 5.08 mm max height**

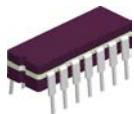
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

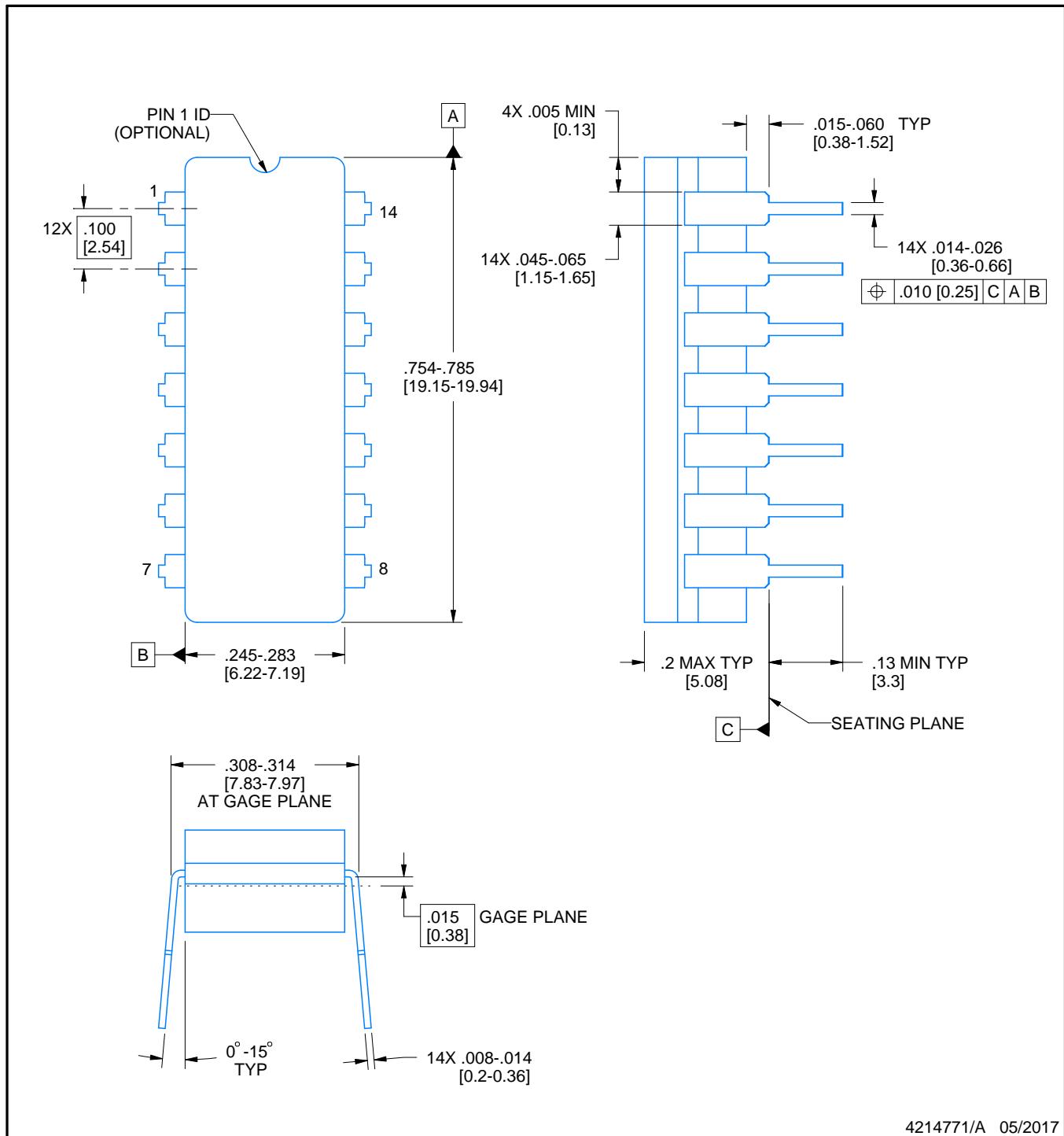
J0014A



# PACKAGE OUTLINE

## CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

### NOTES:

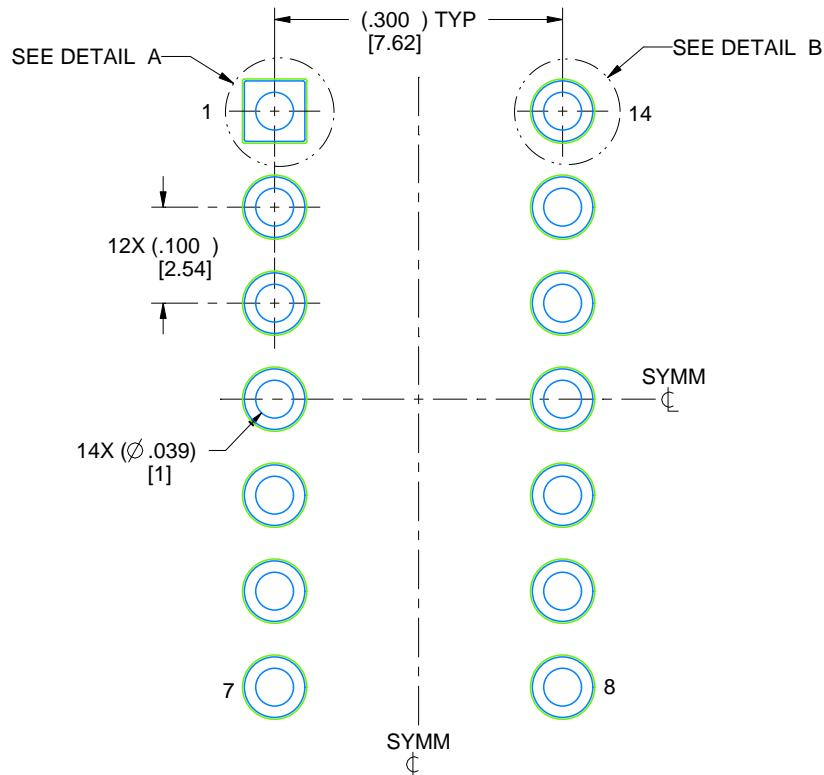
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

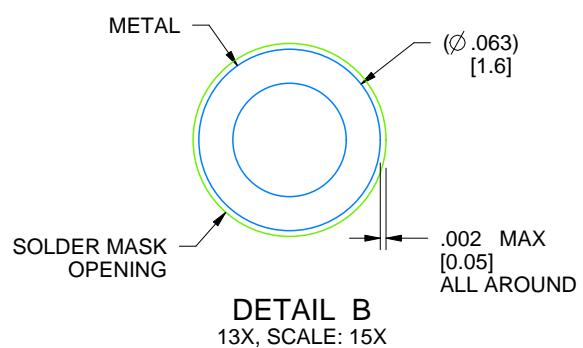
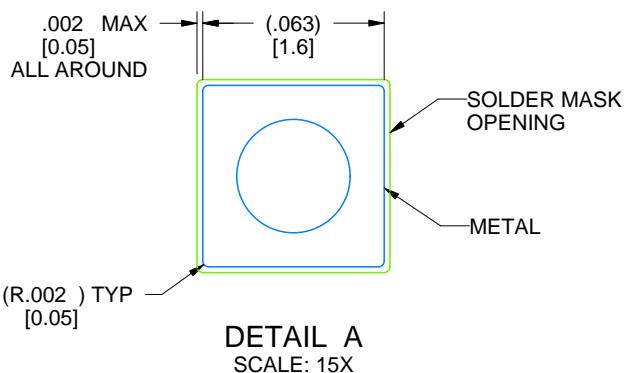
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



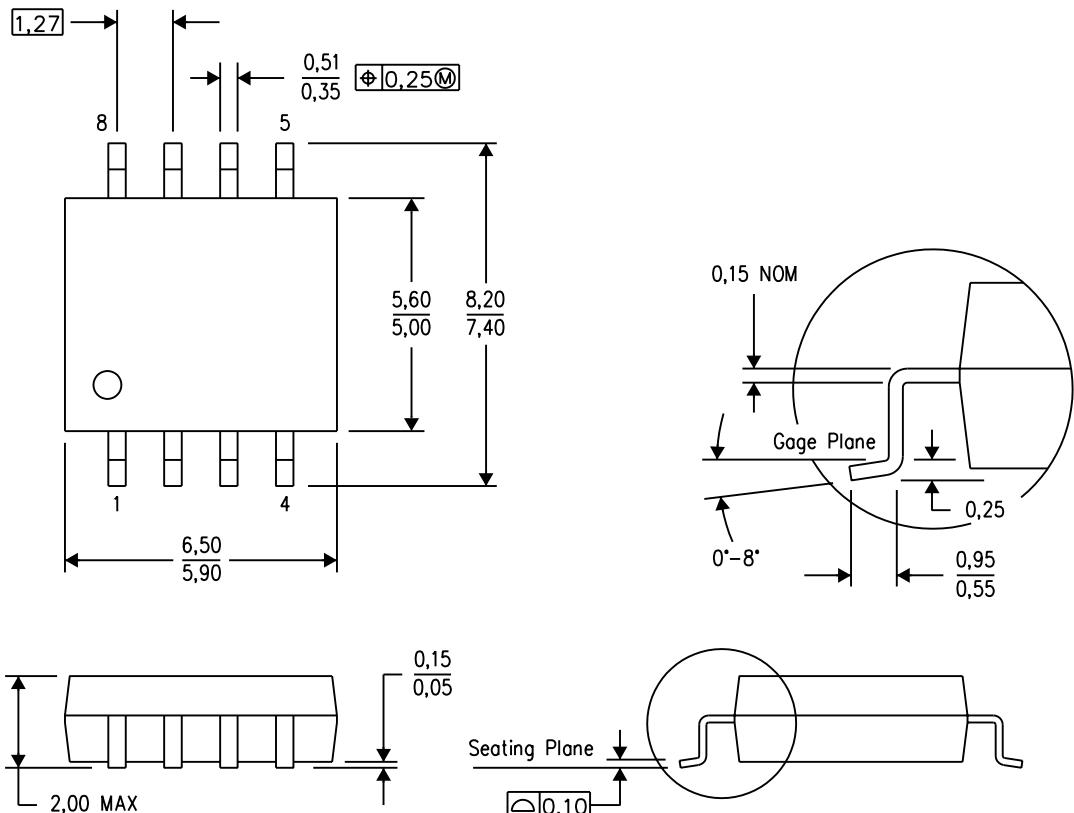
4214771/A 05/2017

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## MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

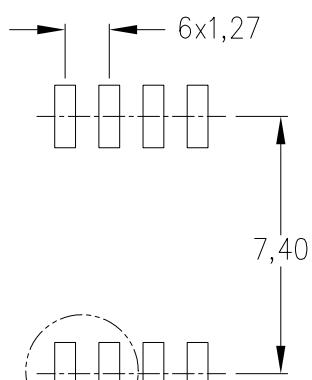
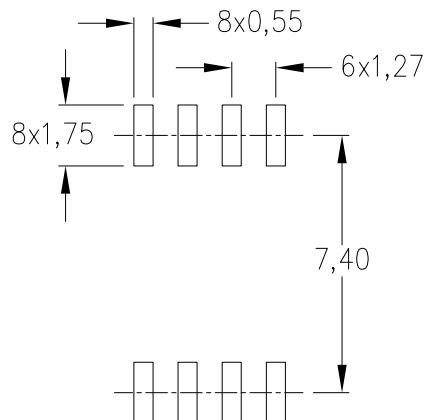
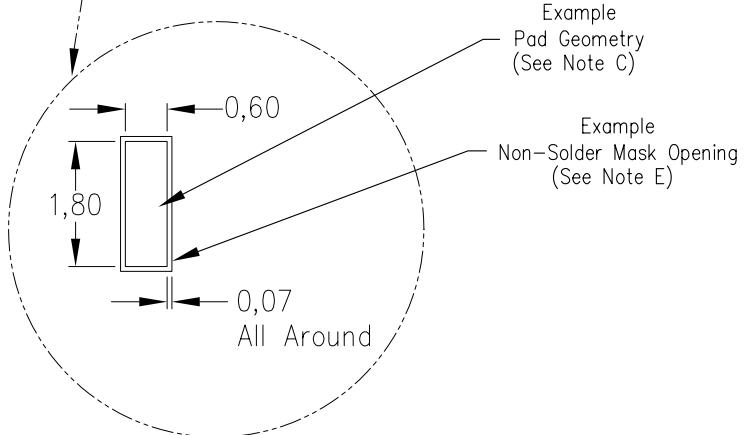


4040063/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C)Stencil Openings  
(Note D)Example  
Non Soldermask Defined PadExample  
Pad Geometry  
(See Note C)Example  
Non-Solder Mask Opening  
(See Note E)

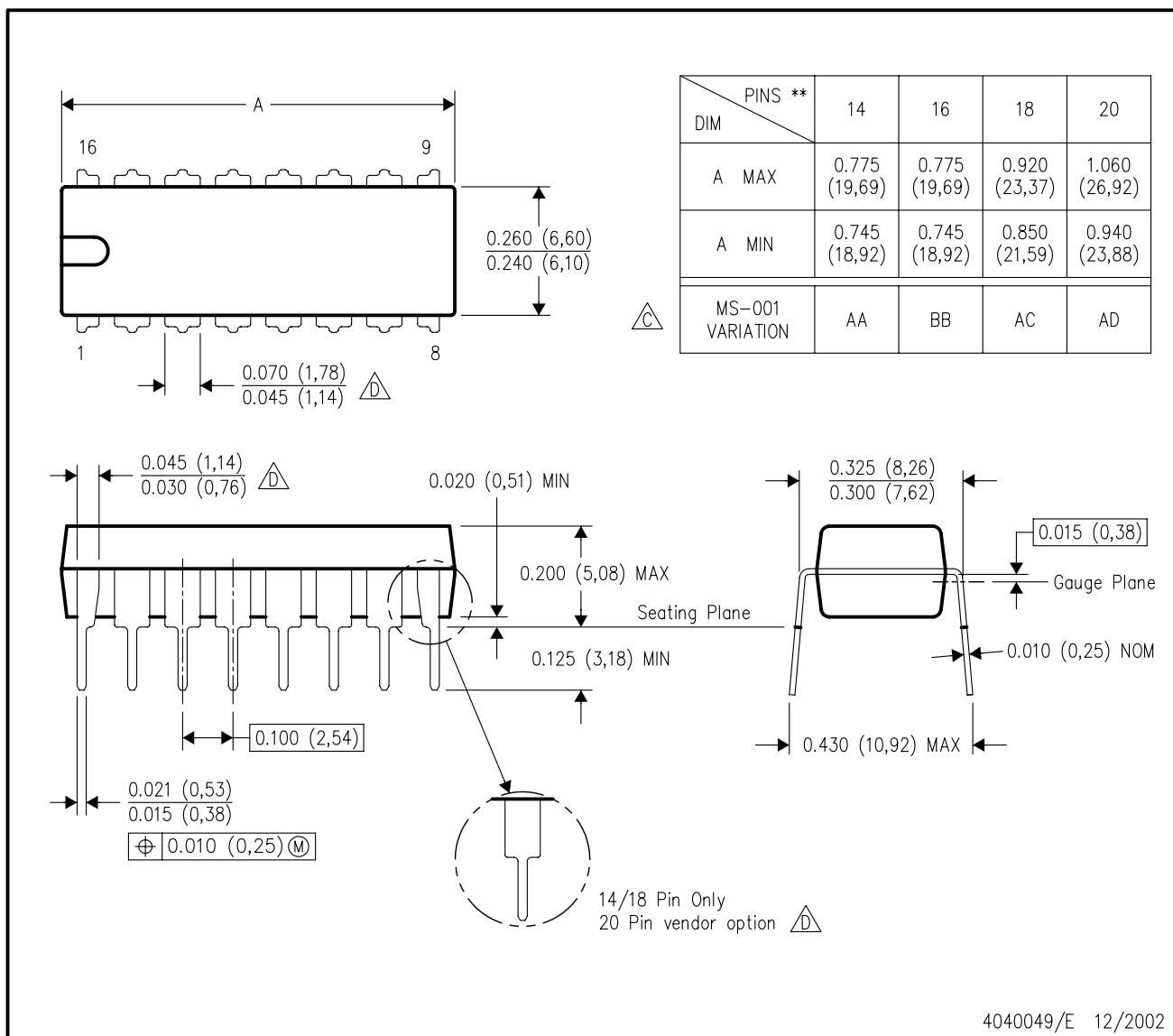
4212188/A 09/11

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.

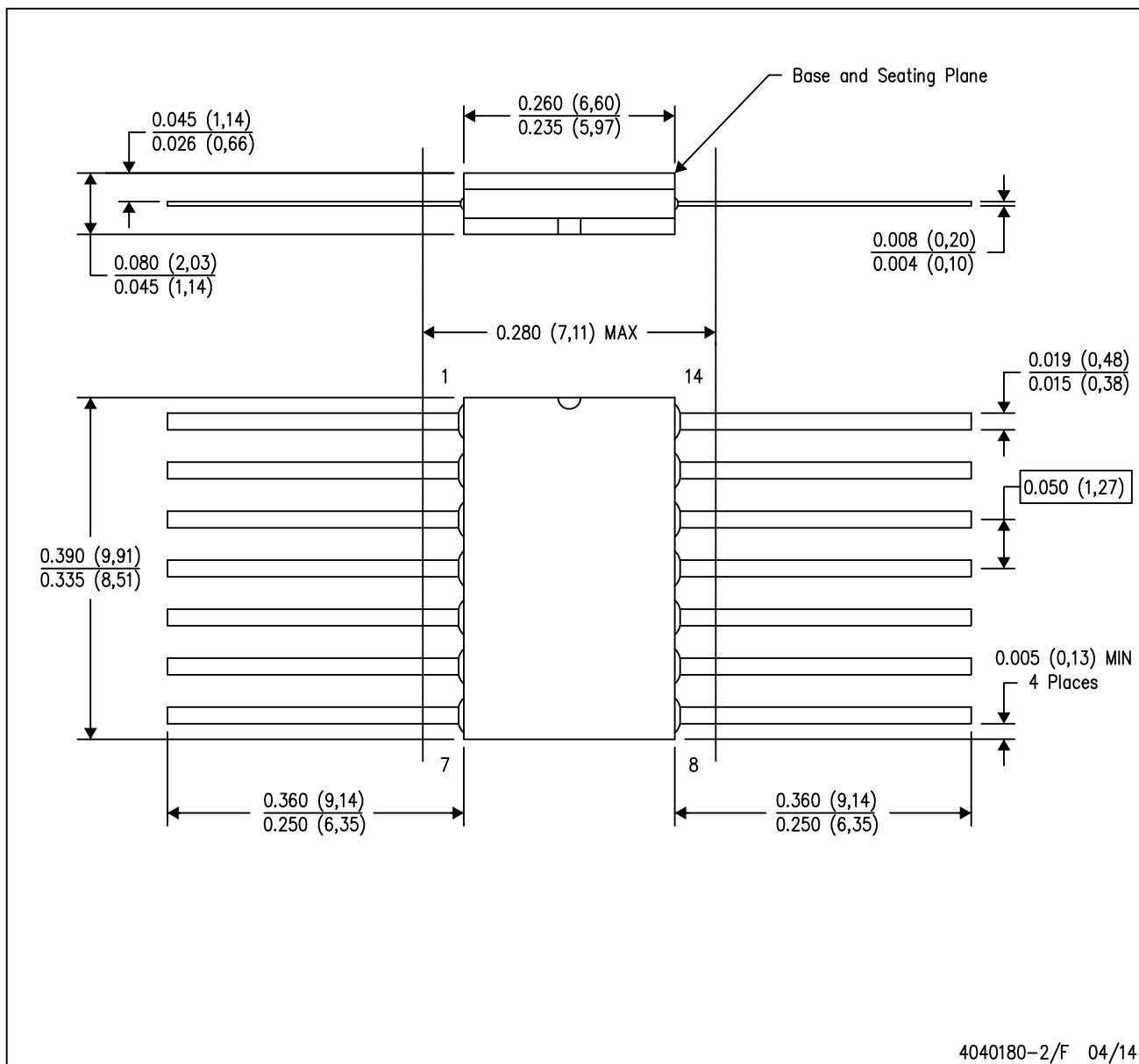
C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

## MECHANICAL DATA

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



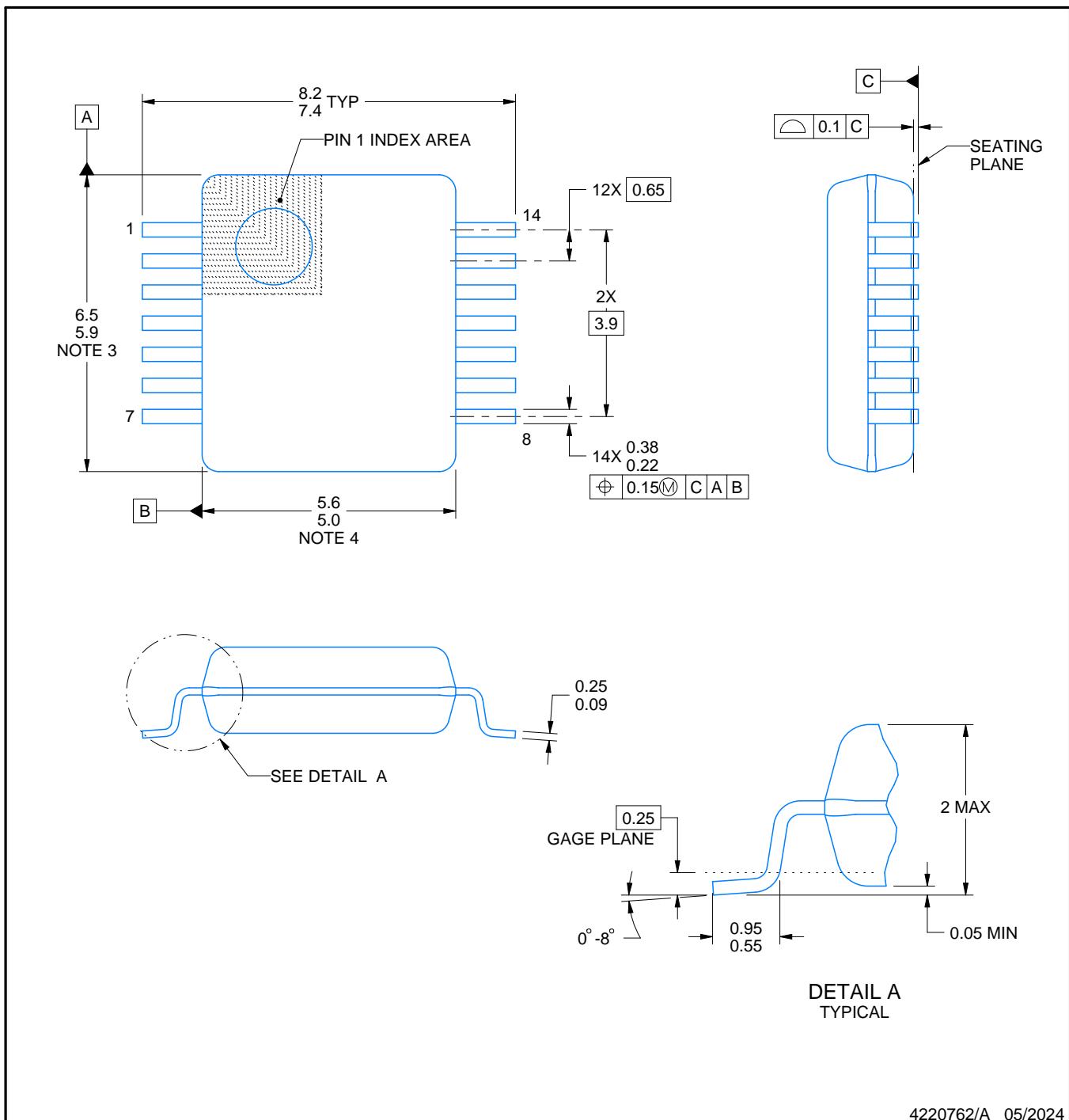
4040180-2/F 04/14

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14

# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



### NOTES:

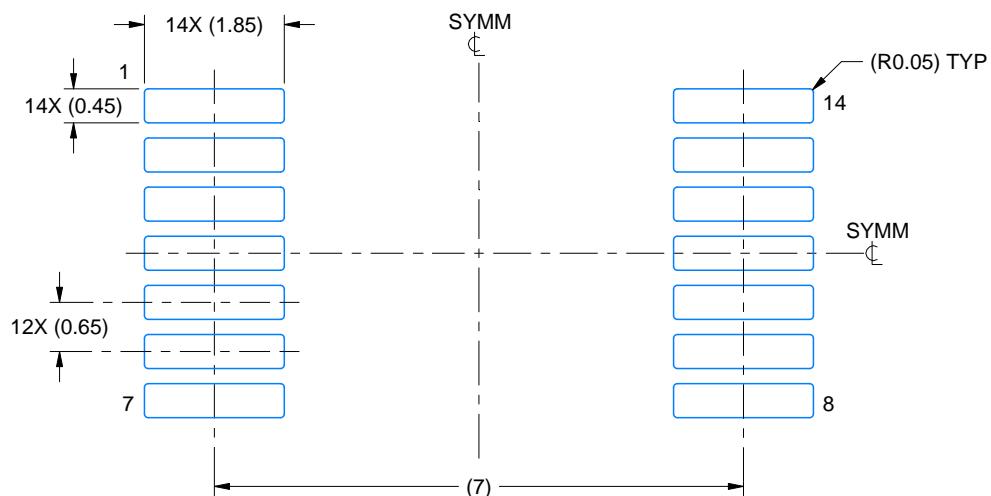
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

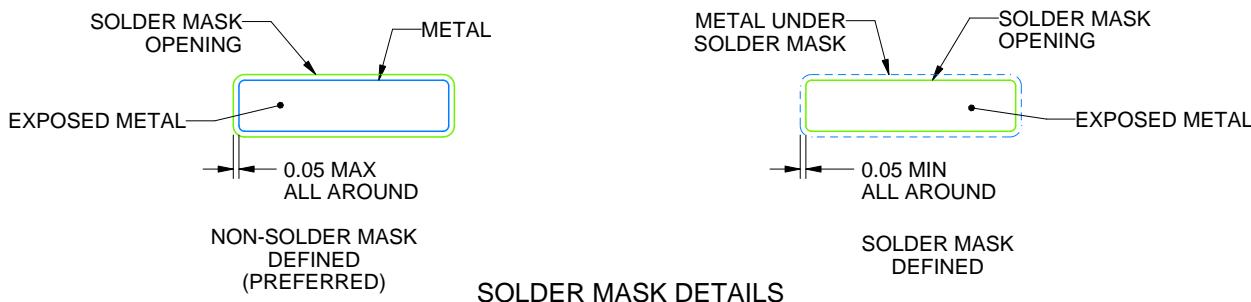
DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

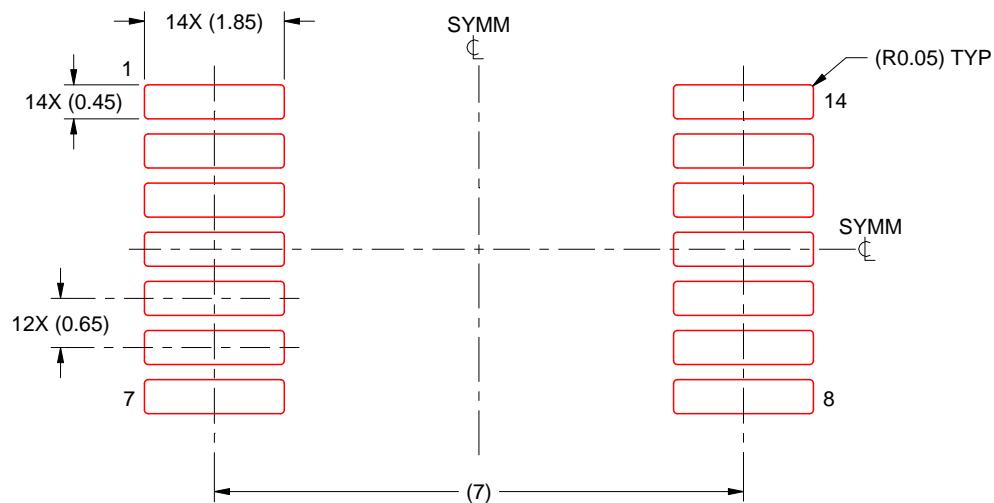
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

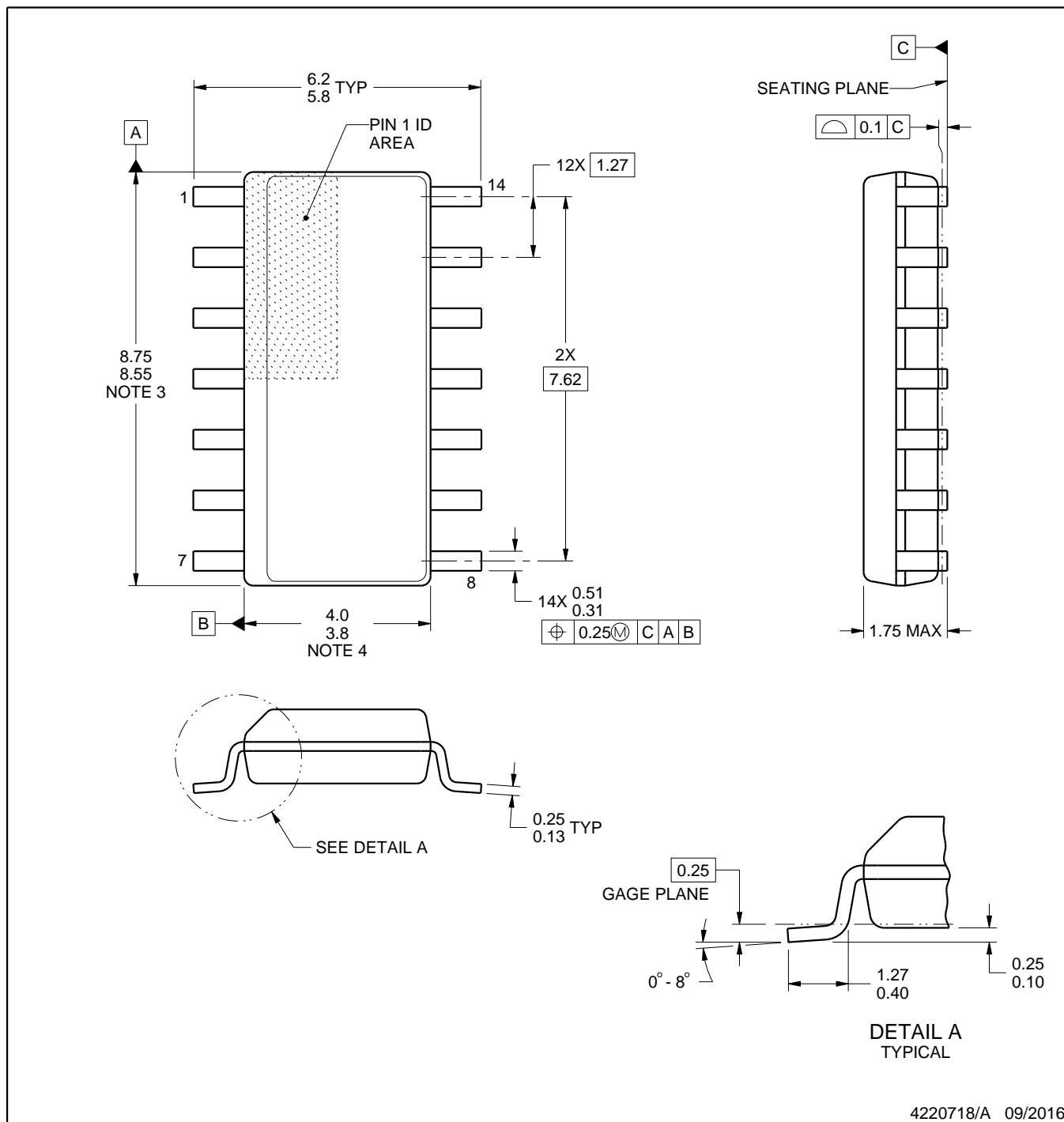
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

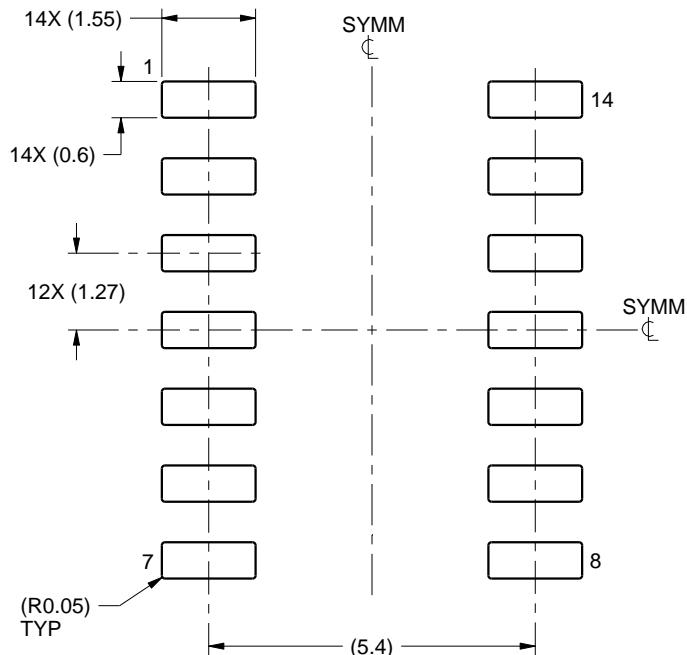
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

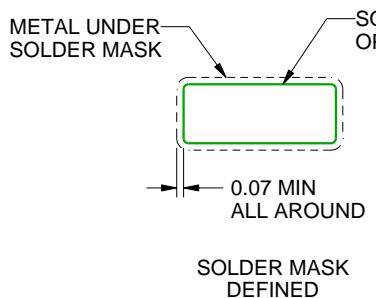
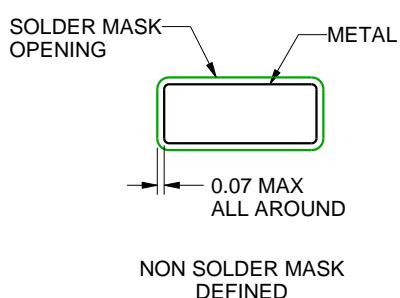
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

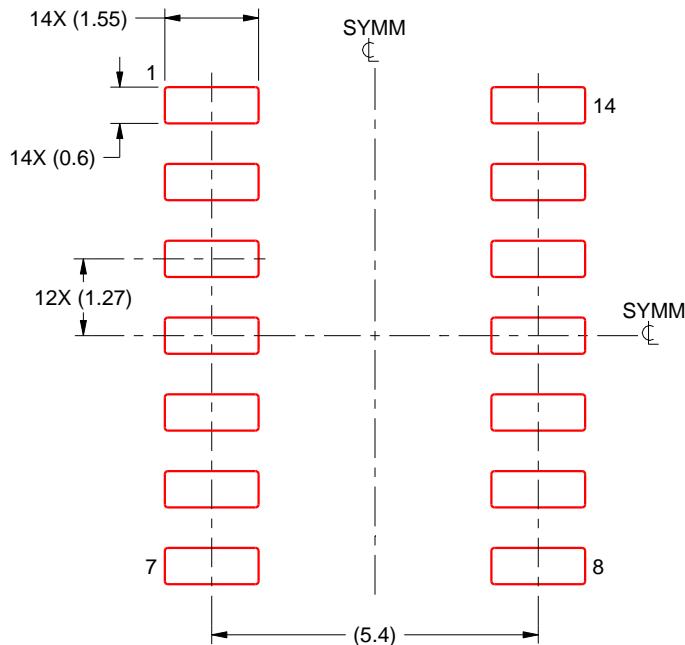
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

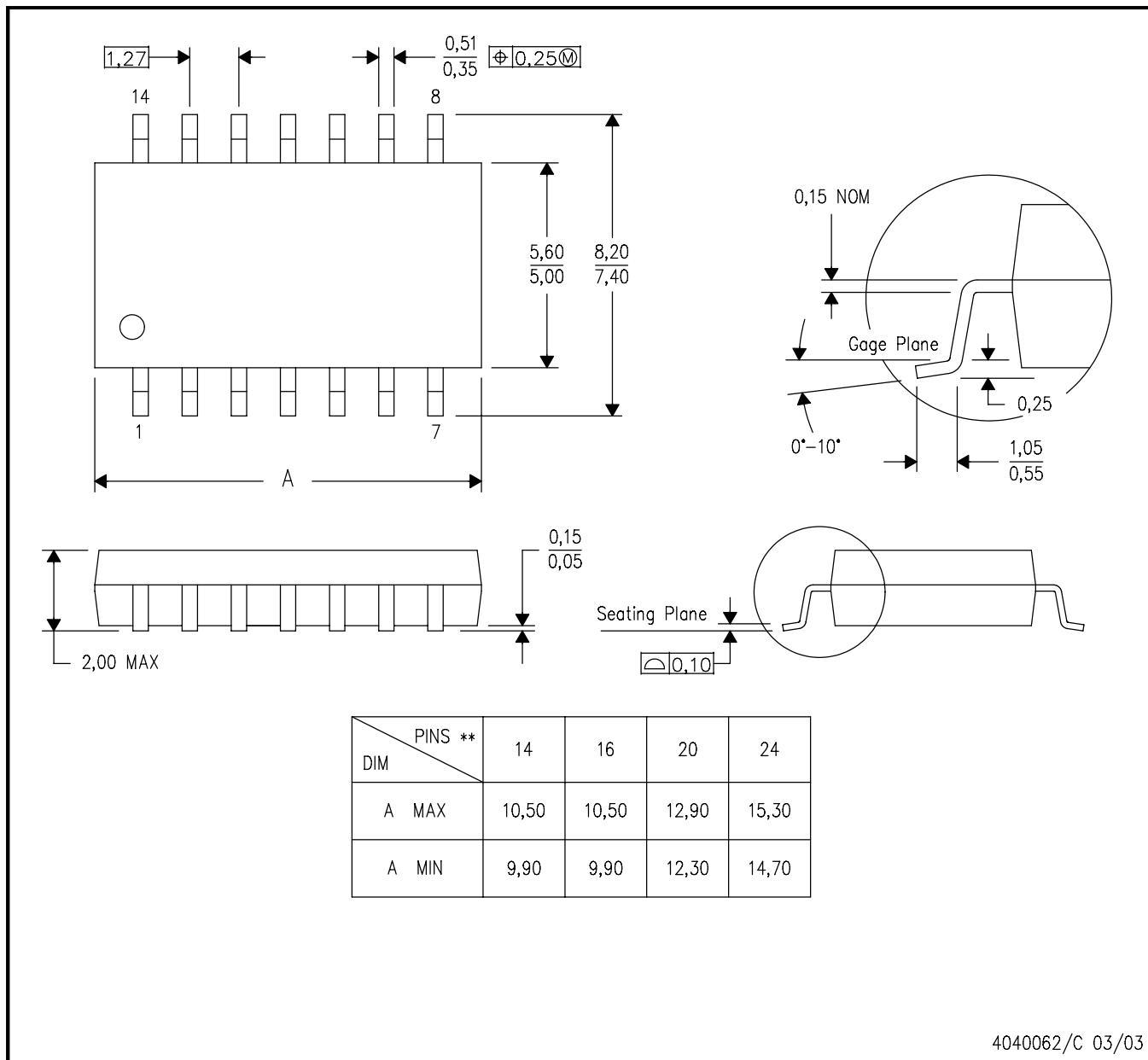
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

**14-PINS SHOWN**

**PLASTIC SMALL-OUTLINE PACKAGE**



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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SN5408, SN54LS08, SN54S08  
 SN7408, SN74LS08, SN74S08  
**QUADRUPLE 2-INPUT POSITIVE-AND GATES**  
 SDLS033 – DECEMBER 1983 – REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

#### description

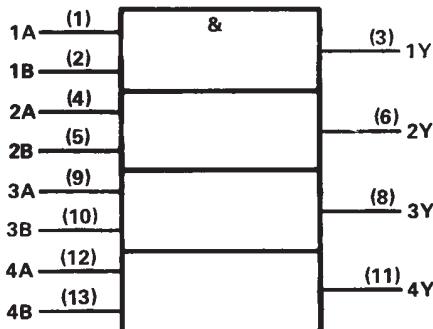
These devices contain four independent 2-input AND gates.

The SN5408, SN54LS08, and SN54S08 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN7408, SN74LS08 and SN74S08 are characterized for operation from  $0^{\circ}$  to  $70^{\circ}\text{C}$ .

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

#### logic symbol†

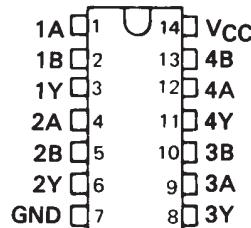


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

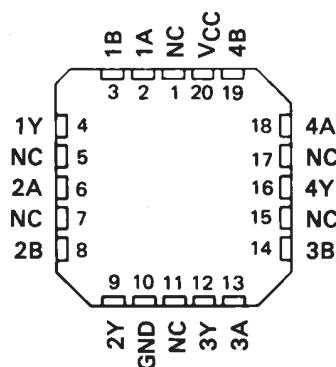
Pin numbers shown are for D, J, N, and W packages.

SN5408, SN54LS08, SN54S08 . . . J OR W PACKAGE  
 SN7408 . . . J OR N PACKAGE  
 SN74LS08, SN74S08 . . . D, J OR N PACKAGE

(TOP VIEW)

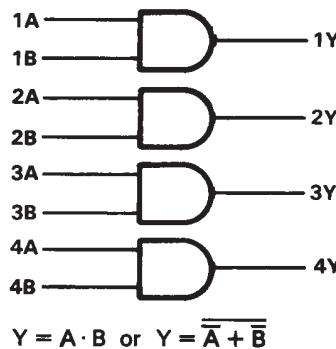


SN54LS08, SN54S08 . . . FK PACKAGE  
 (TOP VIEW)



NC—No internal connection

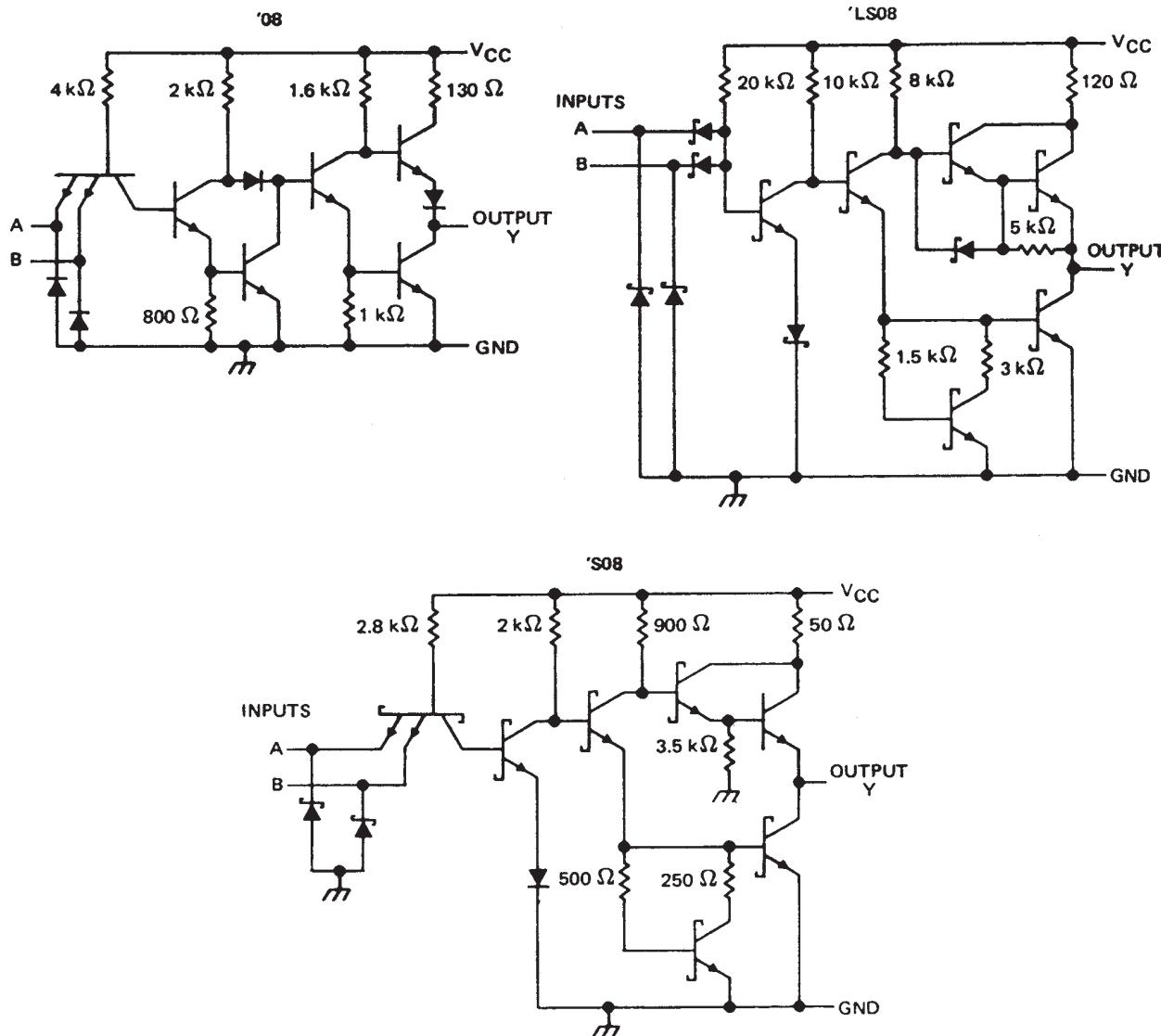
#### logic diagram (positive logic)



**SN5408, SN54LS08, SN54S08  
SN7408, SN74LS08, SN74S08  
QUADRUPLE 2-INPUT POSITIVE-AND GATES**

SDLS033 – DECEMBER 1983 – REVISED MARCH 1988

### schematics (each gate)



Resistor values are nominal.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, V <sub>CC</sub> (see Note 1) . . . . .	7 V
Input voltage: '08, 'S08 . . . . .	5.5 V
'LS08 . . . . .	7 V
Operating free-air temperature range: SN54' . . . . .	-55°C to 125°C
SN74' . . . . .	0°C to 70°C
Storage temperature range . . . . .	-65°C to 150°C

**NOTE 1:** Voltage values are with respect to network ground terminal.



SN5408, SN54LS08, SN54S08  
 SN7408, SN74LS08, SN74S08  
**QUADRUPLE 2-INPUT POSITIVE-AND GATES**  
 SDLS033 – DECEMBER 1983 – REVISED MARCH 1988

**recommended operating conditions**

		SN5408			SN7408			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$I_{OH}$	High-level output current			-0.8			-0.8	mA
$I_{OL}$	Low-level output current			16			16	mA
$T_A$	Operating free-air temperature	-55		125	0		70	$^{\circ}\text{C}$

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS †	SN5408			SN7408			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IK}$	$V_{CC} = \text{MIN}$ , $I_I = -12 \text{ mA}$			-1.5			-1.5	V
$V_{OH}$	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $I_{OH} = -0.8 \text{ mA}$	2.4	3.4		2.4	3.4		V
$V_{OL}$	$V_{CC} = \text{MIN}$ , $V_{IL} = 0.8 \text{ V}$ , $I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
$I_I$	$V_{CC} = \text{MAX}$ , $V_I = 5.5 \text{ V}$			1			1	mA
$I_{IH}$	$V_{CC} = \text{MAX}$ , $V_I = 2.4 \text{ V}$			40			40	$\mu\text{A}$
$I_{IL}$	$V_{CC} = \text{MAX}$ , $V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
$I_{OS\$}$	$V_{CC} = \text{MAX}$	-20		-55	-18		-55	mA
$I_{CCH}$	$V_{CC} = \text{MAX}$ , $V_I = 4.5 \text{ V}$		11	21		11	21	mA
$I_{CCL}$	$V_{CC} = \text{MAX}$ , $V_I = 0 \text{ V}$		20	33		20	33	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

§ Not more than one output should be shorted at a time.

**switching characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$  (see note 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	A or B	Y	$R_L = 400 \Omega$ , $C_L = 15 \text{ pF}$		17.5	27	ns
					12	19	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

**SN5408, SN54LS08, SN54S08**

**SN7408, SN74LS08, SN74S08**

**QUADRUPLE 2-INPUT POSITIVE-AND GATES**

SDLS033 – DECEMBER 1983 – REVISED MARCH 1988

**recommended operating conditions**

	SN54LS08			SN74LS08			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub> Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub> High-level input voltage	2			2			V
V <sub>IL</sub> Low-level input voltage			0.7			0.8	V
I <sub>OH</sub> High-level output current			-0.4			-0.4	mA
I <sub>OL</sub> Low-level output current			4			8	mA
T <sub>A</sub> Operating free-air temperature	-55		125	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS †	SN54LS08			SN74LS08			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA			-1.5			-1.5	V
V <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, I <sub>OH</sub> = -0.4 mA	2.5	3.4		2.7	3.4		V
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, I <sub>OL</sub> = 4 mA		0.25	0.4	0.25	0.4		V
	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, I <sub>OL</sub> = 8 mA				0.35	0.5		
I <sub>I</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V			0.1			0.1	mA
I <sub>IH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V			20			20	µA
I <sub>IL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V			-0.4			-0.4	mA
I <sub>OS\$</sub>	V <sub>CC</sub> = MAX	-20	-100		-20	-100		mA
I <sub>CCH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 4.5 V		2.4	4.8	2.4	4.8		mA
I <sub>CCL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0 V		4.4	8.8	4.4	8.8		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

\$ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	A or B	Y	R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 15 pF	8	15		ns
t <sub>PHL</sub>				10	20		ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN5408, SN54LS08, SN54S08  
 SN7408, SN74LS08, SN74S08  
**QUADRUPLE 2-INPUT POSITIVE-AND GATES**  
 SDLS033 – DECEMBER 1983 – REVISED MARCH 1988

**recommended operating conditions**

		SN54S08			SN74S08			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage			0.8			0.8	V
I <sub>OH</sub>	High-level output current			-1			-1	mA
I <sub>OL</sub>	Low-level output current			20			20	mA
T <sub>A</sub>	Operating free-air temperature	-55		125	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS †	SN54S08			SN74S08			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA			-1.2			-1.2	V
V <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, I <sub>OH</sub> = -1 mA	2.5	3.4		2.7	3.4		V
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8 V I <sub>OL</sub> = 20 mA			0.5			0.5	V
I <sub>I</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V			1			1	mA
I <sub>IH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V			50			50	µA
I <sub>IL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5 V			-2			-2	mA
I <sub>OS\$</sub>	V <sub>CC</sub> = MAX	-40		-100	-40		-100	mA
I <sub>CCH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 4.5 V		18	32	18	32		mA
I <sub>CCL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0 V		32	57	32	57		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

\$ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	A or B	Y	R <sub>L</sub> = 280 Ω, C <sub>L</sub> = 15 pF	4.5	7		ns
t <sub>PHL</sub>				5	7.5		ns
t <sub>PLH</sub>			R <sub>L</sub> = 280 Ω, C <sub>L</sub> = 50 pF	6			ns
t <sub>PHL</sub>				7.5			ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
JM38510/08003BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/08003BCA	Samples
JM38510/08003BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/08003BDA	Samples
JM38510/08003BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/08003BDA	Samples
JM38510/31004B2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/31004B2A	Samples
JM38510/31004B2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/31004B2A	Samples
JM38510/31004BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/31004BCA	Samples
JM38510/31004BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/31004BCA	Samples
JM38510/31004BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/31004BDA	Samples
JM38510/31004BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/31004BDA	Samples
JM38510/31004SCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/31004SCA	Samples
JM38510/31004SCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/31004SCA	Samples
JM38510/31004SDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/31004SDA	Samples
JM38510/31004SDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/31004SDA	Samples
M38510/08003BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/08003BCA	Samples
M38510/08003BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/08003BCA	Samples
M38510/08003BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/08003BDA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
M38510/08003BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/08003BDA	Samples
M38510/31004B2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/31004B2A	Samples
M38510/31004B2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/31004B2A	Samples
M38510/31004BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/31004BCA	Samples
M38510/31004BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/31004BCA	Samples
M38510/31004BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/31004BDA	Samples
M38510/31004BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/31004BDA	Samples
M38510/31004SCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/31004SCA	Samples
M38510/31004SCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/31004SCA	Samples
M38510/31004SDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/31004SDA	Samples
M38510/31004SDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/31004SDA	Samples
SN54LS08J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS08J	Samples
SN54LS08J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS08J	Samples
SN54S08J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54S08J	Samples
SN54S08J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54S08J	Samples
SN74LS08D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS08	Samples
SN74LS08D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS08	Samples
SN74LS08DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS08	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS08DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS08	Samples
SN74LS08DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS08	Samples
SN74LS08DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS08	Samples
SN74LS08DRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS08	Samples
SN74LS08DRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS08	Samples
SN74LS08N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS08N	Samples
SN74LS08N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS08N	Samples
SN74LS08NE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS08N	Samples
SN74LS08NE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS08N	Samples
SN74LS08NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS08	Samples
SN74LS08NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS08	Samples
SN74S08D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	S08	Samples
SN74S08D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	S08	Samples
SN74S08N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74S08N	Samples
SN74S08N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74S08N	Samples
SNJ54LS08FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS08FK	Samples
SNJ54LS08FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS08FK	Samples
SNJ54LS08J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS08J	Samples
SNJ54LS08J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS08J	Samples
SNJ54LS08W	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS08W	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54LS08W	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS08W	Samples
SNJ54S08FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54S 08FK	Samples
SNJ54S08FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54S 08FK	Samples
SNJ54S08J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54S08J	Samples
SNJ54S08J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54S08J	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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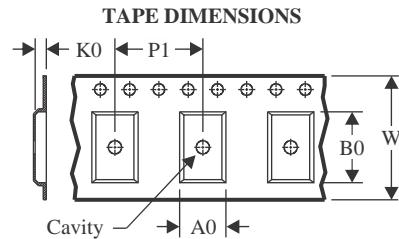
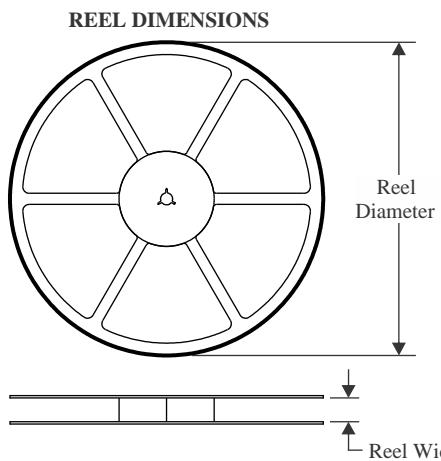
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LS08, SN54LS08-SP, SN54S08, SN74LS08, SN74S08 :**

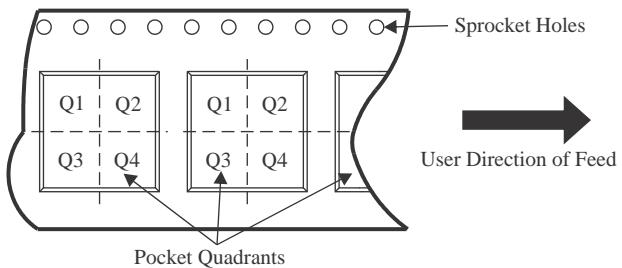
- Catalog : [SN74LS08](#), [SN54LS08](#), [SN74S08](#)
- Military : [SN54LS08](#), [SN54S08](#)
- Space : [SN54LS08-SP](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

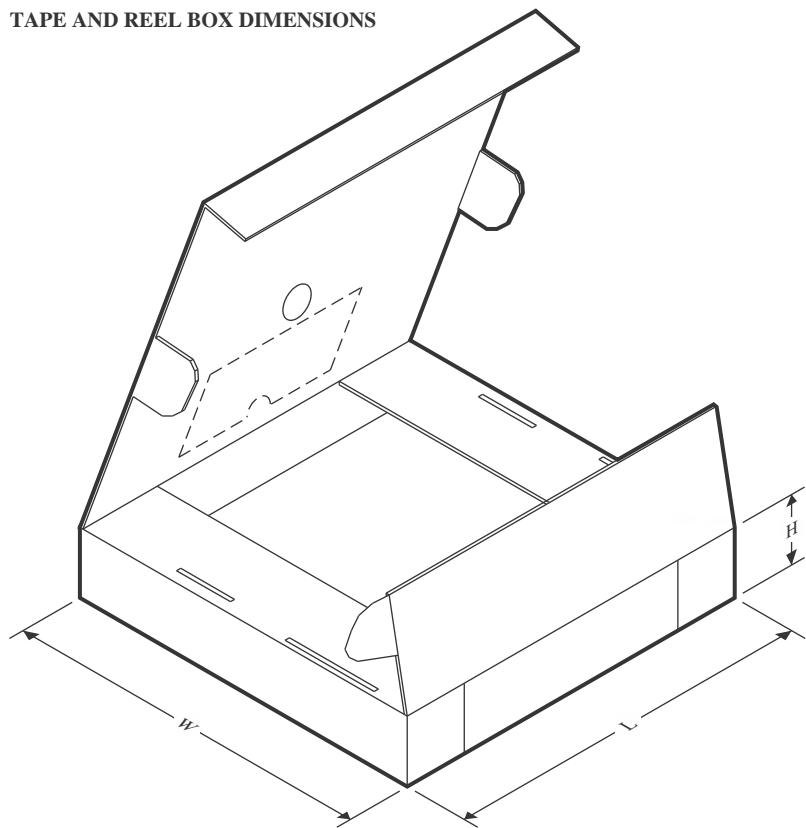
**TAPE AND REEL INFORMATION**

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

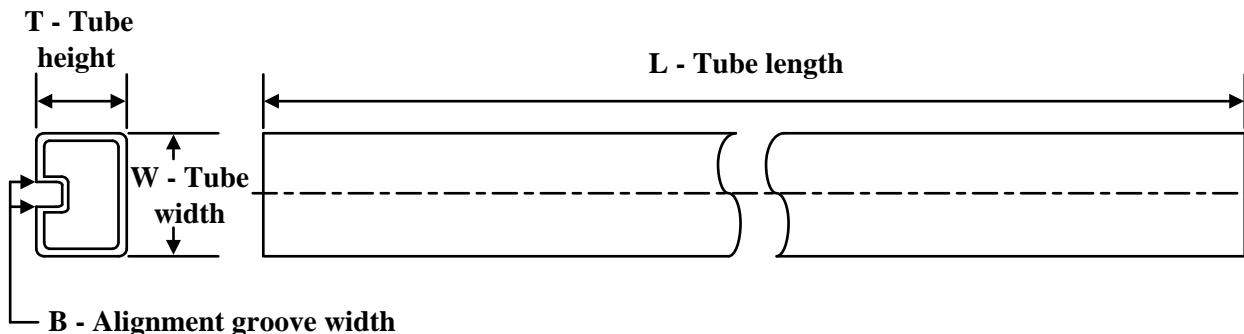
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS08DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LS08DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS08NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS08DBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74LS08DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LS08NSR	SO	NS	14	2000	367.0	367.0	38.0

**TUBE**


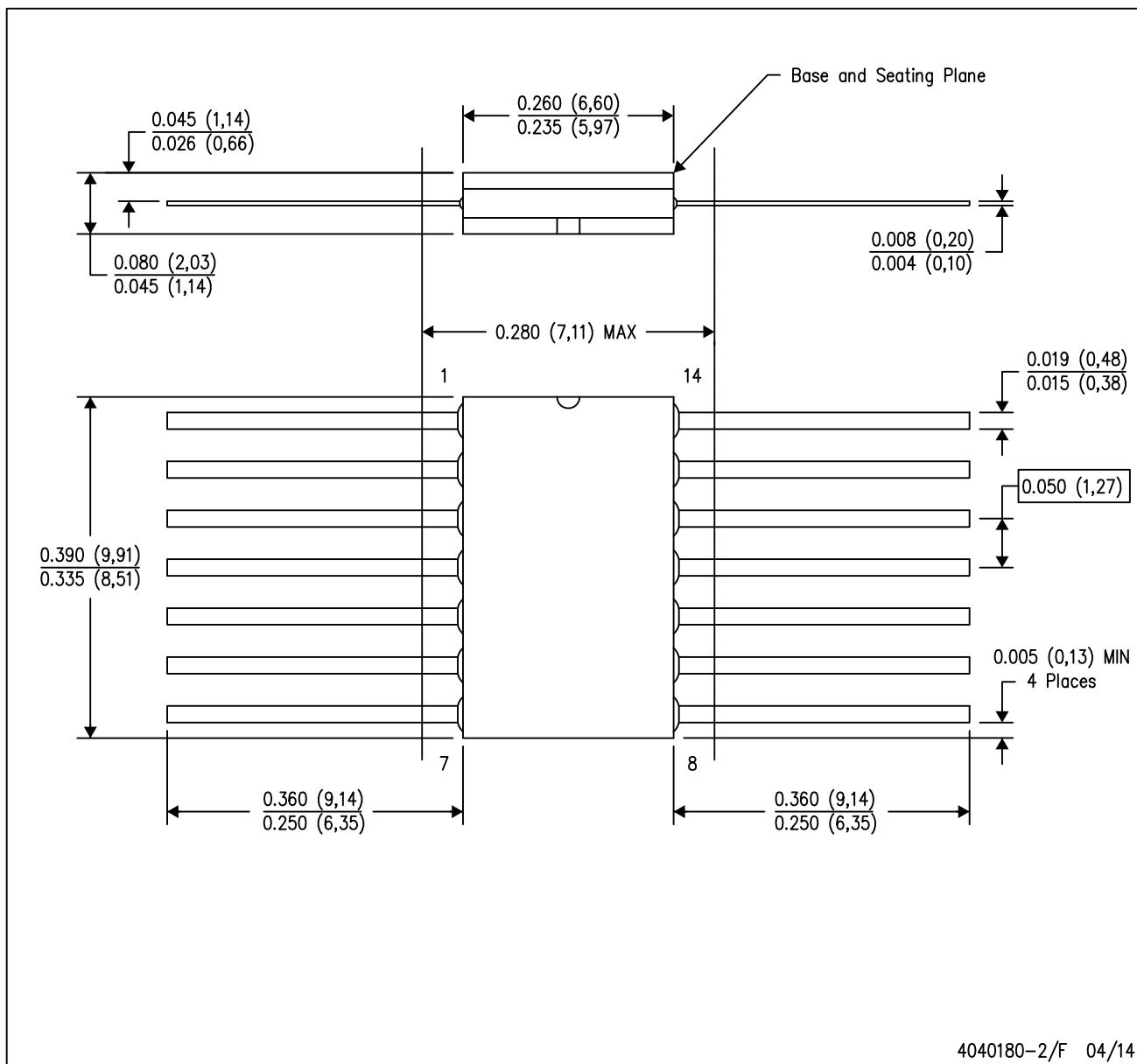
\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T ( $\mu$ m)	B (mm)
JM38510/08003BDA	W	CFP	14	25	506.98	26.16	6220	NA
JM38510/31004B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/31004BDA	W	CFP	14	25	506.98	26.16	6220	NA
JM38510/31004SDA	W	CFP	14	25	506.98	26.16	6220	NA
M38510/08003BDA	W	CFP	14	25	506.98	26.16	6220	NA
M38510/31004B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/31004BDA	W	CFP	14	25	506.98	26.16	6220	NA
M38510/31004SDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74LS08D	D	SOIC	14	50	506.6	8	3940	4.32
SN74LS08N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS08N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS08NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS08NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74S08D	D	SOIC	14	50	506.6	8	3940	4.32
SN74S08N	N	PDIP	14	25	506	13.97	11230	4.32
SN74S08N	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54LS08FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS08W	W	CFP	14	25	506.98	26.16	6220	NA
SNJ54S08FK	FK	LCCC	20	55	506.98	12.06	2030	NA

## MECHANICAL DATA

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK

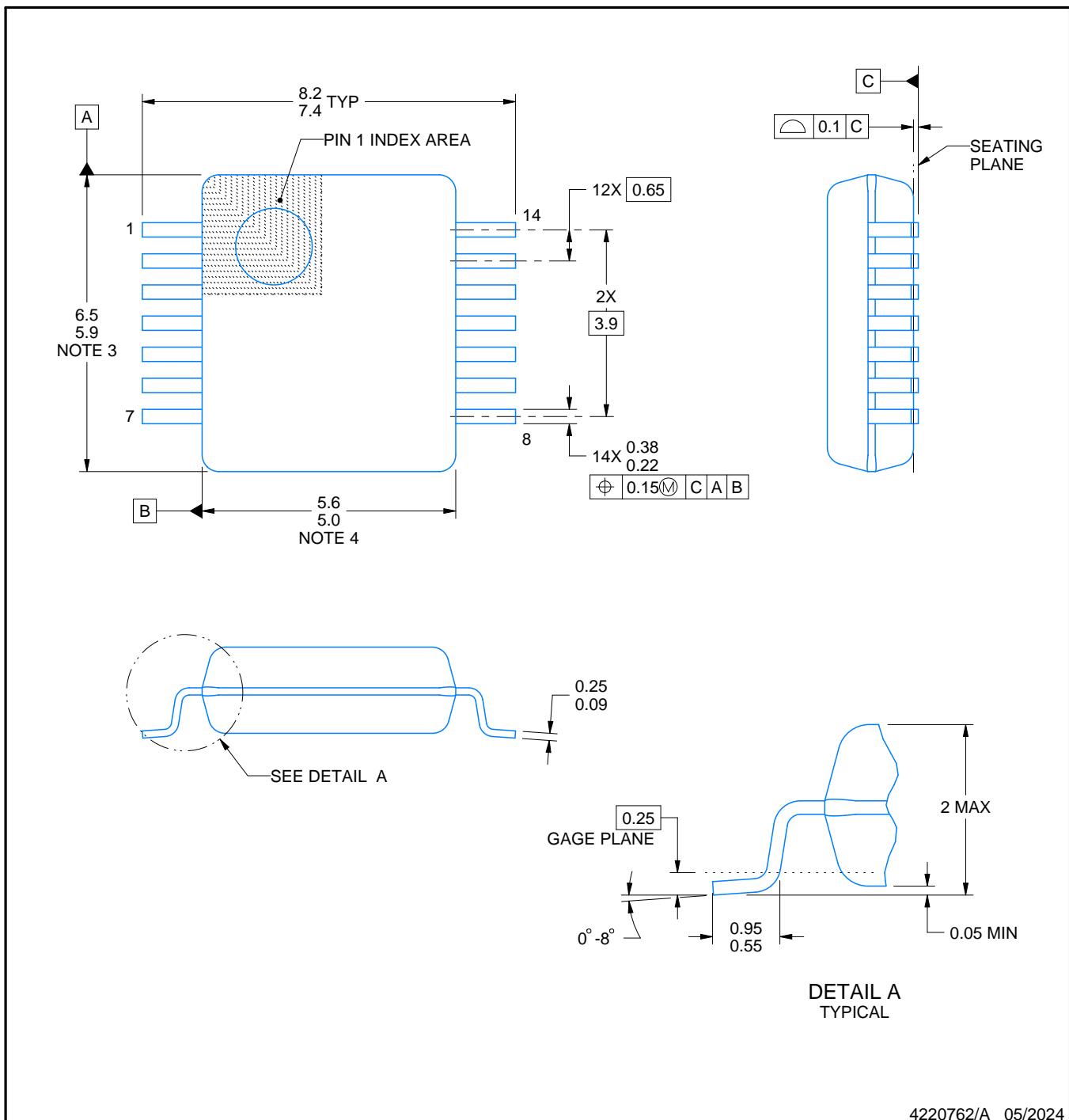


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14

# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



### NOTES:

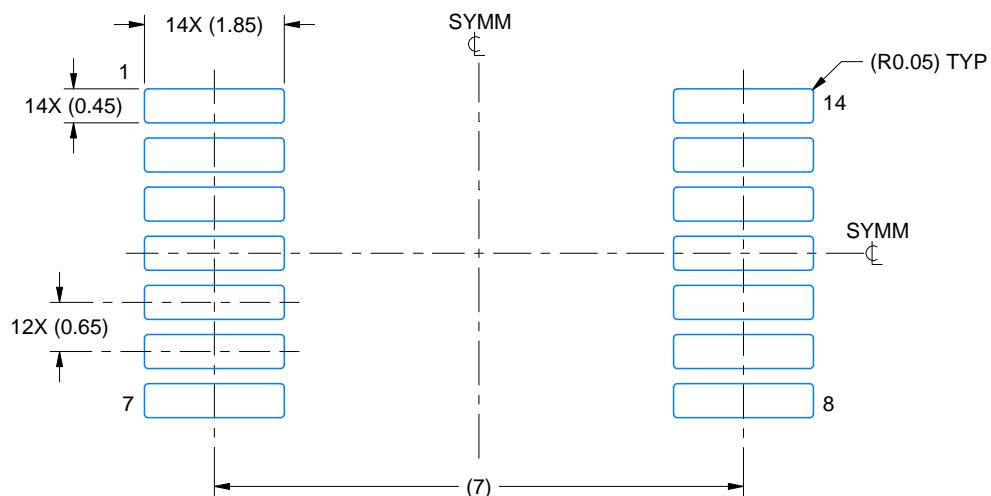
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

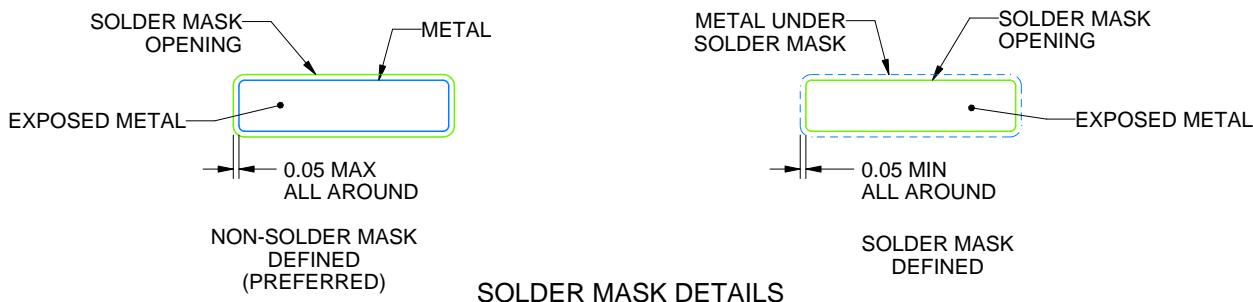
DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220762/A 05/2024

NOTES: (continued)

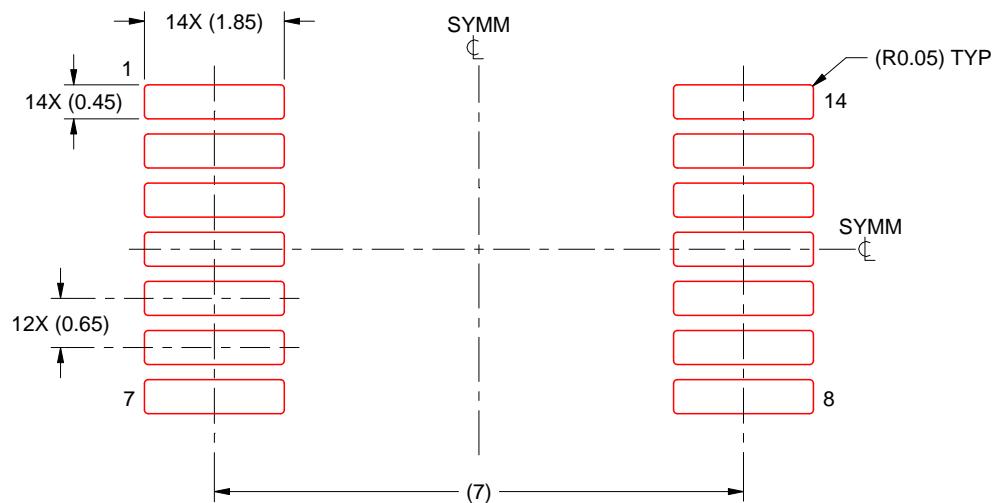
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

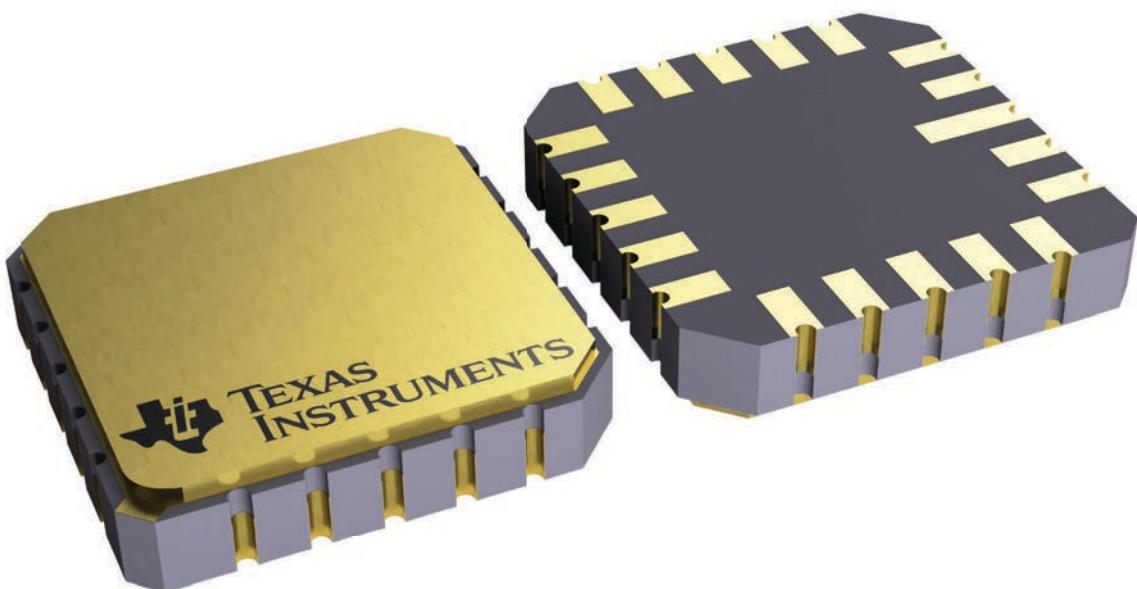
**FK 20**

**LCCC - 2.03 mm max height**

**8.89 x 8.89, 1.27 mm pitch**

**LEADLESS CERAMIC CHIP CARRIER**

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



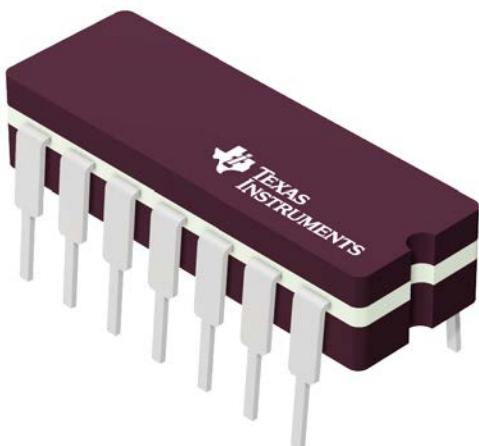
4229370VA\

# GENERIC PACKAGE VIEW

J 14

**CDIP - 5.08 mm max height**

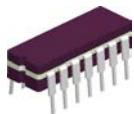
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

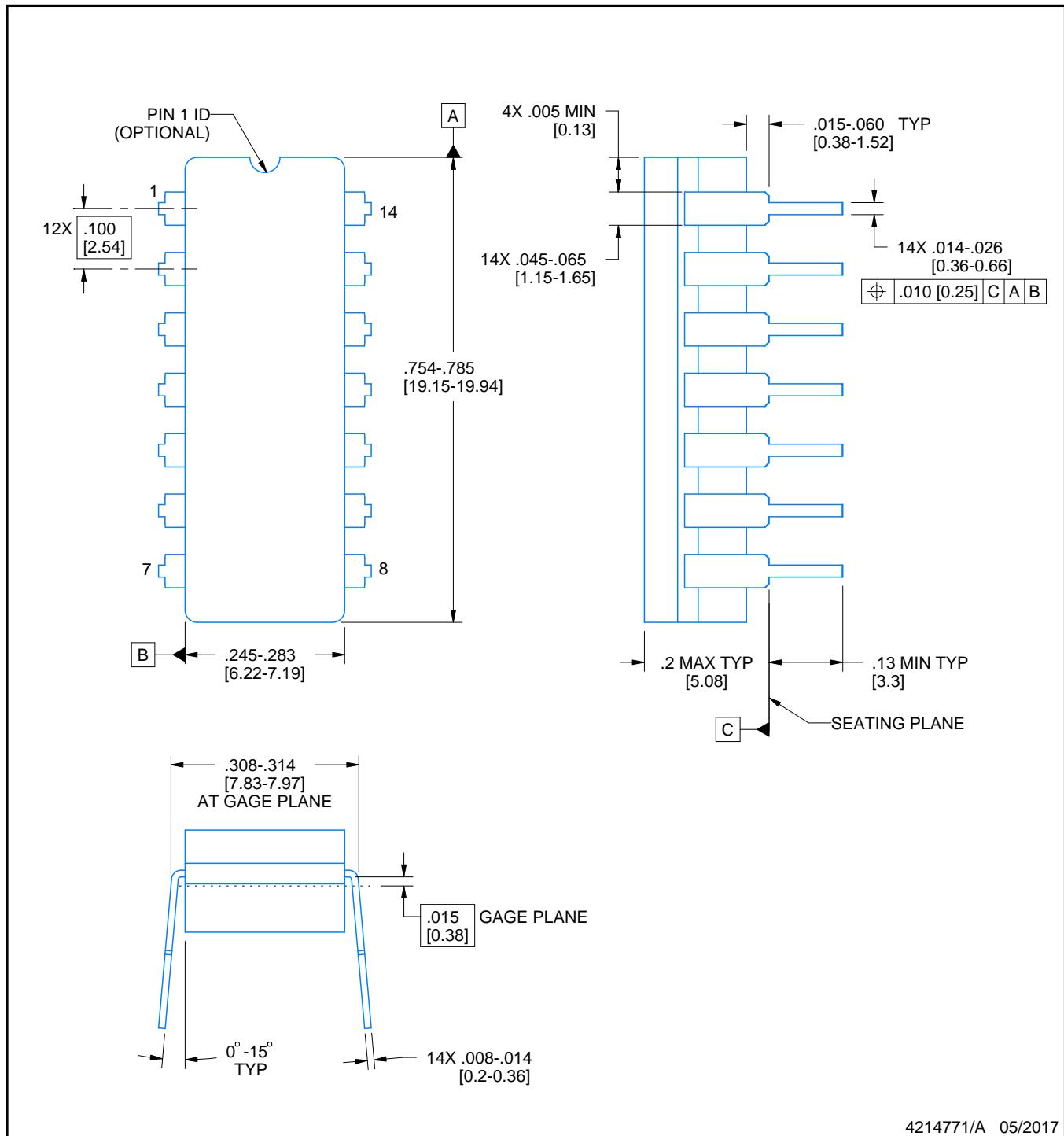
J0014A



# PACKAGE OUTLINE

## CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

### NOTES:

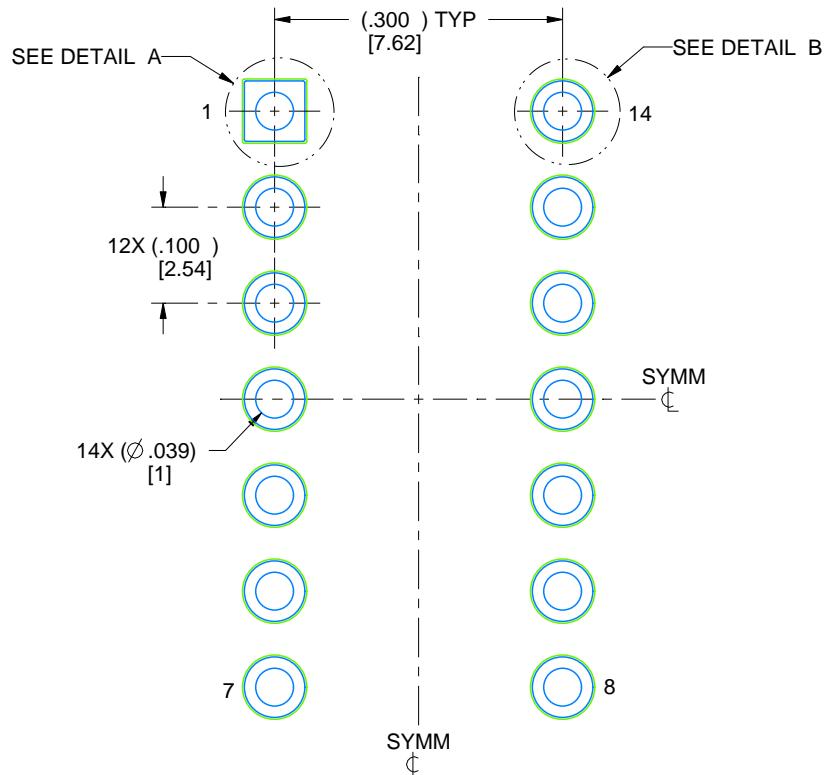
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

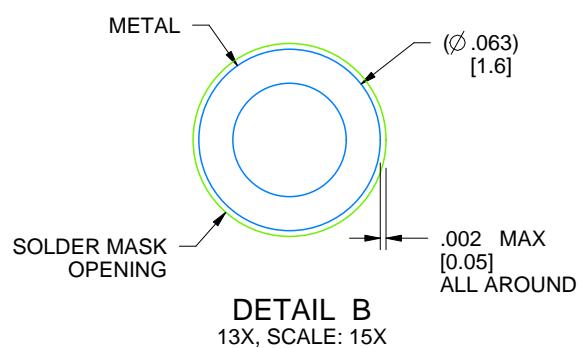
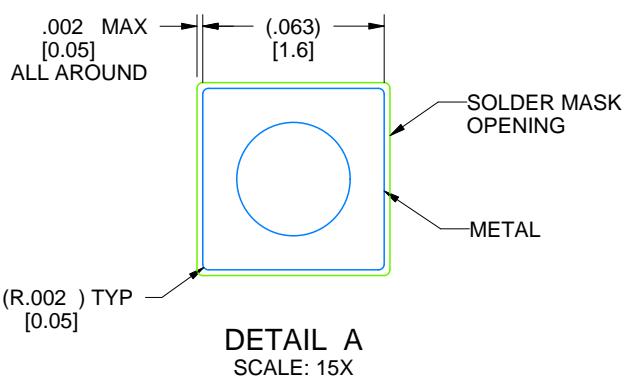
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X

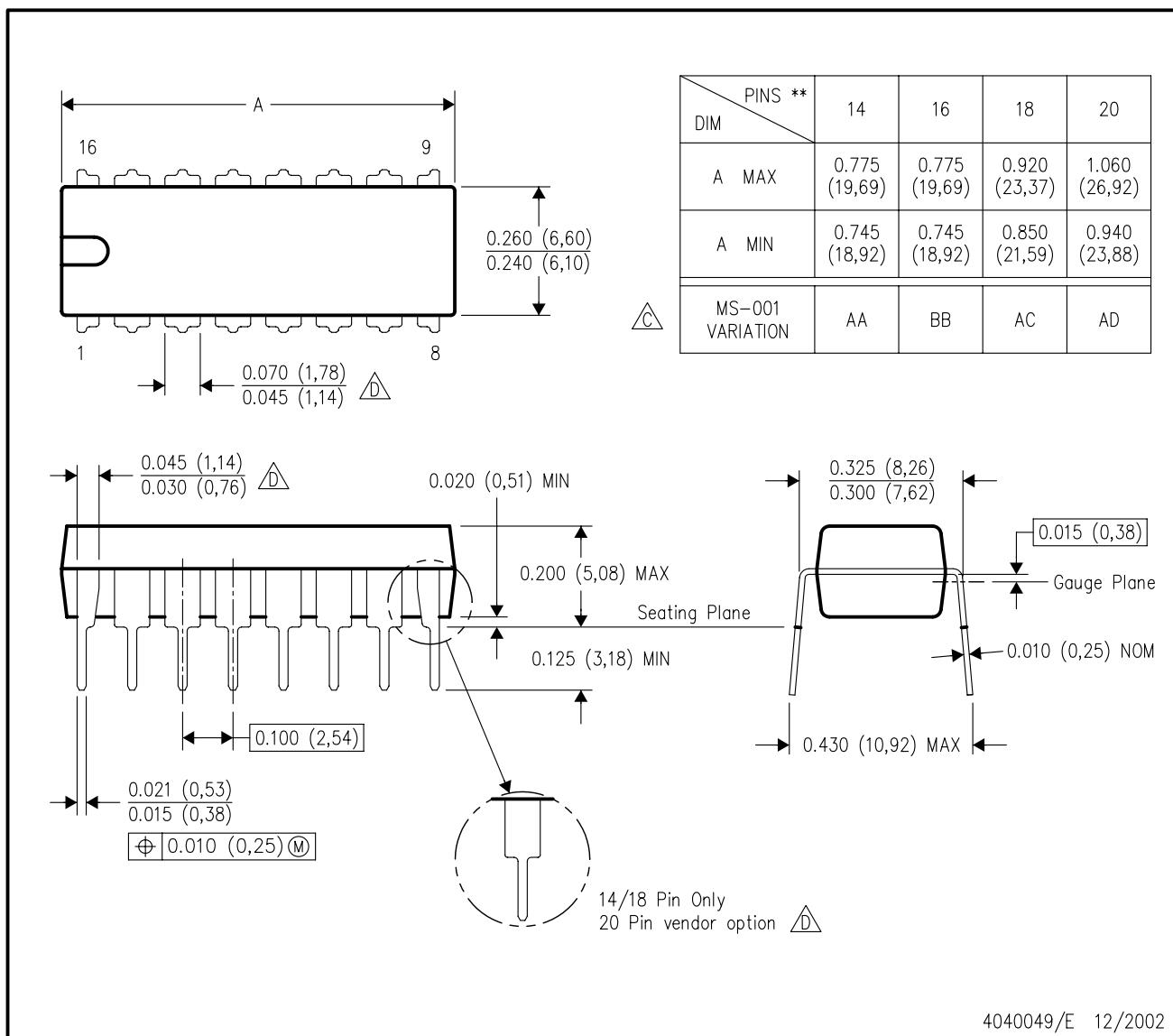


4214771/A 05/2017

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.

△C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

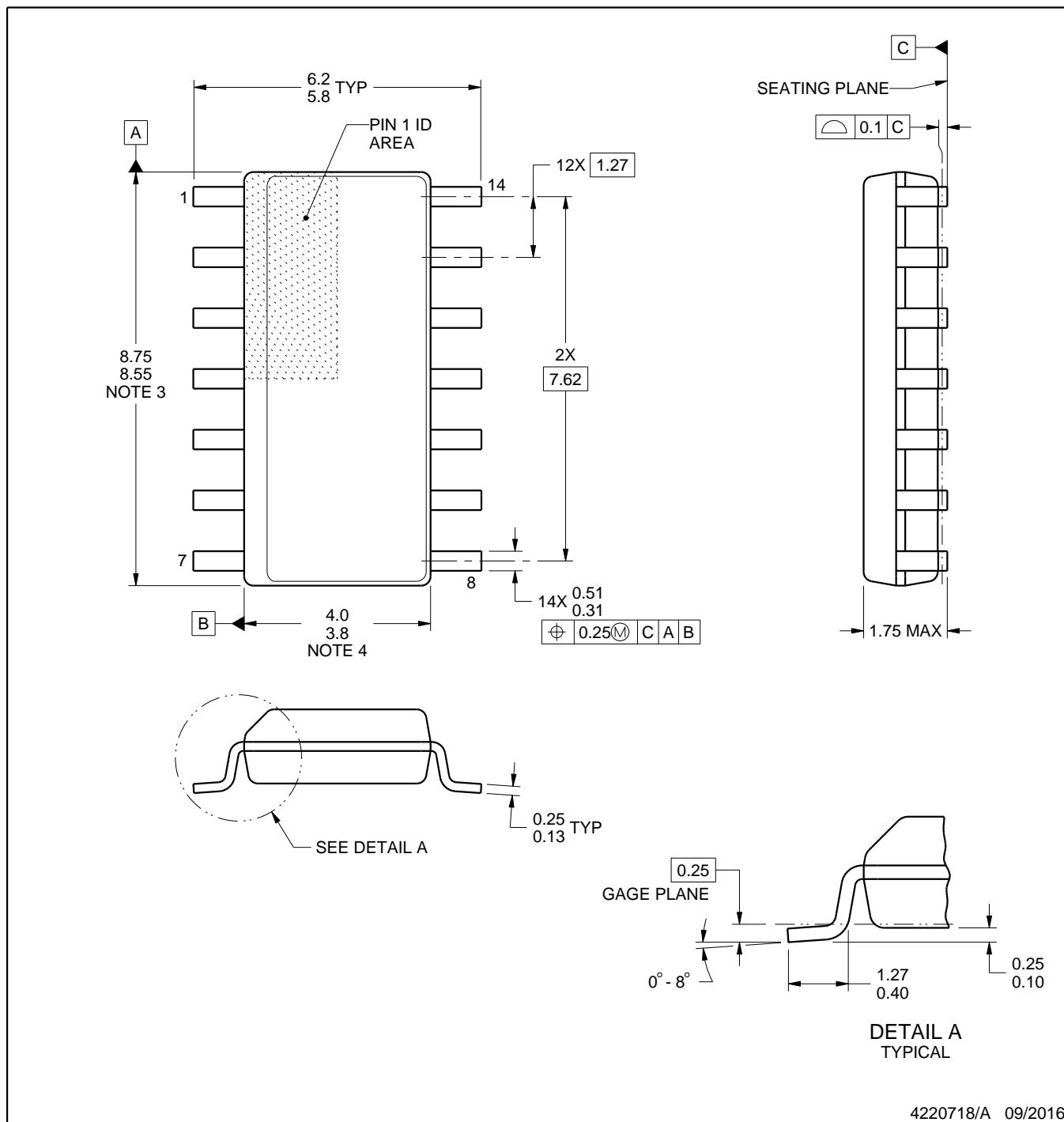
△D The 20 pin end lead shoulder width is a vendor option, either half or full width.

# PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

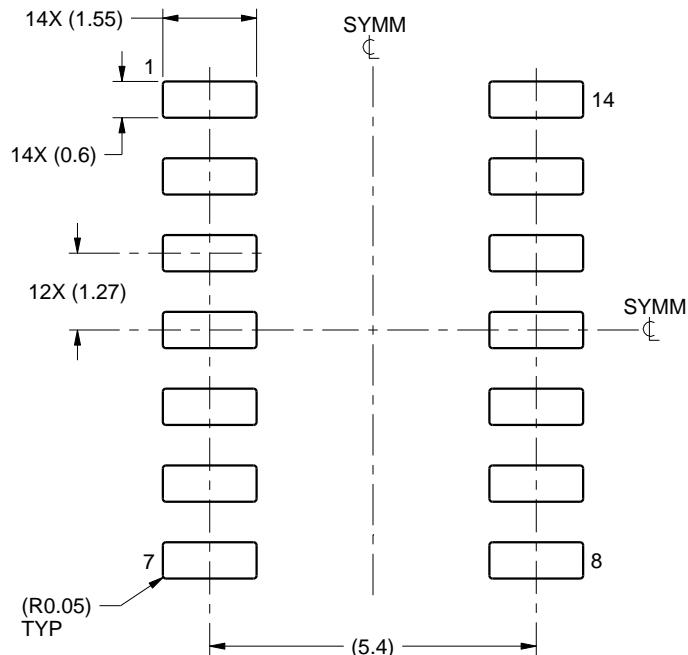
- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

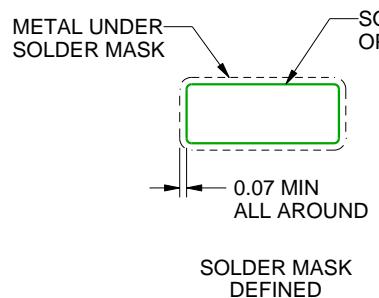
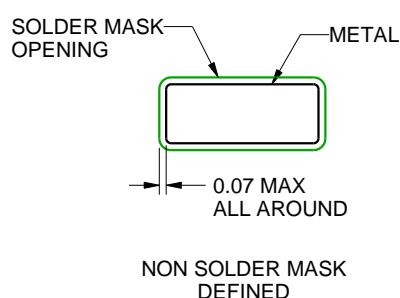
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

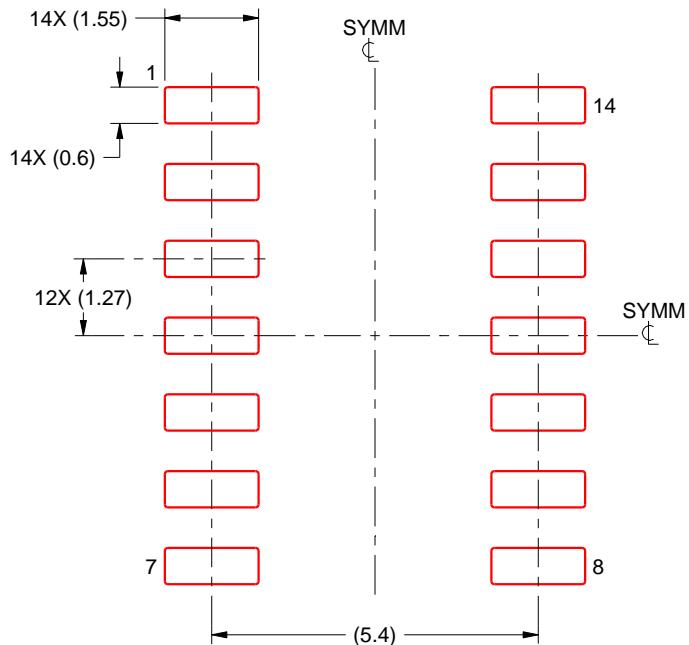
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

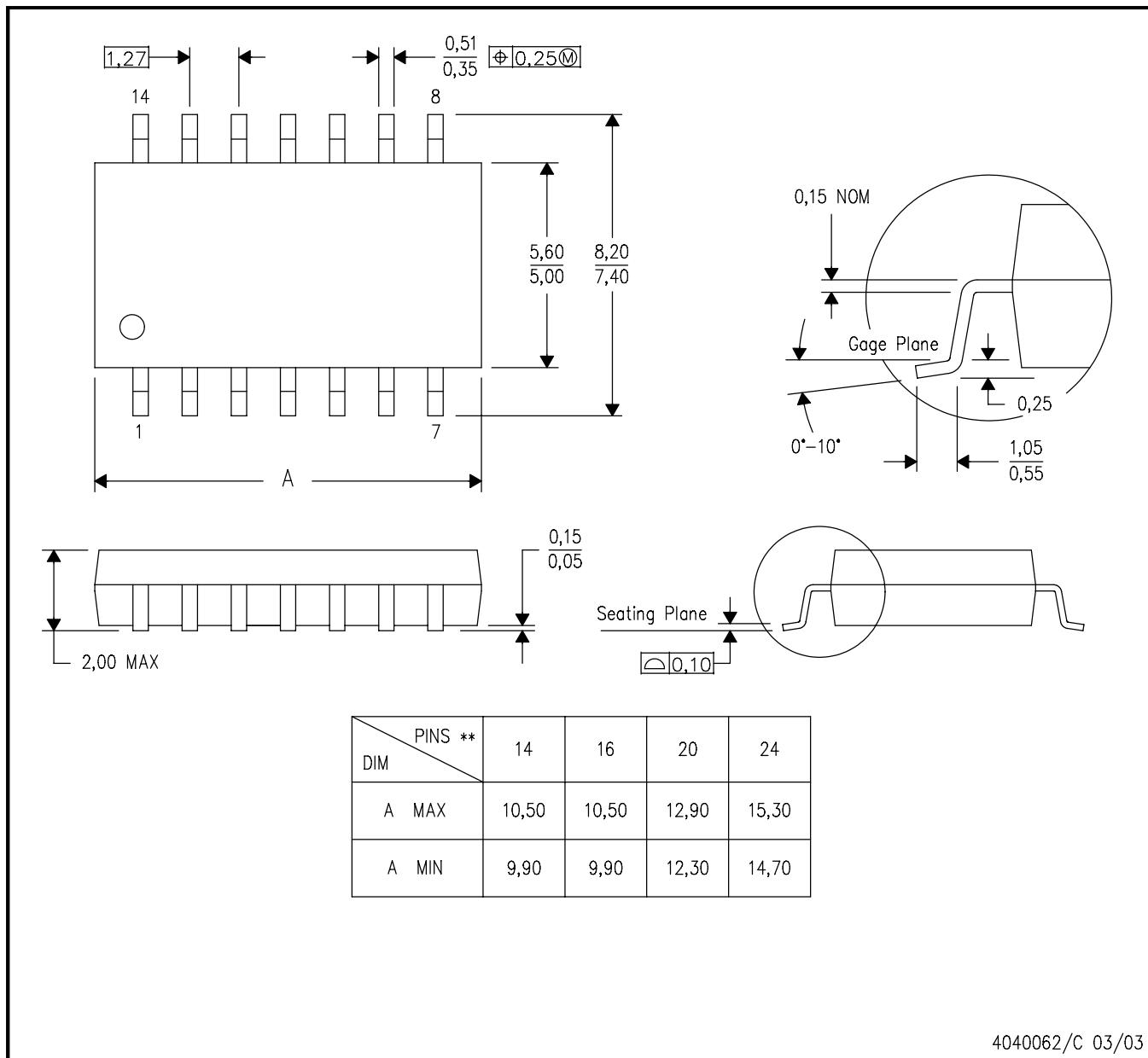
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

**14-PINS SHOWN**

**PLASTIC SMALL-OUTLINE PACKAGE**



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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**SN5432, SN54LS32, SN54S32,  
SN7432, SN74LS32, SN74S32**  
**QUADRUPLE 2-INPUT POSITIVE-OR GATES**

DECEMBER 1983 - REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

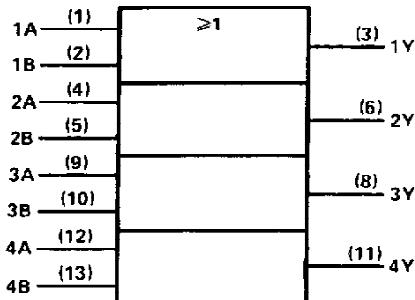
**description**

These devices contain four independent 2-input OR gates.

The SN5432, SN54LS32 and SN54S32 are characterized for operation over the full military range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN7432, SN74LS32 and SN74S32 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

**FUNCTION TABLE (each gate)**

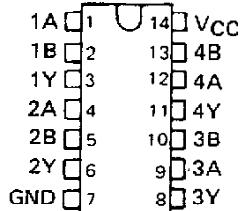
INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

**logic symbol†**

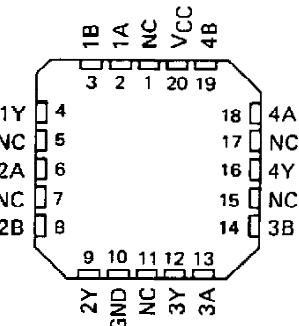
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for D, J, N, or W packages.

SN5432, SN54LS32, SN54S32 . . . J OR W PACKAGE  
SN7432 . . . N PACKAGE  
SN74LS32, SN74S32 . . . D OR N PACKAGE

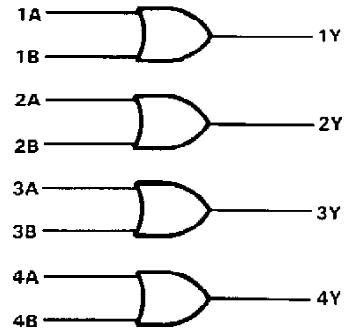
(TOP VIEW)



SN54LS32, SN54S32 . . . FK PACKAGE  
(TOP VIEW)



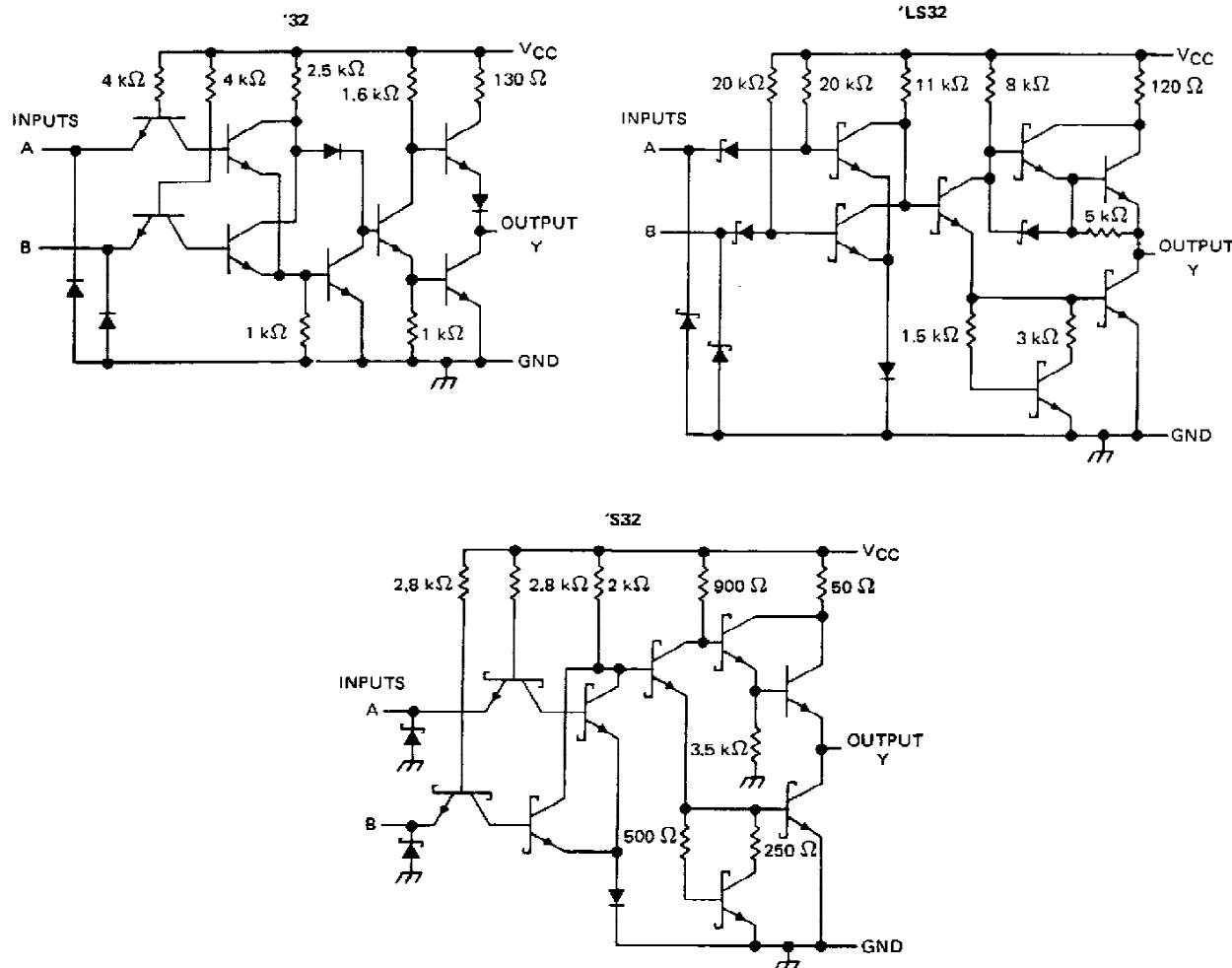
NC - No internal connection

**logic diagram****positive logic**

$$Y = A + B \text{ or } Y = \overline{\overline{A} \cdot \overline{B}}$$

**SN5432, SN54LS32, SN54S32,  
SN7432, SN74LS32, SN74S32  
QUADRUPLE 2-INPUT POSITIVE-OR GATES**

schematics (each gate)



Resistor values shown are nominal.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, V <sub>CC</sub> (see Note 1) . . . . .	7 V
Input voltage: '32, 'S32 . . . . .	5.5 V
'LS32 . . . . .	7 V
Operating free-air temperature: SN54' . . . . .	-55°C to 125°C
SN74' . . . . .	0°C to 70°C
Storage temperature range . . . . .	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TEXAS  
INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SN5432, SN7432  
QUADRUPLE 2-INPUT POSITIVE-OR GATES

**recommended operating conditions**

	SN5432			SN7432			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub> Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub> High-level input voltage	2			2			V
V <sub>IL</sub> Low-level input voltage			0.8			0.8	V
I <sub>OH</sub> High-level output current			-0.8			-0.8	mA
I <sub>OL</sub> Low-level output current			16			16	mA
T <sub>A</sub> Operating free-air temperature	-55	125	0	0	70	70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS†	SN5432			SN7432			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -12 mA			-1.5			-1.5	V
V <sub>QH</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, I <sub>OH</sub> = -0.8 mA	2.4	3.4		2.4	3.4		V
V <sub>QL</sub>	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 16 mA		0.2	0.4	0.2	0.4		V
I <sub>I</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V			1			1	mA
I <sub>IH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V			40			40	µA
I <sub>IL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V			1.6			-1.6	mA
I <sub>OSS</sub>	V <sub>CC</sub> = MAX	-20	-55	-18	-18	-55	-55	mA
I <sub>CCH</sub>	V <sub>CC</sub> = MAX, See Note 2		15	22	15	22		mA
I <sub>CCL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0 V	23	38		23	38		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time.

NOTE 2: One input at 4.5 V, all others at GND.

**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	A or B	Y	R <sub>L</sub> = 400 Ω, C <sub>L</sub> = 15 pF	10	15	ns	
t <sub>PHL</sub>				14	22	ns	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



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# SN54LS32, SN74LS32 QUADRUPLE 2-INPUT POSITIVE-OR GATES

## recommended operating conditions

	SN54LS32			SN74LS32			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub> Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub> High-level input voltage	2			2			V
V <sub>IL</sub> Low-level input voltage			0.7			0.8	V
I <sub>OH</sub> High-level output current			-0.4			-0.4	mA
I <sub>OL</sub> Low-level output current			4			8	mA
T <sub>A</sub> Operating free-air temperature	-55		125	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS32			SN74LS32			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA			-1.5			-1.5	V
V <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, I <sub>OH</sub> = -0.4 mA	2.5	3.4		2.7	3.4		V
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, I <sub>OL</sub> = 4 mA	0.25	0.4		0.25	0.4		V
	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, I <sub>OL</sub> = 8 mA				0.35	0.5		
I <sub>I</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V			0.1			0.1	mA
I <sub>IH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V			20			20	μA
I <sub>IL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V			-0.4			-0.4	mA
I <sub>OS\$</sub>	V <sub>CC</sub> = MAX	-20		-100	-20		-100	mA
I <sub>CCH</sub>	V <sub>CC</sub> = MAX, See Note 2	3.1	6.2		3.1	6.2		mA
I <sub>CCL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0 V	4.9	9.8		4.9	9.8		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

\$ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

NOTE 2: One input at 4.5 V, all others at GND.

## switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
			R <sub>L</sub> = 2 kΩ	C <sub>L</sub> = 15 pF				
t <sub>PLH</sub> t <sub>PHL</sub>	A or B	Y			14	22		ns
					14	22		ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

SN54S32, SN74S32  
QUADRUPLE 2-INPUT POSITIVE-OR GATES

**recommended operating conditions**

	SN54S32			SN74S32			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub> Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub> High-level input voltage	2			2			V
V <sub>IL</sub> Low-level input voltage			0.8			0.8	V
I <sub>OH</sub> High-level output current			-1			-1	mA
I <sub>OL</sub> Low-level output current			20			20	mA
T <sub>A</sub> Operating free-air temperature	-55	125	0	0	70	70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS <sup>†</sup>	SN54S32			SN74S32			UNIT	
		MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX		
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA			-1.2			-1.2	V	
V <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, I <sub>OH</sub> = -1 mA	2.5	3.4		2.7	3.4		V	
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 20 mA			0.5			0.5	V	
I <sub>I</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V			1			1	mA	
I <sub>IH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V			50			50	μA	
I <sub>IIL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5 V			-2			-2	mA	
I <sub>OS</sub> <sup>§</sup>	V <sub>CC</sub> = MAX	-40	-100	-40	-100	-40	-100	mA	
I <sub>CCH</sub>	V <sub>CC</sub> = MAX, See Note 2			18	32		18	32	mA
I <sub>CCL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0 V			38	68		38	68	mA

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

<sup>§</sup> Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

NOTE 2: One input at 4.5 V, all others at GND.

**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	A or B	Y	R <sub>L</sub> = 280 Ω, C <sub>L</sub> = 15 pF	4	7	ns	
t <sub>PHL</sub>				4	7	ns	
t <sub>PLH</sub>	A or B	Y	R <sub>L</sub> = 280 Ω, C <sub>L</sub> = 50 pF	5		ns	
t <sub>PHL</sub>				5		ns	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9557401QCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9557401QC A SNJ5432J	Samples
5962-9557401QDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9557401QD A SNJ5432W	Samples
5962-9557401QDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9557401QD A SNJ5432W	Samples
JM38510/30501B2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30501B2A	Samples
JM38510/30501B2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30501B2A	Samples
JM38510/30501BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30501BCA	Samples
JM38510/30501BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30501BCA	Samples
JM38510/30501BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30501BDA	Samples
JM38510/30501BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30501BDA	Samples
JM38510/30501SCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30501SCA	Samples
JM38510/30501SCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30501SCA	Samples
JM38510/30501SDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30501SDA	Samples
JM38510/30501SDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30501SDA	Samples
M38510/30501B2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30501B2A	Samples
M38510/30501B2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30501B2A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
M38510/30501BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30501BCA	Samples
M38510/30501BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30501BCA	Samples
M38510/30501BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30501BDA	Samples
M38510/30501BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30501BDA	Samples
M38510/30501SCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30501SCA	Samples
M38510/30501SCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30501SCA	Samples
M38510/30501SDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30501SDA	Samples
M38510/30501SDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30501SDA	Samples
SN5432J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN5432J	Samples
SN5432J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN5432J	Samples
SN54LS32J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS32J	Samples
SN54LS32J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS32J	Samples
SN54S32J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54S32J	Samples
SN54S32J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54S32J	Samples
SN7432N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN7432N	Samples
SN7432N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN7432N	Samples
SN7432NE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN7432N	Samples
SN7432NE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN7432N	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS32D	OBsolete	SOIC	D	14		TBD	Call TI	Call TI	0 to 70	LS32	
SN74LS32D	OBsolete	SOIC	D	14		TBD	Call TI	Call TI	0 to 70	LS32	
SN74LS32DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS32	Samples
SN74LS32DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS32	Samples
SN74LS32DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS32	Samples
SN74LS32DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS32	Samples
SN74LS32DRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS32	Samples
SN74LS32DRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS32	Samples
SN74LS32DRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS32	Samples
SN74LS32DRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS32	Samples
SN74LS32N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS32N	Samples
SN74LS32N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS32N	Samples
SN74LS32NE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS32N	Samples
SN74LS32NE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS32N	Samples
SN74LS32NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS32	Samples
SN74LS32NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS32	Samples
SN74LS32NSRG4	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS32	Samples
SN74LS32NSRG4	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS32	Samples
SN74S32D	OBsolete	SOIC	D	14		TBD	Call TI	Call TI	0 to 70	S32	
SN74S32D	OBsolete	SOIC	D	14		TBD	Call TI	Call TI	0 to 70	S32	
SN74S32DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	S32	Samples
SN74S32DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	S32	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74S32N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74S32N	Samples
SN74S32N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74S32N	Samples
SNJ5432J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9557401QC A SNJ5432J	Samples
SNJ5432J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9557401QC A SNJ5432J	Samples
SNJ5432W	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9557401QD A SNJ5432W	Samples
SNJ5432W	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9557401QD A SNJ5432W	Samples
SNJ54LS32FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS 32FK	Samples
SNJ54LS32FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS 32FK	Samples
SNJ54LS32J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS32J	Samples
SNJ54LS32J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS32J	Samples
SNJ54LS32W	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS32W	Samples
SNJ54LS32W	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS32W	Samples
SNJ54S32J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54S32J	Samples
SNJ54S32J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54S32J	Samples
SNJ54S32W	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54S32W	Samples
SNJ54S32W	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54S32W	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN5432, SN54LS32, SN54LS32-SP, SN54S32, SN7432, SN74LS32, SN74S32 :**

• Catalog : [SN7432](#), [SN74LS32](#), [SN54LS32](#), [SN74S32](#)

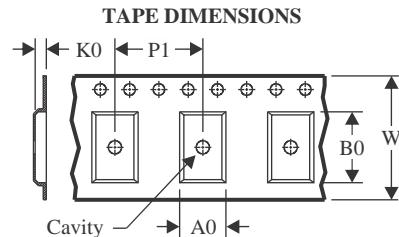
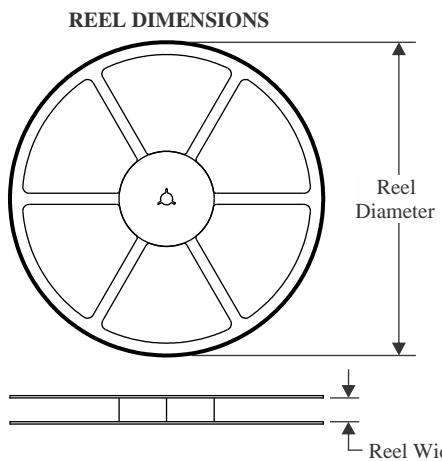
• Military : [SN5432](#), [SN54LS32](#), [SN54S32](#)

• Space : [SN54LS32-SP](#)

NOTE: Qualified Version Definitions:

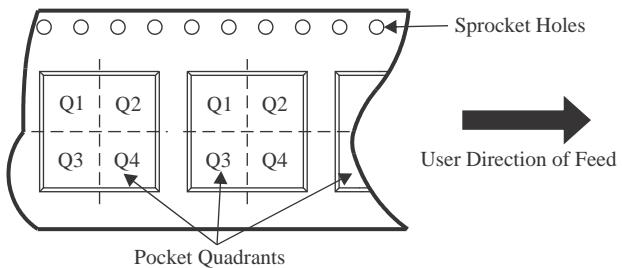
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TAPE AND REEL INFORMATION



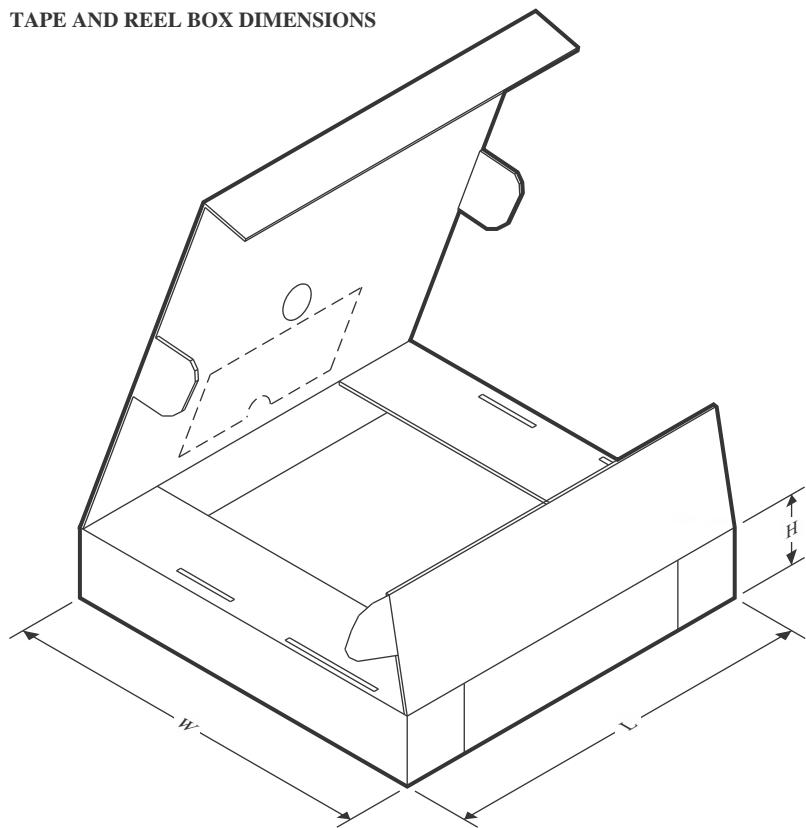
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



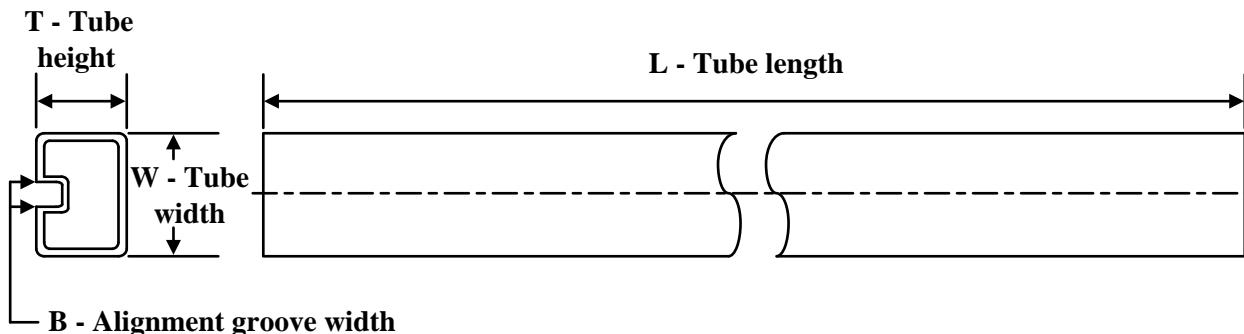
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS32DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LS32DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS32NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74S32DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS32DBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74LS32DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LS32NSR	SO	NS	14	2000	356.0	356.0	35.0
SN74S32DR	SOIC	D	14	2500	356.0	356.0	35.0

**TUBE**


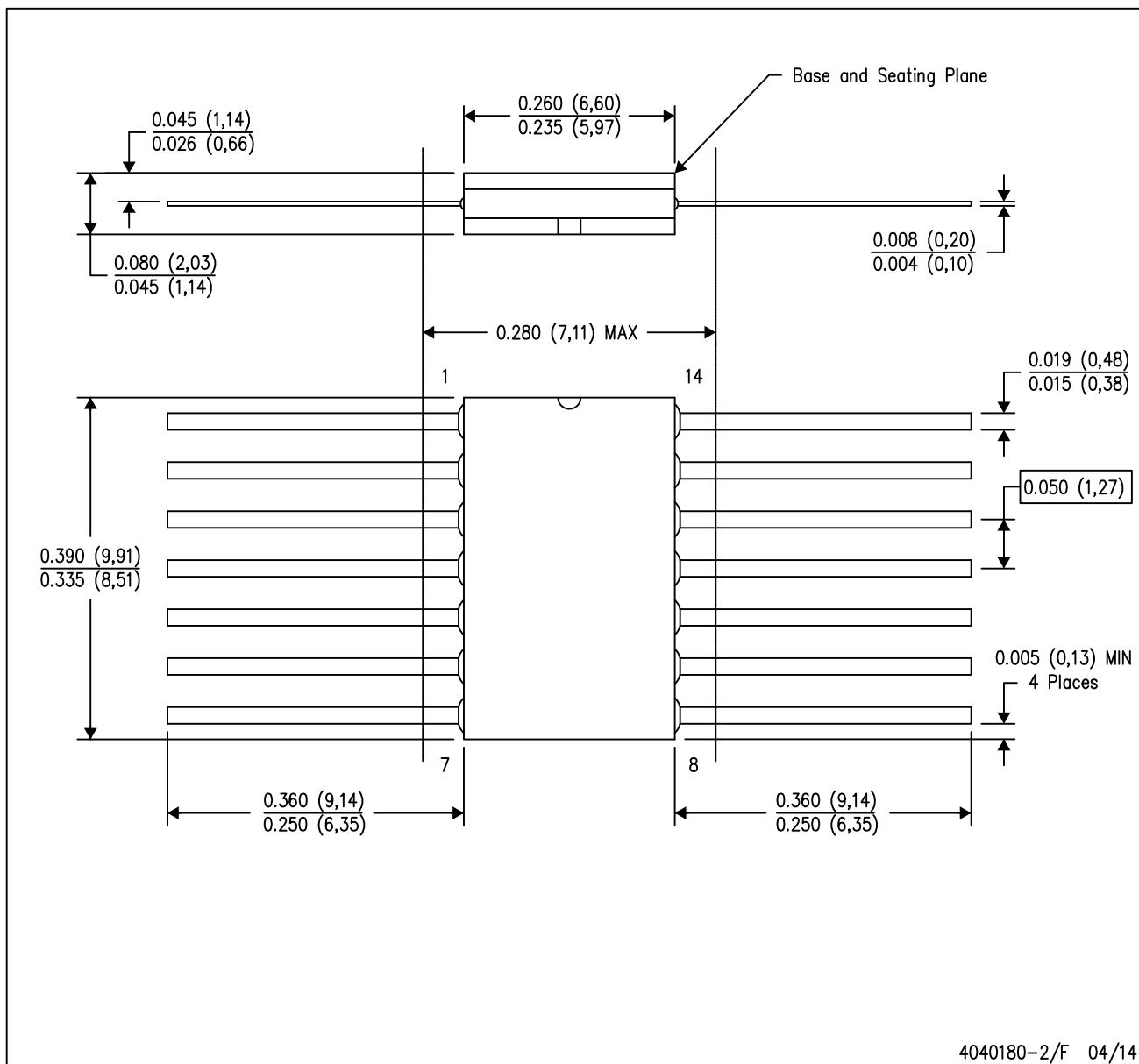
\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T ( $\mu$ m)	B (mm)
5962-9557401QDA	W	CFP	14	25	506.98	26.16	6220	NA
JM38510/30501B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/30501BDA	W	CFP	14	25	506.98	26.16	6220	NA
JM38510/30501SDA	W	CFP	14	25	506.98	26.16	6220	NA
M38510/30501B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/30501BDA	W	CFP	14	25	506.98	26.16	6220	NA
M38510/30501SDA	W	CFP	14	25	506.98	26.16	6220	NA
SN7432N	N	PDIP	14	25	506	13.97	11230	4.32
SN7432N	N	PDIP	14	25	506	13.97	11230	4.32
SN7432NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN7432NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS32N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS32N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS32NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS32NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74S32N	N	PDIP	14	25	506	13.97	11230	4.32
SN74S32N	N	PDIP	14	25	506	13.97	11230	4.32
SNJ5432W	W	CFP	14	25	506.98	26.16	6220	NA
SNJ54LS32FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS32W	W	CFP	14	25	506.98	26.16	6220	NA
SNJ54S32W	W	CFP	14	25	506.98	26.16	6220	NA

## MECHANICAL DATA

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



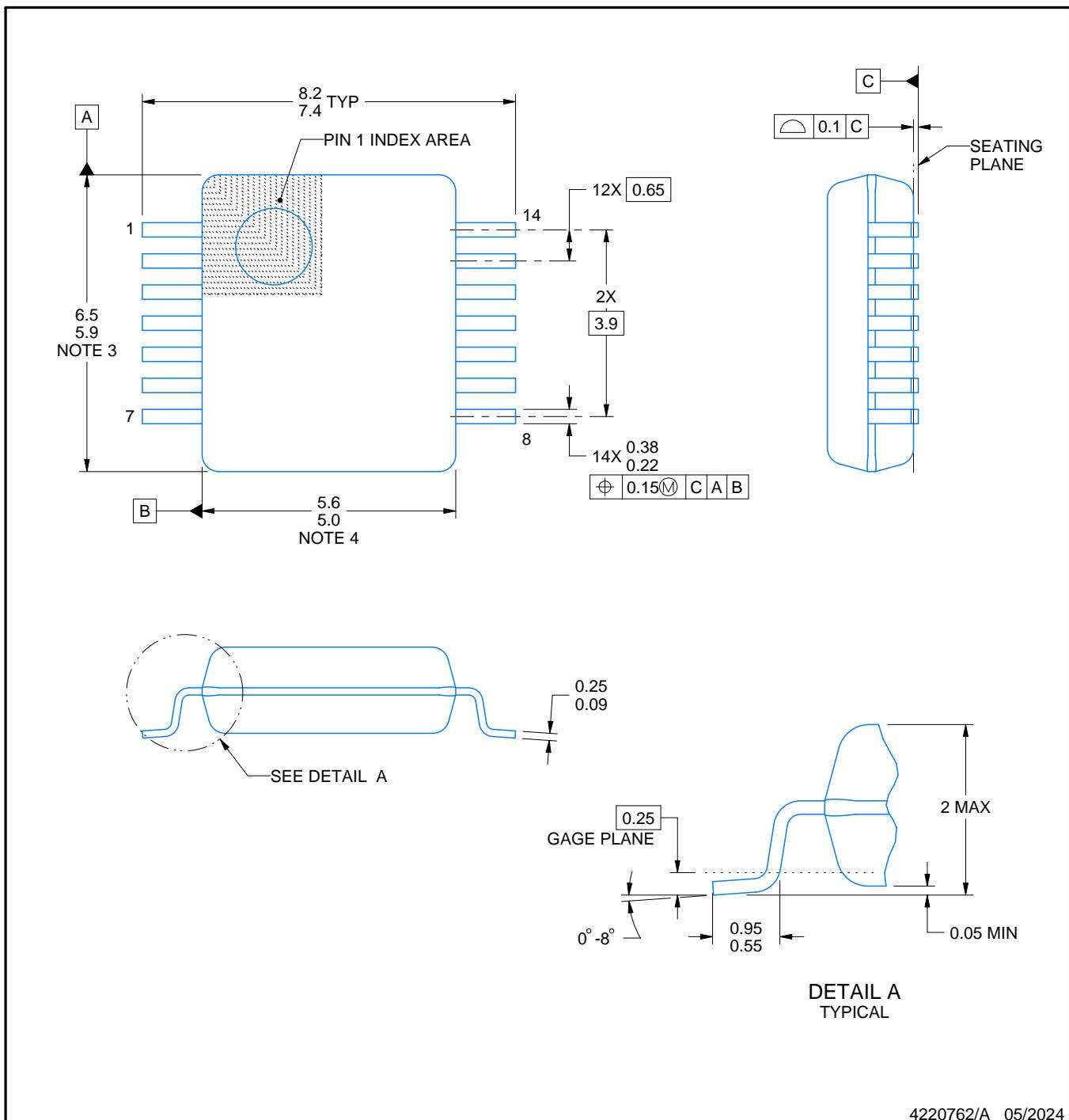
4040180-2/F 04/14

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14

# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



### NOTES:

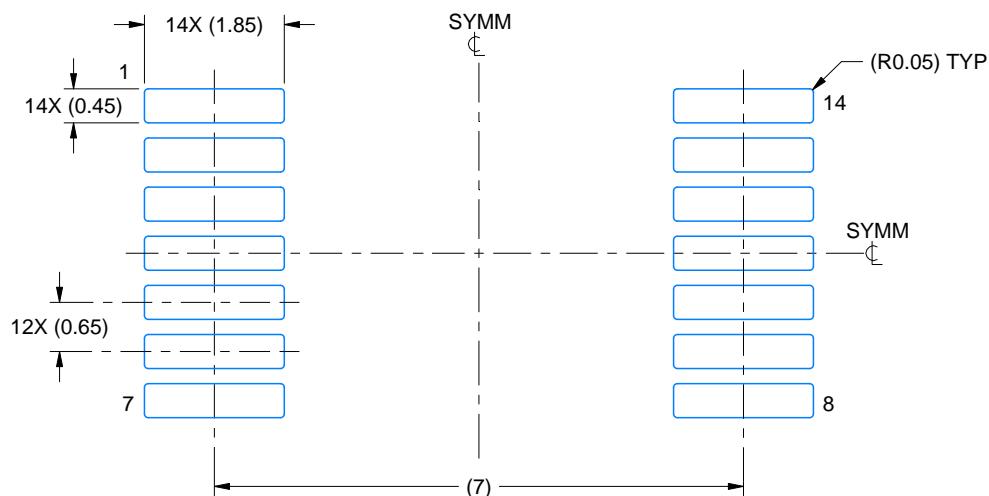
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

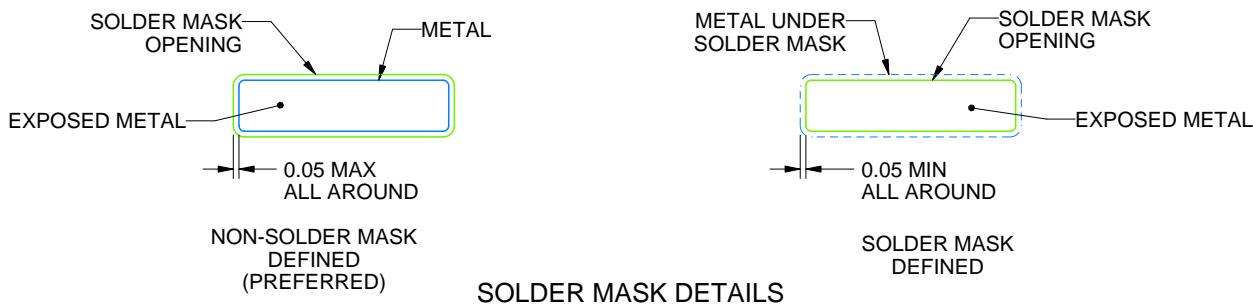
DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220762/A 05/2024

NOTES: (continued)

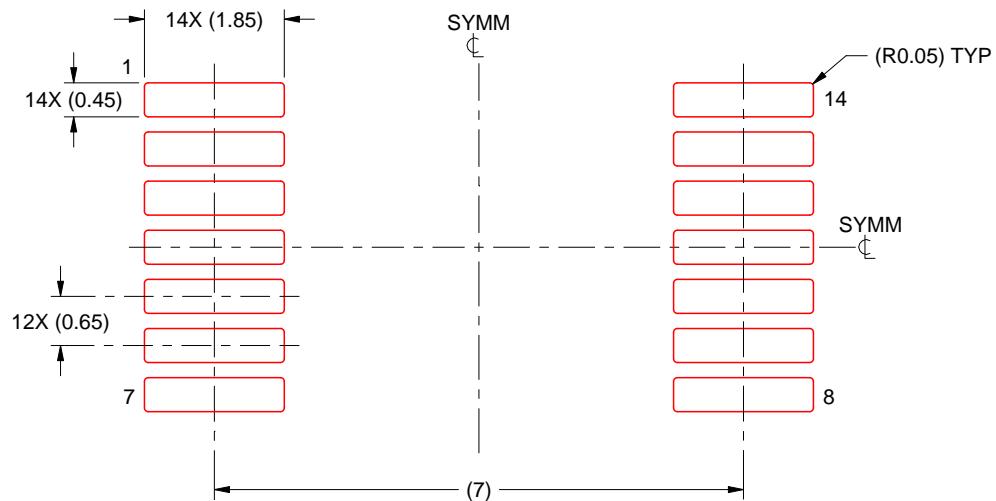
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

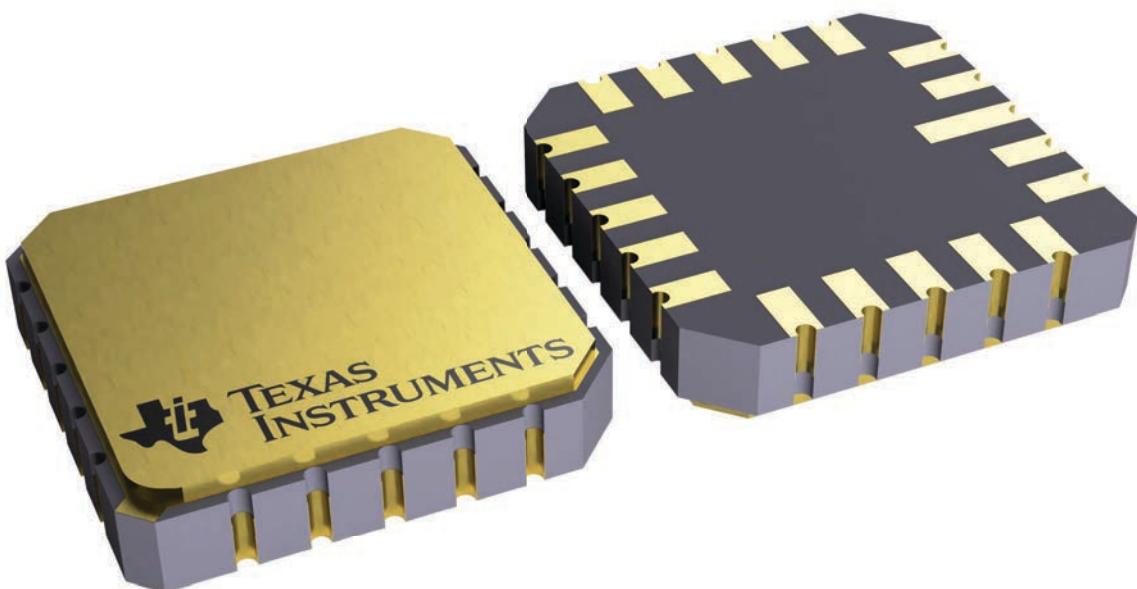
**FK 20**

**LCCC - 2.03 mm max height**

**8.89 x 8.89, 1.27 mm pitch**

**LEADLESS CERAMIC CHIP CARRIER**

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



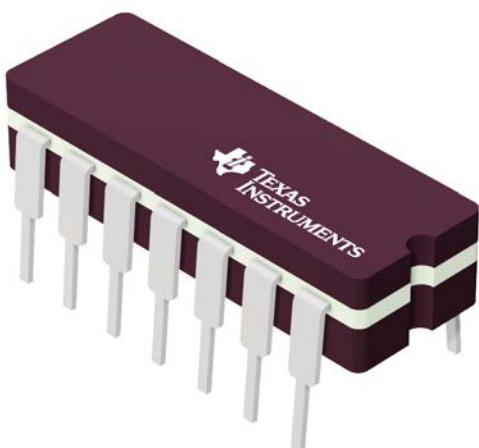
4229370VA\

# GENERIC PACKAGE VIEW

J 14

**CDIP - 5.08 mm max height**

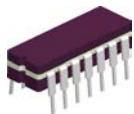
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

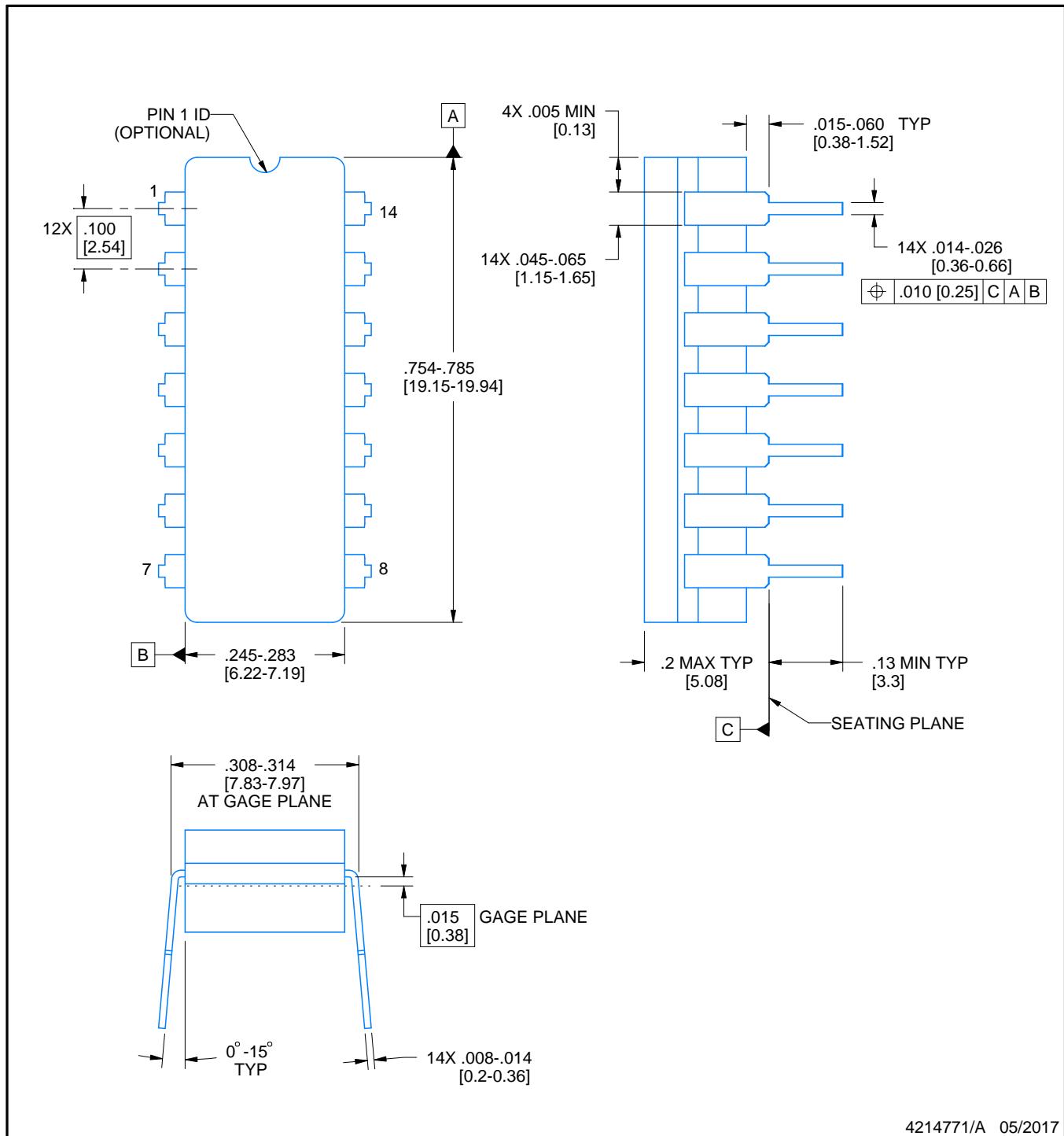
J0014A



# PACKAGE OUTLINE

## CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

### NOTES:

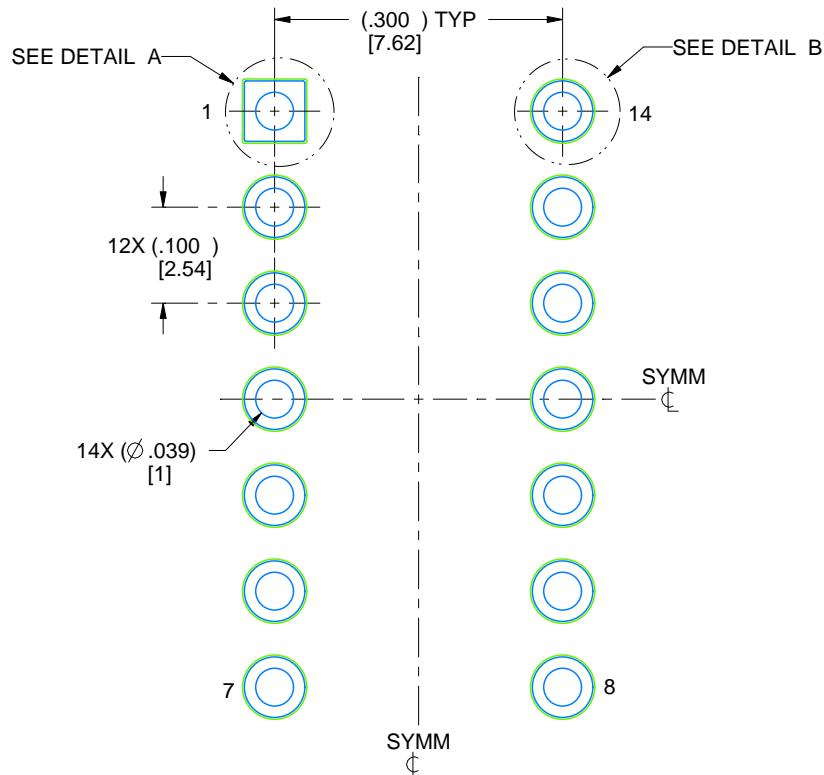
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

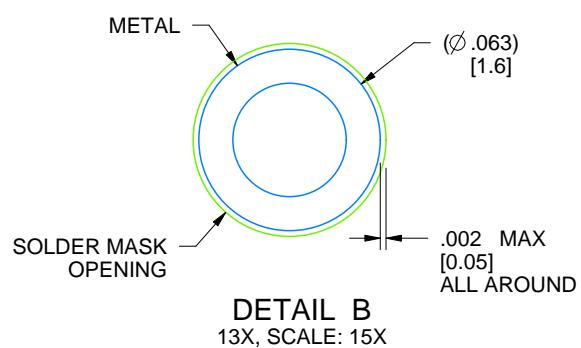
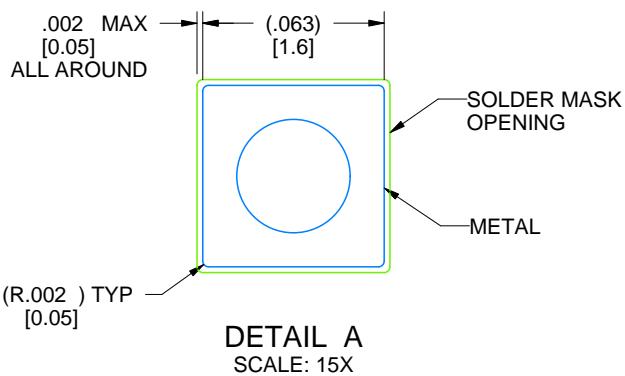
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X

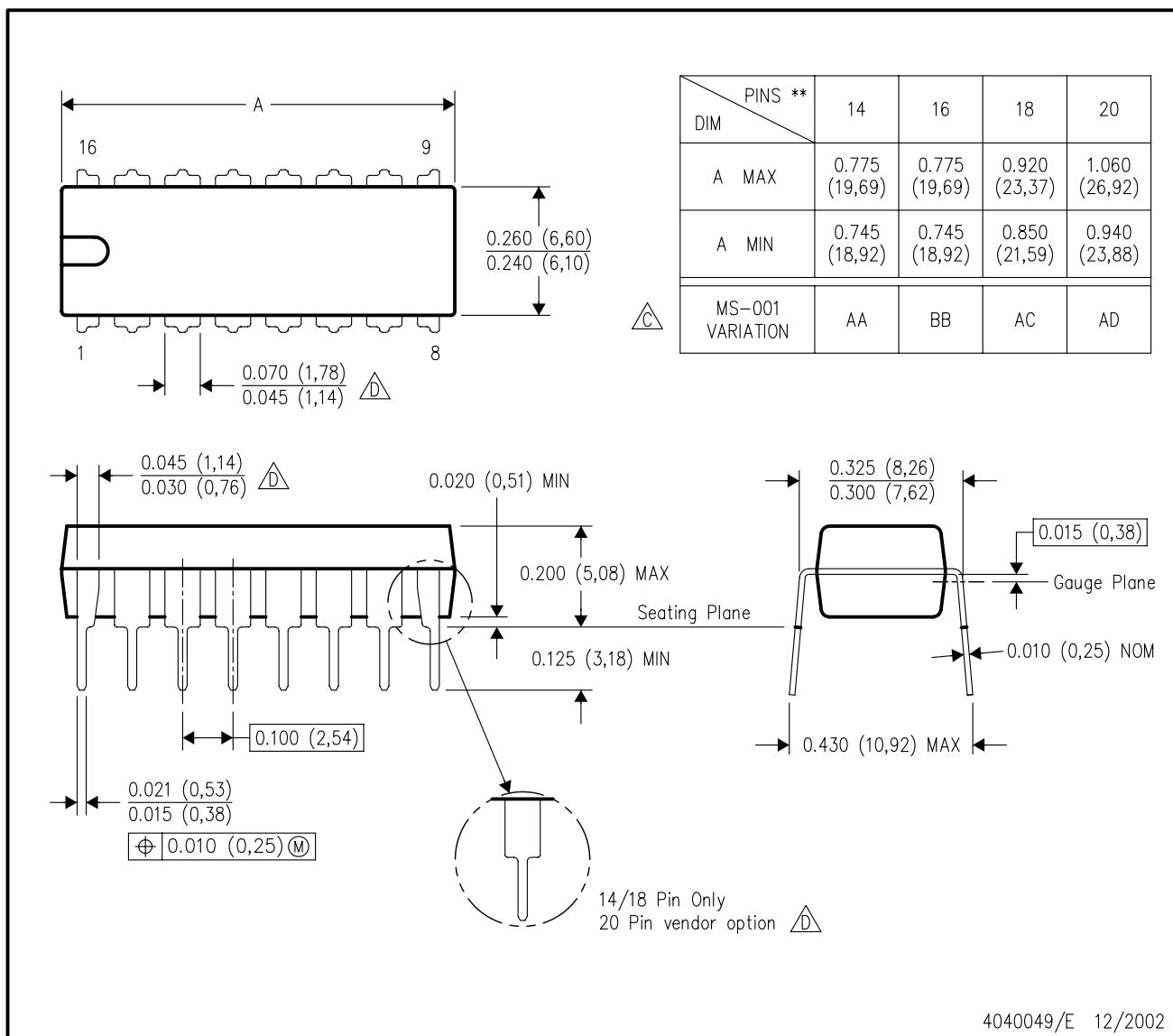


4214771/A 05/2017

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

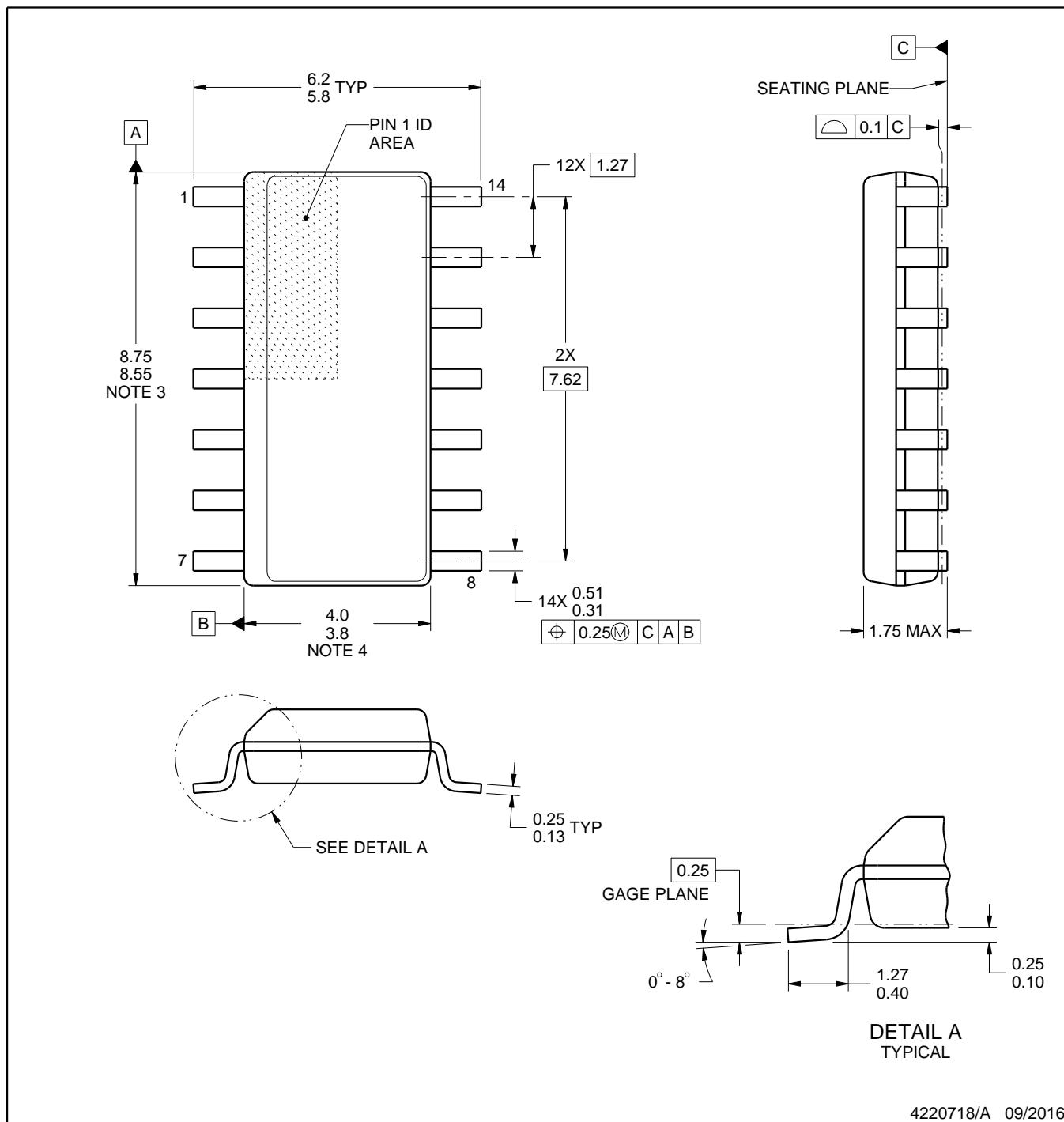
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

# PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

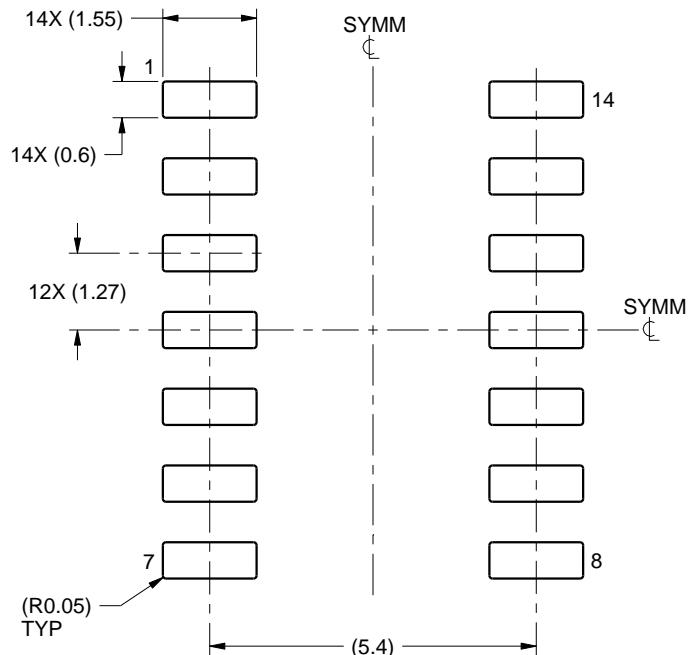
- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

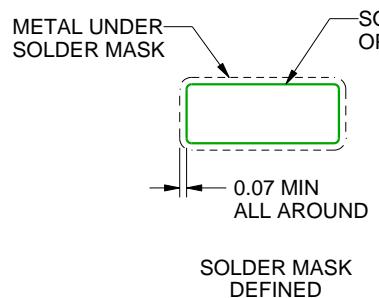
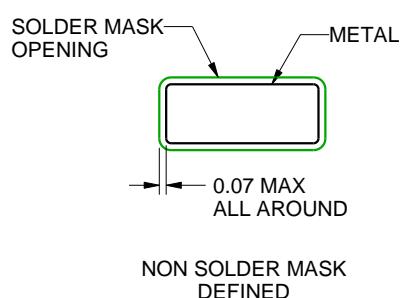
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

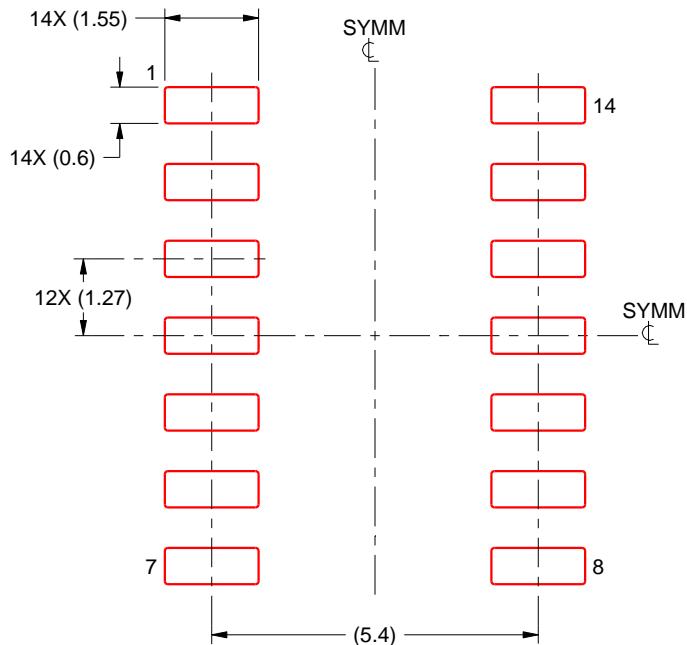
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

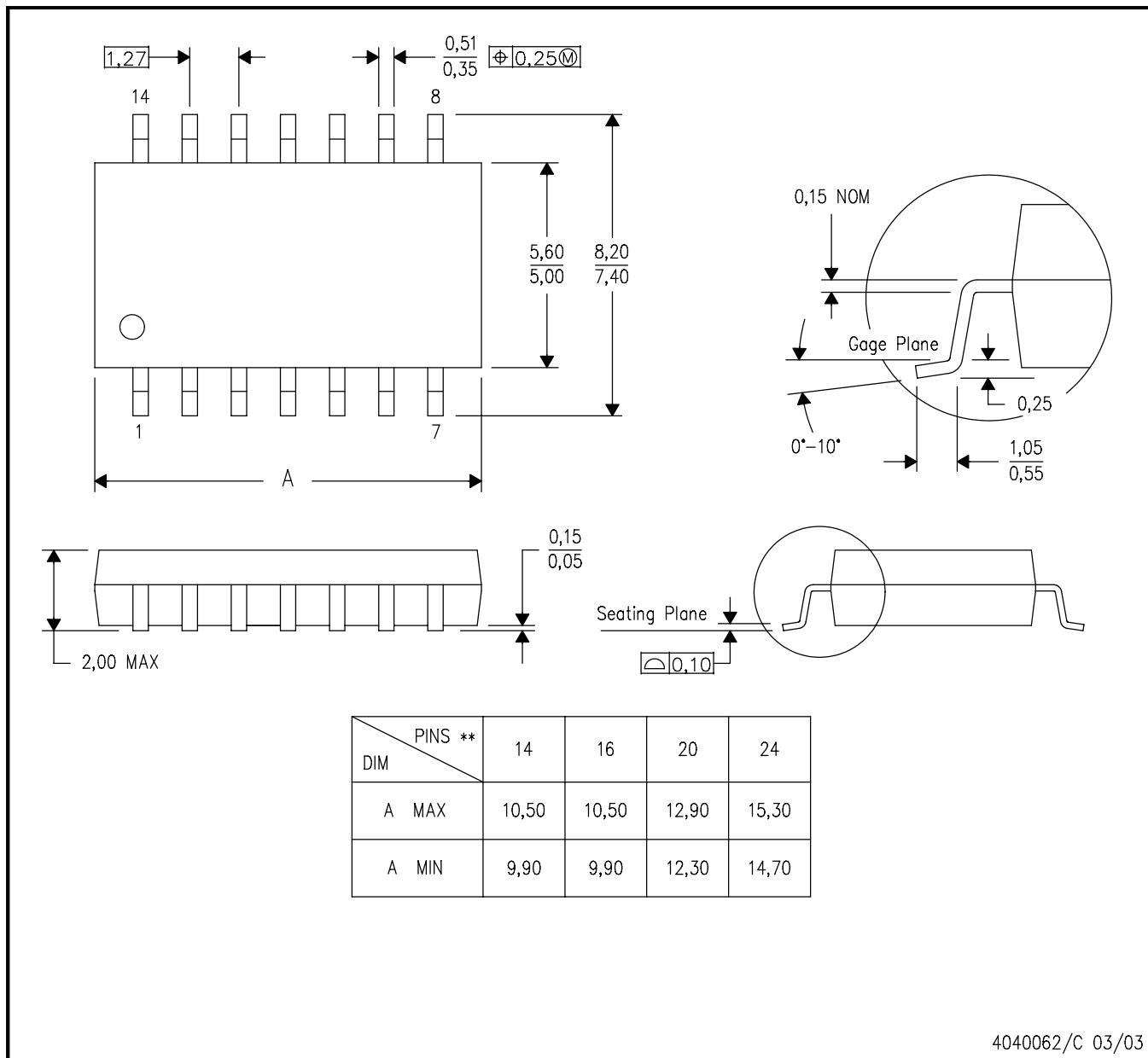
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

**14-PINS SHOWN**

**PLASTIC SMALL-OUTLINE PACKAGE**



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

4040062/C 03/03

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- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

### description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

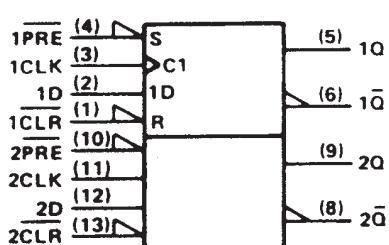
The SN54' family is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74' family is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

FUNCTION TABLE

INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H <sup>†</sup>	H <sup>†</sup>
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q <sub>0</sub>	$\bar{Q}_0$

<sup>†</sup> The output levels in this configuration are not guaranteed to meet the minimum levels in  $V_{OH}$  if the lows at preset and clear are near  $V_{IL}$  maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

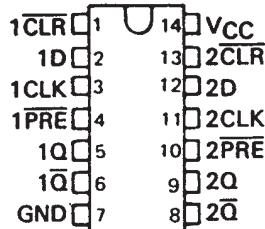
### logic symbol <sup>‡</sup>



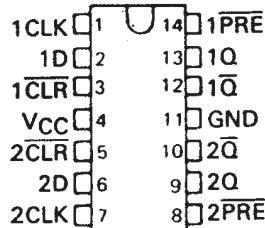
<sup>‡</sup>This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

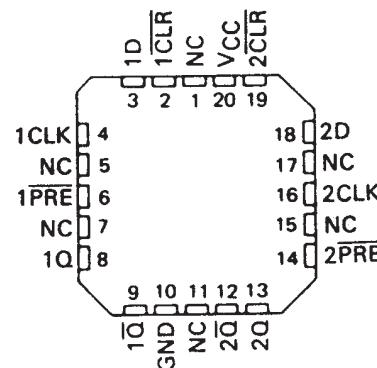
**SN5474 . . . J PACKAGE**  
 SN54LS74A, SN54S74 . . . J OR W PACKAGE  
 SN7474 . . . N PACKAGE  
 SN74LS74A, SN74S74 . . . D OR N PACKAGE  
 (TOP VIEW)



**SN5474 . . . W PACKAGE**  
 (TOP VIEW)

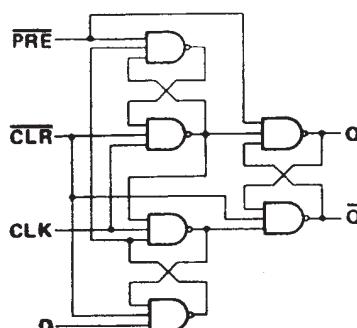


**SN54LS74A, SN54S74 . . . FK PACKAGE**  
 (TOP VIEW)



NC - No internal connection

### logic diagram (positive logic)



**SN5474, SN54LS74A, SN54S74**

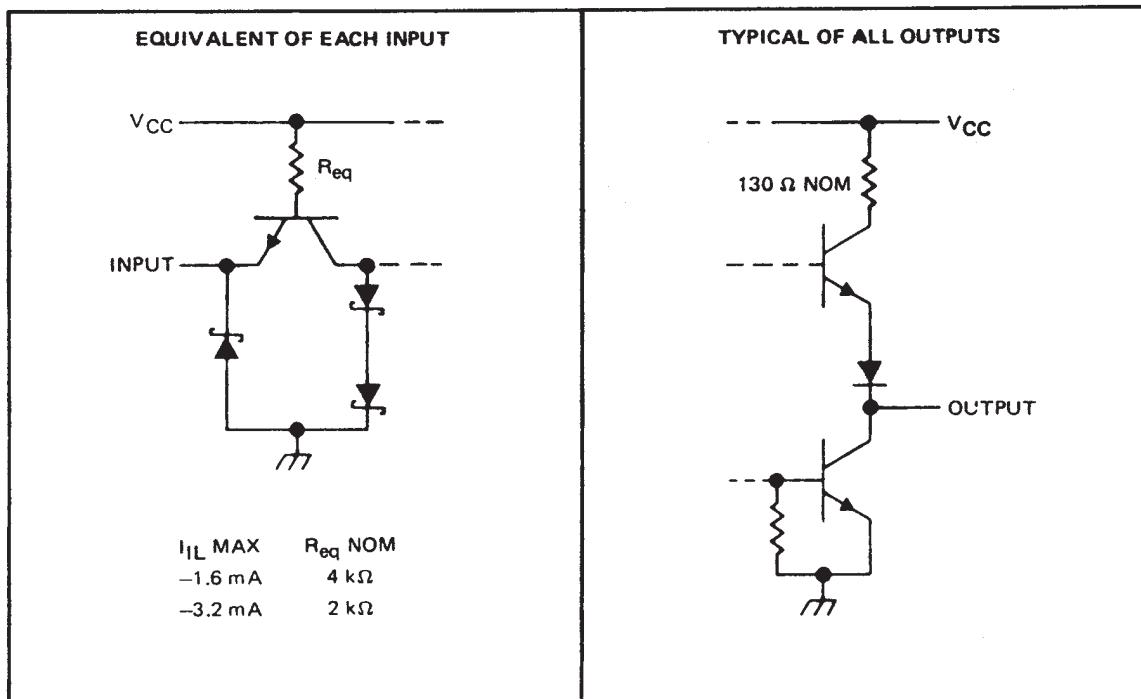
**SN7474, SN74LS74A, SN74S74**

**DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR**

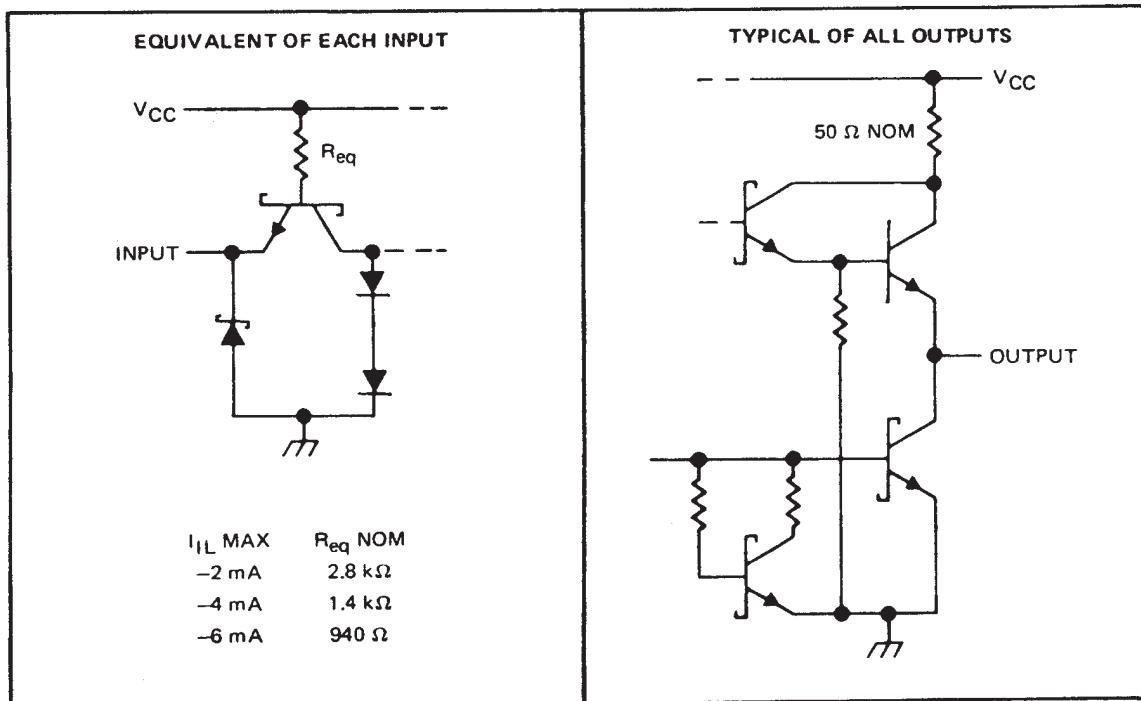
SDLS119 – DECEMBER 1983 – REVISED MARCH 1988

**schematics of inputs and outputs**

**74**



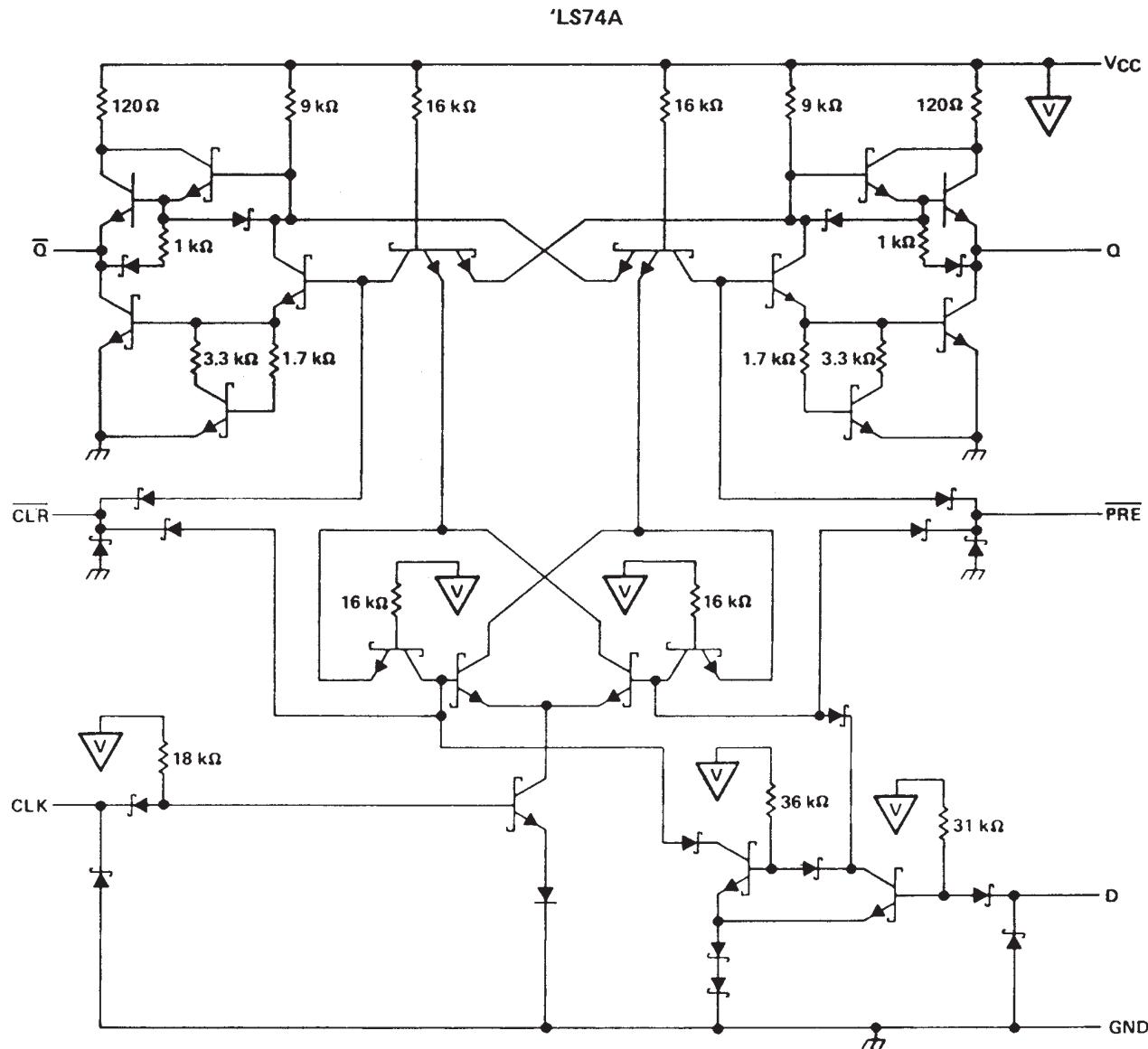
**'S74**



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**DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR**

SDLS119 – DECEMBER 1983 – REVISED MARCH 1988

**schematic****absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, V <sub>CC</sub> (see Note 1) . . . . .	7 V
Input voltage: '74, 'S74 . . . . .	5.5 V
'LS74A . . . . .	7 V
Operating free-air temperature range: SN54' . . . . .	-55°C to 125°C
SN74' . . . . .	0°C to 70°C
Storage temperature range . . . . .	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

**SN5474, SN54LS74A, SN54S74****SN7474, SN74LS74A, SN74S74****DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR**

SDLS119 - DECEMBER 1983 - REVISED MARCH 1988

**recommended operating conditions**

			SN5474			SN7474			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage		2			2			V
V <sub>IL</sub>	Low-level input voltage				0.8			0.8	V
I <sub>OH</sub>	High-level output current				-0.4			-0.4	mA
I <sub>OL</sub>	Low-level output current				16			16	mA
t <sub>w</sub>	Pulse duration	CLK high	30			30			ns
		CLK low	37			37			
		PRE or CLR low	30			30			
t <sub>su</sub>	Input setup time before CLK t		20			20			ns
t <sub>h</sub>	Input hold time-data after CLK t		5			5			ns
T <sub>A</sub>	Operating free-air temperature		-55		125	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS <sup>†</sup>			SN5474			SN7474			UNIT
				MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -12 mA				-1.5			-1.5		V
V <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -0.4 mA			2.4	3.4		2.4	3.4		V
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 16 mA			0.2	0.4		0.2	0.4		V
I <sub>I</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V					1			1	mA
I <sub>IH</sub>	D CLR All Other	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V			40			40		μA
					120			120		
					80			80		
I <sub>IL</sub>	D PRE <sup>§</sup> CLR <sup>§</sup> CLK	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V			-1.6			-1.6		mA
					-1.6			-1.6		
					-3.2			-3.2		
					-3.2			-3.2		
I <sub>OS</sub> <sup>¶</sup>	V <sub>CC</sub> = MAX			-20	-57	-18	-18	-57		mA
I <sub>CC</sub> <sup>#</sup>	V <sub>CC</sub> = MAX, See Note 2				8.5	15		8.5	15	mA

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.<sup>‡</sup>All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.<sup>§</sup>Clear is tested with preset high and preset is tested with clear high.<sup>¶</sup>Not more than one output should be shown at a time.

#Average per flip-flop.

NOTE 2: With all outputs open, I<sub>CC</sub> is measured with the Q and  $\bar{Q}$  outputs high in turn. At the time of measurement, the clock input is grounded.**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
f <sub>max</sub>			R <sub>L</sub> = 400 Ω, C <sub>L</sub> = 15 pF	15	25		MHz	
t <sub>PLH</sub>	PRE or CLR	Q or $\bar{Q}$			25		ns	
t <sub>PHL</sub>					40		ns	
t <sub>PLH</sub>	CLK	Q or $\bar{Q}$			14	25	ns	
t <sub>PHL</sub>					20	40	ns	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

## DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

SDS119 - DECEMBER 1983 - REVISED MARCH 1988

## recommended operating conditions

			SN54LS74A			SN74LS74A			UNIT	
	MIN	NOM	MAX	MIN	NOM	MAX				
V <sub>CC</sub>	Supply voltage			4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage			2			2			V
V <sub>IL</sub>	Low-level input voltage				0.7			0.8		V
I <sub>OH</sub>	High-level output current					-0.4			-0.4	mA
I <sub>OL</sub>	Low-level output current					4		8		mA
f <sub>clock</sub>	Clock frequency			0	25		0	25		MHz
t <sub>w</sub>	Pulse duration	CLK high		25			25			ns
		PRE or CLR low		25			25			
t <sub>su</sub>	Setup time-before CLK↑	High-level data		20			20			ns
		Low-level data		20			20			
t <sub>h</sub>	Hold time-data after CLK↑			5			5			ns
T <sub>A</sub>	Operating free-air temperature			-55	125		0	70		°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>†</sup>			SN54LS74A			SN74LS74A			UNIT
				MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = MIN,	I <sub>I</sub> = -18 mA			-1.5			-1.5		V
V <sub>OH</sub>	V <sub>CC</sub> = MIN,	V <sub>IH</sub> = 2 V,	V <sub>IL</sub> = MAX,	2.5	3.4		2.7	3.4		V
V <sub>OL</sub>	V <sub>CC</sub> = MIN,	V <sub>IL</sub> = MAX,	V <sub>IH</sub> = 2 V,		0.25	0.4	0.25	0.4		V
	I <sub>OL</sub> = 4 mA						0.35	0.5		
I <sub>I</sub>	D or CLK	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 7 V		0.1		0.1			mA
	CLR or PRE				0.2		0.2			
I <sub>IH</sub>	D or CLK	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 2.7 V		20		20			μA
	CLR or PRE				40		40			
I <sub>IIL</sub>	D or CLK	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 0.4 V		-0.4		-0.4			mA
	CLR or PRE				-0.8		-0.8			
I <sub>OS\$</sub>	V <sub>CC</sub> = MAX,	See Note 4		-20	-100	-20	-100			mA
I <sub>CC</sub> (Total)	V <sub>CC</sub> = MAX,	See Note 2		4	8		4	8		mA

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.<sup>‡</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.<sup>§</sup> Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.NOTE 2: With all outputs open, I<sub>CC</sub> is measured with the Q and  $\bar{Q}$  outputs high in turn. At the time of measurement, the clock input is grounded.NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V<sub>O</sub> = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>max</sub>			R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 15 pF	25	33		MHz
t <sub>PLH</sub>	CLR, PRE or CLK	Q or $\bar{Q}$		13	25		ns
t <sub>PHL</sub>				25	40		ns

Note 3: Load circuits and voltage waveforms are shown in Section 1.

**SN5474, SN54LS74A, SN54S74**

**SN7474, SN74LS74A, SN74S74**

**DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR**

SDLS119 – DECEMBER 1983 – REVISED MARCH 1988

**recommended operating conditions**

			SN54S74			SN74S74			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.75	5	6.25	V
V <sub>IH</sub>	High-level input voltage		2			2			V
V <sub>IL</sub>	Low-level input voltage				0.8			0.8	V
I <sub>OH</sub>	High-level output current				-1			-1	mA
I <sub>OL</sub>	Low-level output current				20			20	mA
t <sub>w</sub>	Pulse duration	CLK high	6			6			ns
		CLK low	7.3			7.3			
		CLR or PRE low	7			7			
t <sub>su</sub>	Setup time, before CLK ↑	High-level data	3			3			ns
		Low-level data	3			3			
t <sub>h</sub>	Input hold time - data after CLK ↑		2			2			ns
T <sub>A</sub>	Operating free-air temperature		-55		125	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS <sup>†</sup>			SN54S74			SN74S74			UNIT
	MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA,				-1.2			-1.2		V
V <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -1 mA			2.5	3.4		2.7	3.4		V
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 20 mA				0.5			0.5		V
I <sub>I</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V				1			1		mA
I <sub>IH</sub>	D	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V			50			50		μA
	CLR		150			150				
	PRE or CLK		100			100				
I <sub>IL</sub>	D	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5 V			-2			-2		mA
	CLR <sup>§</sup>		-6			-6				
	PRE <sup>§</sup>		-4			-4				
	CLK		-4			-4				
I <sub>OS</sub> <sup>§</sup>	V <sub>CC</sub> = MAX			-40	-100		-40	-100		mA
I <sub>CC</sub> <sup>#</sup>	V <sub>CC</sub> = MAX, See Note 2				15	25		15	25	mA

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup>All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

<sup>§</sup>Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

<sup>¶</sup>Clear is tested with preset high and preset is tested with clear high.

<sup>#</sup>Average per flip-flop.

NOTE 2: With all outputs open, I<sub>CC</sub> is measured with the Q and  $\bar{Q}$  outputs high in turn. At the time of measurement, the clock input is grounded.

**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN TYP MAX			UNIT
				75	110	MHz	
f <sub>max</sub>				4	6	ns	
t <sub>PLH</sub>	PRE or CLR	Q or $\bar{Q}$		9	13.5	ns	
t <sub>PHL</sub>	PRE or CLR (CLK high)	$\bar{Q}$ or Q	R <sub>L</sub> = 280 Ω, C <sub>L</sub> = 15 pF	5	8		ns
	PRE or CLR (CLK low)	Q or $\bar{Q}$		6	9	ns	
t <sub>PLH</sub>	CLK	Q or $\bar{Q}$		6	9	ns	
t <sub>PHL</sub>							

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
JM38510/07101BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/07101BCA	Samples
JM38510/07101BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/07101BDA	Samples
JM38510/07101BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/07101BDA	Samples
JM38510/30102B2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30102B2A	Samples
JM38510/30102B2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30102B2A	Samples
JM38510/30102BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30102BCA	Samples
JM38510/30102BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30102BCA	Samples
JM38510/30102BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30102BDA	Samples
JM38510/30102BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30102BDA	Samples
JM38510/30102SCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30102SCA	Samples
JM38510/30102SCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30102SCA	Samples
JM38510/30102SDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30102SDA	Samples
JM38510/30102SDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30102SDA	Samples
M38510/07101BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/07101BCA	Samples
M38510/07101BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/07101BCA	Samples
M38510/07101BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/07101BDA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
M38510/07101BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/07101BDA	Samples
M38510/30102B2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30102B2A	Samples
M38510/30102B2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30102B2A	Samples
M38510/30102BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30102BCA	Samples
M38510/30102BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30102BCA	Samples
M38510/30102BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30102BDA	Samples
M38510/30102BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30102BDA	Samples
M38510/30102SCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30102SCA	Samples
M38510/30102SCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30102SCA	Samples
M38510/30102SDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30102SDA	Samples
M38510/30102SDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30102SDA	Samples
SN54LS74AJ	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS74AJ	Samples
SN54LS74AJ	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS74AJ	Samples
SN54S74J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54S74J	Samples
SN54S74J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54S74J	Samples
SN74LS74AD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70	LS74A	
SN74LS74AD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70	LS74A	
SN74LS74ADBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS74A	Samples
SN74LS74ADBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS74A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS74ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS74A	Samples
SN74LS74ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS74A	Samples
SN74LS74ADRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS74A	Samples
SN74LS74ADRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS74A	Samples
SN74LS74AN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS74AN	Samples
SN74LS74AN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS74AN	Samples
SN74LS74ANE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS74AN	Samples
SN74LS74ANE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS74AN	Samples
SN74LS74ANSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS74A	Samples
SN74LS74ANSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS74A	Samples
SN74LS74ANSRG4	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS74A	Samples
SN74LS74ANSRG4	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS74A	Samples
SN74S74D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	S74	Samples
SN74S74D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	S74	Samples
SN74S74N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74S74N	Samples
SN74S74N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74S74N	Samples
SNJ54LS74AFK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS 74AFK	Samples
SNJ54LS74AFK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS 74AFK	Samples
SNJ54LS74AJ	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS74AJ	Samples
SNJ54LS74AJ	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS74AJ	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54LS74AW	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS74AW	Samples
SNJ54LS74AW	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS74AW	Samples
SNJ54S74J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54S74J	Samples
SNJ54S74J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54S74J	Samples
SNJ54S74W	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54S74W	Samples
SNJ54S74W	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54S74W	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

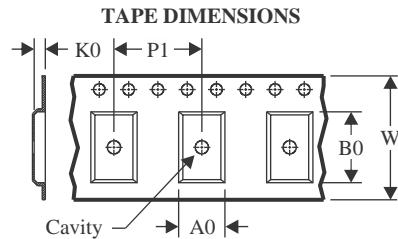
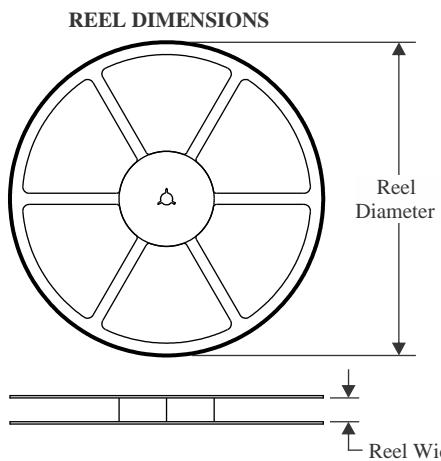
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LS74A, SN54LS74A-SP, SN54S74, SN74LS74A, SN74S74 :**

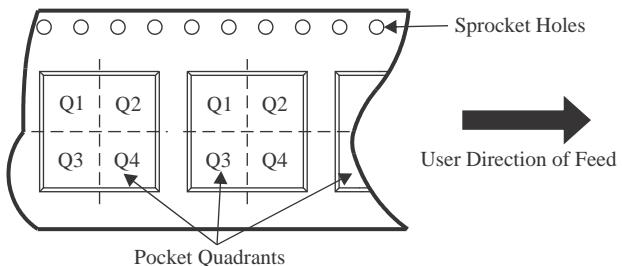
- Catalog : [SN74LS74A](#), [SN54LS74A](#), [SN74S74](#)
- Military : [SN54LS74A](#), [SN54S74](#)
- Space : [SN54LS74A-SP](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

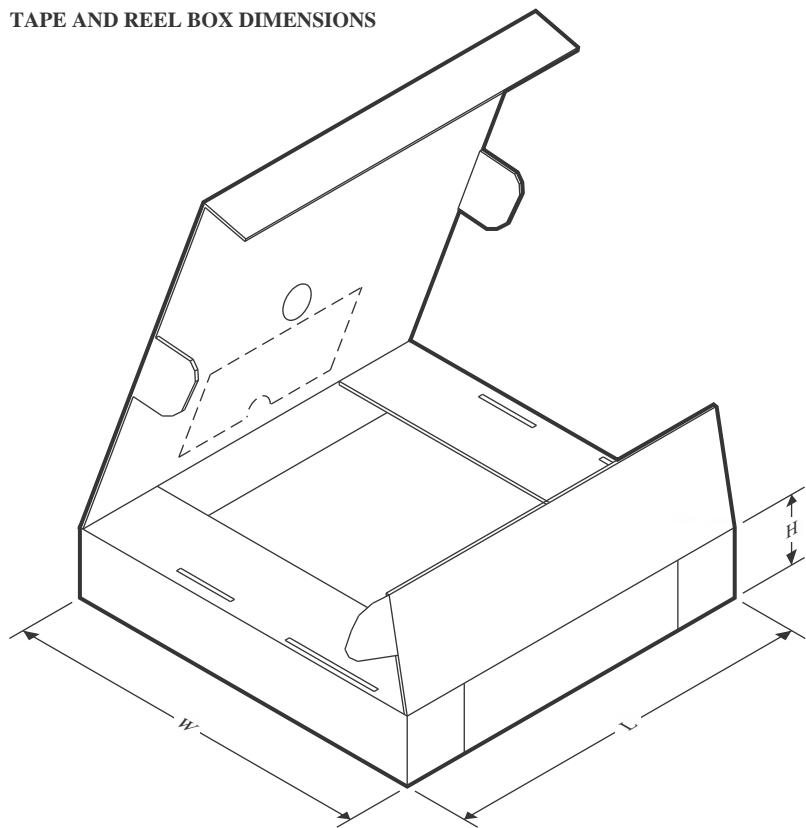
**TAPE AND REEL INFORMATION**

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

\*All dimensions are nominal

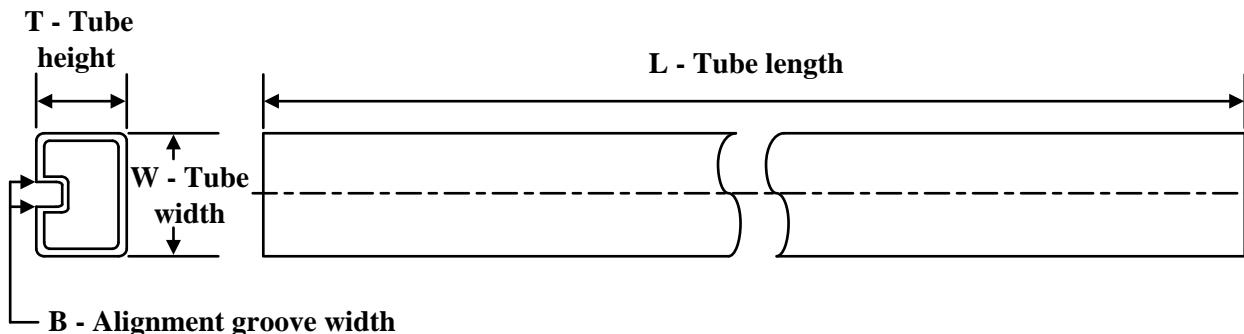
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS74ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LS74ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS74ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS74ADBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74LS74ADR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LS74ANSR	SO	NS	14	2000	367.0	367.0	38.0

## TUBE



\*All dimensions are nominal

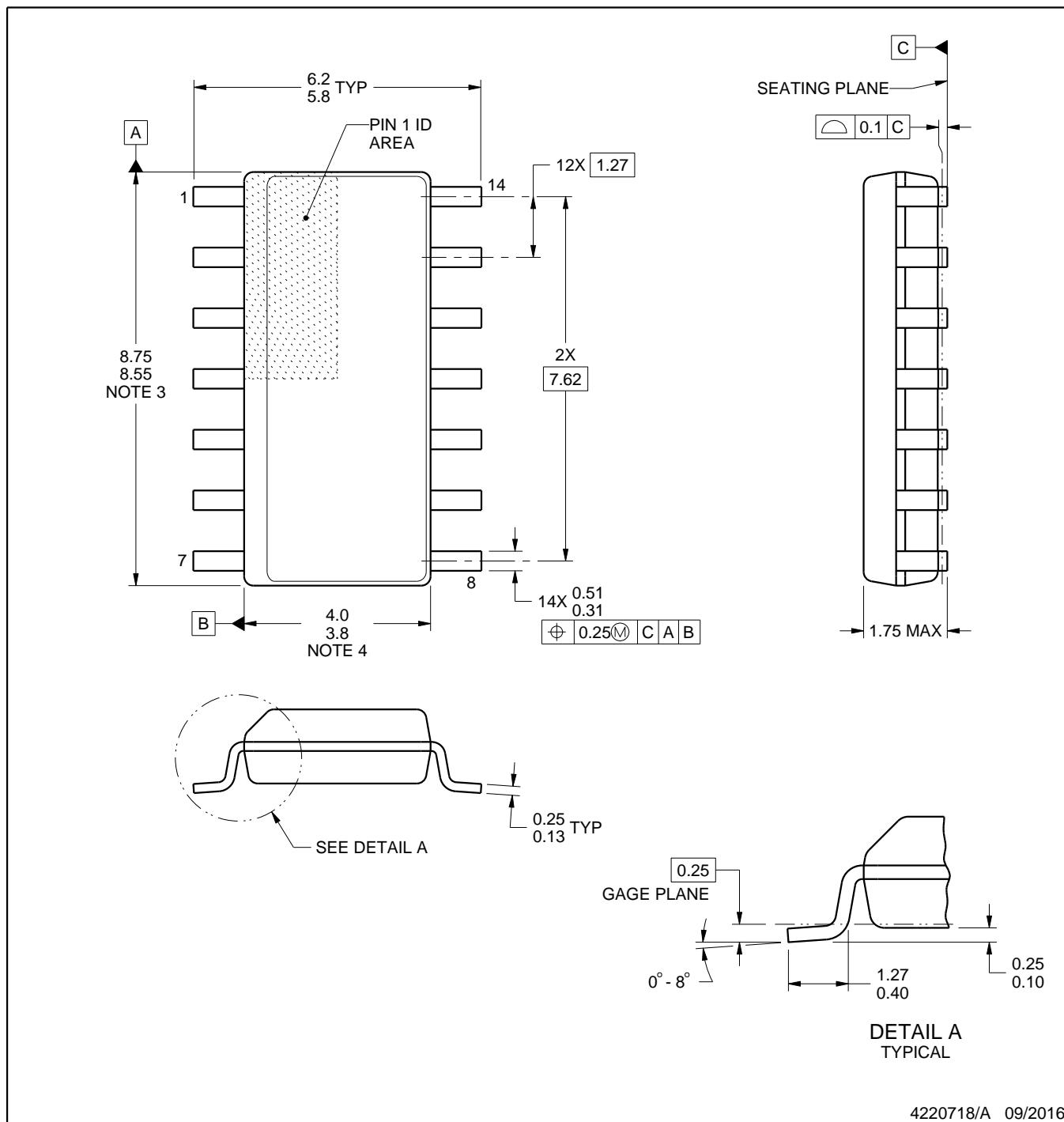
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T ( $\mu$ m)	B (mm)
JM38510/07101BDA	W	CFP	14	25	506.98	26.16	6220	NA
JM38510/30102B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/30102BDA	W	CFP	14	25	506.98	26.16	6220	NA
JM38510/30102SDA	W	CFP	14	25	506.98	26.16	6220	NA
M38510/07101BDA	W	CFP	14	25	506.98	26.16	6220	NA
M38510/30102B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/30102BDA	W	CFP	14	25	506.98	26.16	6220	NA
M38510/30102SDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74LS74AN	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS74AN	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS74ANE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS74ANE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74S74D	D	SOIC	14	50	506.6	8	3940	4.32
SN74S74N	N	PDIP	14	25	506	13.97	11230	4.32
SN74S74N	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54LS74AFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS74AW	W	CFP	14	25	506.98	26.16	6220	NA
SNJ54S74W	W	CFP	14	25	506.98	26.16	6220	NA

# PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

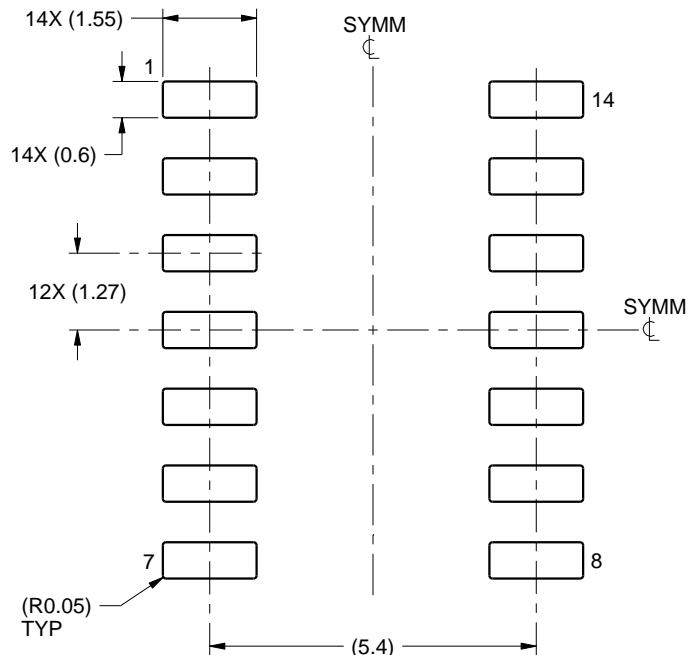
- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

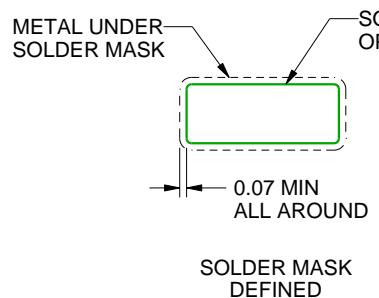
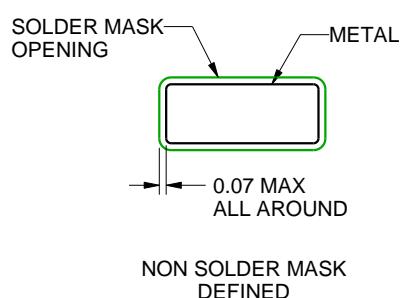
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

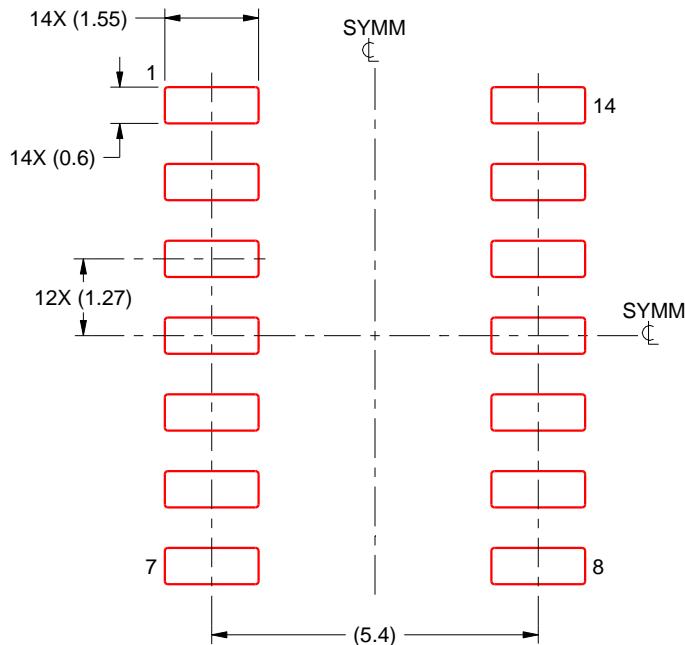
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

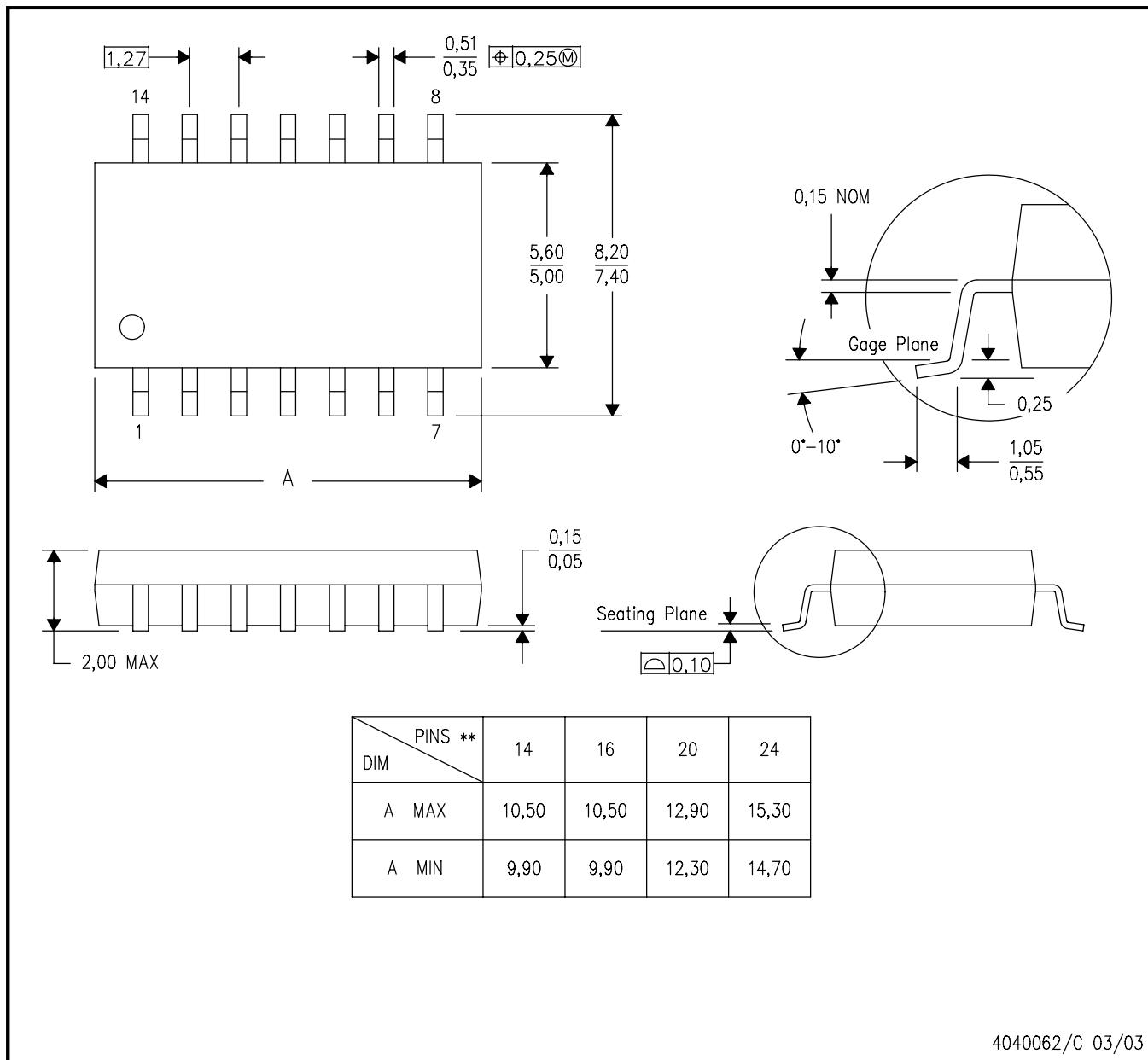
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

**14-PINS SHOWN**

**PLASTIC SMALL-OUTLINE PACKAGE**

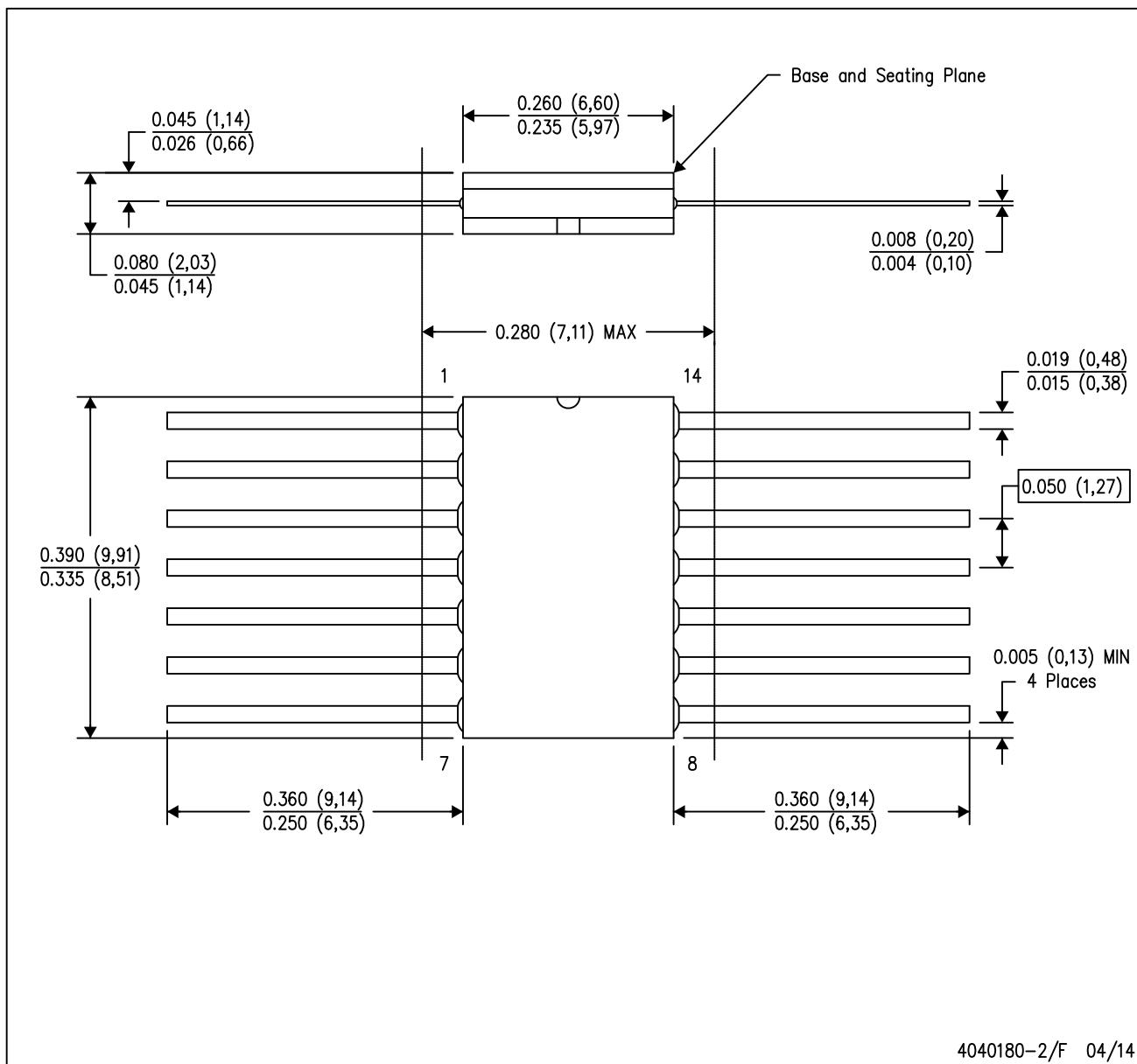


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## MECHANICAL DATA

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK

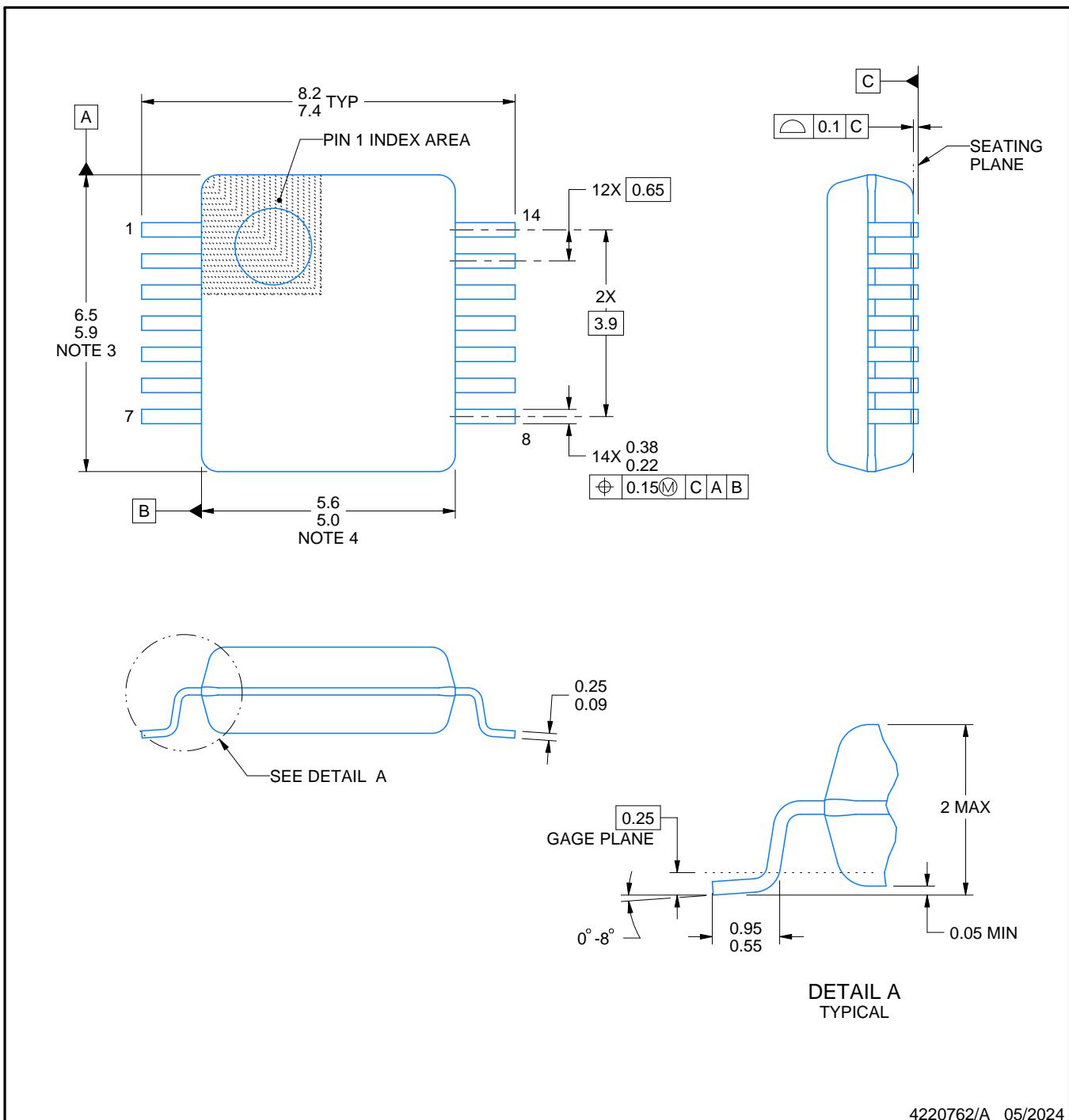


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14

# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



### NOTES:

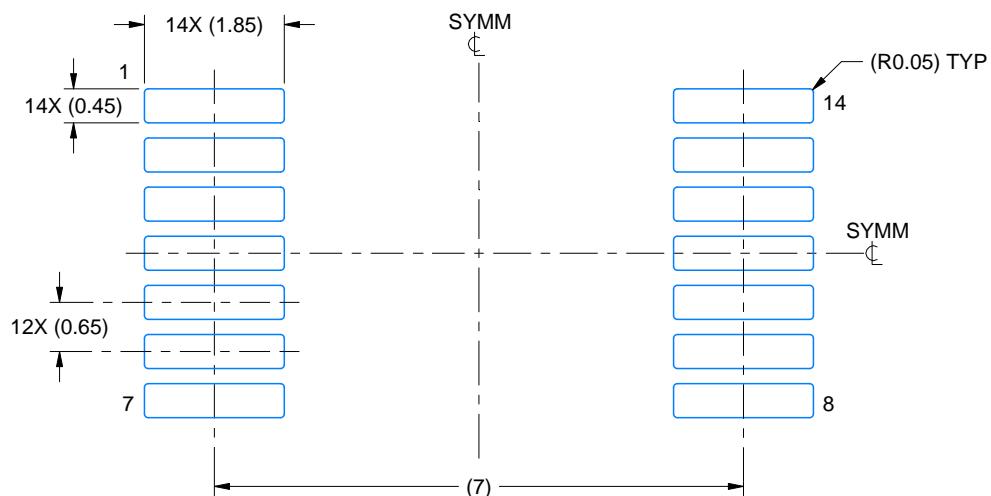
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

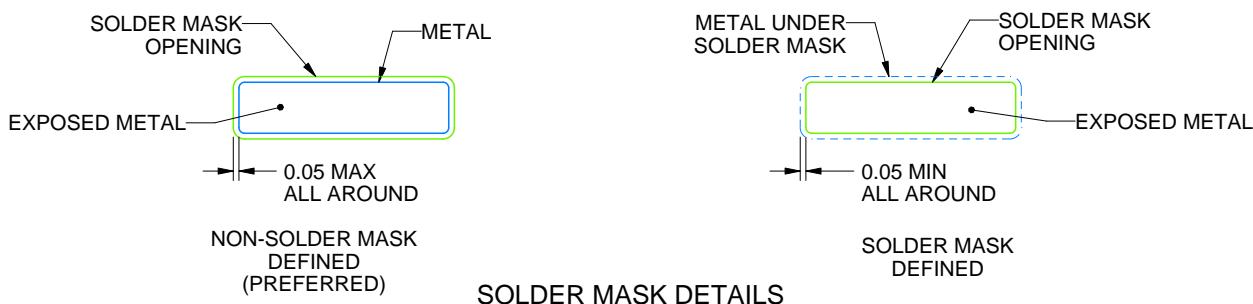
DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220762/A 05/2024

NOTES: (continued)

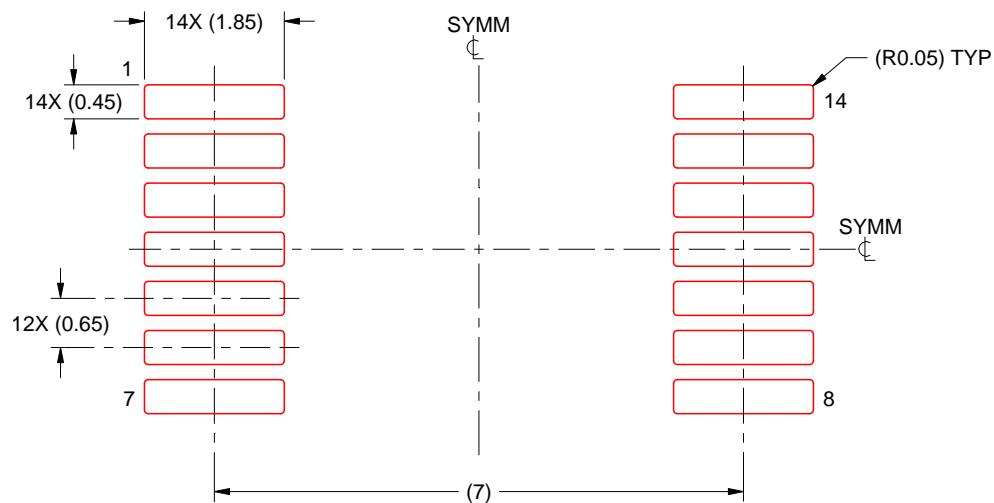
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

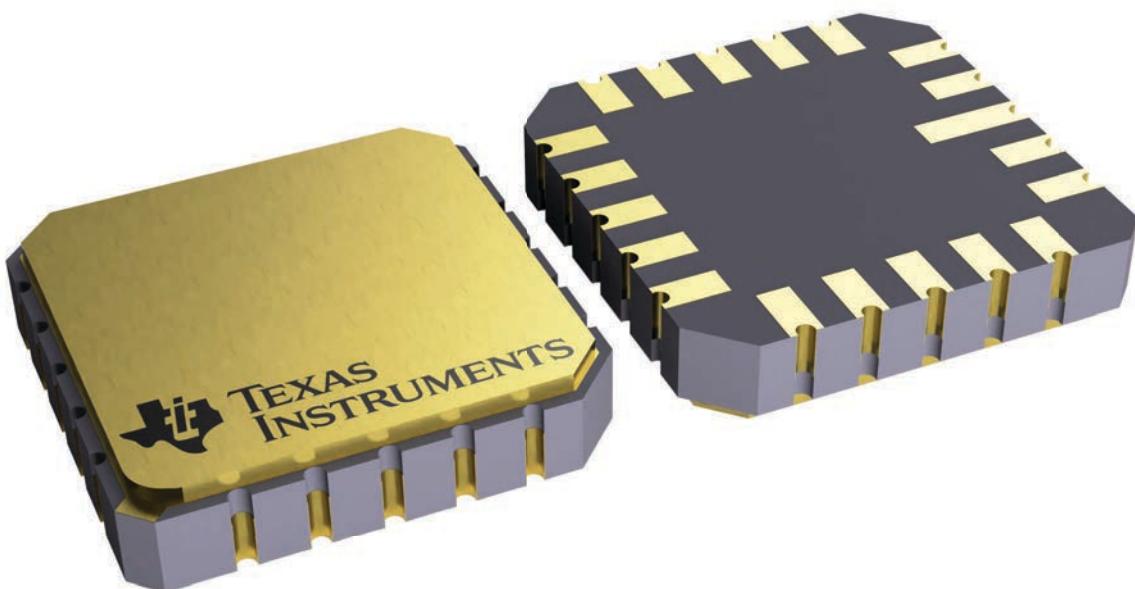
**FK 20**

**LCCC - 2.03 mm max height**

**8.89 x 8.89, 1.27 mm pitch**

**LEADLESS CERAMIC CHIP CARRIER**

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



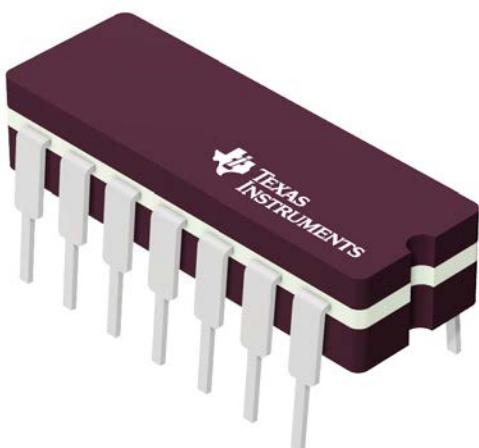
4229370VA\

# GENERIC PACKAGE VIEW

J 14

**CDIP - 5.08 mm max height**

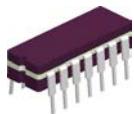
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

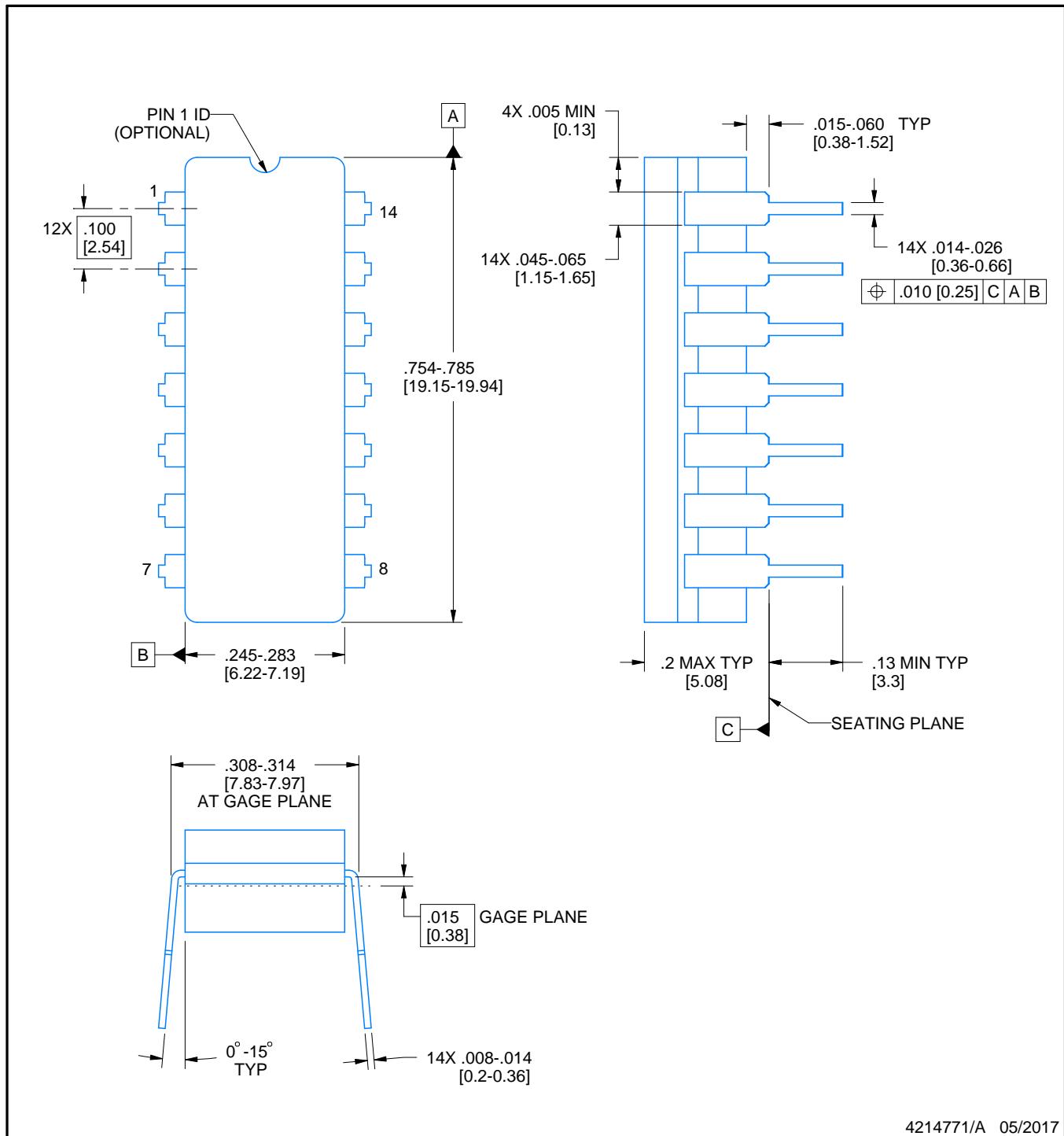
J0014A



# PACKAGE OUTLINE

## CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

### NOTES:

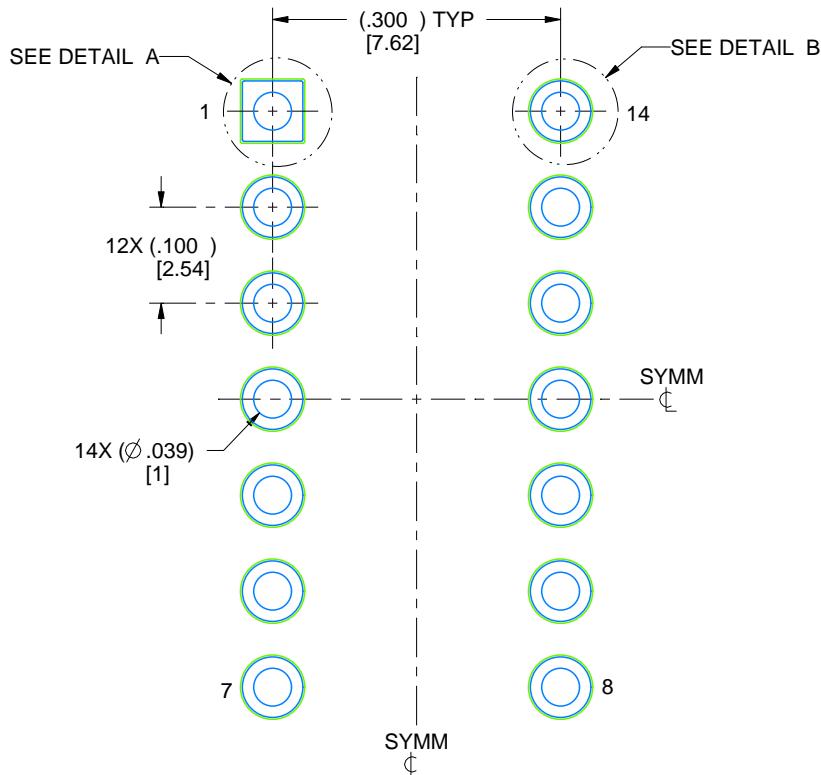
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

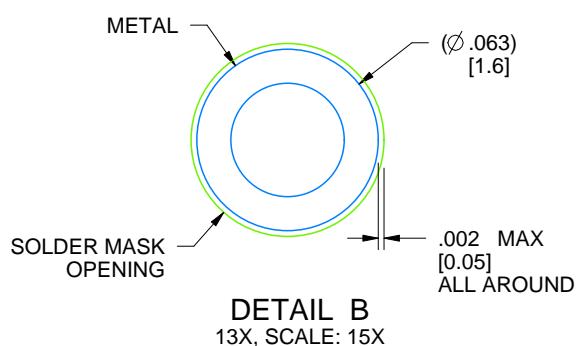
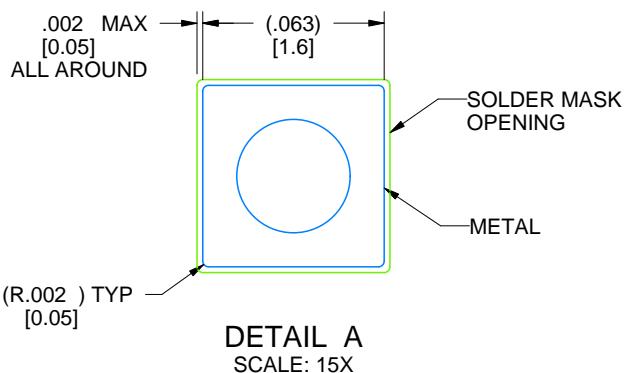
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X

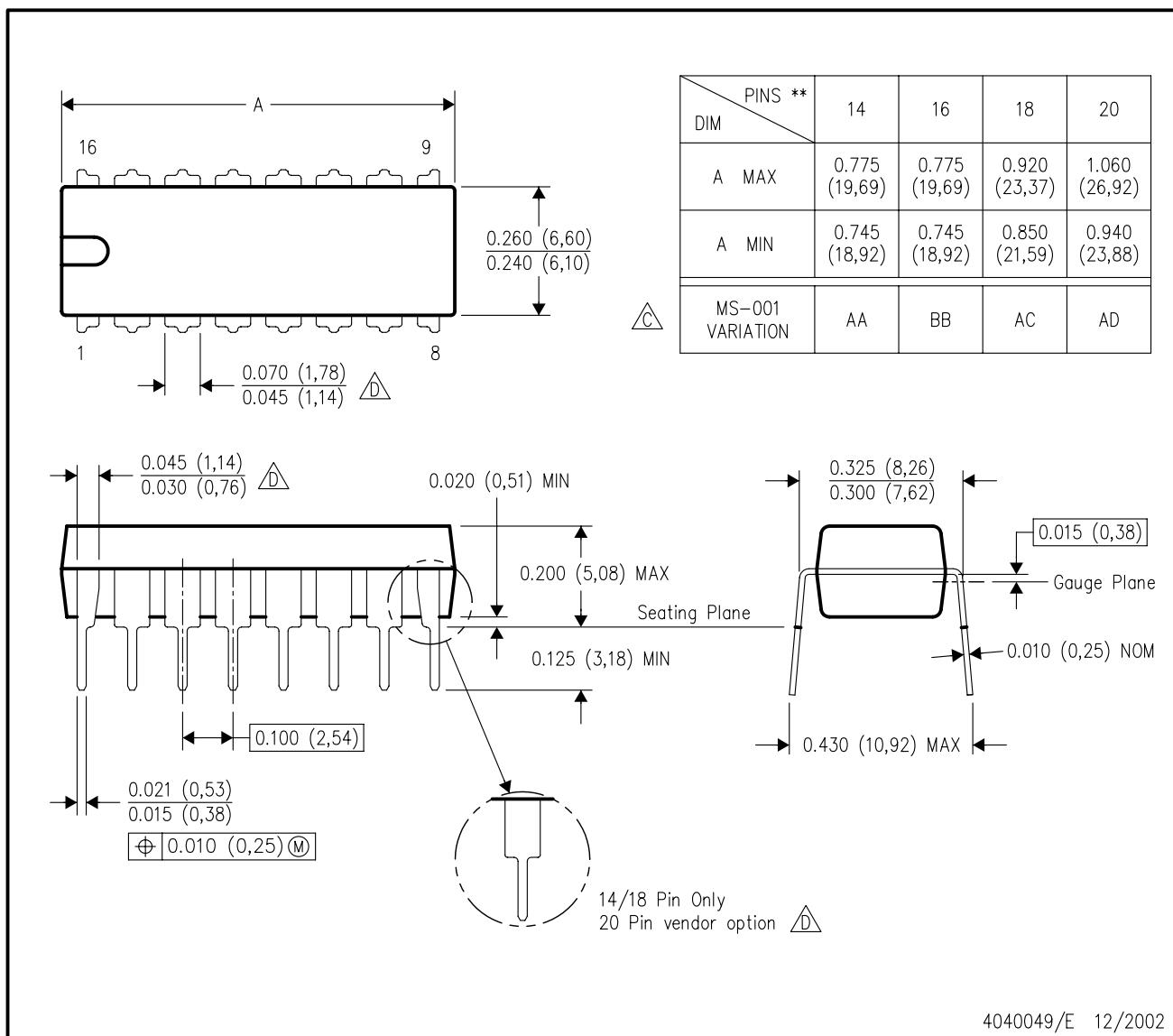


4214771/A 05/2017

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



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**SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93  
SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93  
DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS**

SDLS940A - MARCH 1974 - REVISED MARCH 1988

- '90A, 'LS90 . . . Decade Counters
- '92A, 'LS92 . . . Divide By-Twelve Counters
- '93A, 'LS93 . . . 4-Bit Binary Counters

TYPES	TYPICAL POWER DISSIPATION
'90A	145 mW
'92A, '93A	130 mW
'LS90, 'LS92, 'LS93	45 mW

#### description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '90A and 'LS90, divide-by-six for the '92A and 'LS92, and the divide-by-eight for the '93A and 'LS93.

All of these counters have a gated zero reset and the '90A and 'LS90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

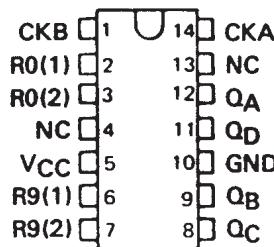
To use their maximum count length (decade, divide-by-twelve, or four-bit binary) of these counters, the CKB input is connected to the QA output. The input count pulses are applied to CKA input and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '90A or 'LS90 counters by connecting the QD output to the CKA input and applying the input count to the CKB input which gives a divide-by-ten square wave at output QA.

**SN5490A, SN54LS90 . . . J OR W PACKAGE**

**SN7490A . . . N PACKAGE**

**SN74LS90 . . . D OR N PACKAGE**

(TOP VIEW)

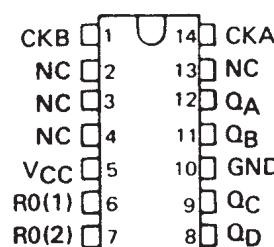


**SN5492A, SN54LS92 . . . J OR W PACKAGE**

**SN7492A . . . N PACKAGE**

**SN74LS92 . . . D OR N PACKAGE**

(TOP VIEW)

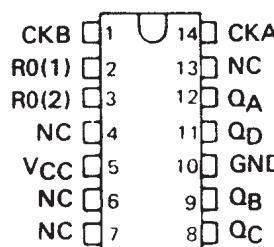


**SN5493A, SN54LS93 . . . J OR W PACKAGE**

**SN7493 . . . N PACKAGE**

**SN74LS93 . . . D OR N PACKAGE**

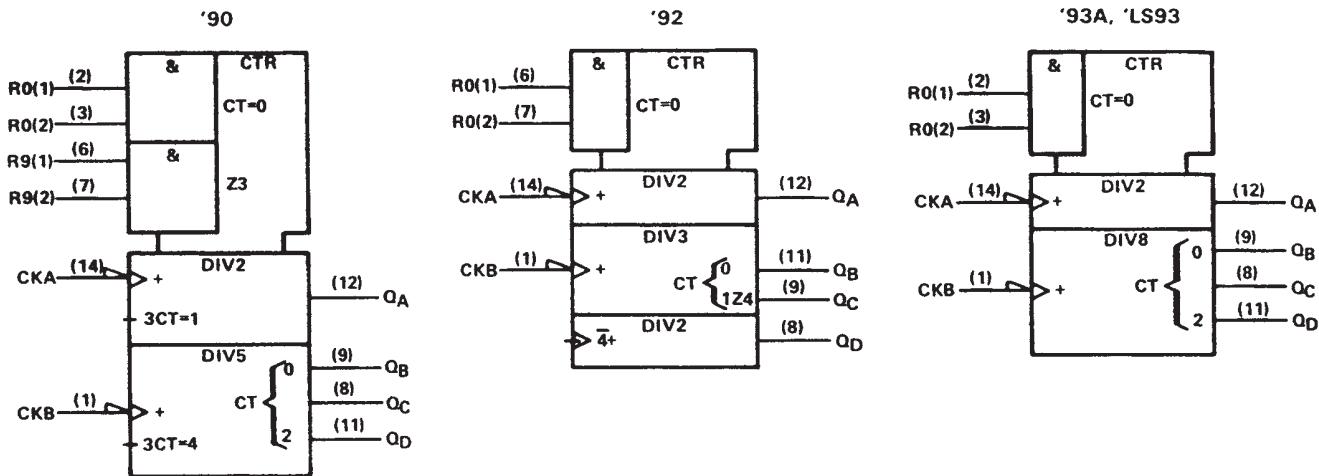
(TOP VIEW)



**SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93  
 SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93  
 DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS**

SDLS940A – MARCH 1974 – REVISED MARCH 1988

**logic symbols<sup>†</sup>**



<sup>†</sup>These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

**SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93  
SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93  
DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS**

SDLS940A - MARCH 1974 - REVISED MARCH 1988

'90A, 'LS90  
BCD COUNT SEQUENCE  
(See Note A)

COUNT	OUTPUT			
	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

'90A, 'LS90  
BI-QUINARY (5-2)  
(See Note B)

COUNT	OUTPUT			
	Q <sub>A</sub>	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

'92A, 'LS92  
COUNT SEQUENCE  
(See Note C)

COUNT	OUTPUT			
	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

'90A, 'LS90  
RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT
R <sub>0(1)</sub>	R <sub>0(2)</sub>	R <sub>9(1)</sub>	R <sub>9(2)</sub>	Q <sub>D</sub> Q <sub>C</sub> Q <sub>B</sub> Q <sub>A</sub>
H	H	L	X	L L L L
H	H	X	L	L L L L
X	X	H	H	H L L H
X	L	X	L	COUNT
L	X	L	X	COUNT
L	X	X	L	COUNT
X	L	L	X	COUNT

'92A, 'LS92, '93A, 'LS93  
RESET/COUNT FUNCTION TABLE

RESET INPUTS		OUTPUT
R <sub>0(1)</sub>	R <sub>0(2)</sub>	Q <sub>D</sub> Q <sub>C</sub> Q <sub>B</sub> Q <sub>A</sub>
H	H	L L L L
L	X	COUNT
X	L	COUNT

- NOTES: A. Output Q<sub>A</sub> is connected to input CKB for BCD count.  
B. Output Q<sub>D</sub> is connected to input CKA for bi-quinary count.  
C. Output Q<sub>A</sub> is connected to input CKB.  
D. H = high level, L = low level, X = irrelevant

'93A, 'LS93  
COUNT SEQUENCE  
(See Note C)

COUNT	OUTPUT			
	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

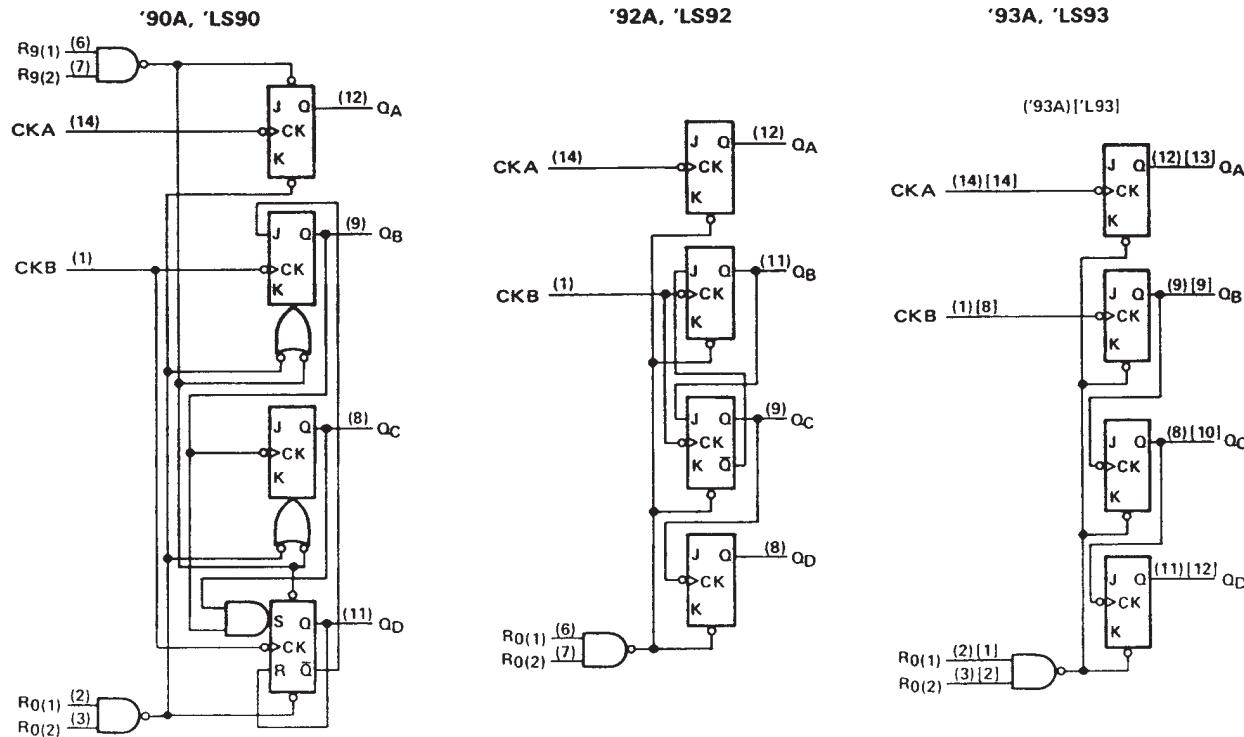


POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93  
SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93  
DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS**

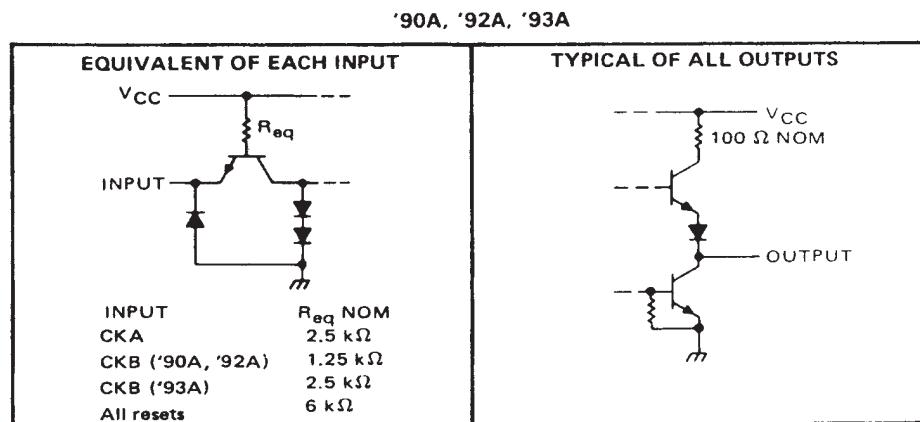
SDLS940A – MARCH 1974 – REVISED MARCH 1988

**logic diagrams (positive logic)**



The J and K inputs shown without connection are for reference only and are functionally at a high level.  
Pin numbers shown in () are for the 'LS93 and '93A and pin numbers shown in [ ] are for the 54L93.

**schematics of inputs and outputs**

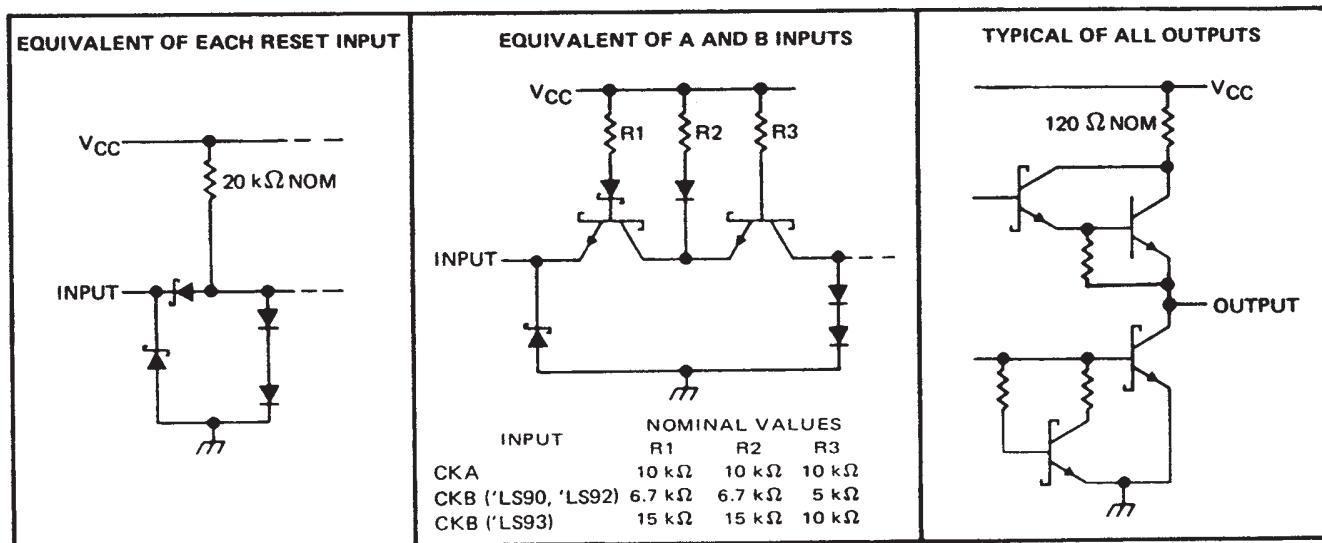


**SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93  
 SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93  
 DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS**

SDLS940A – MARCH 1974 – REVISED MARCH 1988

**schematics of inputs and outputs (continued)**

'LS90, 'LS92, 'LS93



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93  
SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93  
DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS**

SDLS940A – MARCH 1974 – REVISED MARCH 1988

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, $V_{CC}$ (see Note 1)	7 V					
Input voltage	5.5 V					
Interemitter voltage (see Note 2)	5.5 V					
Operating free-air temperature range: SN5490A, SN5492A, SN5493A	–55°C to 125°C					
SN7490A, SN7492A, SN7493A	0°C to 70°C					
Storage temperature range	–65°C to 150°C					

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.

2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the two  $R_O$  inputs, and for the '90A circuit, it also applies between the two  $R_g$  inputs.

**recommended operating conditions**

		SN5490A, SN5492A			SN7490A, SN7492A			UNIT	
		SN5493A			SN7493A				
		MIN	NOM	MAX	MIN	NOM	MAX		
Supply voltage, $V_{CC}$		4.5	5	5.5	4.75	5	5.25	V	
High-level output current, $I_{OH}$				–800			–800	$\mu A$	
Low-level output current, $I_{OL}$				16			16	mA	
Count frequency, $f_{count}$ (see Figure 1)	A input	0	32	0	32			MHz	
	B input	0	16	0	16				
Pulse width, $t_w$	A input	15			15			ns	
	B input	30			30				
	Reset inputs	15			15				
Reset inactive-state setup time, $t_{su}$		25			25			ns	
Operating free-air temperature, $T_A$	–55		125	0	70			°C	

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER <sup>†</sup>	TEST CONDITIONS <sup>†</sup>	'90A			'92A			'93A			UNIT
		MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
$V_{IH}$ High-level input voltage		2			2			2			V
$V_{IL}$ Low-level input voltage			0.8			0.8			0.8		V
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			–1.5			–1.5			–1.5	V
$V_{OH}$ High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu A$	2.4	3.4		2.4	3.4		2.4	3.4		V
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}^{\$}$		0.2	0.4		0.2	0.4		0.2	0.4	V
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1			1	mA
$I_{IH}$ High-level input current	Any reset			40			40			40	$\mu A$
	CKA			80			80			80	
	CKB			120			120			80	
$I_{IL}$ Low-level input current	Any reset			–1.6			–1.6			–1.6	mA
	CKA			–3.2			–3.2			–3.2	
	CKB			–4.8			–4.8			–3.2	
$I_{OS}$ Short-circuit output current <sup>§</sup>		$V_{CC} = \text{MAX}$	SN54'	–20	–57	–20	–57	–20	–57	–57	mA
			SN74'	–18	–57	–18	–57	–18	–57	–57	
$I_{CC}$ Supply current	$V_{CC} = \text{MAX}$ , See Note 3		29	42		26	39		26	39	mA

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup> All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$ .

<sup>§</sup> Not more than one output should be shorted at a time.

<sup>¶</sup>  $I_Q$  outputs are tested at  $I_{OL} = 16 \text{ mA}$  plus the limit value for  $I_{IL}$  for the CKB input. This permits driving the CKB input while maintaining full fan-out capability.

NOTE 3:  $I_{CC}$  is measured with all outputs open, both  $R_O$  inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93  
SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93  
DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS**

SDLS940A – MARCH 1974 – REVISED MARCH 1988

switching characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER <sup>†</sup>	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'90A			'92A			'93A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$f_{max}$	CKA	Q <sub>A</sub>	$C_L = 15 \text{ pF}$ , $R_L = 400 \Omega$ , See Figure 1	32	42		32	42		32	42		MHz
	CKB	Q <sub>B</sub>		16			16			16			
	t <sub>PLH</sub>	CKA		10	16		10	16		10	16		ns
	t <sub>PHL</sub>	CKA		12	18		12	18		12	18		
	t <sub>PLH</sub>	CKA		32	48		32	48		46	70		ns
	t <sub>PHL</sub>	CKA		34	50		34	50		46	70		
	t <sub>PLH</sub>	CKB		10	16		10	16		10	16		ns
	t <sub>PHL</sub>	CKB		14	21		14	21		14	21		
	t <sub>PLH</sub>	CKB		21	32		10	16		21	32		ns
	t <sub>PHL</sub>	CKB		23	35		14	21		23	35		
$t_{PLH}$	CKB	Q <sub>D</sub>		21	32		21	32		34	51		ns
	t <sub>PHL</sub>	CKB		23	35		23	35		34	51		
	t <sub>PLH</sub>	Set-to-0	Any	26	40		26	40		26	40		ns
	t <sub>PHL</sub>	Set-to-9	Q <sub>A</sub> , Q <sub>D</sub>	20	30								ns
t <sub>PHL</sub>			Q <sub>B</sub> , Q <sub>C</sub>	26	40								ns

<sup>†</sup> $f_{max}$  = maximum count frequency

$t_{PLH}$  = propagation delay time, low-to-high-level output

$t_{PHL}$  = propagation delay time, high-to-low-level output



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**SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93  
SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93  
DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS**

SDLS940A – MARCH 1974 – REVISED MARCH 1988

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V <sub>CC</sub> (see Note 1)				7 V		
Input voltage: R inputs				7 V		
A and B inputs				5.5 V		
Operating free-air temperature range: SN54LS' Circuits				–55°C to 125°C		
SN74LS' Circuits				0°C to 70°C		
Storage temperature range				–65°C to 150°C		

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS90			SN74LS90			UNIT	
		SN54LS92			SN74LS92				
		SN54LS93			SN74LS93				
		MIN	NOM	MAX	MIN	NOM	MAX		
Supply voltage, V <sub>CC</sub>		4.5	5	5.5	4.75	5	5.25	V	
High-level output current, I <sub>OH</sub>				–400			–400	μA	
Low-level output current, I <sub>OL</sub>				4			8	mA	
Count frequency, f <sub>count</sub> (see Figure 1)	A input	0	32	0	32			MHz	
	B input	0	16	0	16				
Pulse width, t <sub>w</sub>	A input	15		15				ns	
	B input	30		30					
	Reset inputs	30		30					
Reset inactive-state setup time, t <sub>su</sub>		25		25				ns	
Operating free-air temperature, T <sub>A</sub>		–55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>†</sup>	SN54LS90			SN74LS90			UNIT
			MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
V <sub>IH</sub> High-level input voltage			2			2			V
V <sub>IL</sub> Low-level input voltage				0.7			0.8		V
V <sub>IK</sub> Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = –18 mA			–1.5			–1.5		V
V <sub>OH</sub> High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>IL</sub> max, I <sub>OH</sub> = –400 μA		2.5	3.4		2.7	3.4		V
V <sub>OL</sub> Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 4 mA <sup>¶</sup> V <sub>IL</sub> = V <sub>IL</sub> max, I <sub>OL</sub> = 8 mA <sup>¶</sup>		0.25	0.4		0.25	0.4		V
I <sub>I</sub> Input current at maximum input voltage	Any reset	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V		0.1			0.1		
	CKA	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V		0.2			0.2		
	CKB			0.4			0.4		
I <sub>IIH</sub> High-level input current	Any reset	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V		20			20		μA
	CKA			40			40		
	CKB			80			80		
I <sub>IIL</sub> Low-level input current	Any reset	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V		–0.4			–0.4		mA
	CKA			–2.4			–2.4		
	CKB			–3.2			–3.2		
I <sub>OS</sub> Short-circuit output current <sup>§</sup>	V <sub>CC</sub> = MAX		–20	–100		–20	–100		mA
I <sub>CC</sub> Supply current	V <sub>CC</sub> = MAX, See Note 3	'LS90		9	15		9	15	mA
		'LS92		9	15		9	15	

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup>All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

<sup>¶</sup>Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

<sup>§</sup>Q<sub>A</sub> outputs are tested at specified I<sub>OL</sub> plus the limit value of I<sub>IIL</sub> for the CKB input. This permits driving the CKB input while maintaining full fan-out capability.

NOTE 3: I<sub>CC</sub> is measured with all outputs open, both R<sub>O</sub> inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93  
SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93  
DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS**

SDLS940A – MARCH 1974 – REVISED MARCH 1988

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>†</sup>	SN54LS93			SN74LS93			UNIT
		MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
V <sub>IH</sub> High-level input voltage		2			2			V
V <sub>IL</sub> Low-level input voltage				0.7			0.8	V
V <sub>IK</sub> Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA			-1.5			-1.5	V
V <sub>OH</sub> High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>IL</sub> max, I <sub>OH</sub> = -400 μA	2.5	3.4		2.7	3.4		V
V <sub>OL</sub> Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>IL</sub> max	I <sub>OL</sub> = 4 mA <sup>§</sup>	0.25	0.4	0.25	0.4		V
		I <sub>OL</sub> = 8 mA <sup>§</sup>			0.35	0.5		
I <sub>I</sub> Input current at maximum input voltage	Any reset	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V			0.1		0.1	mA
	CKA or CKB	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V			0.2		0.2	
I <sub>IH</sub> High-level input current	Any reset	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V			20		20	μA
	CKA or CKB				40		80	
I <sub>IIL</sub> Low-level input current	Any reset	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V			-0.4		-0.4	mA
	CKA				-2.4		-2.4	
	CKB				-1.6		-1.6	
I <sub>OS</sub> Short-circuit output current <sup>§</sup>	V <sub>CC</sub> = MAX		-20	-100	-20	-100		mA
I <sub>CC</sub> Supply current	V <sub>CC</sub> = MAX, See Note 3		9	15	9	15		mA

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup>All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

<sup>§</sup>Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

<sup>¶</sup>Q<sub>A</sub> outputs are tested at specified I<sub>OL</sub> plus the limit value for I<sub>IIL</sub> for the CKB input. This permits driving the CKB input while maintaining full fan-out capability.

NOTE 3: I<sub>CC</sub> is measured with all outputs open, both R<sub>O</sub> inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER <sup>#</sup>	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS90			'LS92			'LS93			UNIT	
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
f <sub>max</sub>	CKA	Q <sub>A</sub>	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 kΩ See Figure 1	32	42		32	42		32	42		MHz	
	CKB	Q <sub>B</sub>		16			16			16				
t <sub>PLH</sub>	CKA	Q <sub>A</sub>		10	16		10	16		10	16		ns	
				12	18		12	18		12	18			
t <sub>PLH</sub>	CKA	Q <sub>D</sub>		32	48		32	48		46	70		ns	
				34	50		34	50		46	70			
t <sub>PLH</sub>	CKB	Q <sub>B</sub>		10	16		10	16		10	16		ns	
				14	21		14	21		14	21			
t <sub>PLH</sub>	CKB	Q <sub>C</sub>		21	32		10	16		21	32		ns	
				23	35		14	21		23	35			
t <sub>PLH</sub>	CKB	Q <sub>D</sub>		21	32		21	32		34	51		ns	
				23	35		23	35		34	51			
t <sub>PHL</sub>	Set-to-0	Any		26	40		26	40		26	40		ns	
t <sub>PLH</sub>	Set-to-9	Q <sub>A</sub> , Q <sub>D</sub>		20	30								ns	
		Q <sub>B</sub> , Q <sub>C</sub>		26	40									

#f<sub>max</sub> = maximum count frequency

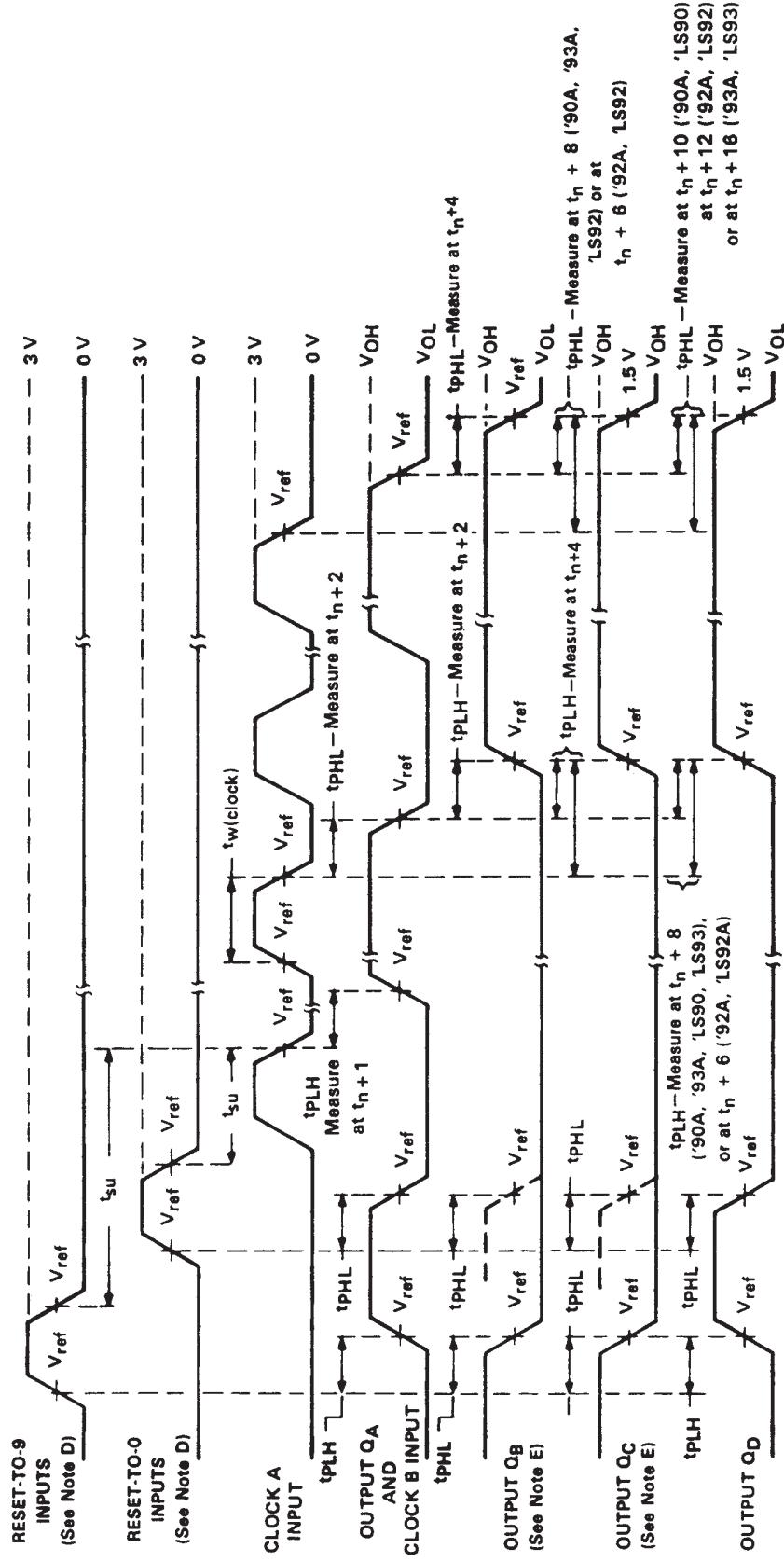
t<sub>PLH</sub> = propagation delay time, low-to-high-level output

t<sub>PHL</sub> = propagation delay time, high-to-low-level output

SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93  
 SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93  
**DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS**

SDLS940A – MARCH 1974 – REVISED MARCH 1988

**PARAMETER MEASUREMENT INFORMATION**



NOTES: A. Input pulses are supplied by a generator having the following characteristics:

for '90A, '92A, '93A, 'LS92, 'LS93,  $t_r \leq 5$  ns,  $t_f \leq 5$  ns, PRR = 1 MHz, duty cycle = 50%,  $Z_{out} \approx 50$  ohms;

for 'LS90, 'LS92, 'LS93,  $t_r \leq 15$  ns,  $t_f \leq 5$  ns, PRR = 1 MHz, duty cycle = 50%,  $Z_{out} \approx 50$  ohms.

B.  $C_L$  includes probe and jig capacitance.

C. All diodes are 1N3064 or equivalent.

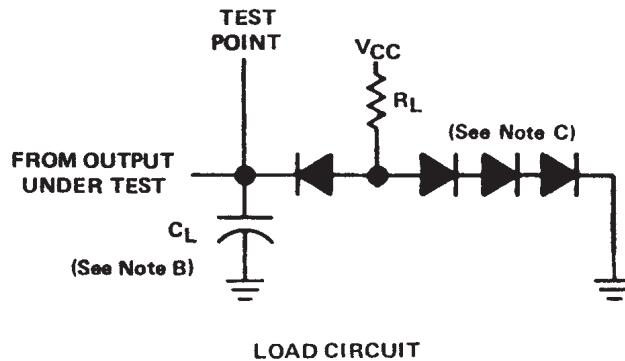
D. Each reset input is tested separately with the other reset at 4.5 V.

E. Reference waveforms are shown with dashed lines.

F. For '90A, '92A, and '93A;  $V_{ref} = 1.5$  V. For 'LS90, 'LS92, and 'LS93;  $V_{ref} = 1.3$  V.

**FIGURE 1A**

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. Input pulses are supplied by a generator having the following characteristics:  
 for '90A, '92A, '93A,  $t_r \leq 5$  ns,  $t_f \leq 5$  ns, PRR = 1 MHz, duty cycle = 50%,  $Z_{out} \approx 50$  ohms;  
 for 'LS90, 'LS92, 'LS93,  $t_r \leq 15$  ns,  $t_f \leq 5$  ns, PRR = 1 MHz, duty cycle = 50%,  $Z_{out} \approx 50$  ohms.
  - B.  $C_L$  includes probe and jig capacitance.
  - C. All diodes are 1N3064 or equivalent.
  - D. Each reset input is tested separately with the other reset at 4.5 V.
  - E. Reference waveforms are shown with dashed lines.
  - F. For '90A, '92A, and '93A;  $V_{ref} = 1.5$  V. For 'LS90, 'LS92, and 'LS93;  $V_{ref} = 1.3$  V.

FIGURE 1B

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
7603201CA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7603201CA SNJ54LS90J	Samples
7700101CA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7700101CA SNJ54LS93J	Samples
7700101DA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7700101DA SNJ54LS93W	Samples
JM38510/31501BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 31501BCA	Samples
JM38510/31502BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 31502BCA	Samples
JM38510/31502BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 31502BDA	Samples
M38510/31501BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 31501BCA	Samples
M38510/31502BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 31502BCA	Samples
M38510/31502BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 31502BDA	Samples
SN54LS90J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS90J	Samples
SN54LS93J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS93J	Samples
SN74LS90D	OBSOLETE	SOIC	D	14	TBD	RoHS & Green	Call TI	Call TI	0 to 70	LS90	
SN74LS90DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS90	Samples
SN74LS90N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS90N	Samples
SN74LS90NE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS90N	Samples
SN74LS92D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS92	Samples
SN74LS92N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS92N	Samples
SN74LS92NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS92	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS93D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS93	Samples
SN74LS93N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS93N	Samples
SNJ54LS90J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7603201CA SNJ54LS90J	Samples
SNJ54LS93J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7700101CA SNJ54LS93J	Samples
SNJ54LS93W	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7700101DA SNJ54LS93W	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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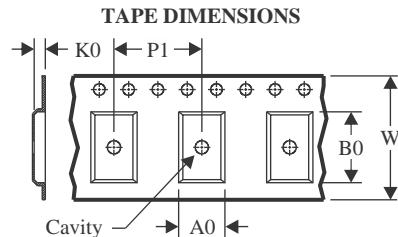
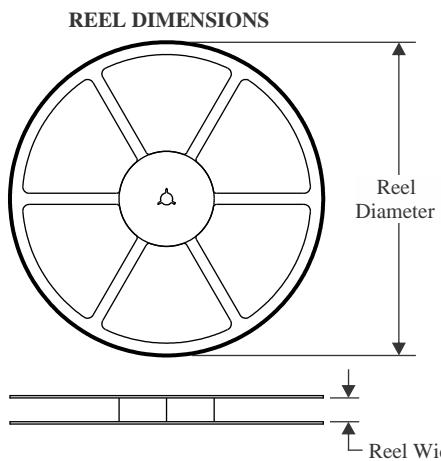
**OTHER QUALIFIED VERSIONS OF SN54LS90, SN54LS93, SN74LS90, SN74LS93 :**

- Catalog : [SN74LS90](#), [SN74LS93](#)
- Military : [SN54LS90](#), [SN54LS93](#)

NOTE: Qualified Version Definitions:

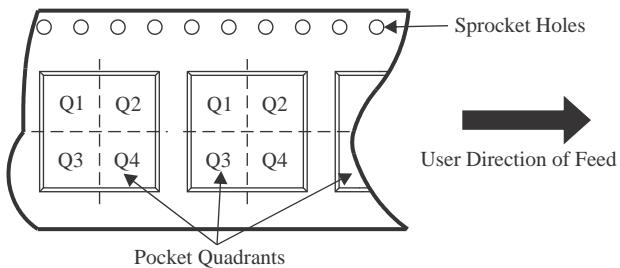
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



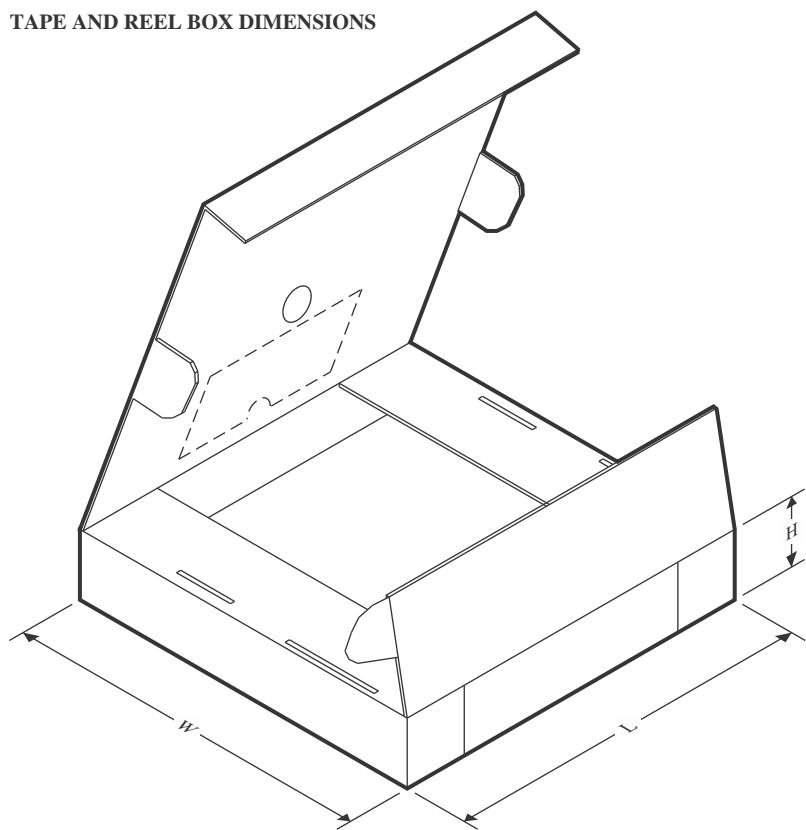
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



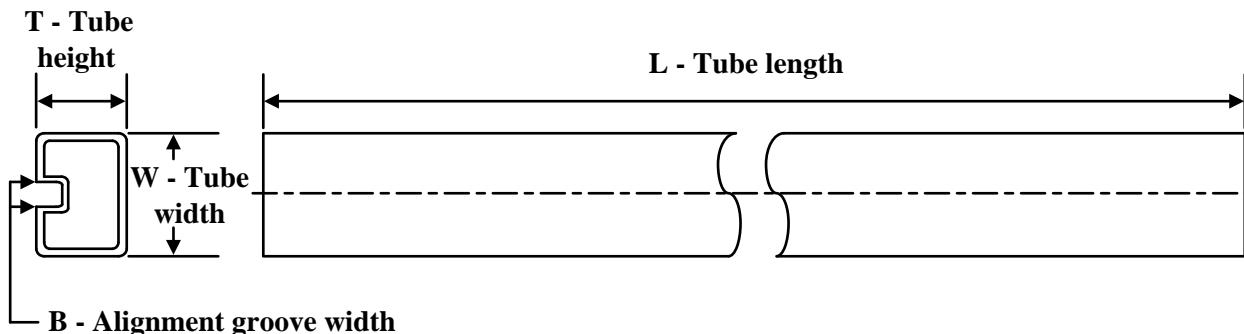
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS90DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS92NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS90DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LS92NSR	SO	NS	14	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

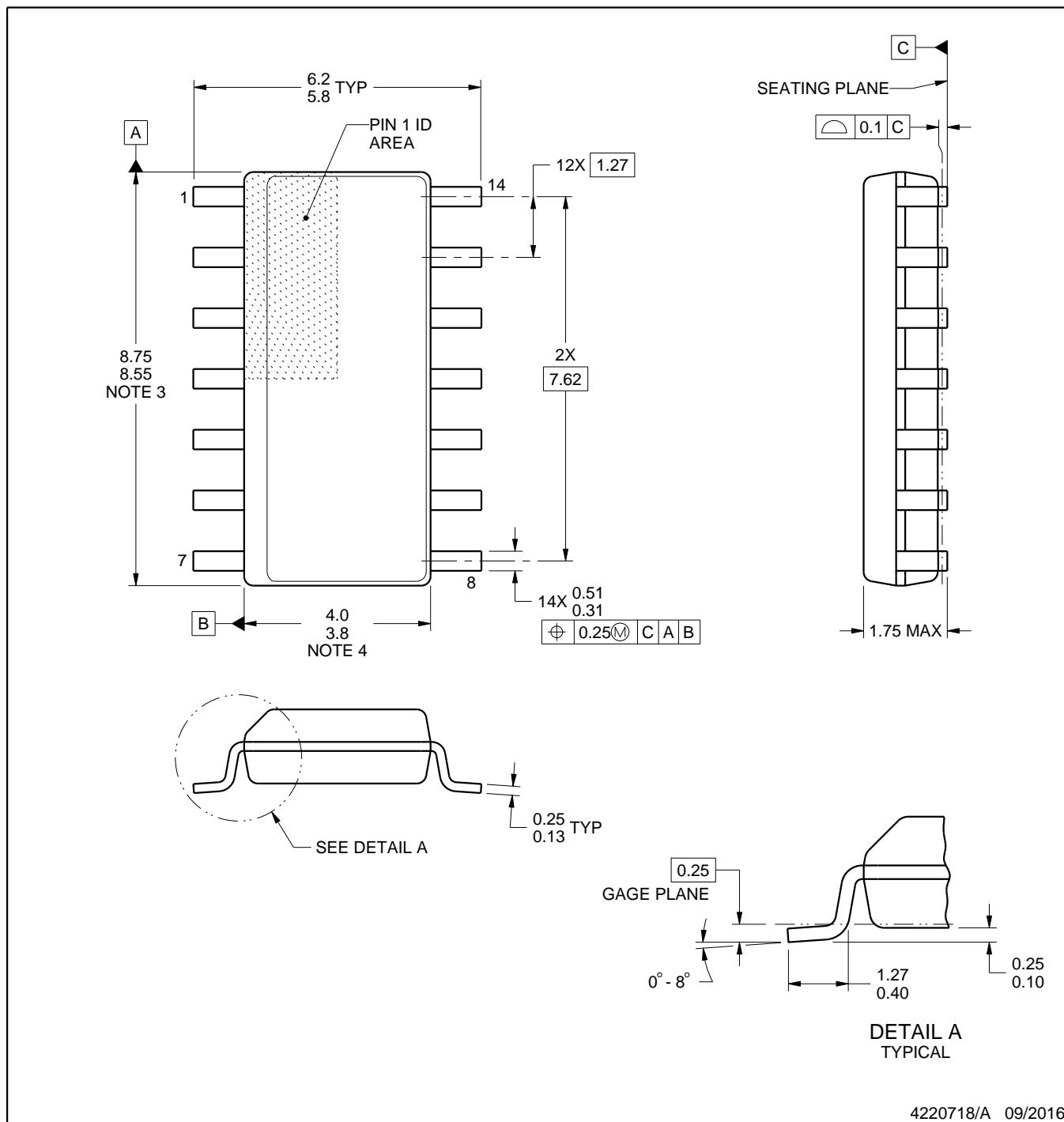
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T ( $\mu$ m)	B (mm)
7700101DA	W	CFP	14	25	506.98	26.16	6220	NA
JM38510/31502BDA	W	CFP	14	25	506.98	26.16	6220	NA
M38510/31502BDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74LS90N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS90N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS90NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS90NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS92D	D	SOIC	14	50	506.6	8	3940	4.32
SN74LS92N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS92N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS93D	D	SOIC	14	50	506.6	8	3940	4.32
SN74LS93N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS93N	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54LS93W	W	CFP	14	25	506.98	26.16	6220	NA

# PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

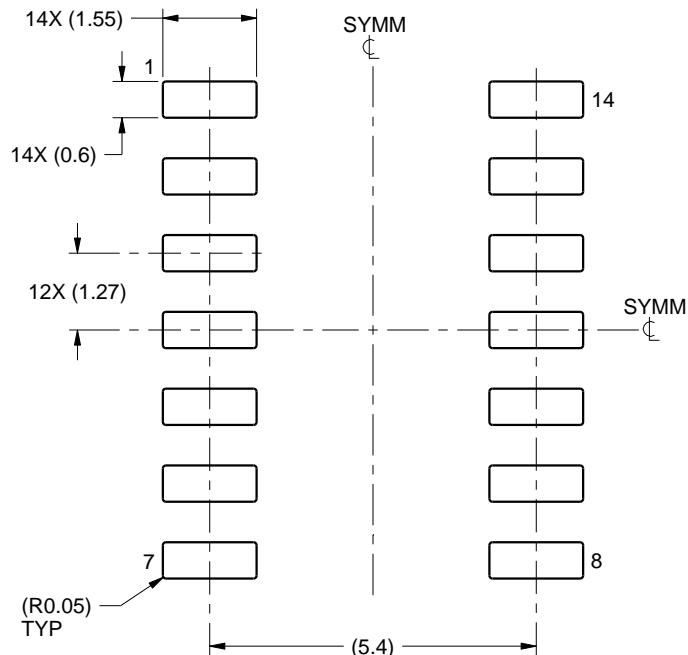
- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

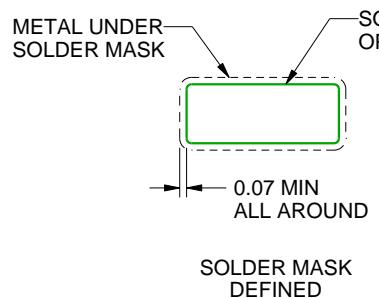
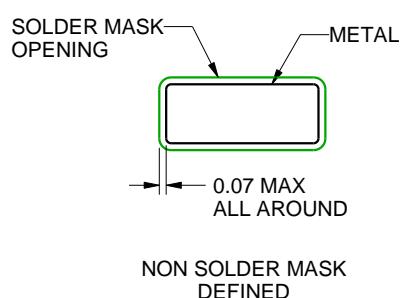
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

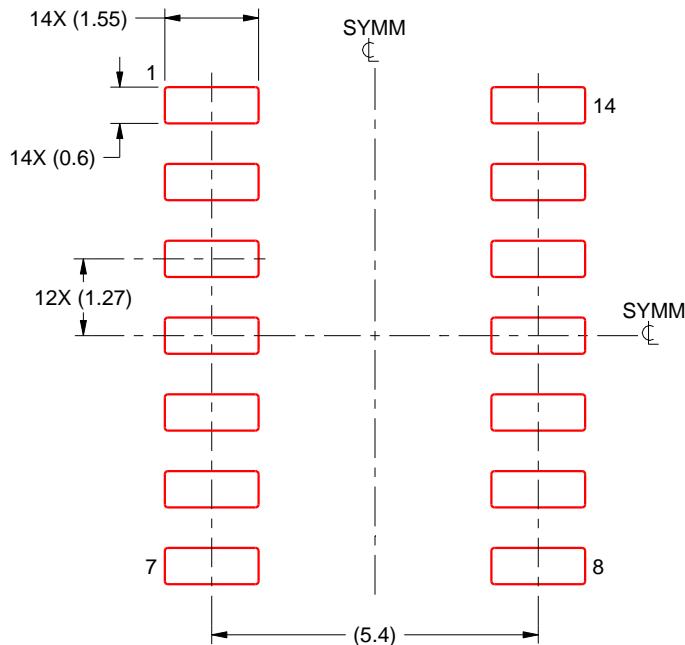
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

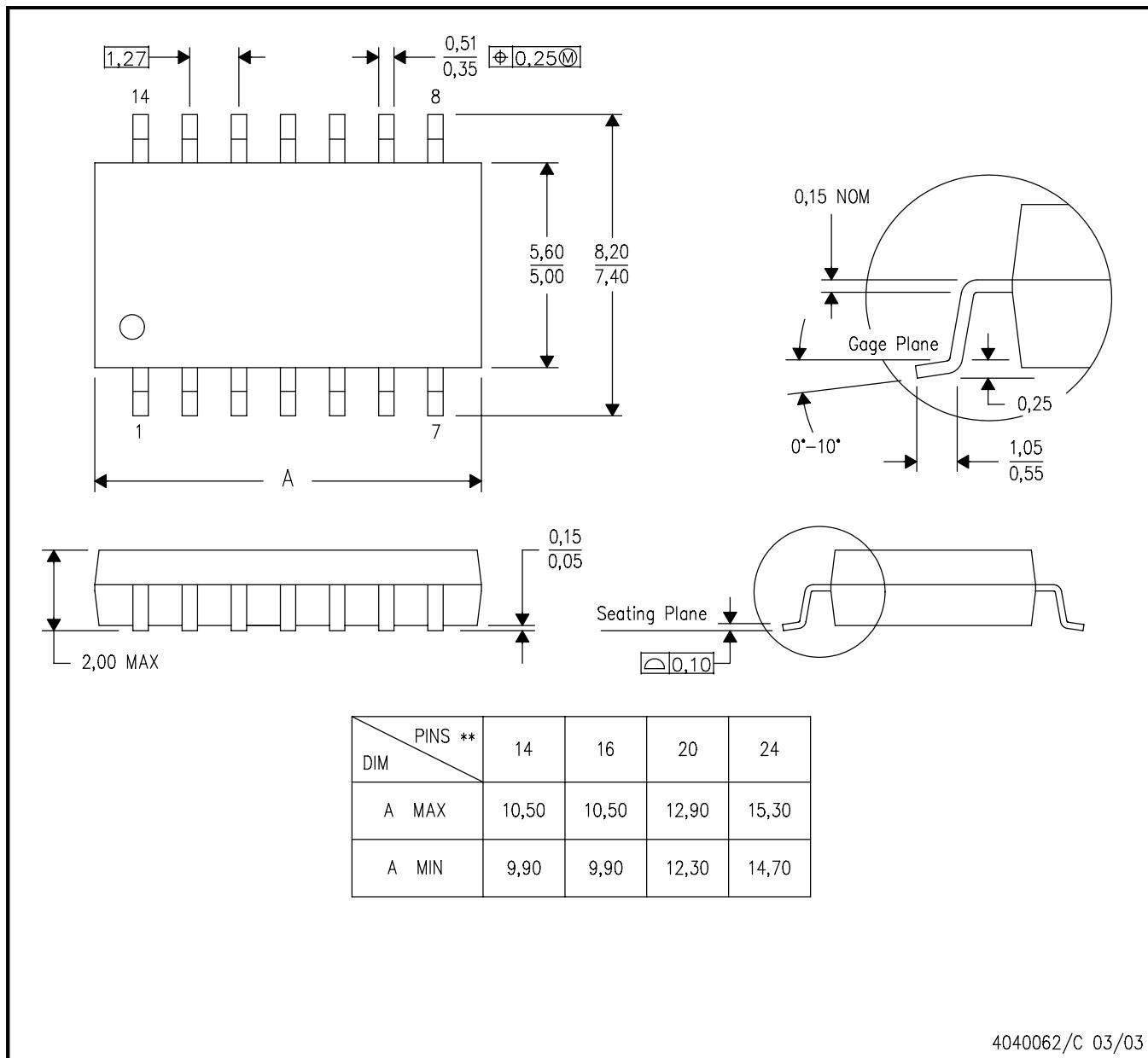
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

**14-PINS SHOWN**

**PLASTIC SMALL-OUTLINE PACKAGE**

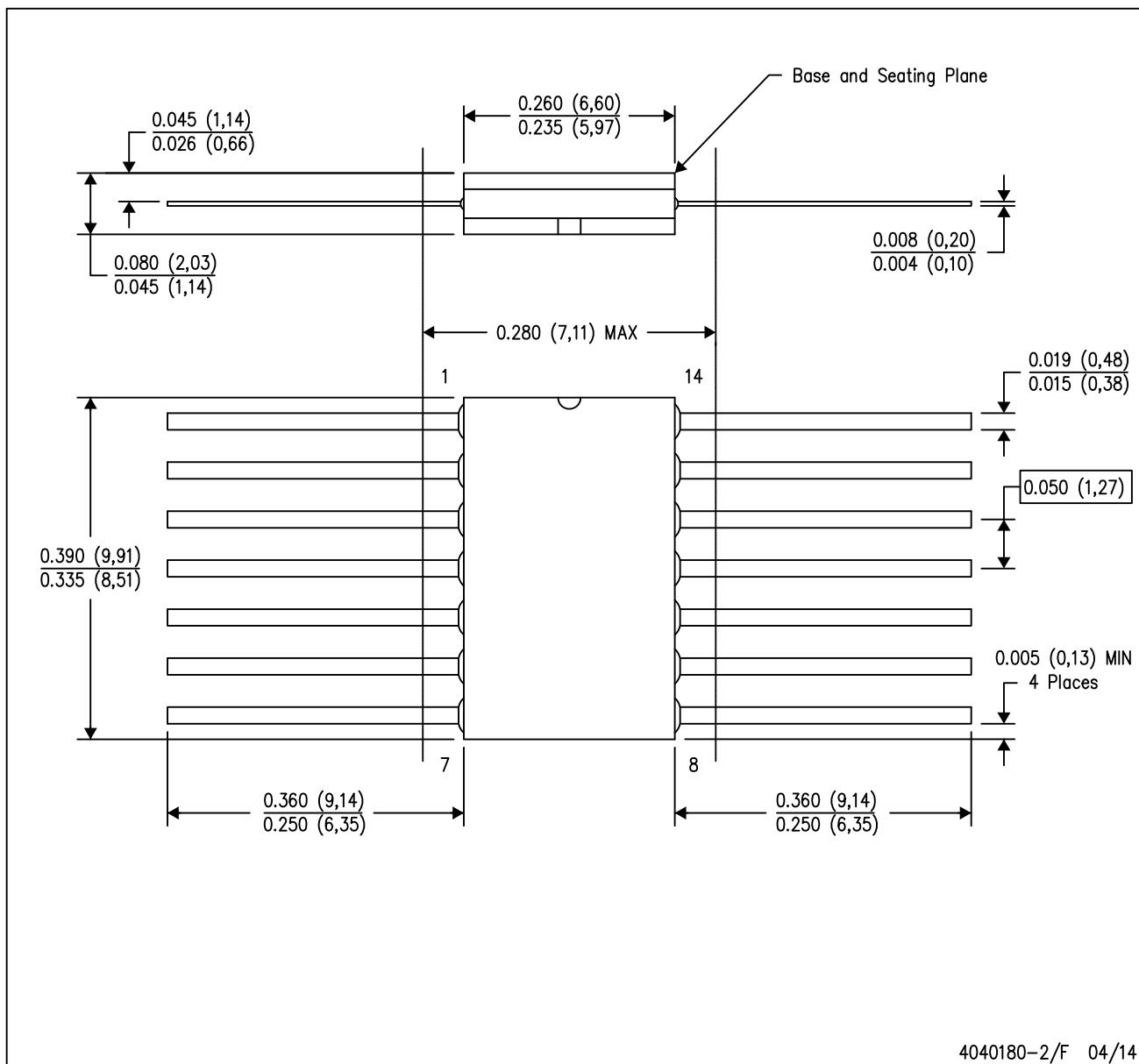


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## MECHANICAL DATA

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



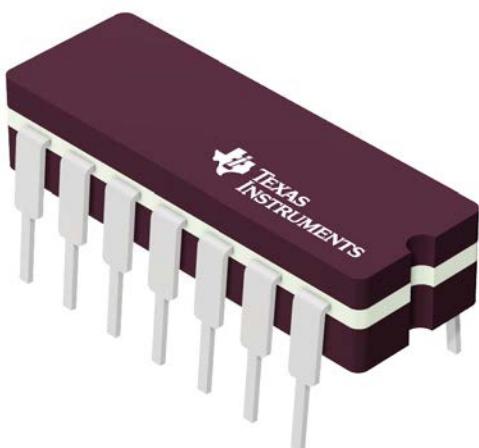
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14

# GENERIC PACKAGE VIEW

J 14

**CDIP - 5.08 mm max height**

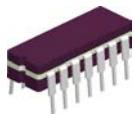
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

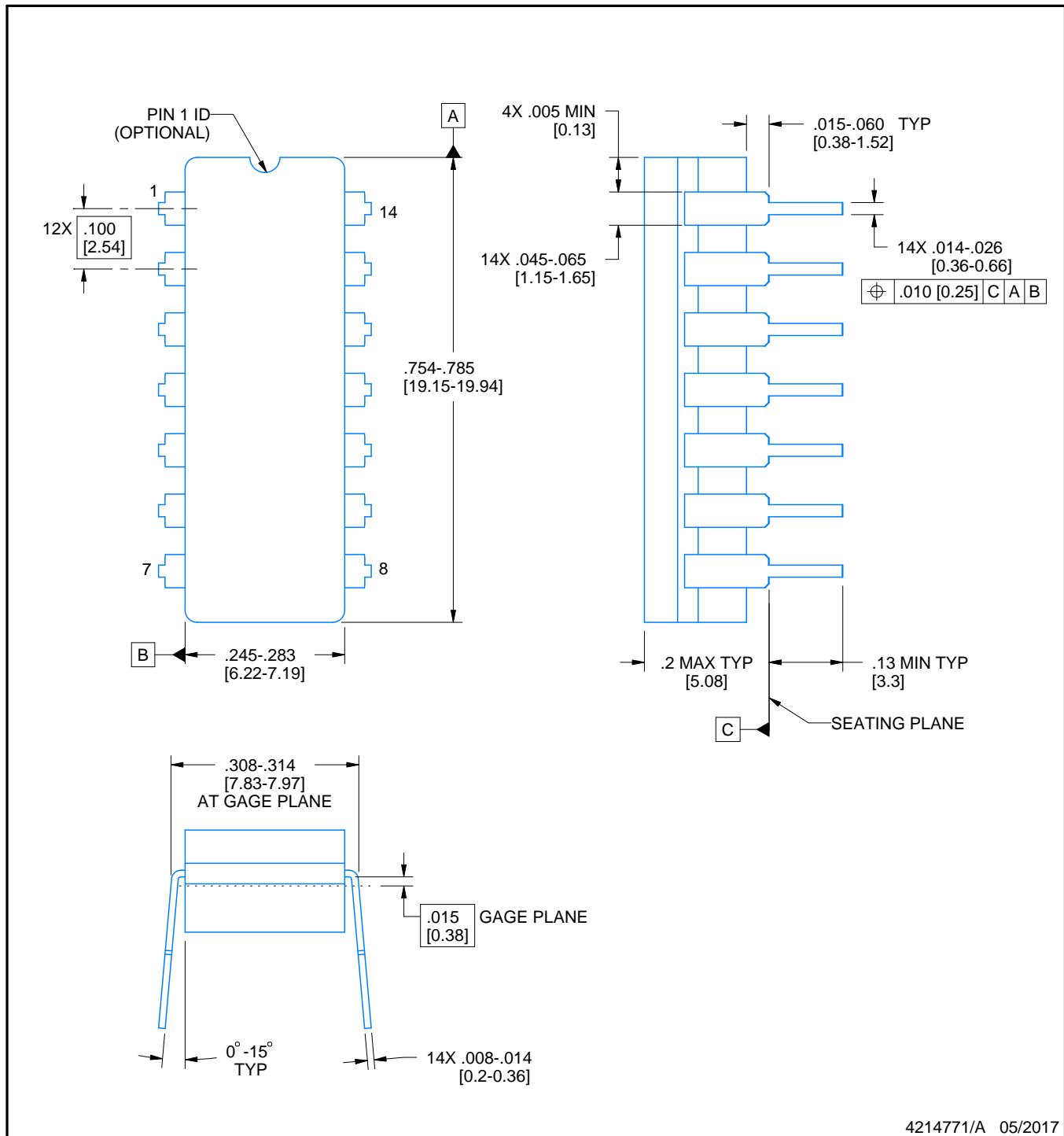
J0014A



# PACKAGE OUTLINE

## CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

### NOTES:

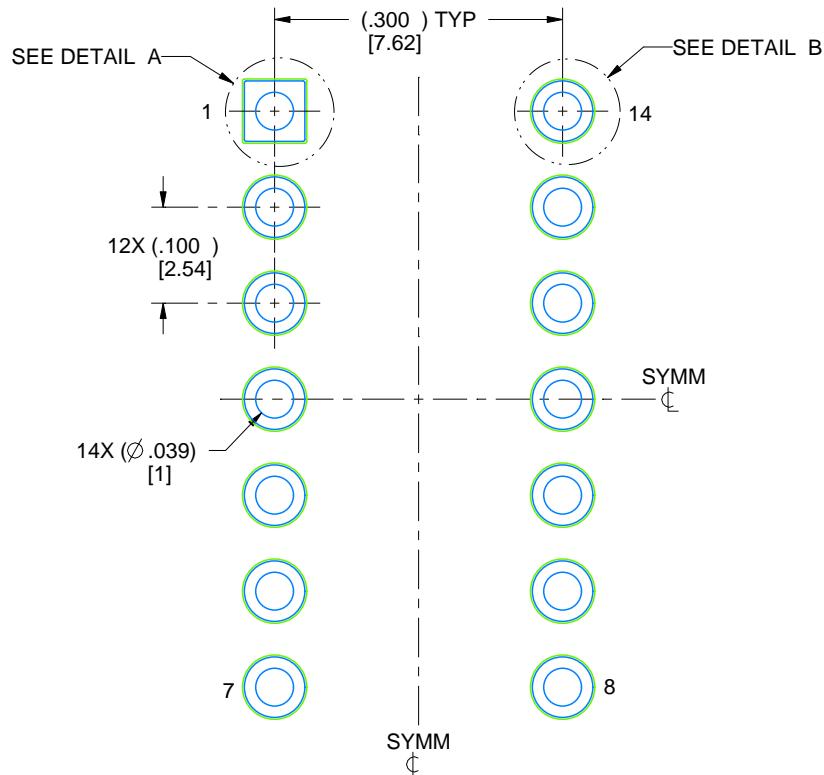
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

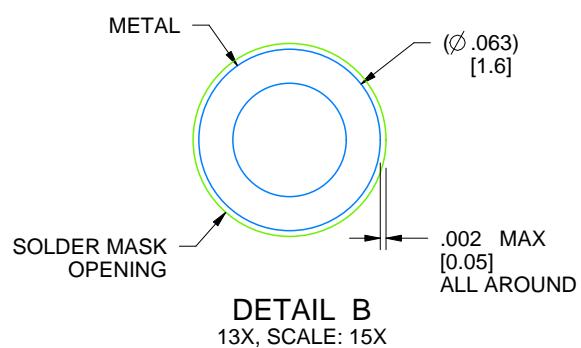
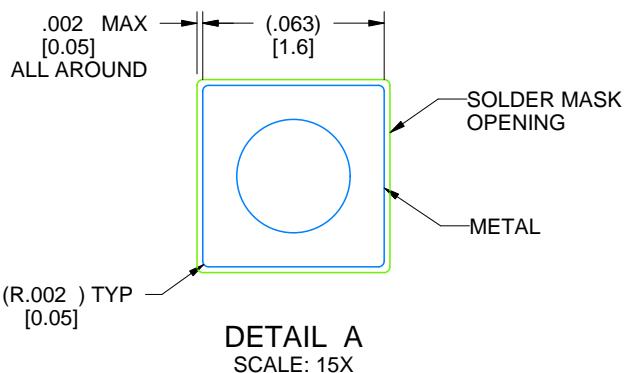
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X

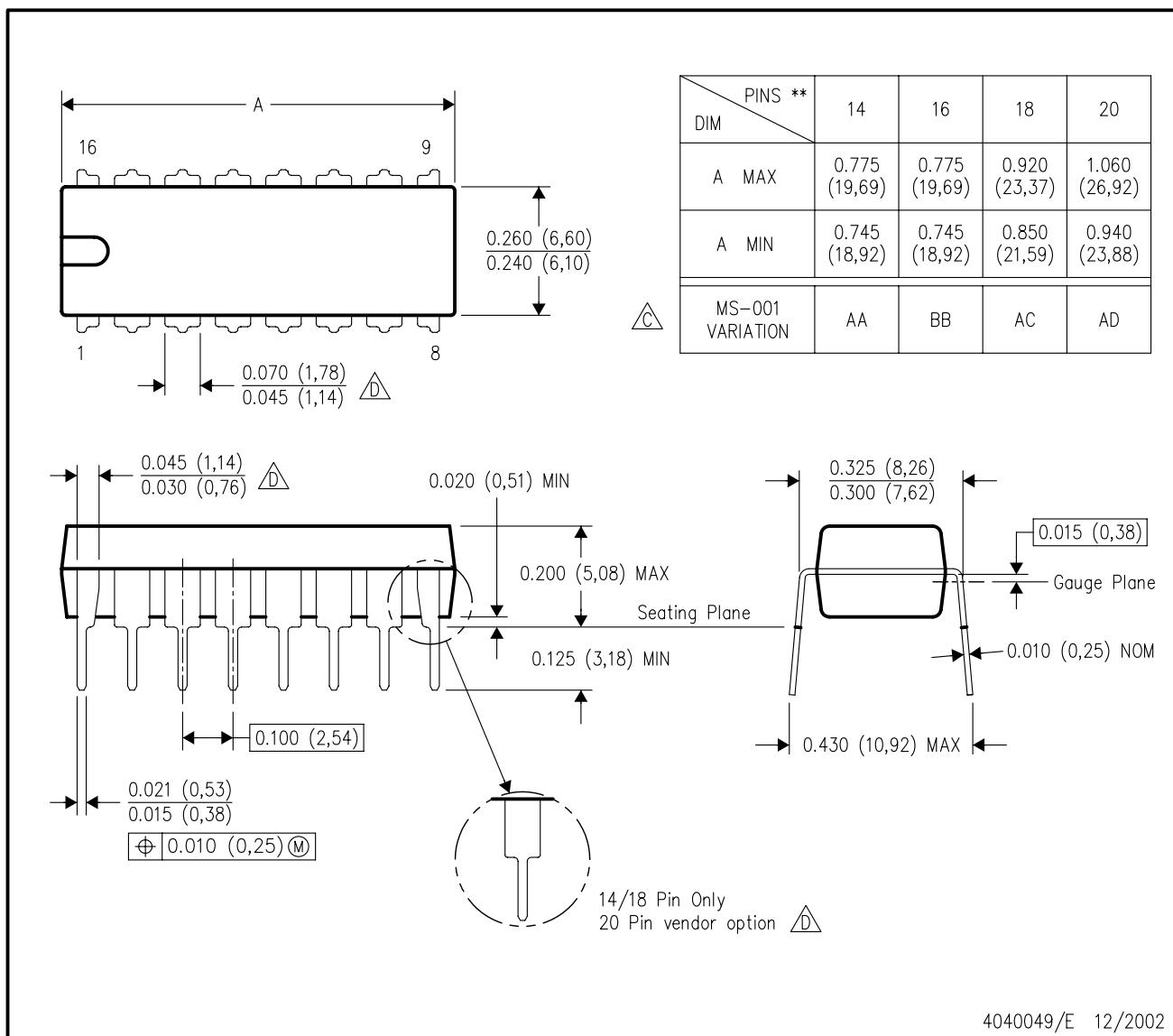


4214771/A 05/2017

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.

Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

The 20 pin end lead shoulder width is a vendor option, either half or full width.

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## Data Sheet

## TMP35/TMP36/TMP37

### FEATURES

- Low voltage operation (2.7 V to 5.5 V)**
- Calibrated directly in °C**
- 10 mV/°C scale factor (20 mV/°C on TMP37)**
- ±2°C accuracy over temperature (typ)**
- ±0.5°C linearity (typ)**
- Stable with large capacitive loads**
- Specified –40°C to +125°C, operation to +150°C**
- Less than 50 µA quiescent current**
- Shutdown current 0.5 µA max**
- Low self-heating**
- Qualified for automotive applications**

### APPLICATIONS

- Environmental control systems**
- Thermal protection**
- Industrial process control**
- Fire alarms**
- Power system monitors**
- CPU thermal management**

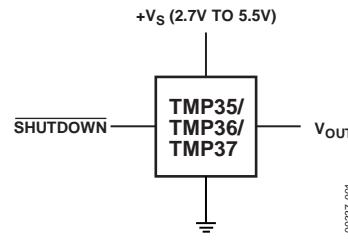
### GENERAL DESCRIPTION

The TMP35/TMP36/TMP37 are low voltage, precision centigrade temperature sensors. They provide a voltage output that is linearly proportional to the Celsius (centigrade) temperature. The TMP35/TMP36/TMP37 do not require any external calibration to provide typical accuracies of ±1°C at +25°C and ±2°C over the –40°C to +125°C temperature range.

The low output impedance of the TMP35/TMP36/TMP37 and its linear output and precise calibration simplify interfacing to temperature control circuitry and ADCs. All three devices are intended for single-supply operation from 2.7 V to 5.5 V maximum. The supply current runs well below 50 µA, providing very low self-heating—less than 0.1°C in still air. In addition, a shutdown function is provided to cut the supply current to less than 0.5 µA.

The TMP35 is functionally compatible with the LM35/LM45 and provides a 250 mV output at 25°C. The TMP35 reads temperatures from 10°C to 125°C. The TMP36 is specified from –40°C to +125°C, provides a 750 mV output at 25°C, and operates to 125°C from a single 2.7 V supply. The TMP36 is functionally compatible with the LM50. Both the TMP35 and TMP36 have an output scale factor of 10 mV/°C.

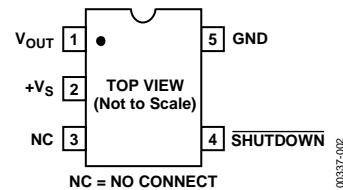
### FUNCTIONAL BLOCK DIAGRAM



00337-001

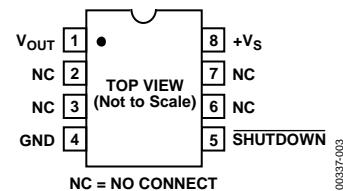
Figure 1.

### PIN CONFIGURATIONS



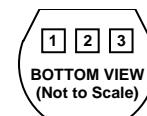
00337-002

Figure 2. RJ-5 (SOT-23)



00337-003

Figure 3. R-8 (SOIC\_N)



00337-004

Figure 4. T-3 (TO-92)

The TMP37 is intended for applications over the range of 5°C to 100°C and provides an output scale factor of 20 mV/°C. The TMP37 provides a 500 mV output at 25°C. Operation extends to 150°C with reduced accuracy for all devices when operating from a 5 V supply.

The TMP35/TMP36/TMP37 are available in low cost 3-lead TO-92, 8-lead SOIC\_N, and 5-lead SOT-23 surface-mount packages.

## TABLE OF CONTENTS

Features .....	1
Applications .....	1
General Description .....	1
Functional Block Diagram .....	1
Pin Configurations .....	1
Revision History .....	2
Specifications.....	3
Absolute Maximum Ratings.....	4
Thermal Resistance .....	4
ESD Caution.....	4
Typical Performance Characteristics .....	5
Functional Description .....	8
Applications Information .....	9
Shutdown Operation.....	9
Mounting Considerations .....	9
Thermal Environment Effects .....	9
Basic Temperature Sensor Connections.....	10
Fahrenheit Thermometers .....	10
Average and Differential Temperature Measurement .....	12
Microprocessor Interrupt Generator.....	13
Thermocouple Signal Conditioning with Cold-Junction Compensation.....	14
Using TMP35/TMP36/TMP37 Sensors in Remote Locations .....	15
Temperature to 4–20 mA Loop Transmitter .....	15
Temperature-to-Frequency Converter .....	16
Driving Long Cables or Heavy Capacitive Loads .....	17
Commentary on Long-Term Stability .....	17
Outline Dimensions .....	18
Ordering Guide .....	19
Automotive Products .....	19

## REVISION HISTORY

### 5/15—Rev. G to Rev. H

Changed TMP3x to TMP35/TMP36/TMP37 .....	Throughout
Changes to Figure 28.....	12
Changes to Ordering Guide .....	19

### 11/13—Rev. F to Rev. G

Change to Table 1, Long-Term Stability Parameter .....	3
Change to Caption for Figure 38 .....	18
Changes to Ordering Guide .....	19

### 11/10—Rev. E to Rev. F

Changes to Features.....	1
Updated Outline Dimensions .....	18
Changes to Ordering Guide .....	19
Added Automotive Products Section.....	20

### 8/08—Rev. D to Rev. E

Updated Outline Dimensions .....	18
Changes to Ordering Guide .....	19

### 3/05—Rev. C to Rev. D

Updated Format.....	Universal
Changes to Specifications .....	3
Additions to Absolute Maximum Ratings.....	4
Updated Outline Dimensions .....	18
Changes to Ordering Guide .....	19

### 10/02—Rev. B to Rev. C

Changes to Specifications .....	3
Deleted Text from Commentary on Long-Term Stability Section.....	13
Updated Outline Dimensions.....	14

### 9/01—Rev. A to Rev. B

Edits to Specifications .....	2
Addition of New Figure 1 .....	2
Deletion of Wafer Test Limits Section .....	3

### 6/97—Rev. 0 to Rev. A

### 3/96—Revision 0: Initial Version

## SPECIFICATIONS

$V_S = 2.7 \text{ V to } 5.5 \text{ V}$ ,  $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , unless otherwise noted.

Table 1.

Parameter <sup>1</sup>	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
ACCURACY						
TMP35/TMP36/TMP37 (F Grade)		$T_A = 25^\circ\text{C}$		$\pm 1$	$\pm 2$	$^\circ\text{C}$
TMP35/TMP36/TMP37 (G Grade)		$T_A = 25^\circ\text{C}$		$\pm 1$	$\pm 3$	$^\circ\text{C}$
TMP35/TMP36/TMP37 (F Grade)		Over rated temperature		$\pm 2$	$\pm 3$	$^\circ\text{C}$
TMP35/TMP36/TMP37 (G Grade)		Over rated temperature		$\pm 2$	$\pm 4$	$^\circ\text{C}$
Scale Factor, TMP35		$10^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		10		$\text{mV}/^\circ\text{C}$
Scale Factor, TMP36		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		10		$\text{mV}/^\circ\text{C}$
Scale Factor, TMP37		$5^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$		20		$\text{mV}/^\circ\text{C}$
		$5^\circ\text{C} \leq T_A \leq 100^\circ\text{C}$		20		$\text{mV}/^\circ\text{C}$
		$3.0 \text{ V} \leq V_S \leq 5.5 \text{ V}$				
Load Regulation		$0 \mu\text{A} \leq I_L \leq 50 \mu\text{A}$				
		$-40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$	6	20		$\text{m}^\circ\text{C}/\mu\text{A}$
		$-105^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	25	60		$\text{m}^\circ\text{C}/\mu\text{A}$
Power Supply Rejection Ratio	PSRR	$T_A = 25^\circ\text{C}$		30	100	$\text{m}^\circ\text{C}/\text{V}$
		$3.0 \text{ V} \leq V_S \leq 5.5 \text{ V}$		50		$\text{m}^\circ\text{C}/\text{V}$
Linearity				0.5		$^\circ\text{C}$
Long-Term Stability		$T_A = 150^\circ\text{C}$ for 1000 hours		0.4		$^\circ\text{C}$
SHUTDOWN						
Logic High Input Voltage	$V_{IH}$	$V_S = 2.7 \text{ V}$	1.8			V
Logic Low Input Voltage	$V_{IL}$	$V_S = 5.5 \text{ V}$			400	$\text{mV}$
OUTPUT						
TMP35 Output Voltage		$T_A = 25^\circ\text{C}$		250		$\text{mV}$
TMP36 Output Voltage		$T_A = 25^\circ\text{C}$		750		$\text{mV}$
TMP37 Output Voltage		$T_A = 25^\circ\text{C}$		500		$\text{mV}$
Output Voltage Range			100		2000	$\text{mV}$
Output Load Current	$I_L$		0		50	$\mu\text{A}$
Short-Circuit Current	$I_{SC}$	Note 2			250	$\mu\text{A}$
Capacitive Load Driving	$C_L$	No oscillations <sup>2</sup>	1000	10000		pF
Device Turn-On Time		Output within $\pm 1^\circ\text{C}$ , $100 \text{ k}\Omega    100 \text{ pF}$ load <sup>2</sup>	0.5	1		ms
POWER SUPPLY						
Supply Range	$V_S$		2.7		5.5	V
Supply Current	$I_{SY}(\text{ON})$	Unloaded			50	$\mu\text{A}$
Supply Current (Shutdown)	$I_{SY}(\text{OFF})$	Unloaded		0.01	0.5	$\mu\text{A}$

<sup>1</sup> Does not consider errors caused by self-heating.

<sup>2</sup> Guaranteed but not tested.

## ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter <sup>1,2</sup>	Rating
Supply Voltage	7 V
Shutdown Pin	$\text{GND} \leq \text{SHUTDOWN} \leq +V_s$
Output Pin	$\text{GND} \leq V_{\text{OUT}} \leq +V_s$
Operating Temperature Range	-55°C to +150°C
Die Junction Temperature	175°C
Storage Temperature Range	-65°C to +160°C
IR Reflow Soldering	
Peak Temperature	220°C (0°C/5°C)
Time at Peak Temperature Range	10 sec to 20 sec
Ramp-Up Rate	3°C/sec
Ramp-Down Rate	-6°C/sec
Time 25°C to Peak Temperature	6 min
IR Reflow Soldering—Pb-Free Package	
Peak Temperature	260°C (0°C)
Time at Peak Temperature Range	20 sec to 40 sec
Ramp-Up Rate	3°C/sec
Ramp-Down Rate	-6°C/sec
Time 25°C to Peak Temperature	8 min

<sup>1</sup> Digital inputs are protected; however, permanent damage can occur on unprotected units from high energy electrostatic fields. Keep units in conductive foam or packaging at all times until ready to use. Use proper antistatic handling procedures.

<sup>2</sup> Remove power before inserting or removing units from their sockets.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is, a device in socket.

Table 3. Thermal Resistance

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
TO-92 (T-3-1)	162	120	°C/W
SOIC_N (R-8)	158	43	°C/W
SOT-23 (RJ-5)	300	180	°C/W

### ESD CAUTION



#### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## TYPICAL PERFORMANCE CHARACTERISTICS

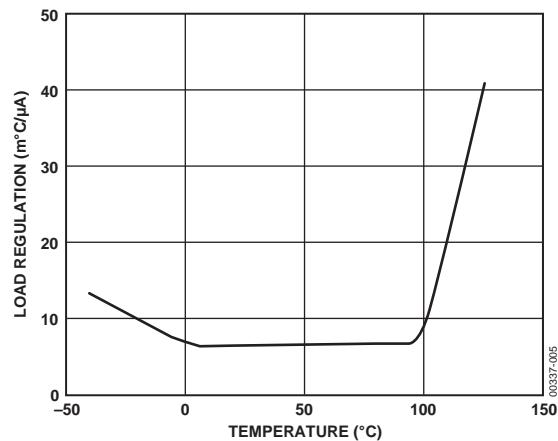


Figure 5. Load Regulation vs. Temperature (m°C/µA)

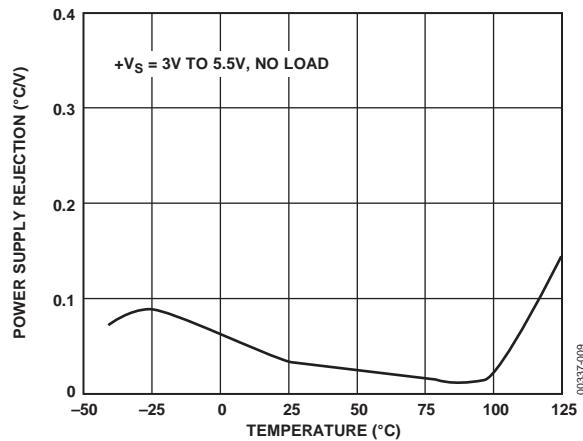


Figure 8. Power Supply Rejection vs. Temperature

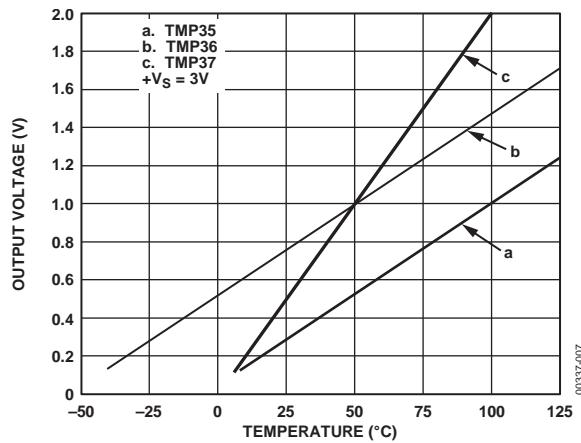


Figure 6. Output Voltage vs. Temperature

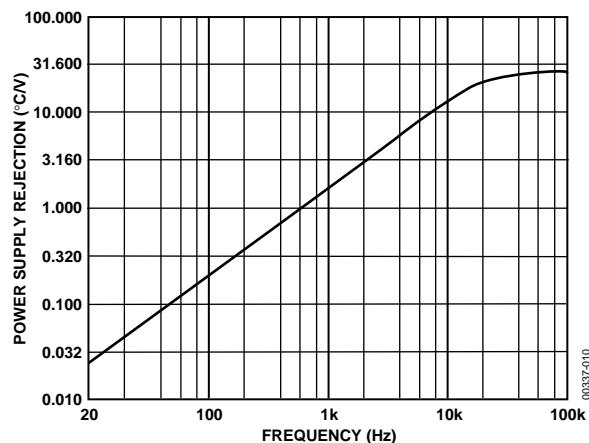


Figure 9. Power Supply Rejection vs. Frequency

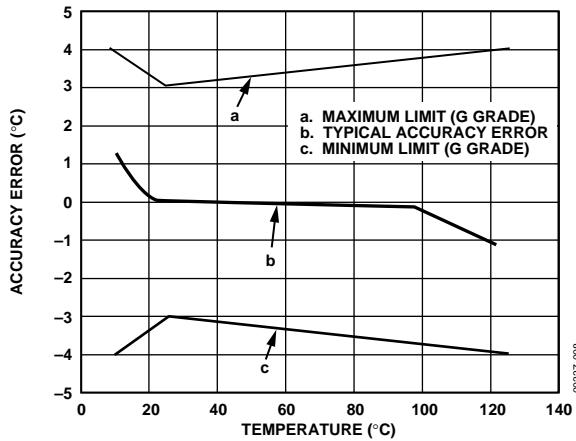


Figure 7. Accuracy Error vs. Temperature

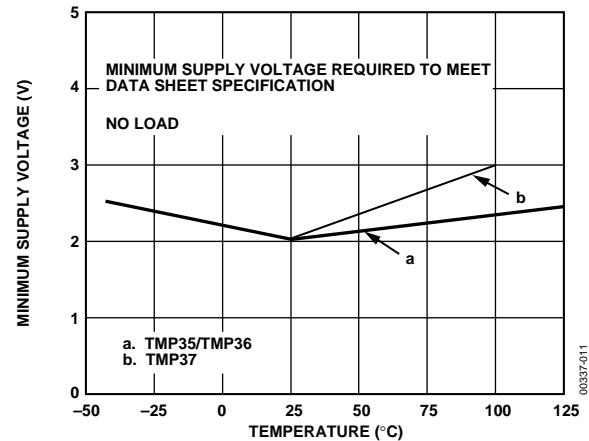


Figure 10. Minimum Supply Voltage vs. Temperature

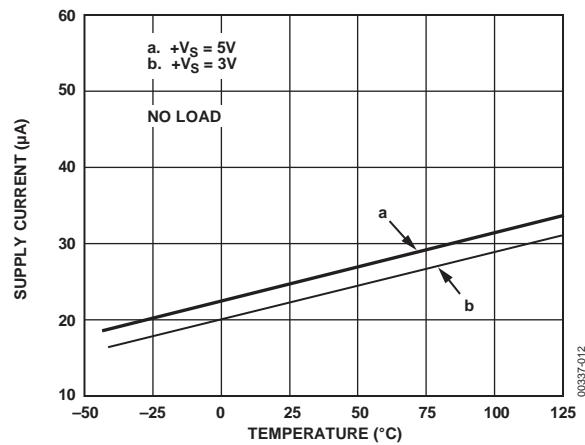


Figure 11. Supply Current vs. Temperature

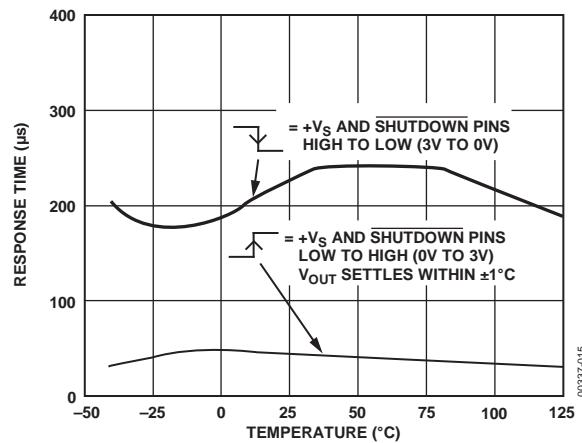
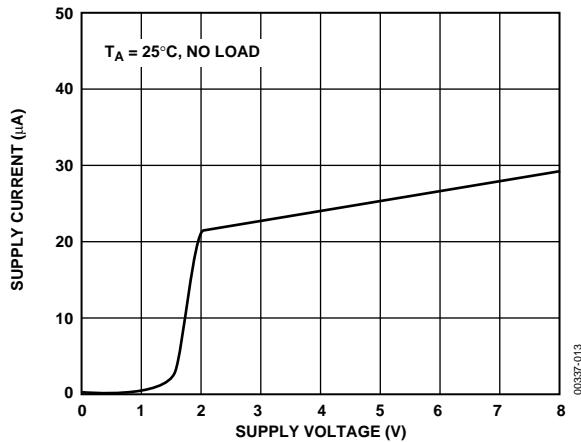
Figure 14.  $V_{OUT}$  Response Time for  $+V_S$  Power-Up/Power-Down vs. Temperature

Figure 12. Supply Current vs. Supply Voltage

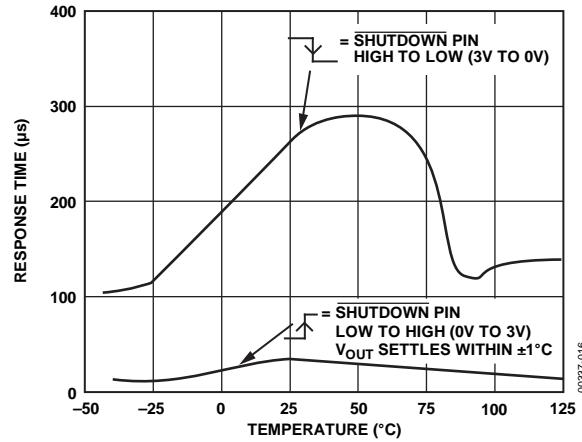
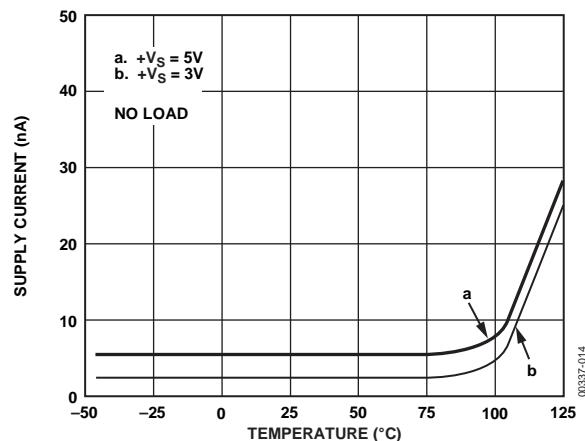
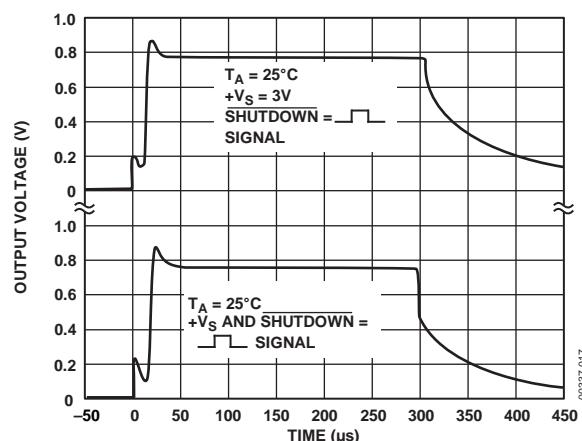
Figure 15.  $V_{OUT}$  Response Time for SHUTDOWN Pin vs. Temperature

Figure 13. Supply Current vs. Temperature (Shutdown = 0 V)

Figure 16.  $V_{OUT}$  Response Time to SHUTDOWN Pin and  $+V_S$  Pin vs. Time

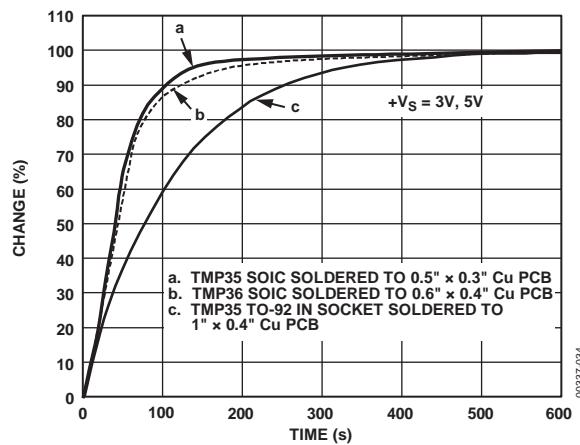


Figure 17. Thermal Response Time in Still Air

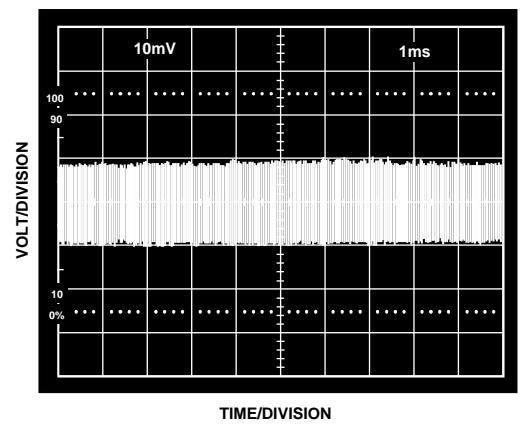
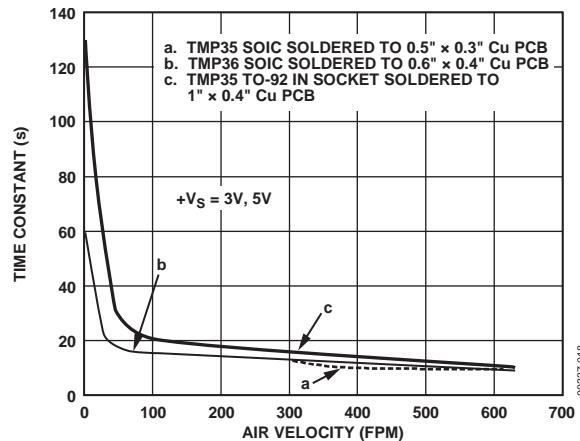
Figure 20. Temperature Sensor Wideband Output Noise Voltage;  
Gain = 100, BW = 157 kHz

Figure 18. Thermal Response Time Constant in Forced Air

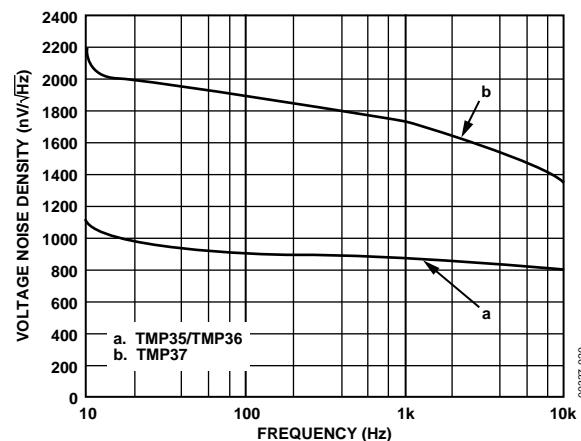


Figure 21. Voltage Noise Spectral Density vs. Frequency

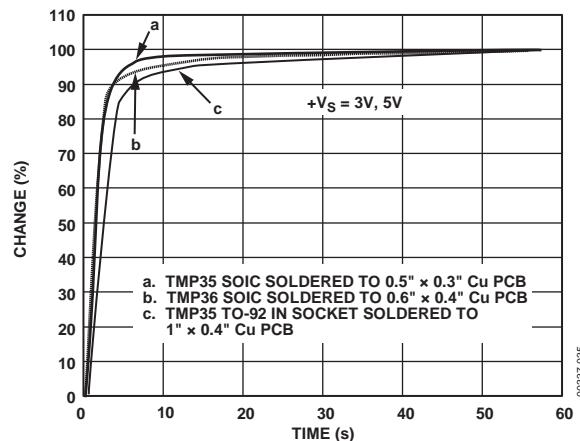


Figure 19. Thermal Response Time in Stirred Oil Bath

## FUNCTIONAL DESCRIPTION

An equivalent circuit for the TMP35/TMP36/TMP37 micropower, centigrade temperature sensors is shown in Figure 22. The core of the temperature sensor is a band gap core that comprises transistors Q1 and Q2, biased by Q3 to approximately 8  $\mu$ A. The band gap core operates both Q1 and Q2 at the same collector current level; however, because the emitter area of Q1 is 10 times that of Q2, the  $V_{BE}$  of Q1 and the  $V_{BE}$  of Q2 are not equal by the following relationship:

$$\Delta V_{BE} = V_T \times \ln\left(\frac{A_{E,Q1}}{A_{E,Q2}}\right)$$

Resistors R1 and R2 are used to scale this result to produce the output voltage transfer characteristic of each temperature sensor and, simultaneously, R2 and R3 are used to scale the  $V_{BE}$  of Q1 as an offset term in  $V_{OUT}$ . Table 4 summarizes the differences in the output characteristics of the three temperature sensors.

The output voltage of the temperature sensor is available at the emitter of Q4, which buffers the band gap core and provides load current drive. The current gain of Q4, working with the available base current drive from the previous stage, sets the short-circuit current limit of these devices to 250  $\mu$ A.

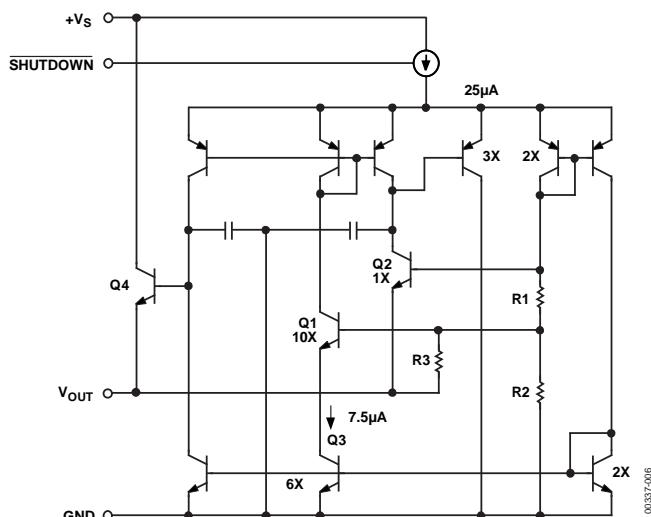


Figure 22. Temperature Sensor Simplified Equivalent Circuit

Table 4. TMP35/TMP36/TMP37 Output Characteristics

Sensor	Offset Voltage (V)	Output Voltage Scaling (mV/ $^{\circ}$ C)	Output Voltage at 25 $^{\circ}$ C (mV)
TMP35	0	10	250
TMP36	0.5	10	750
TMP37	0	20	500

## APPLICATIONS INFORMATION

### SHUTDOWN OPERATION

All TMP35/TMP36/TMP37 devices include a shutdown capability, which reduces the power supply drain to less than 0.5  $\mu\text{A}$  maximum. This feature, available only in the SOIC\_N and the SOT-23 packages, is TTL/CMOS level-compatible, provided that the temperature sensor supply voltage is equal in magnitude to the logic supply voltage. Internal to the TMP35/TMP36/TMP37 at the SHUTDOWN pin, a pull-up current source to  $+V_S$  is connected. This allows the SHUTDOWN pin to be driven from an open-collector/drain driver. A logic low, or zero-volt condition, on the SHUTDOWN pin is required to turn off the output stage. During shutdown, the output of the temperature sensors becomes high impedance where the potential of the output pin is then determined by external circuitry. If the shutdown feature is not used, it is recommended that the SHUTDOWN pin be connected to  $+V_S$  (Pin 8 on the SOIC\_N; Pin 2 on the SOT-23).

The shutdown response time of these temperature sensors is shown in Figure 14, Figure 15, and Figure 16.

### MOUNTING CONSIDERATIONS

If the TMP35/TMP36/TMP37 temperature sensors are thermally attached and protected, they can be used in any temperature measurement application where the maximum temperature range of the medium is between  $-40^\circ\text{C}$  and  $+125^\circ\text{C}$ . Properly cemented or glued to the surface of the medium, these sensors are within  $0.01^\circ\text{C}$  of the surface temperature. Caution should be exercised, especially with T-3 packages, because the leads and any wiring to the device can act as heat pipes, introducing errors if the surrounding air-surface interface is not isothermal. Avoiding this condition is easily achieved by dabbing the leads of the temperature sensor and the hookup wires with a bead of thermally conductive epoxy. This ensures that the TMP35/TMP36/TMP37 die temperature is not affected by the surrounding air temperature. Because plastic IC packaging technology is used, excessive mechanical stress should be avoided when fastening the device with a clamp or a screw-on heat tab. Thermally conductive epoxy or glue, which must be electrically nonconductive, is recommended under typical mounting conditions.

These temperature sensors, as well as any associated circuitry, should be kept insulated and dry to avoid leakage and corrosion. In wet or corrosive environments, any electrically isolated metal or ceramic well can be used to shield the temperature sensors. Condensation at very cold temperatures can cause errors and should be avoided by sealing the device, using electrically non-conductive epoxy paints or dip or any one of the many printed circuit board coatings and varnishes.

### THERMAL ENVIRONMENT EFFECTS

The thermal environment in which the TMP35/TMP36/TMP37 sensors are used determines two important characteristics: self-heating effects and thermal response time. Figure 23 illustrates a thermal model of the TMP35/TMP36/TMP37 temperature sensors, which is useful in understanding these characteristics.

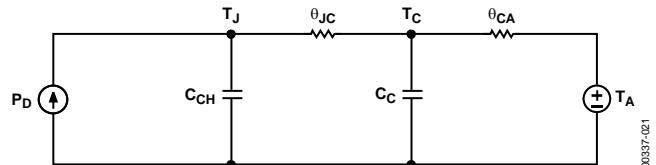


Figure 23. Thermal Circuit Model

In the T-3 package, the thermal resistance junction-to-case,  $\theta_{JC}$ , is  $120^\circ\text{C}/\text{W}$ . The thermal resistance case-to-ambient,  $C_A$ , is the difference between  $\theta_{JA}$  and  $\theta_{JC}$ , and is determined by the characteristics of the thermal connection. The power dissipation of the temperature sensor,  $P_D$ , is the product of the total voltage across the device and its total supply current, including any current delivered to the load. The rise in die temperature above the ambient temperature of the medium is given by

$$T_J = P_D \times (\theta_{JC} + \theta_{CA}) + T_A$$

Thus, the die temperature rise of a TMP35 SOT-23 package mounted into a socket in still air at  $25^\circ\text{C}$  and driven from a 5 V supply is less than  $0.04^\circ\text{C}$ .

The transient response of the TMP35/TMP36/TMP37 sensors to a step change in the temperature is determined by the thermal resistances and the thermal capacities of the die,  $C_{CH}$ , and the case,  $C_C$ . The thermal capacity of  $C_C$  varies with the measurement medium because it includes anything in direct contact with the package. In all practical cases, the thermal capacity of  $C_C$  is the limiting factor in the thermal response time of the sensor and can be represented by a single-pole RC time constant response. Figure 17 and Figure 19 show the thermal response time of the TMP35/TMP36/TMP37 sensors under various conditions. The thermal time constant of a temperature sensor is defined as the time required for the sensor to reach 63.2% of the final value for a step change in the temperature. For example, the thermal time constant of a TMP35 SOIC package sensor mounted onto a  $0.5'' \times 0.3''$  PCB is less than 50 sec in air, whereas in a stirred oil bath, the time constant is less than 3 sec.

## BASIC TEMPERATURE SENSOR CONNECTIONS

Figure 24 illustrates the basic circuit configuration for the TMP35/TMP36/TMP37 temperature sensors. The table in Figure 24 shows the pin assignments of the temperature sensors for the three package types. For the SOT-23, Pin 3 is labeled NC, as are Pin 2, Pin 3, Pin 6, and Pin 7 on the SOIC\_N package. It is recommended that no electrical connections be made to these pins. If the shutdown feature is not needed on the SOT-23 or on the SOIC\_N package, the SHUTDOWN pin should be connected to +Vs.

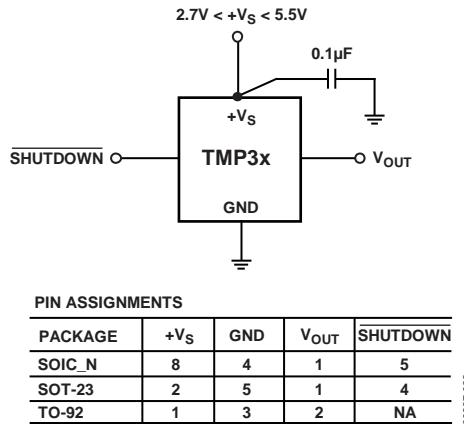


Figure 24. Basic Temperature Sensor Circuit Configuration

Note the 0.1  $\mu$ F bypass capacitor on the input. This capacitor should be a ceramic type, have very short leads (surface-mount is preferable), and be located as close as possible in physical proximity to the temperature sensor supply pin. Because these temperature sensors operate on very little supply current and may be exposed to very hostile electrical environments, it is important to minimize the effects of radio frequency interference (RFI) on these devices. The effect of RFI on these temperature sensors specifically and on analog ICs in general is manifested as abnormal dc shifts in the output voltage due to the rectification of the high frequency ambient noise by the IC. When the devices are operated in the presence of high frequency radiated or conducted noise, a large value tantalum capacitor ( $\pm 2.2 \mu$ F) placed across the 0.1  $\mu$ F ceramic capacitor may offer additional noise immunity.

## FAHRENHEIT THERMOMETERS

Although the TMP35/TMP36/TMP37 temperature sensors are centigrade temperature sensors, a few components can be used to convert the output voltage and transfer characteristics to directly read Fahrenheit temperatures. Figure 25 shows an example of a simple Fahrenheit thermometer using either the TMP35 or the TMP37. Using the TMP35, this circuit can be used to sense temperatures from 41°F to 257°F with an output transfer characteristic of 1 mV/°F; using the TMP37, this circuit can be used to sense temperatures from 41°F to 212°F with an output transfer characteristic of 2 mV/°F. This particular approach does not lend itself to the TMP36 because of its inherent 0.5 V output offset. The circuit is constructed with an AD589, a 1.23 V voltage reference, and four resistors whose values for each sensor are shown in the table in Figure 25. The scaling of the output resistance levels ensures minimum output loading on the temperature sensors. A generalized expression for the transfer equation of the circuit is given by

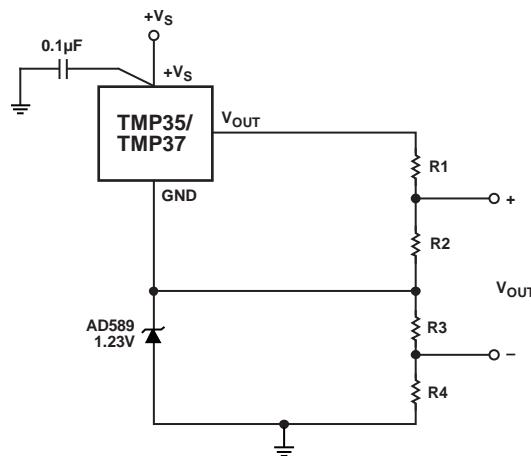
$$V_{OUT} = \left( \frac{R1}{R1 + R2} \right) (TMP35) + \left( \frac{R3}{R3 + R4} \right) (AD589)$$

where:

$V_{OUT}$  is the output voltage of the TMP35 or the TMP37 at the measurement temperature,  $T_M$ .

$AD589$  is the output voltage of the reference, that is, 1.23 V.

The output voltage of this circuit is not referenced to the circuit's common ground. If this output voltage were applied directly to the input of an ADC, the ADC common ground should be adjusted accordingly.



SENSOR	TCV <sub>OUT</sub>	R1 (kΩ)	R2 (kΩ)	R3 (kΩ)	R4 (kΩ)
TMP35	1mV/°F	45.3	10	10	374
TMP37	2mV/°F	45.3	10	10	182

00337-023

Figure 25. TMP35/TMP37 Fahrenheit Thermometers

The same circuit principles can be applied to the [TMP36](#), but because of the inherent offset of the [TMP36](#), the circuit uses only two resistors, as shown in Figure 26. In this circuit, the output voltage transfer characteristic is 1 mV/°F but is referenced to the common ground of the circuit; however, there is a 58 mV (58°F) offset in the output voltage. For example, the output voltage of the circuit reads 18 mV if the [TMP36](#) is placed in a -40°F ambient environment and 315 mV at +257°F.

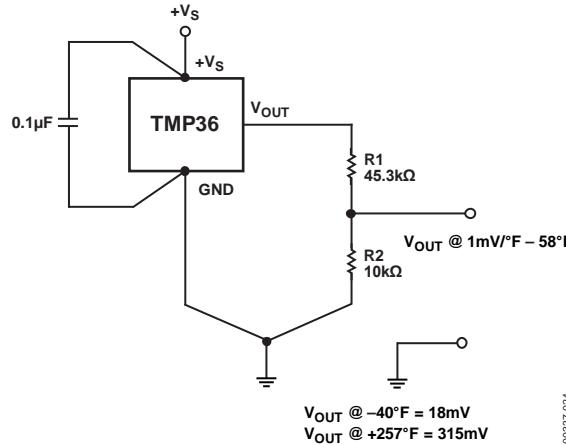


Figure 26. [TMP36](#) Fahrenheit Thermometer Version 1

At the expense of additional circuitry, the offset produced by the circuit in Figure 26 can be avoided by using the circuit in Figure 27. In this circuit, the output of the [TMP36](#) is conditioned by a single-supply, micropower op amp, the [OP193](#). Although the entire circuit operates from a single 3 V supply, the output voltage of the circuit reads the temperature directly, with a transfer characteristic of 1 mV/°F, without offset. This is accomplished through an [ADM660](#), which is a supply voltage inverter. The 3 V supply is inverted and applied to the V- terminal of the [OP193](#). Thus, for a temperature range between -40°F and +257°F, the output of the circuit reads -40 mV to +257 mV. A general expression for the transfer equation of the circuit is given by

$$V_{OUT} = \left( \frac{R6}{R5 + R6} \right) \left( 1 + \frac{R4}{R3} \right) (\text{TMP36}) - \left( \frac{R4}{R3} \right) \left( \frac{V_S}{2} \right)$$

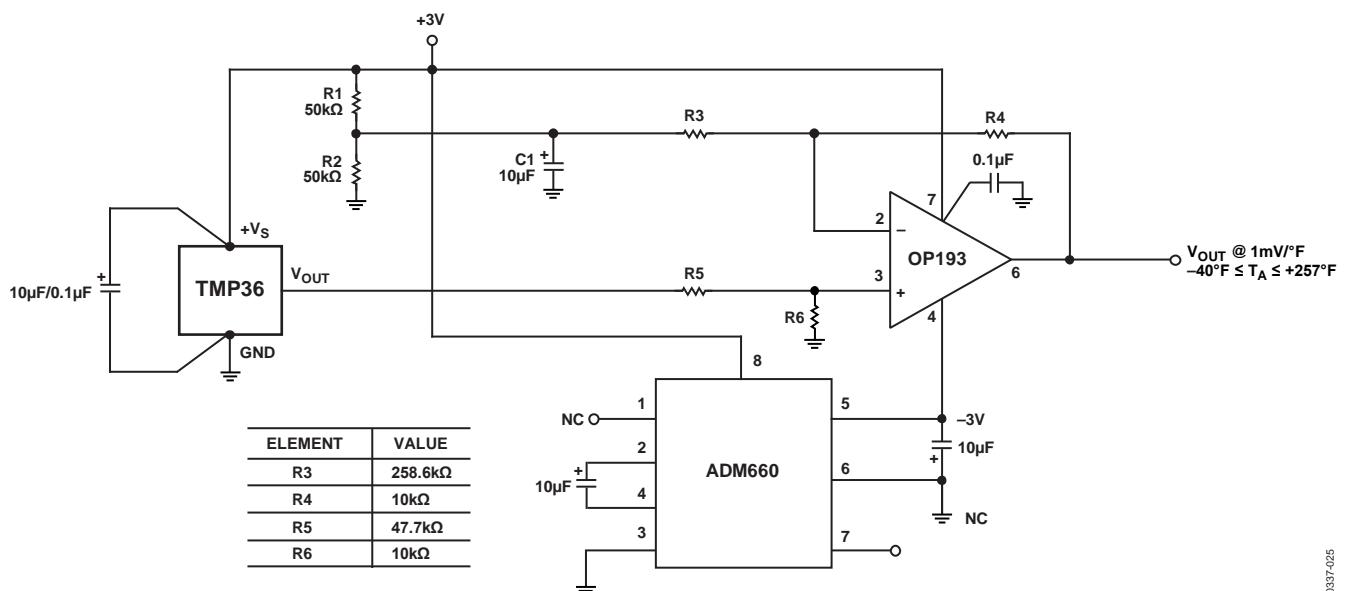


Figure 27. [TMP36](#) Fahrenheit Thermometer Version 2

## AVERAGE AND DIFFERENTIAL TEMPERATURE MEASUREMENT

In many commercial and industrial environments, temperature sensors often measure the average temperature in a building, or the difference in temperature between two locations on a factory floor or in an industrial process. The circuits in Figure 28 and Figure 29 demonstrate an inexpensive approach to average and differential temperature measurement.

In Figure 28, an OP193 sums the outputs of three temperature sensors to produce an output voltage scaled by 10 mV/°C that represents the average temperature at three locations. The circuit can be extended to include as many temperature sensors as required as long as the transfer equation of the circuit is maintained. In this application, it is recommended that one temperature sensor type be used throughout the circuit; otherwise, the output voltage of the circuit cannot produce an accurate reading of the various ambient conditions.

The circuit in Figure 29 illustrates how a pair of TMP35/TMP36/TMP37 sensors used with an OP193 configured as a difference amplifier can read the difference in temperature between two locations. In these applications, it is always possible that one temperature sensor is reading a temperature below that of the other sensor. To accommodate this condition, the output of the OP193 is offset to a voltage at one-half the supply via R5 and R6. Thus, the output voltage of the circuit is measured relative to this point, as shown in Figure 29. Using the TMP36, the output voltage of the circuit is scaled by 10 mV/°C. To minimize the error in the difference between the two measured temperatures, a common, readily available thin-film resistor network is used for R1 to R4.

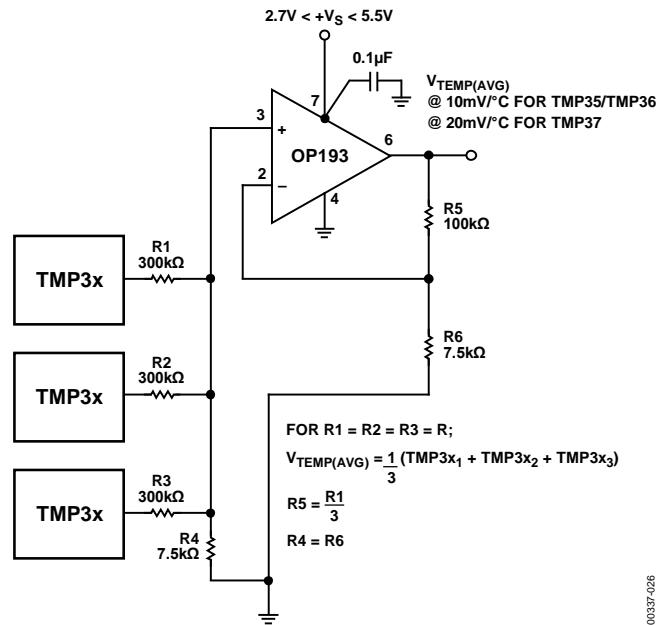
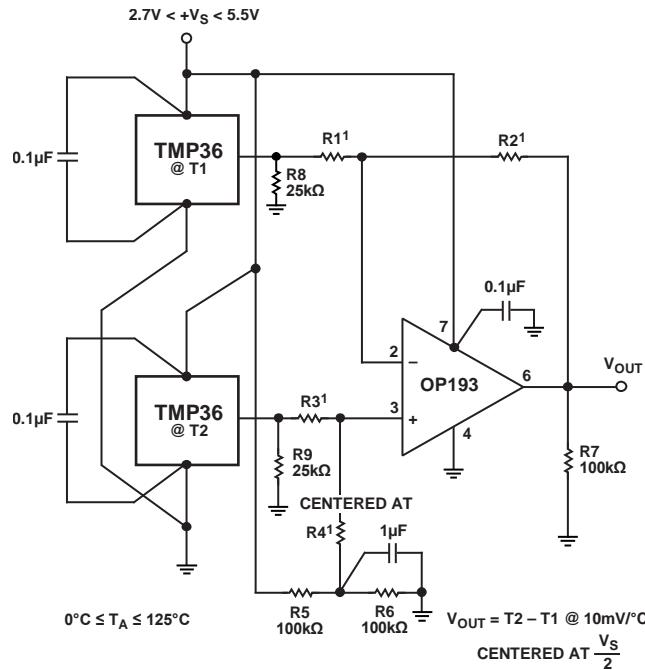


Figure 28. Configuring Multiple Sensors for Average Temperature Measurements

00337-026



NOTE:

<sup>1</sup> R1-R4, CADDOCK T914-100k-100, OR EQUIVALENT.

Figure 29. Configuring Multiple Sensors for Differential Temperature Measurements

00337-027

## MICROPROCESSOR INTERRUPT GENERATOR

These inexpensive temperature sensors can be used with a voltage reference and an analog comparator to configure an interrupt generator for microprocessor applications. With the popularity of fast microprocessors, the need to indicate a microprocessor overtemperature condition has grown tremendously. The circuit in Figure 30 demonstrates one way to generate an interrupt using a **TMP35**, a **CMP402** analog comparator, and a **REF191**, a 2 V precision voltage reference.

The circuit is designed to produce a logic high interrupt signal if the microprocessor temperature exceeds 80°C. This 80°C trip point was arbitrarily chosen (final value set by the microprocessor thermal reference design) and is set using an R3 to R4 voltage divider of the **REF191** output voltage. Because the output of the **TMP35** is scaled by 10 mV/°C, the voltage at the inverting terminal of the **CMP402** is set to 0.8 V.

Because temperature is a slowly moving quantity, the possibility for comparator chatter exists. To avoid this condition, hysteresis is used around the comparator. In this application, a hysteresis of 5°C about the trip point was arbitrarily chosen; the ultimate value for hysteresis should be determined by the end application. The output logic voltage swing of the comparator with R1 and R2 determines the amount of comparator hysteresis. Using a 3.3 V supply, the output logic voltage swing of the **CMP402** is 2.6 V; therefore, for a hysteresis of 5°C (50 mV at 10 mV/°C), R1 is set to 20 kΩ, and R2 is set to 1 MΩ. An expression for the hysteresis of this circuit is given by

$$V_{HYS} = \left( \frac{R1}{R2} \right) (V_{LOGIC SWING, CMP402})$$

Because this circuit is probably used in close proximity to high speed digital circuits, R1 is split into equal values and a 1000 pF capacitor is used to form a low-pass filter on the output of the **TMP35**. Furthermore, to prevent high frequency noise from contaminating the comparator trip point, a 0.1 μF capacitor is used across R4.

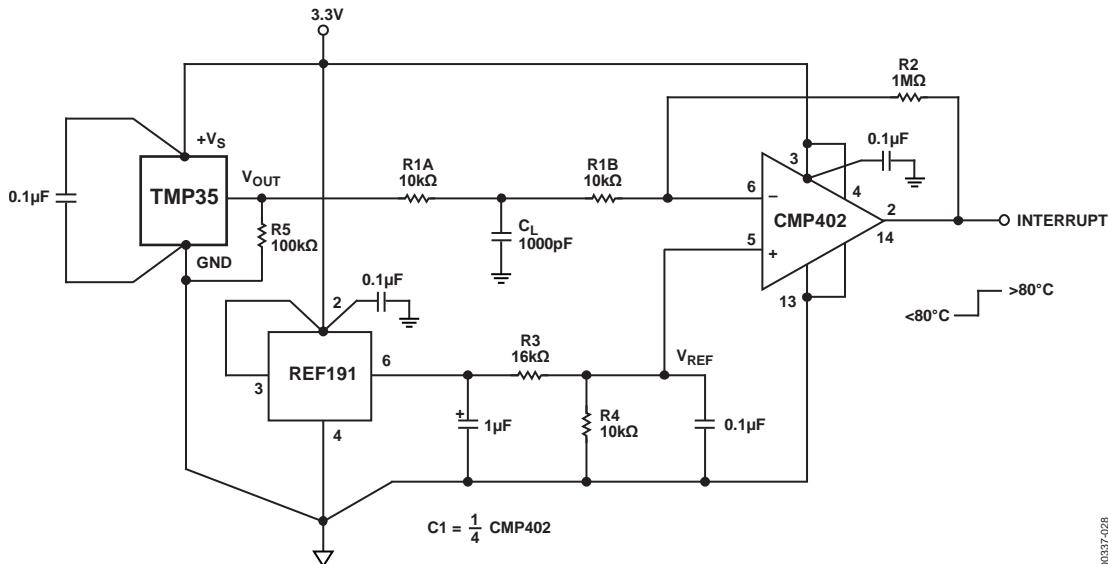


Figure 30. Microprocessor Overtemperature Interrupt Generator

00337-028

## THERMOCOUPLE SIGNAL CONDITIONING WITH COLD-JUNCTION COMPENSATION

The circuit in Figure 31 conditions the output of a Type K thermocouple, while providing cold-junction compensation for temperatures between 0°C and 250°C. The circuit operates from a single 3.3 V to 5.5 V supply and is designed to produce an output voltage transfer characteristic of 10 mV/°C.

A Type K thermocouple exhibits a Seebeck coefficient of approximately 41  $\mu\text{V}/^\circ\text{C}$ ; therefore, at the cold junction, the **TMP35**, with a temperature coefficient of 10 mV/°C, is used with R1 and R2 to introduce an opposing cold-junction temperature coefficient of -41  $\mu\text{V}/^\circ\text{C}$ . This prevents the isothermal, cold-junction connection between the PCB tracks of the circuit

and the wires of the thermocouple from introducing an error in the measured temperature. This compensation works extremely well for circuit ambient temperatures in the range of 20°C to 50°C. Over a 250°C measurement temperature range, the thermocouple produces an output voltage change of 10.151 mV. Because the required output full-scale voltage of the circuit is 2.5 V, the gain of the circuit is set to 246.3. Choosing R4 equal to 4.99 k $\Omega$  sets R5 equal to 1.22 M $\Omega$ . Because the closest 1% value for R5 is 1.21 M $\Omega$ , a 50 k $\Omega$  potentiometer is used with R5 for fine trim of the full-scale output voltage. Although the **OP193** is a superior single-supply, micropower operational amplifier, its output stage is not rail-to-rail; therefore, the 0°C output voltage level is 0.1 V. If this circuit is digitized by a single-supply ADC, the ADC common should be adjusted to 0.1 V accordingly.

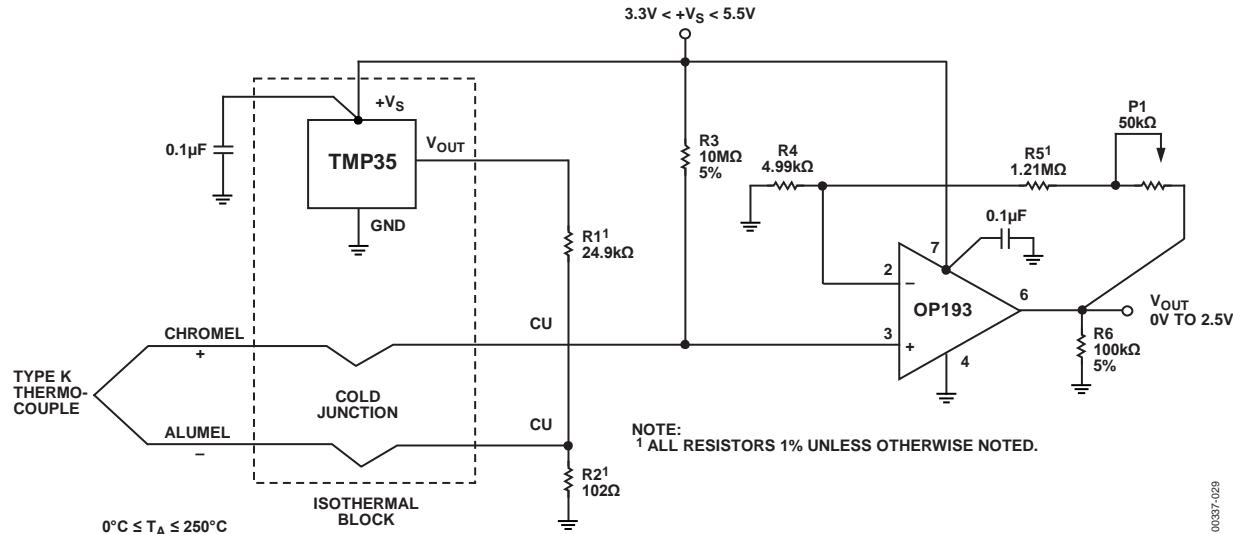


Figure 31. Single-Supply, Type K Thermocouple Signal Conditioning Circuit with Cold-Junction Compensation

00337-029

## USING TMP35/TMP36/TMP37 SENSORS IN REMOTE LOCATIONS

In many industrial environments, sensors are required to operate in the presence of high ambient noise. These noise sources take many forms, for example, SCR transients, relays, radio transmitters, arc welders, and ac motors. They can also be used at considerable distances from the signal conditioning circuitry. These high noise environments are typically in the form of electric fields, so the voltage output of the temperature sensor can be susceptible to contamination from these noise sources.

Figure 32 illustrates a way to convert the output voltage of a TMP35/TMP36/TMP37 sensor into a current to be transmitted down a long twisted pair shielded cable to a ground referenced receiver. The temperature sensors are not capable of high output current operation; thus, a standard PNP transistor is used to boost the output current drive of the circuit. As shown in the table in Figure 32, the values of R2 and R3 were chosen to produce an arbitrary full-scale output current of 2 mA. Lower values for the full-scale current are not recommended. The minimum-scale output current produced by the circuit could be contaminated by ambient magnetic fields operating in the near vicinity of the circuit/cable pair. Because the circuit uses an external transistor, the minimum recommended operating voltage for this circuit is 5 V. To minimize the effects of EMI (or RFI), both the circuit and the temperature sensor supply pins are bypassed with good quality ceramic capacitors.

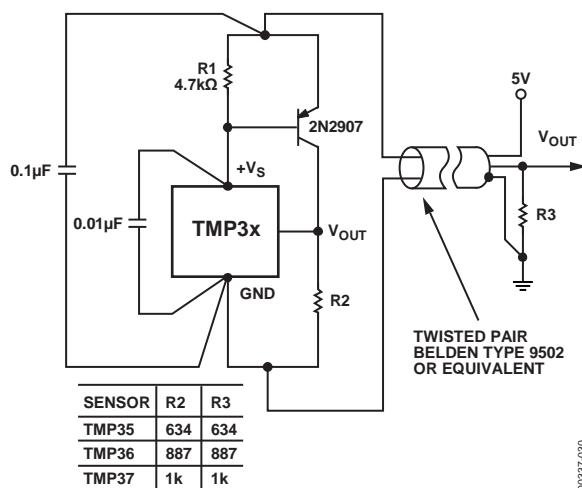


Figure 32. Remote, 2-Wire Boosted Output Current Temperature Sensor

## TEMPERATURE TO 4–20 mA LOOP TRANSMITTER

In many process control applications, 2-wire transmitters are used to convey analog signals through noisy ambient environments. These current transmitters use a zero-scale signal current of 4 mA, which can be used to power the signal conditioning circuitry of the transmitter. The full-scale output signal in these transmitters is 20 mA.

Figure 33 illustrates a circuit that transmits temperature information in this fashion. Using a TMP35/TMP36/TMP37 as the temperature sensor, the output current is linearly proportional to the temperature of the medium. The entire circuit operates from the 3 V output of the REF193. The REF193 requires no external trimming because of its tight initial output voltage tolerance and the low supply current of the TMP35/TMP36/TMP37, the OP193, and the REF193. The entire circuit consumes less than 3 mA from a total budget of 4 mA. The OP193 regulates the output current to satisfy the current summation at the noninverting node of the OP193. A generalized expression for the KCL equation at Pin 3 of the OP193 is given by

$$I_{OUT} = \left( \frac{1}{R_7} \right) \times \left( \frac{\text{TMP3x} \times R_3}{R_1} + \frac{V_{REF} \times R_3}{R_2} \right)$$

For each temperature sensor, Table 5 provides the values for the components P1, P2, and R1 to R4.

Table 5. Circuit Element Values for Loop Transmitter

Sensor	R1	P1	R2	P2	R3	R4
TMP35	97.6 kΩ	5 kΩ	1.58 MΩ	100 kΩ	140 kΩ	56.2 kΩ
TMP36	97.6 kΩ	5 kΩ	931 kΩ	50 kΩ	97.6 kΩ	47 kΩ
TMP37	97.6 kΩ	5 kΩ	10.5 kΩ	500 Ω	84.5 kΩ	8.45 kΩ

The 4 mA offset trim is provided by P2, and P1 provides the full-scale gain trim of the circuit at 20 mA. These two trims do not interact because the noninverting input of the OP193 is held at a virtual ground. The zero-scale and full-scale output currents of the circuit are adjusted according to the operating temperature range of each temperature sensor. The Schottky diode, D1, is required in this circuit to prevent loop supply power-on transients from pulling the noninverting input of the OP193 more than 300 mV below its inverting input. Without this diode, such transients can cause phase reversal of the operational amplifier and possible latch-up of the transmitter. The loop supply voltage compliance of the circuit is limited by the maximum applied input voltage to the REF193; it is from 9 V to 18 V.

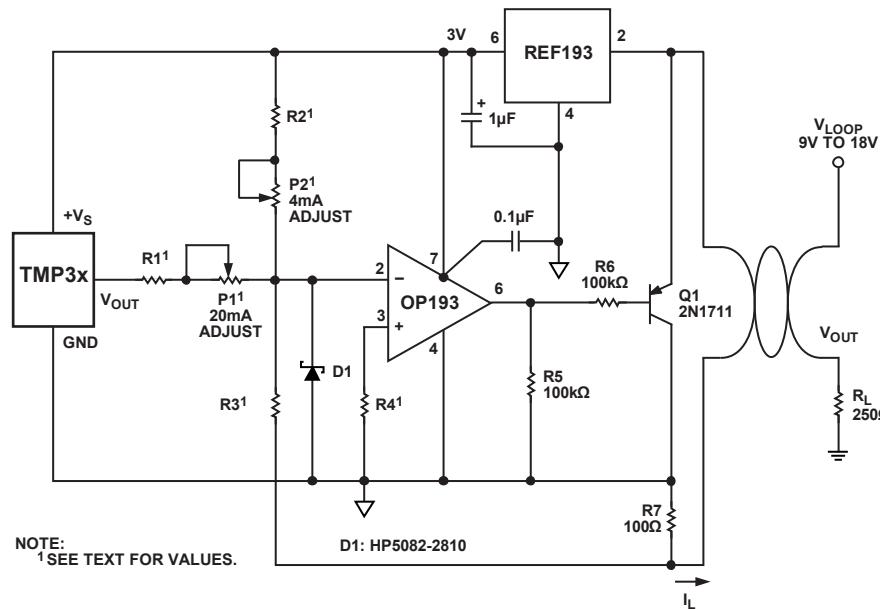


Figure 33. Temperature to 4–20 mA Loop Transmitter

## TEMPERATURE-TO-FREQUENCY CONVERTER

Another common method of transmitting analog information from a remote location is to convert a voltage to an equivalent value in the frequency domain. This is readily done with any of the low cost, monolithic voltage-to-frequency converters (VFCs) available. These VFCs feature a robust, open-collector output transistor for easy interfacing to digital circuitry. The digital signal produced by the VFC is less susceptible to contamination from external noise sources and line voltage drops because the only important information is the frequency of the digital signal. When the conversions between temperature and frequency are done accurately, the temperature data from the sensors can be reliably transmitted.

The circuit in Figure 34 illustrates a method by which the outputs of these temperature sensors can be converted to a frequency using the AD654. The output signal of the AD654 is a square wave that is proportional to the dc input voltage across Pin 4 and Pin 3. The transfer equation of the circuit is given by

$$f_{OUT} = \left( \frac{V_{TPM} - V_{OFFSET}}{10 \times (R_T \times C_T)} \right)$$

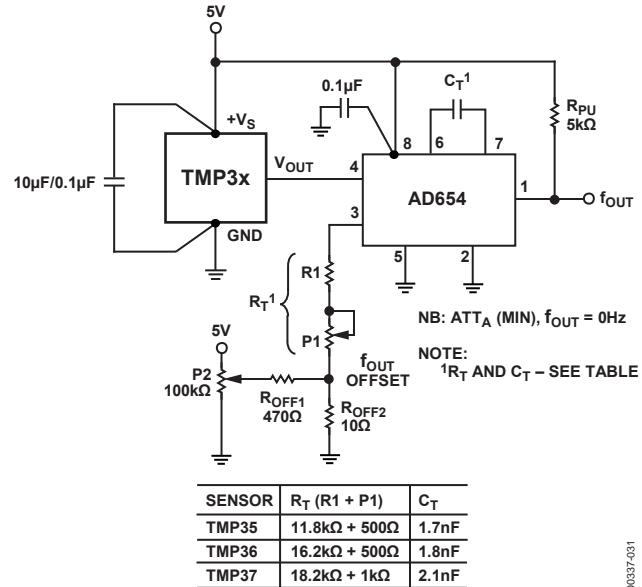


Figure 34. Temperature-to-Frequency Converter

An offset trim network ( $f_{\text{OUT OFFSET}}$ ) is included with this circuit to set  $f_{\text{OUT}}$  to 0 Hz when the minimum output voltage of the temperature sensor is reached. Potentiometer P1 is required to calibrate the absolute accuracy of the [AD654](#). The table in Figure 34 illustrates the circuit element values for each of the three sensors. The nominal offset voltage required for 0 Hz output from the [TMP35](#) is 50 mV; for the [TMP36](#) and [TMP37](#), the offset voltage required is 100 mV. For the circuit values shown, the output frequency transfer characteristic of the circuit was set at 50 Hz/ $^{\circ}\text{C}$  in all cases. At the receiving end, a frequency-to-voltage converter (FVC) can be used to convert the frequency back to a dc voltage for further processing. One such FVC is the [AD650](#).

For complete information about the [AD650](#) and the [AD654](#), consult the individual data sheets for those devices.

### DRIVING LONG CABLES OR HEAVY CAPACITIVE LOADS

Although the [TMP35/TMP36/TMP37](#) temperature sensors can drive capacitive loads up to 10,000 pF without oscillation, output voltage transient response times can be improved by using a small resistor in series with the output of the temperature sensor, as shown in Figure 35. As an added benefit, this resistor forms a low-pass filter with the cable capacitance, which helps to reduce bandwidth noise. Because the temperature sensor is likely to be used in environments where the ambient noise level can be very high, this resistor helps to prevent rectification by the devices of the high frequency noise. The combination of this resistor and the supply bypass capacitor offers the best protection.

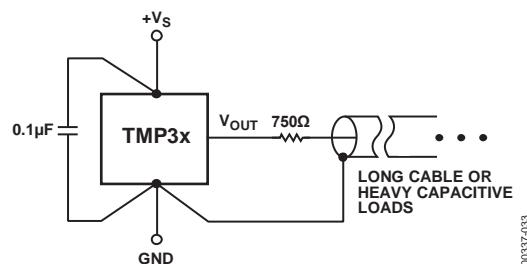


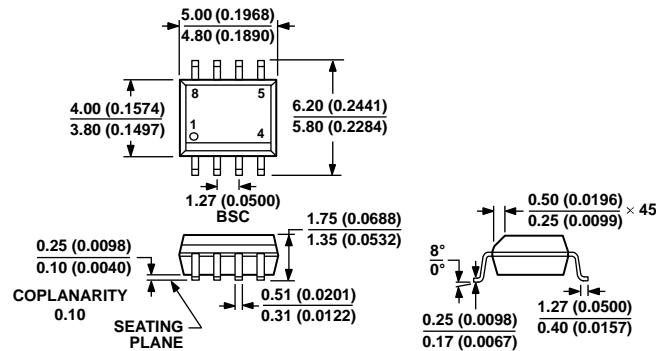
Figure 35. Driving Long Cables or Heavy Capacitive Loads

### COMMENTARY ON LONG-TERM STABILITY

The concept of long-term stability has been used for many years to describe the amount of parameter shift that occurs during the lifetime of an IC. This is a concept that has been typically applied to both voltage references and monolithic temperature sensors. Unfortunately, integrated circuits cannot be evaluated at room temperature (25°C) for 10 years or more to determine this shift. As a result, manufacturers very typically perform accelerated lifetime testing of integrated circuits by operating ICs at elevated temperatures (between 125°C and 150°C) over a shorter period of time (typically, between 500 and 1000 hours).

As a result of this operation, the lifetime of an integrated circuit is significantly accelerated due to the increase in rates of reaction within the semiconductor material.

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

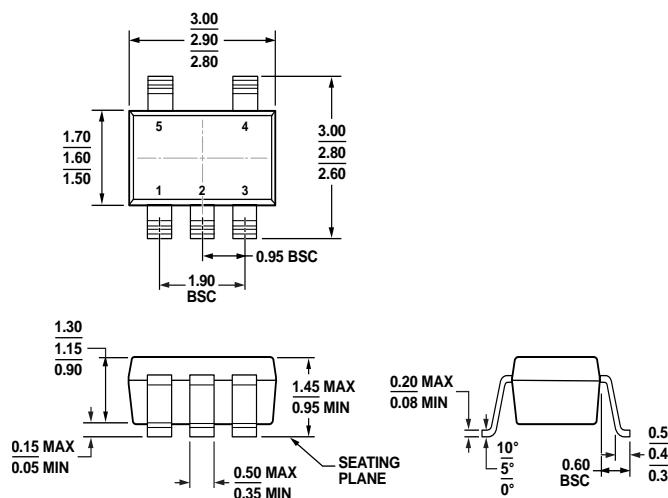
01207-A

Figure 36. 8-Lead Standard Small Outline Package [SOIC\_N]

Narrow Body

(R-8)

Dimensions shown in millimeters and (inches)



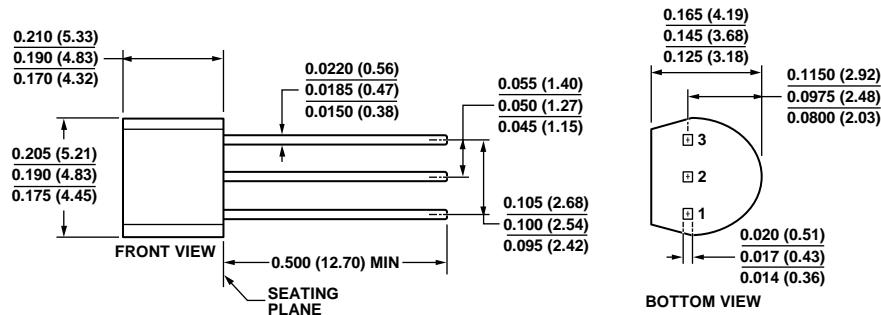
COMPLIANT TO JEDEC STANDARDS MO-178-AA

Figure 37. 5-Lead Small Outline Transistor Package [SOT-23]

(RJ-5)

Dimensions shown in millimeters

11-01-2010-A



COMPLIANT TO JEDEC STANDARDS TO-226-AA  
 CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

04208-A

Figure 38. 3-Pin Plastic Header-Style Package [TO-92]

(T-3-1)

Dimensions shown in inches and (millimeters)

## ORDERING GUIDE

Model <sup>1, 2</sup>	Accuracy at 25°C (°C max)	Linear Operating Temperature Range	Package Description	Package Option	Branding
TMP35FSZ-REEL	±2.0	10°C to 125°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8	
TMP35GRTZ-REEL7	±3.0	10°C to 125°C	5-Lead Small Outline Transistor Package (SOT-23)	RJ-5	#T11
TMP35GT9Z	±3.0	10°C to 125°C	3-Pin Plastic Header-Style Package (TO-92)	T-3-1	
ADW75001Z-0REEL7	±3.0	-40°C to +125°C	5-Lead Small Outline Transistor Package (SOT-23)	RJ-5	#T6G
TMP36FS	±2.0	-40°C to +125°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8	
TMP36FS-REEL	±2.0	-40°C to +125°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8	
TMP36FSZ	±2.0	-40°C to +125°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8	
TMP36FSZ-REEL	±2.0	-40°C to +125°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8	
TMP36GRT-REEL7	±3.0	-40°C to +125°C	5-Lead Small Outline Transistor Package (SOT-23)	RJ-5	T6G
TMP36GRTZ-REEL7	±3.0	-40°C to +125°C	5-Lead Small Outline Transistor Package (SOT-23)	RJ-5	#T6G
TMP36GSZ	±3.0	-40°C to +125°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8	
TMP36GSZ-REEL	±3.0	-40°C to +125°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8	
TMP36GSZ-REEL7	±3.0	-40°C to +125°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8	
TMP36GT9	±3.0	-40°C to +125°C	3-Pin Plastic Header-Style Package (TO-92)	T-3-1	
TMP36GT9Z	±3.0	-40°C to +125°C	3-Pin Plastic Header-Style Package (TO-92)	T-3-1	
TMP36-PT7		-40°C to +125°C	Chips or Die		
TMP37FT9Z	±2.0	5°C to 100°C	3-Pin Plastic Header-Style Package (TO-92)	T-3-1	
TMP37GRTZ-REEL7	±3.0	5°C to 100°C	5-Lead Small Outline Transistor Package (SOT-23)	RJ-5	#T12

<sup>1</sup> Z = RoHS Compliant Part.<sup>2</sup> W = Qualified for Automotive Applications.

## AUTOMOTIVE PRODUCTS

The ADW75001Z-0REEL7 model is available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that this automotive model may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

# P2N2222A

## Amplifier Transistors

### NPN Silicon

#### Features

- These are Pb-Free Devices\*

**MAXIMUM RATINGS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO}$	40	Vdc
Collector-Base Voltage	$V_{CBO}$	75	Vdc
Emitter-Base Voltage	$V_{EBO}$	6.0	Vdc
Collector Current - Continuous	$I_C$	600	mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	625 5.0	mW mW/ $^\circ\text{C}$
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	1.5 12	W mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

#### THERMAL CHARACTERISTICS

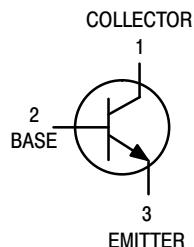
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	$^\circ\text{C}/\text{W}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

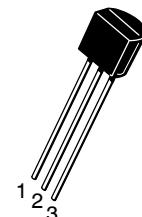


**ON Semiconductor®**

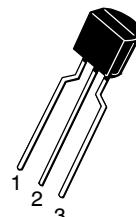
<http://onsemi.com>



TO-92  
CASE 29  
STYLE 17

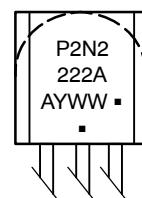


STRAIGHT LEAD  
BULK PACK



BENT LEAD  
TAPE & REEL  
AMMO PACK

#### MARKING DIAGRAM



A = Assembly Location

Y = Year

WW = Work Week

■ = Pb-Free Package

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
P2N2222AG	TO-92 (Pb-Free)	5000 Units/Bulk
P2N2222ARL1G	TO-92 (Pb-Free)	2000/Tape & Ammo

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# P2N222A

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector – Emitter Breakdown Voltage ( $I_C = 10 \mu\text{Adc}$ , $I_B = 0$ )	$V_{(\text{BR})\text{CEO}}$	40	–	Vdc
Collector – Base Breakdown Voltage ( $I_C = 10 \mu\text{Adc}$ , $I_E = 0$ )	$V_{(\text{BR})\text{CBO}}$	75	–	Vdc
Emitter – Base Breakdown Voltage ( $I_E = 10 \mu\text{Adc}$ , $I_C = 0$ )	$V_{(\text{BR})\text{EBO}}$	6.0	–	Vdc
Collector Cutoff Current ( $V_{CE} = 60 \text{ Vdc}$ , $V_{EB(\text{off})} = 3.0 \text{ Vdc}$ )	$I_{\text{CEX}}$	–	10	nAdc
Collector Cutoff Current ( $V_{CB} = 60 \text{ Vdc}$ , $I_E = 0$ ) ( $V_{CB} = 60 \text{ Vdc}$ , $I_E = 0$ , $T_A = 150^\circ\text{C}$ )	$I_{\text{CBO}}$	– –	0.01 10	$\mu\text{Adc}$
Emitter Cutoff Current ( $V_{EB} = 3.0 \text{ Vdc}$ , $I_C = 0$ )	$I_{\text{EBO}}$	–	10	nAdc
Collector Cutoff Current ( $V_{CE} = 10 \text{ V}$ )	$I_{\text{CEO}}$	–	10	nAdc
Base Cutoff Current ( $V_{CE} = 60 \text{ Vdc}$ , $V_{EB(\text{off})} = 3.0 \text{ Vdc}$ )	$I_{\text{BEX}}$	–	20	nAdc

## ON CHARACTERISTICS

DC Current Gain ( $I_C = 0.1 \text{ mAdc}$ , $V_{CE} = 10 \text{ Vdc}$ ) ( $I_C = 1.0 \text{ mAdc}$ , $V_{CE} = 10 \text{ Vdc}$ ) ( $I_C = 10 \text{ mAdc}$ , $V_{CE} = 10 \text{ Vdc}$ ) ( $I_C = 10 \text{ mAdc}$ , $V_{CE} = 10 \text{ Vdc}$ , $T_A = -55^\circ\text{C}$ ) ( $I_C = 150 \text{ mAdc}$ , $V_{CE} = 10 \text{ Vdc}$ ) (Note 1) ( $I_C = 150 \text{ mAdc}$ , $V_{CE} = 1.0 \text{ Vdc}$ ) (Note 1) ( $I_C = 500 \text{ mAdc}$ , $V_{CE} = 10 \text{ Vdc}$ ) (Note 1)	$h_{FE}$	35 50 75 35 100 50 40	– – – – 300 – –	–
Collector – Emitter Saturation Voltage (Note 1) ( $I_C = 150 \text{ mAdc}$ , $I_B = 15 \text{ mAdc}$ ) ( $I_C = 500 \text{ mAdc}$ , $I_B = 50 \text{ mAdc}$ )	$V_{CE(\text{sat})}$	– –	0.3 1.0	Vdc
Base – Emitter Saturation Voltage (Note 1) ( $I_C = 150 \text{ mAdc}$ , $I_B = 15 \text{ mAdc}$ ) ( $I_C = 500 \text{ mAdc}$ , $I_B = 50 \text{ mAdc}$ )	$V_{BE(\text{sat})}$	0.6 –	1.2 2.0	Vdc

## SMALL-SIGNAL CHARACTERISTICS

Current – Gain – Bandwidth Product (Note 2) ( $I_C = 20 \text{ mAdc}$ , $V_{CE} = 20 \text{ Vdc}$ , $f = 100 \text{ MHz}$ )C	$f_T$	300	–	MHz
Output Capacitance ( $V_{CB} = 10 \text{ Vdc}$ , $I_E = 0$ , $f = 1.0 \text{ MHz}$ )	$C_{\text{obo}}$	–	8.0	pF
Input Capacitance ( $V_{EB} = 0.5 \text{ Vdc}$ , $I_C = 0$ , $f = 1.0 \text{ MHz}$ )	$C_{\text{ibo}}$	–	25	pF
Input Impedance ( $I_C = 1.0 \text{ mAdc}$ , $V_{CE} = 10 \text{ Vdc}$ , $f = 1.0 \text{ kHz}$ ) ( $I_C = 10 \text{ mAdc}$ , $V_{CE} = 10 \text{ Vdc}$ , $f = 1.0 \text{ kHz}$ )	$h_{ie}$	2.0 0.25	8.0 1.25	kΩ
Voltage Feedback Ratio ( $I_C = 1.0 \text{ mAdc}$ , $V_{CE} = 10 \text{ Vdc}$ , $f = 1.0 \text{ kHz}$ ) ( $I_C = 10 \text{ mAdc}$ , $V_{CE} = 10 \text{ Vdc}$ , $f = 1.0 \text{ kHz}$ )	$h_{re}$	– –	8.0 4.0	$\times 10^{-4}$
Small-Signal Current Gain ( $I_C = 1.0 \text{ mAdc}$ , $V_{CE} = 10 \text{ Vdc}$ , $f = 1.0 \text{ kHz}$ ) ( $I_C = 10 \text{ mAdc}$ , $V_{CE} = 10 \text{ Vdc}$ , $f = 1.0 \text{ kHz}$ )	$h_{fe}$	50 75	300 375	–
Output Admittance ( $I_C = 1.0 \text{ mAdc}$ , $V_{CE} = 10 \text{ Vdc}$ , $f = 1.0 \text{ kHz}$ ) ( $I_C = 10 \text{ mAdc}$ , $V_{CE} = 10 \text{ Vdc}$ , $f = 1.0 \text{ kHz}$ )	$h_{oe}$	5.0 25	35 200	$\mu\text{Mhos}$
Collector Base Time Constant ( $I_E = 20 \text{ mAdc}$ , $V_{CB} = 20 \text{ Vdc}$ , $f = 31.8 \text{ MHz}$ )	$r_b' C_c$	–	150	ps
Noise Figure ( $I_C = 100 \mu\text{Adc}$ , $V_{CE} = 10 \text{ Vdc}$ , $R_S = 1.0 \text{ k}\Omega$ , $f = 1.0 \text{ kHz}$ )	$N_F$	–	4.0	dB

1. Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

2.  $f_T$  is defined as the frequency at which  $|h_{fe}|$  extrapolates to unity.

# P2N222A

ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$  unless otherwise noted) (Continued)

Characteristic	Symbol	Min	Max	Unit
<b>SWITCHING CHARACTERISTICS</b>				
Delay Time ( $V_{CC} = 30 \text{ Vdc}$ , $V_{BE(\text{off})} = -2.0 \text{ Vdc}$ , $I_C = 150 \text{ mAdc}$ , $I_{B1} = 15 \text{ mAdc}$ ) (Figure 1)	$t_d$	—	10	ns
Rise Time ( $V_{CC} = 30 \text{ Vdc}$ , $I_C = 150 \text{ mAdc}$ , $I_{B1} = I_{B2} = 15 \text{ mAdc}$ ) (Figure 2)	$t_r$	—	25	ns
Storage Time ( $V_{CC} = 30 \text{ Vdc}$ , $I_C = 150 \text{ mAdc}$ , $I_{B1} = I_{B2} = 15 \text{ mAdc}$ ) (Figure 2)	$t_s$	—	225	ns
Fall Time ( $V_{CC} = 30 \text{ Vdc}$ , $I_C = 150 \text{ mAdc}$ , $I_{B1} = I_{B2} = 15 \text{ mAdc}$ ) (Figure 2)	$t_f$	—	60	ns

## SWITCHING TIME EQUIVALENT TEST CIRCUITS

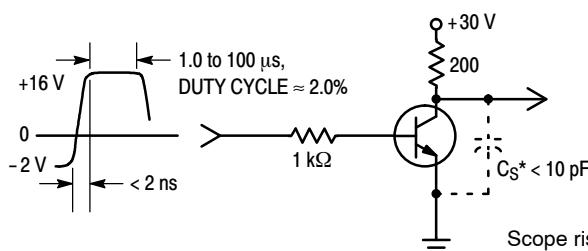


Figure 1. Turn-On Time

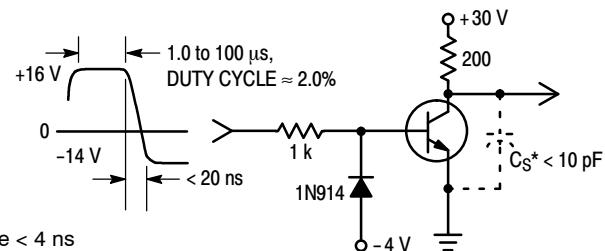


Figure 2. Turn-Off Time

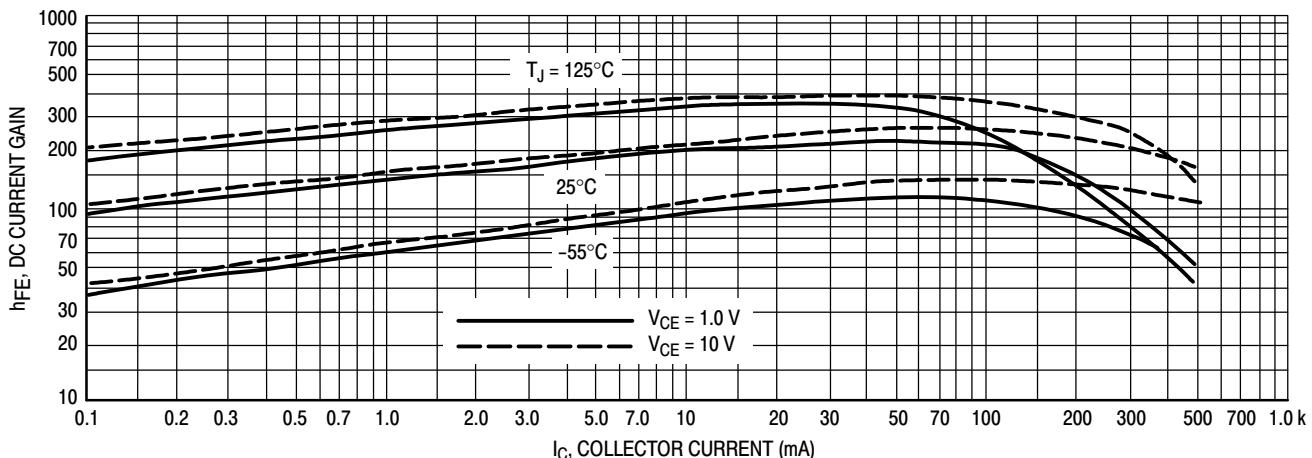


Figure 3. DC Current Gain

# P2N2222A

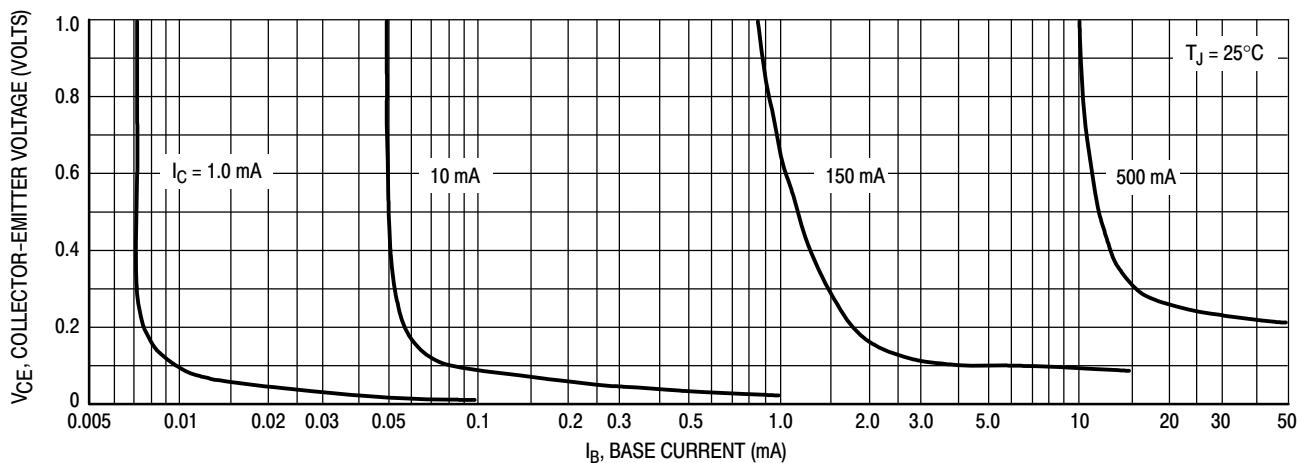


Figure 4. Collector Saturation Region

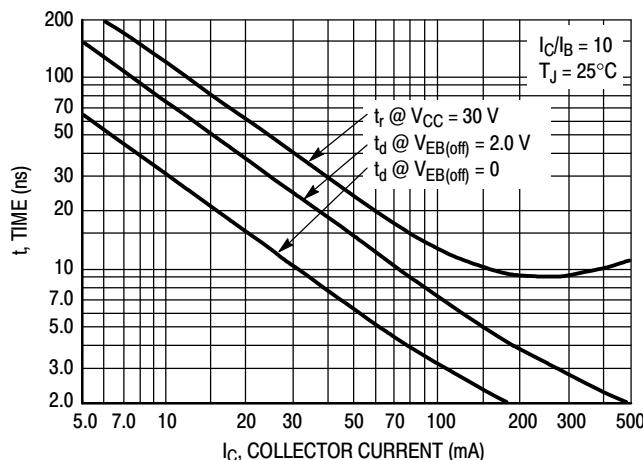


Figure 5. Turn-On Time

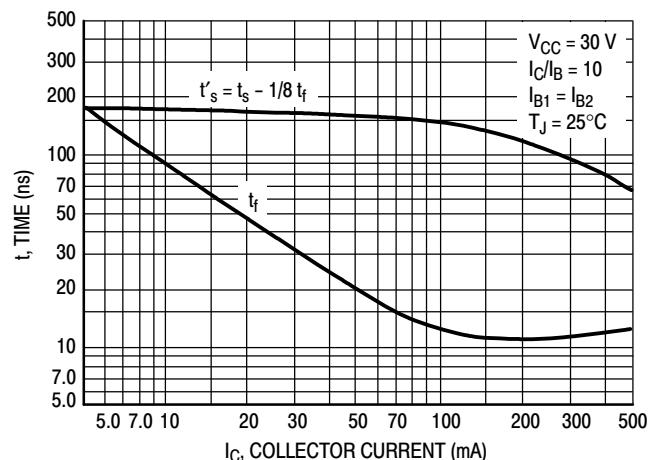


Figure 6. Turn-Off Time

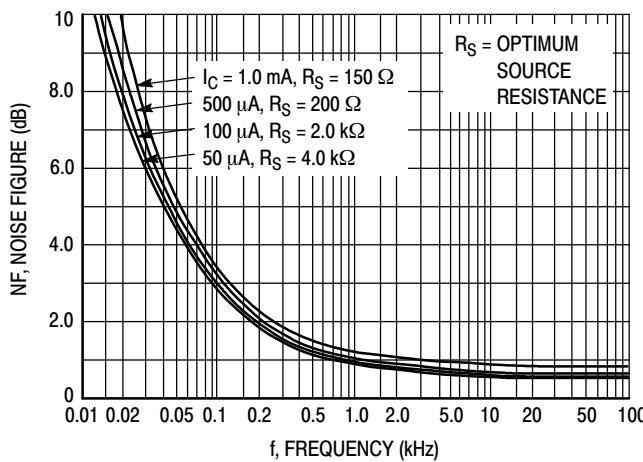


Figure 7. Frequency Effects

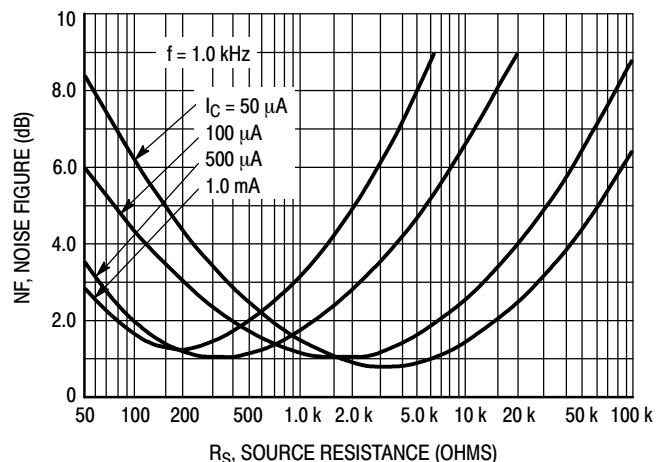
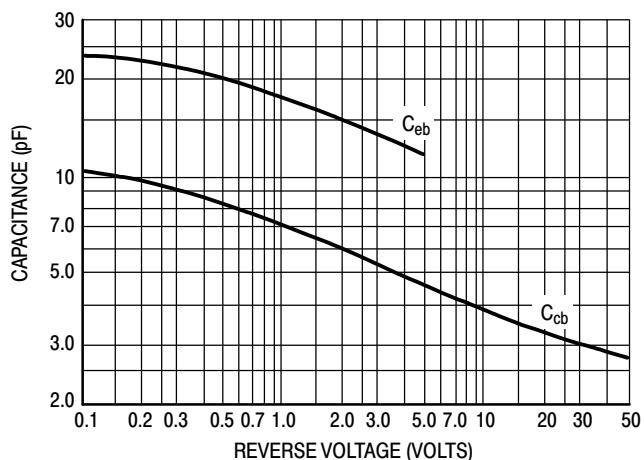
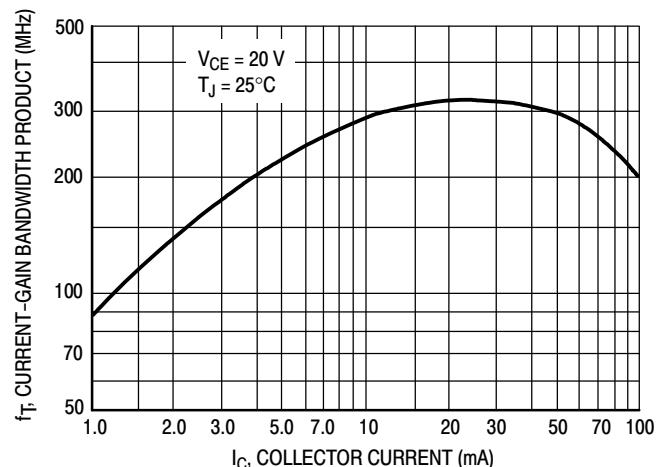


Figure 8. Source Resistance Effects

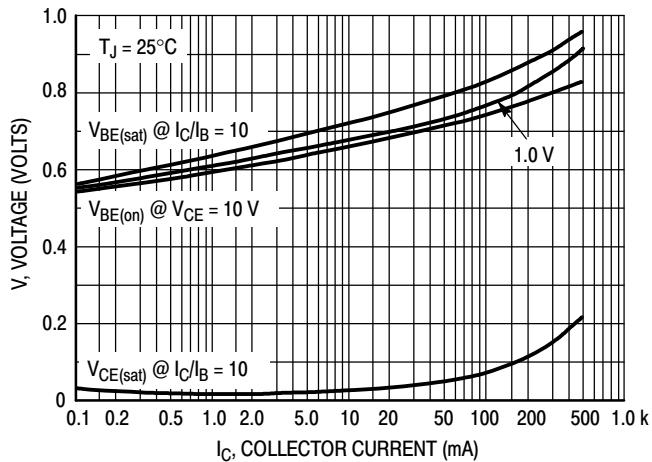
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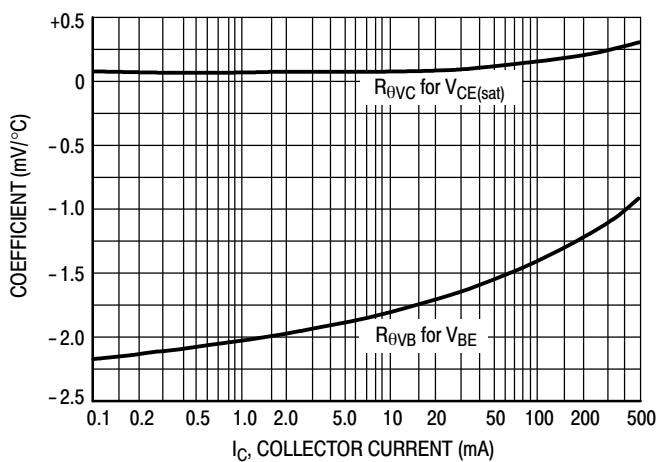
**Figure 9. Capacitances**



**Figure 10. Current-Gain Bandwidth Product**



**Figure 11. "On" Voltages**

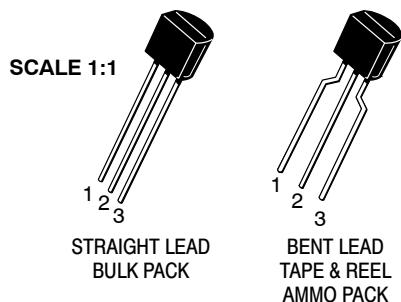


**Figure 12. Temperature Coefficients**

# MECHANICAL CASE OUTLINE

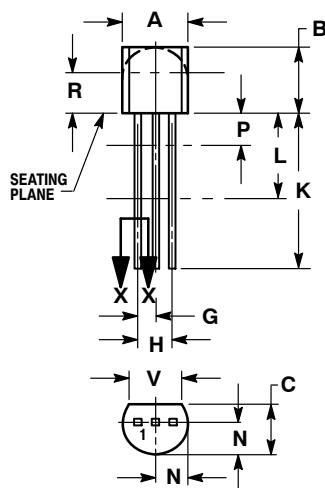
## PACKAGE DIMENSIONS

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CASE 29-11  
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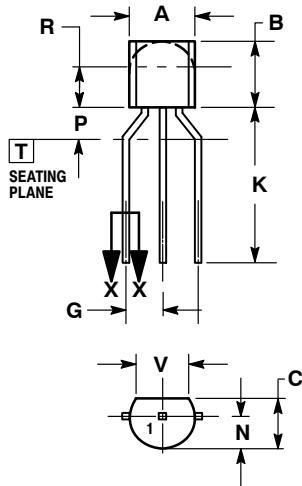


STRAIGHT LEAD  
BULK PACK

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
  4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---

SECTION X-X



BENT LEAD  
TAPE & REEL  
AMMO PACK

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
  4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	MILLIMETERS	
	MIN	MAX
A	4.45	5.20
B	4.32	5.33
C	3.18	4.19
D	0.40	0.54
G	2.40	2.80
J	0.39	0.50
K	12.70	---
N	2.04	2.66
P	1.50	4.00
R	2.93	---
V	3.43	---

SECTION X-X

STYLES ON PAGE 2

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**TO-92 (TO-226)**

CASE 29-11

ISSUE AM

DATE 09 MAR 2007

<b>STYLE 1:</b> PIN 1. Emitter 2. Base 3. Collector	<b>STYLE 2:</b> PIN 1. Base 2. Emitter 3. Collector	<b>STYLE 3:</b> PIN 1. Anode 2. Anode 3. Cathode	<b>STYLE 4:</b> PIN 1. Cathode 2. Cathode 3. Anode	<b>STYLE 5:</b> PIN 1. Drain 2. Source 3. Gate
<b>STYLE 6:</b> PIN 1. Gate 2. Source & Substrate 3. Drain	<b>STYLE 7:</b> PIN 1. Source 2. Drain 3. Gate	<b>STYLE 8:</b> PIN 1. Drain 2. Gate 3. Source & Substrate	<b>STYLE 9:</b> PIN 1. Base 1 2. Emitter 3. Base 2	<b>STYLE 10:</b> PIN 1. Cathode 2. Gate 3. Anode
<b>STYLE 11:</b> PIN 1. Anode 2. Cathode & Anode 3. Cathode	<b>STYLE 12:</b> PIN 1. Main Terminal 1 2. Gate 3. Main Terminal 2	<b>STYLE 13:</b> PIN 1. Anode 1 2. Gate 3. Cathode 2	<b>STYLE 14:</b> PIN 1. Emitter 2. Collector 3. Base	<b>STYLE 15:</b> PIN 1. Anode 1 2. Cathode 3. Anode 2
<b>STYLE 16:</b> PIN 1. Anode 2. Gate 3. Cathode	<b>STYLE 17:</b> PIN 1. Collector 2. Base 3. Emitter	<b>STYLE 18:</b> PIN 1. Anode 2. Cathode 3. Not Connected	<b>STYLE 19:</b> PIN 1. Gate 2. Anode 3. Cathode	<b>STYLE 20:</b> PIN 1. Not Connected 2. Cathode 3. Anode
<b>STYLE 21:</b> PIN 1. Collector 2. Emitter 3. Base	<b>STYLE 22:</b> PIN 1. Source 2. Gate 3. Drain	<b>STYLE 23:</b> PIN 1. Gate 2. Source 3. Drain	<b>STYLE 24:</b> PIN 1. Emitter 2. Collector/Anode 3. Cathode	<b>STYLE 25:</b> PIN 1. MT 1 2. Gate 3. MT 2
<b>STYLE 26:</b> PIN 1. V <sub>CC</sub> 2. Ground 2 3. Output	<b>STYLE 27:</b> PIN 1. MT 2. Substrate 3. MT	<b>STYLE 28:</b> PIN 1. Cathode 2. Anode 3. Gate	<b>STYLE 29:</b> PIN 1. Not Connected 2. Anode 3. Cathode	<b>STYLE 30:</b> PIN 1. Drain 2. Gate 3. Source
<b>STYLE 31:</b> PIN 1. Gate 2. Drain 3. Source	<b>STYLE 32:</b> PIN 1. Base 2. Collector 3. Emitter	<b>STYLE 33:</b> PIN 1. Return 2. Input 3. Output	<b>STYLE 34:</b> PIN 1. Input 2. Ground 3. Logic	<b>STYLE 35:</b> PIN 1. Gate 2. Collector 3. Emitter

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<b>DESCRIPTION:</b>	TO-92 (TO-226)	<b>PAGE 2 OF 3</b>

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**PAGE 3 OF 3**

<b>ISSUE</b>	<b>REVISION</b>	<b>DATE</b>
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