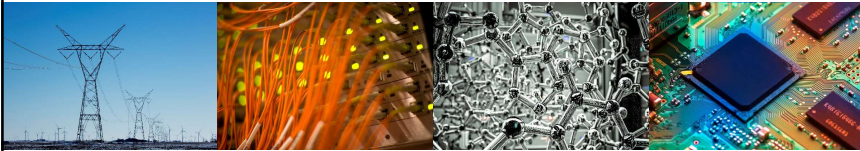


# ECE408/CS483/CSE408 Spring 2020

## Convolutional Neural Networks



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## Objective

- To learn to implement the different types of layers in a Convolutional Neural Network (CNN)

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## MLP (Multi-Layer Perceptron) for an Image

Consider a 250 x 250 image...

- input: 2D image treated as 1D vector
- Fully connected layer is huge:
  - 62,500 ( $250^2$ ) weights per node!
  - Comparable number of nodes gives ~4B weights total!
- Need >1 hidden layer? Bigger images?
- Too much computation, and too much memory.

Traditional feature detection in image processing uses

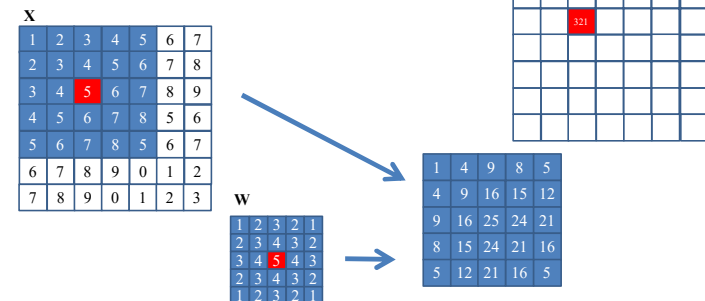
- Filters → Convolution kernels
- Can we use them in neural networks?

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## 2-D Convolution

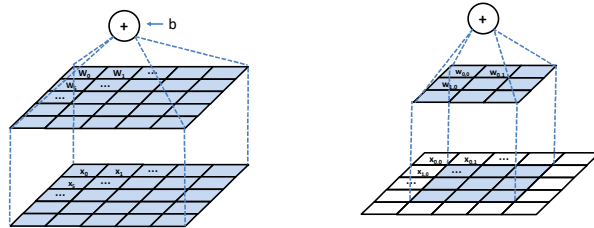


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## Convolution vs Fully-Connected (Weight Sharing)



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## Convolution Naturally Supports Varying Input Sizes

- As discussed so far,
  - perceptron layers have fixed structure, so
  - number of inputs / outputs is fixed.
- Convolution enables variably-sized inputs (observations of the same kind of thing)
  - Audio recording of different lengths
  - Image with more/fewer pixels

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## Example Convolution Inputs

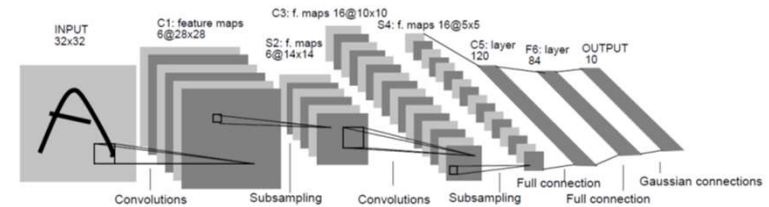
	Single-channel	Multi-channel
1D	audio waveform	Skeleton animation data: 1-D joint angles for each joint
2D	Fourier-transformed audio data Convolve over frequency axis: invariant to frequency shifts Convolve over time axis: invariant to shifts in time	Color image data: 2D data for R,G,B channels
3D	Volumetric data (example: medical imaging)	Color video: 2D data across 1D time for R,G,B channels

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Deeplearningbook.org, ch 9, p 355

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## LeNet-5: CNN for hand-written digit recognition



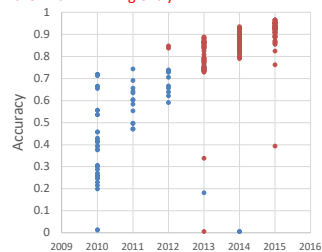
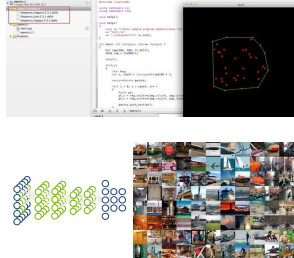
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## Deep Learning Impact in Computer Vision

The Toronto team used GPUs and trained on 1.2M images in their 2012 winning entry.



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## Anatomy of a Convolution Layer

Input features/channels

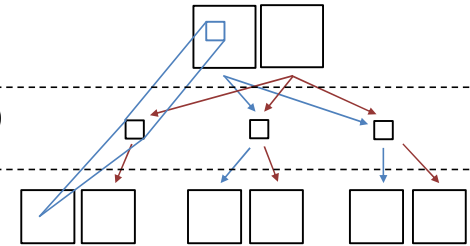
- A inputs ( $N_1 \times N_2$ )

Convolution Layer (or per channel)

- B convolution kernels ( $K_1 \times K_2$ )

Output Features/channels  
(or summed over channels)

- A × B outputs  
 $(N_1 - K_1 + 1) \times (N_2 - K_2 + 1)$



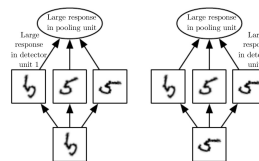
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## 2-D Pooling (Subsampling)

- A subsampling layer
  - Sometimes with bias and non-linearity built in
- Common types: max, average,  $L^2$  norm, weighted average
- Helps make representation invariant to size scaling and small translations in the input



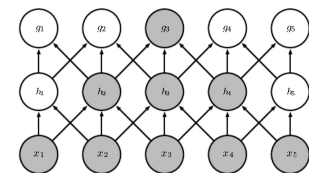
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## Why Convolution (1)

- Sparse interactions
  - Meaningful features in small spatial regions
  - Need fewer parameters (less storage, better statistical characteristics, faster training)
  - Need multiple layers for wide receptive field



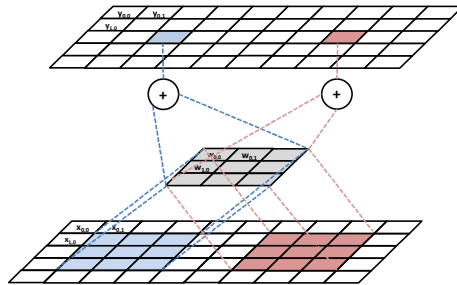
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## Why Convolution (2)

- Parameter sharing
  - Kernel is reused when computing layer output
- Equivariant Representations
  - If input is translated, output is translated the same way
  - Map of where features appear in input



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## Convolution

- 2-D Matrix
- $Y = W \otimes X$
- Kernel smaller than input: smaller receptive field
- Fewer Weights

## Multi-Layer Percep.

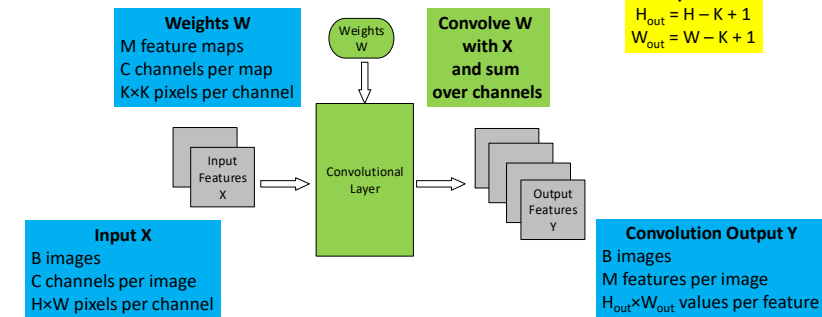
- Vector
- $Y = w x + b$
- Maximum receptive field
- More weights

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## Forward Propagation

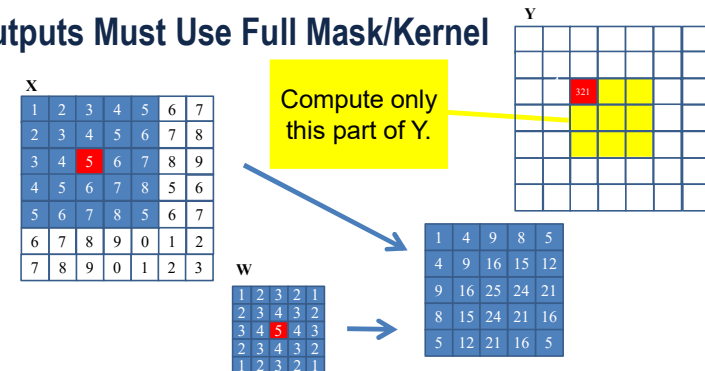


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## Outputs Must Use Full Mask/Kernel

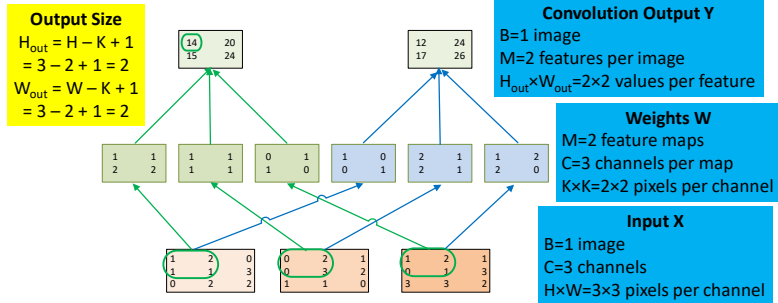


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## Example of the Forward Path of a Convolution Layer



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## Sequential Code: Forward Convolutional Layer

```
void convLayer_forward(int B, int M, int C, int H, int W, int K, float* X, float* W, float* Y) {
    int H_out = H - K + 1; // calculate H_out, W_out
    int W_out = W - K + 1;

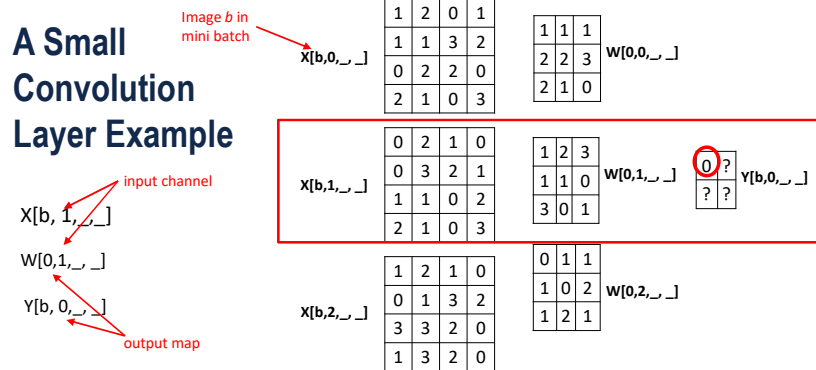
    for (int b = 0; b < B; ++b) // for each image
        for (int m = 0; m < M; ++m) // for each output feature map
            for (int h = 0; h < H_out; ++h) // for each output value (two loops)
                for (int w = 0; w < W_out; ++w) {
                    Y[b, m, h, w] = 0.0f; // initialize sum to 0
                    for (int c = 0; c < C; ++c) // sum over all input channels
                        for (int p = 0; p < K; ++p) // KxK filter
                            for (int q = 0; q < K; ++q)
                                Y[b, m, h, w] += X[b, c, h + p, w + q] * W[m, c, p, q];
                }
    }
```

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## A Small Convolution Layer Example



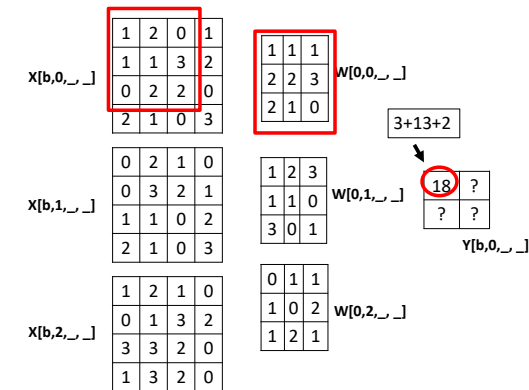
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## A Small Convolution Layer Example

$c = 0$

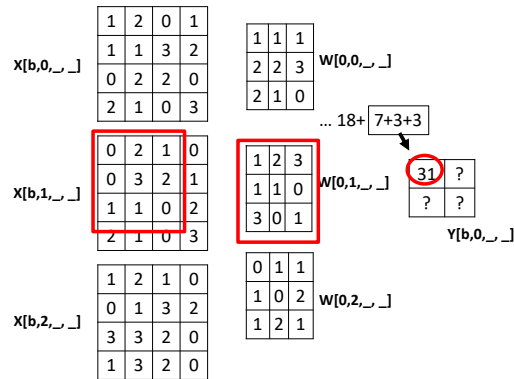


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## A Small Convolution Layer Example $c = 1$

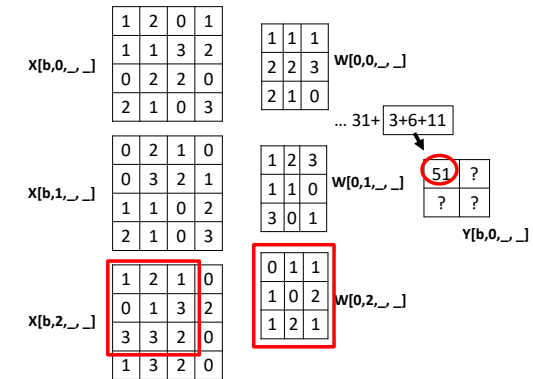


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## A Small Convolution Layer Example $c = 2$



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## Parallelism in a Convolution Layer

**Output feature maps** can be calculated in parallel

- Usually a small number, not sufficient to fully utilize a GPU

All **output** feature map **pixels** can be calculated in parallel

- All rows can be done in parallel
- All pixels in each row can be done in parallel
- Large number but diminishes as we go into deeper layers

All **input feature maps** can be processed in parallel, but need atomic operation or tree reduction (we'll learn later)

**Different layers may demand different strategies.**

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## Design of a Basic Kernel

- Each block computes
  - a tile of output pixels for one feature
  - TILE\_WIDTH pixels in each dimension
- Grid's X dimension maps to M output feature maps
- Grid's Y dimension maps to the tiles in the output feature maps (linearized order).
- (Grid's Z dimension is used for images in batch, which we omit from slides.)

tiles covering an output feature map, marked with linearized indices

0	1	2	3	4
5	6	7	8	9
10	11	12	13	14
15	16	17	18	19

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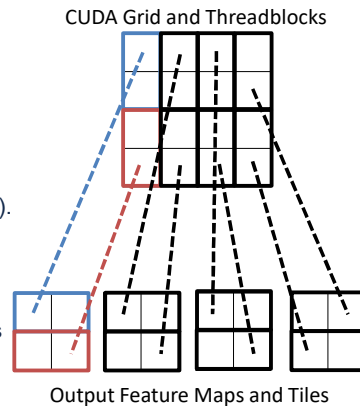
## A Small Example

Assume

- $M = 4$  (4 output feature maps),
- thus 4 blocks in the X dimension, and
- $W_{out} = H_{out} = 8$  (8x8 output features).

If  $TILE\_WIDTH = 4$ ,  
we also need 4 blocks in the Y dimension:

- for each output feature,
- top two blocks in each column calculates the top row of tiles, and
- bottom two calculate the bottom row.



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## Host Code for a Basic Kernel: CUDA Grid

Consider an output feature map:

0	1	2	3	4
5	6	7	8	9
10	11	12	13	14
15	16	17	18	19

- width is  $W_{out}$ , and
- height is  $H_{out}$ .
- Assume these are multiples of  $TILE\_WIDTH$ .

Let  $X_{grid}$  be the number of blocks needed in X dim (5 above).

Let  $Y_{grid}$  be the number of blocks needed in Y dim (4 above).

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## Host Code for a Basic Kernel: CUDA Grid

(Assuming  $W_{out}$  and  $H_{out}$  are multiples of  $TILE\_WIDTH$ .)

```
#define TILE_WIDTH 16      // We will use 4 for small examples.
W_grid = W_out/TILE_WIDTH; // number of horizontal tiles per output map
H_grid = H_out/TILE_WIDTH; // number of vertical tiles per output map
Y = H_grid * W_grid;
```

```
dim3 blockDim(TILE_WIDTH, TILE_WIDTH, 1); // output tile for untiled code
dim3 gridDim(M, Y, 1);
```

```
ConvLayerForward_Kernel<<< gridDim, blockDim>>>(...);
```

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## Partial Kernel Code for a Convolution Layer

```
__global__ void ConvLayerForward_Basic_Kernel
(int C, int W_grid, int K, float* X, float* W, float* Y)
{
    int m = blockIdx.x;
    int h = (blockIdx.y / W_grid) * TILE_WIDTH + threadIdx.y;
    int w = (blockIdx.y % W_grid) * TILE_WIDTH + threadIdx.x;
    float acc = 0.0f;
    for (int c = 0; c < C; c++) { // sum over all input channels
        for (int p = 0; p < K; p++) // loop over KxK filter
            for (int q = 0; q < K; q++)
                acc += X[c, h + p, w + q] * W[m, c, p, q];
    }
    Y[m, h, w] = acc;
}
```

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## Some Observations

### Enough parallelism

- if the total number of pixels
- across all output feature maps is large
- (often the case for CNN layers)

Each input tile

- loaded M times (number of output features), so
- **not efficient in global memory bandwidth,**
- but block scheduling in X dimension should give cache benefits.

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## Subsampling (Pooling) by Scale N

**Convolution Output Y**  
B images  
M features per image  
 $H_{out} \times W_{out}$  values per feature

Average over  $N \times N$  blocks,  
then calculate sigmoid

**Subsampling/Pooling Output S**  
B images  
M features per image  
 $H_{S(N)} \times W_{S(N)}$  values per feature

**Output Size**  
 $H_{S(N)} = \text{floor}(H_{out} / N)$   
 $W_{S(N)} = \text{floor}(W_{out} / N)$

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## Sequential Code: Forward Pooling Layer

```
void poolingLayer_forward(int B, int M, int H_out, int W_out, int N, float* Y, float* S)
{
    for (int b = 0; b < B; ++b)           // for each image
        for (int m = 0; m < M; ++m)       // for each output feature map
            for (int x = 0; x < H_out/N; ++x) // for each output value (two loops)
                for (int y = 0; y < W_out/N; ++y) {
                    float acc = 0.0f;        // initialize sum to 0
                    for (int p = 0; p < N; ++p) // loop over NxN block of Y (two loops)
                        for (int q = 0; q < N; ++q)
                            acc += Y[b, m, N*x + p, N*y + q];
                    acc /= N * N;           // calculate average over block
                    S[b, m, x, y] = sigmoid(acc + bias[m]) // bias, non-linearity
                }
    }
}
```

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## Kernel Implementation of Subsampling Layers

- straightforward mapping from grid to subsampled output feature map pixels
- in GPU kernel,
  - need to manipulate index mapping
  - for accessing the output feature map pixels
  - of the previous convolution layer.
- often merged into the previous convolution layer to save memory bandwidth

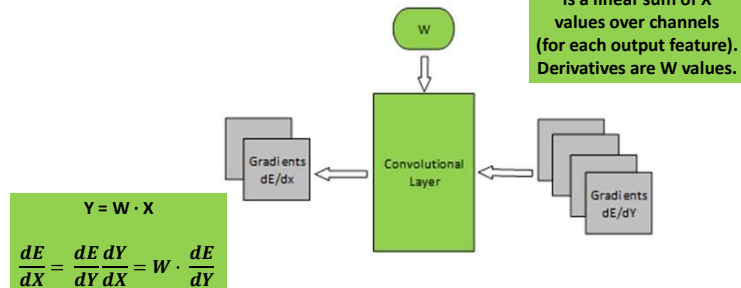
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## Backpropagation



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## Calculating dE/dX from dE/dY

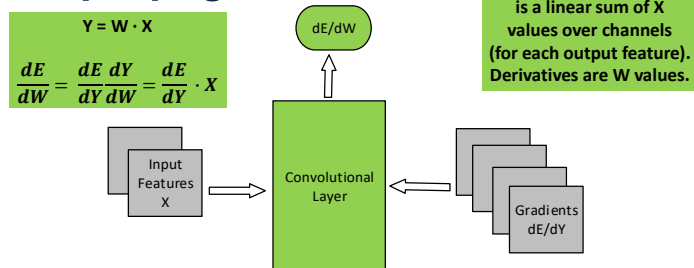
```
void convLayer_backward_dgrad(int B, int M, int C, int H, int W, int K, float *dE_dY, float *W, float *dE_dX) {
    int H_out = H - K + 1;
    int W_out = W - K + 1;
    for (int b = 0; b < B; ++b) {
        for (int c = 0; c < C; ++c) {
            for (int h = 0; h < H; ++h)
                for (int w = 0; w < W; ++w)
                    dE_dX[b, c, h, w] = 0.0f; // initialize to 0
        }
    }
    for (int m = 0; m < M; ++m) {
        for (int h = 0; h < H_out; ++h)
            for (int w = 0; w < W_out; ++w)
                for (int c = 0; c < C; ++c)
                    for (int p = 0; p < K; ++p)
                        for (int q = 0; q < K; ++q)
                            dE_dX[b, c, h + p, w + q] += dE_dY[b, m, h, w] * W[m, c, p, q];
    }
}
```

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## Backpropagation



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## Calculating dE/dW

```
void convLayer_backward_wgrad(int B, int M, int C, int H, int W, int K, float *dE_dY, float *X, float *dE_dW) {
    const int H_out = H - K + 1;
    const int W_out = W - K + 1;
    for (int b = 0; b < B; ++b) {
        for (int m = 0; m < M; ++m)
            for (int c = 0; c < C; ++c)
                for (int p = 0; p < K; ++p)
                    for (int q = 0; q < K; ++q)
                        dE_dW[b, m, c, p, q] = 0.0f; // initialize to 0
    }
    for (int m = 0; m < M; ++m)
        for (int h = 0; h < H_out; ++h)
            for (int w = 0; w < W_out; ++w)
                for (int c = 0; c < C; ++c)
                    for (int p = 0; p < K; ++p)
                        for (int q = 0; q < K; ++q)
                            dE_dW[b, m, c, p, q] += X[b, c, h + p, w + q] * dE_dY[b, m, h, w];
    }
}
```

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