

## Features

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$

## Applications

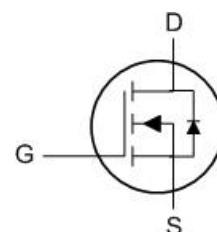
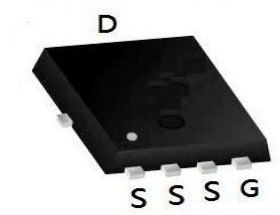
- DC-DC Converters
- Power management functions
- Synchronous-rectification applications

## Product Summary



BVDSS	RDSON	ID
60V	4mΩ	100A

## PDFN3333-8L Pin Configuration

Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		$V_{DS}$	60	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$T_C = 25^\circ\text{C}$	$I_D$	100	A
	$T_C = 100^\circ\text{C}$		64	
Pulsed Drain Current <sup>1</sup>		$I_{DM}$	385	A
Single Pulse Avalanche Energy <sup>2</sup>		EAS	80	mJ
Total Power Dissipation	$T_C = 25^\circ\text{C}$	$P_D$	73.5	W
Operating Junction and Storage Temperature Range		$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$

## Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient <sup>3</sup>	$R_{\theta JA}$	51	$^\circ\text{C/W}$
Thermal Resistance from Junction-to-Case	$R_{\theta JC}$	1.7	$^\circ\text{C/W}$

Electrical Characteristics ( $T_J = 25^\circ\text{C}$ , unless otherwise noted)

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics							
Drain-Source Breakdown Voltage		V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	60	-	-	V
Gate-body Leakage Current		I <sub>GSS</sub>	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±20V	-	-	±100	nA
Zero Gate Voltage Drain Current	T <sub>J</sub> =25°C	I <sub>DSS</sub>	V <sub>DS</sub> = 60V, V <sub>GS</sub> = 0V	-	-	1	μA
	T <sub>J</sub> =100°C			-	-		
Gate-Threshold Voltage		V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	1.2	1.7	2.5	V
Drain-Source On-Resistance <sup>4</sup>		R <sub>DS(on)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 21A	-	4.0	4.8	mΩ
			V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 10A	-	5.2	6.6	
Forward Transconductance <sup>4</sup>		g <sub>fs</sub>	V <sub>DS</sub> = 10V, I <sub>D</sub> = 21A	-	89	-	S
Dynamic Characteristics <sup>5</sup>							
Input Capacitance		C <sub>iss</sub>	V <sub>DS</sub> = 30V, V <sub>GS</sub> =0V, f =1MHz	-	2180	-	pF
Output Capacitance		C <sub>oss</sub>		-	735	-	
Reverse Transfer Capacitance		C <sub>rss</sub>		-	42	-	
Gate Resistance		R <sub>g</sub>	f = 1MHz	-	1.8	-	Ω
Switching Characteristics <sup>5</sup>							
Total Gate Charge		Q <sub>g</sub>	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 30V, I <sub>D</sub> = 21A	-	35	-	nC
Gate-Source Charge		Q <sub>gs</sub>		-	6.6	-	
Gate-Drain Charge		Q <sub>gd</sub>		-	8.4	-	
Turn-On Delay Time		t <sub>d(on)</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> = 30V, R <sub>G</sub> = 3Ω, I <sub>D</sub> = 21A	-	9.4	-	ns
Rise Time		t <sub>r</sub>		-	8.4	-	
Turn-Off Delay Time		t <sub>d(off)</sub>		-	32.5	-	
Fall Time		t <sub>f</sub>		-	12.5	-	
Body Diode Reverse Recovery Time		t <sub>rr</sub>	I <sub>F</sub> =20A, dI/dt=100A/μs	-	50	-	ns
Body Diode Reverse Recovery Charge		Q <sub>rr</sub>		-	20	-	nC
Drain-Source Body Diode Characteristics							
Diode Forward Voltage <sup>4</sup>		V <sub>SD</sub>	I <sub>S</sub> = 21A, V <sub>GS</sub> = 0V	-	-	1.2	V
Continuous Source Current	T <sub>C</sub> =25°C	I <sub>S</sub>	-	-	-	100	A

## Notes:

1. Repetitive rating, pulse width limited by junction temperature  $T_{J(MAX)} = 150^\circ\text{C}$
2. The EAS data shows Max. rating . The test condition is  $V_{DD} = 25V, V_{GS} = 10V, L = 0.1mH, I_{AS} = 40A$ .
3. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 20Z copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$ .
5. This value is guaranteed by design hence it is not included in the production test.

### Typical Characteristics

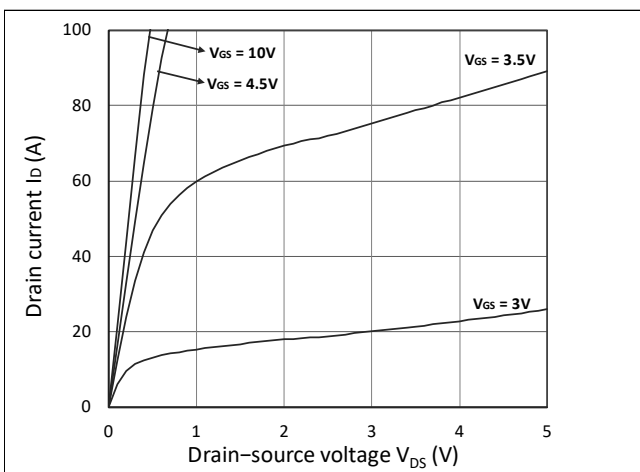


Figure 1. Output Characteristics

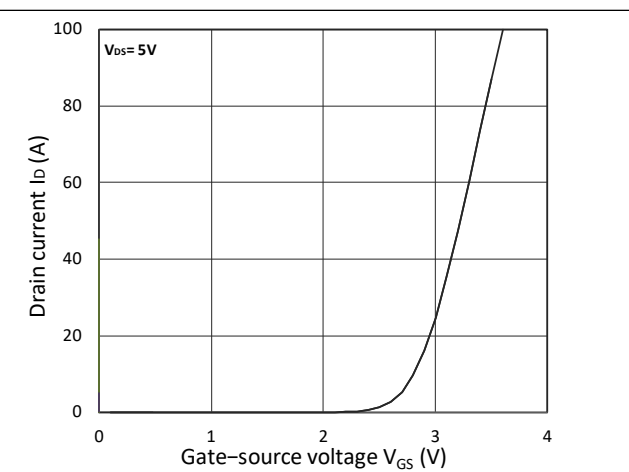


Figure 2. Transfer Characteristics

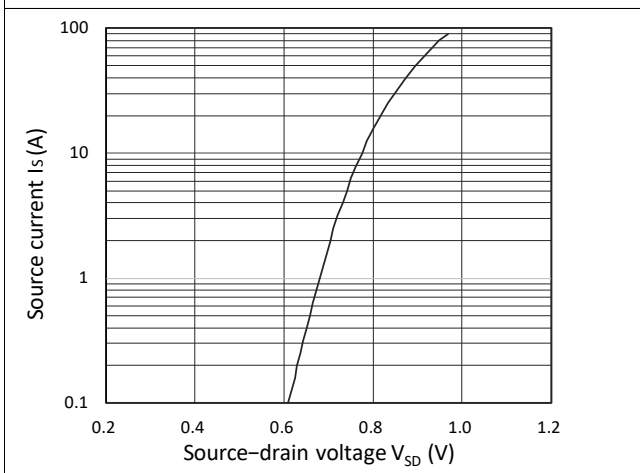


Figure 3. Forward Characteristics of Reverse

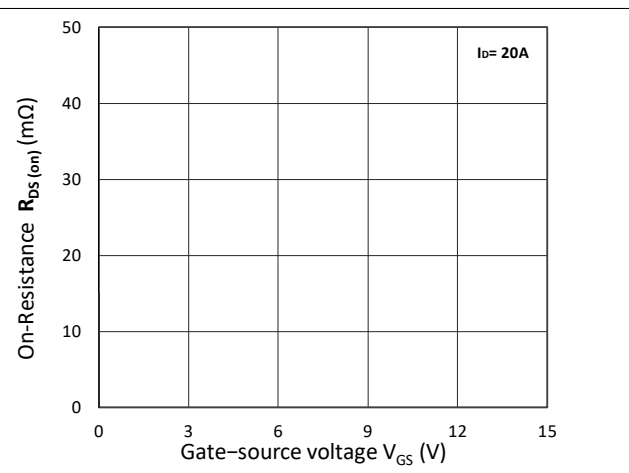


Figure 4.  $R_{DS(on)}$  vs.  $V_{GS}$

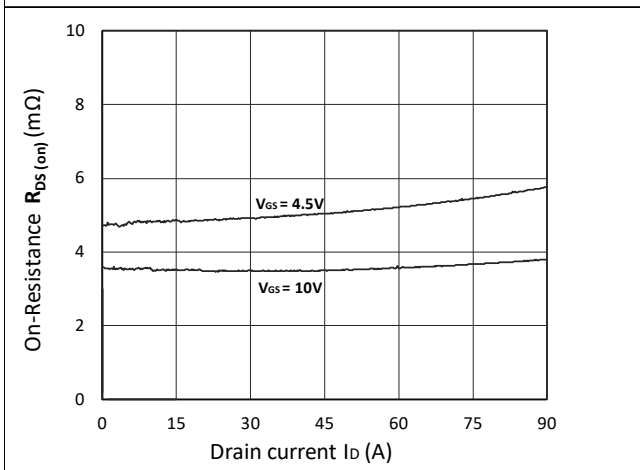


Figure 5.  $R_{DS(on)}$  vs.  $I_D$

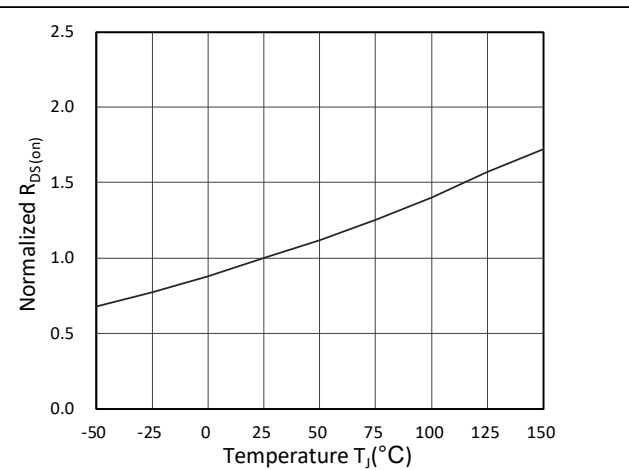


Figure 6. Normalized  $R_{DS(on)}$  vs. Temperature

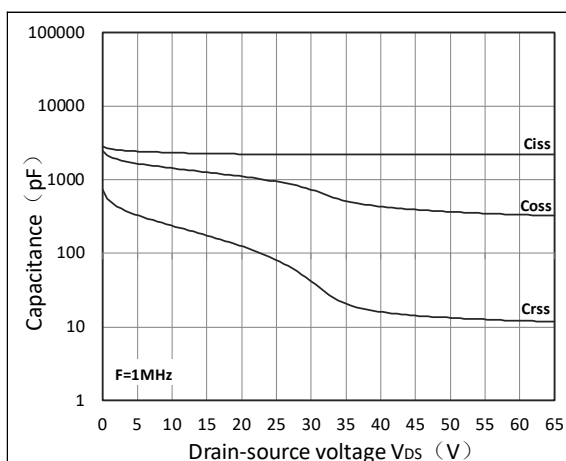


Figure 7. Capacitance Characteristics

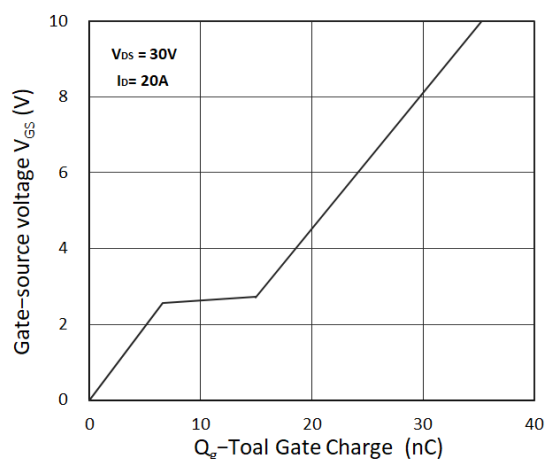


Figure 8. Gate Charge Characteristics

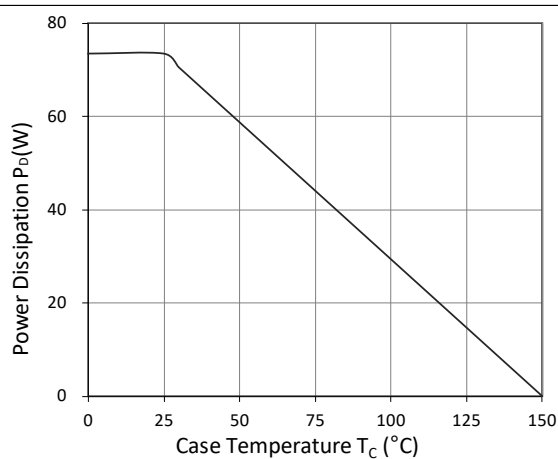


Figure 9. Power Dissipation

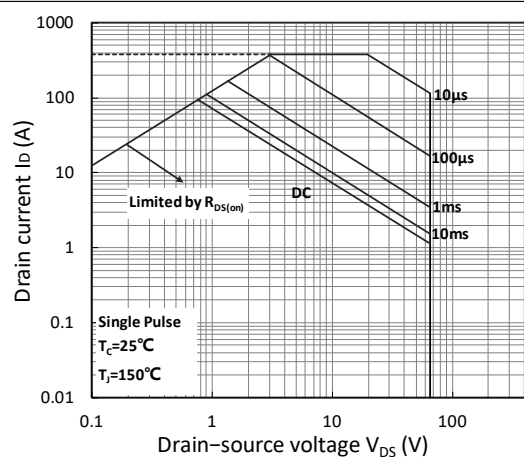


Figure10. Safe Operating Area

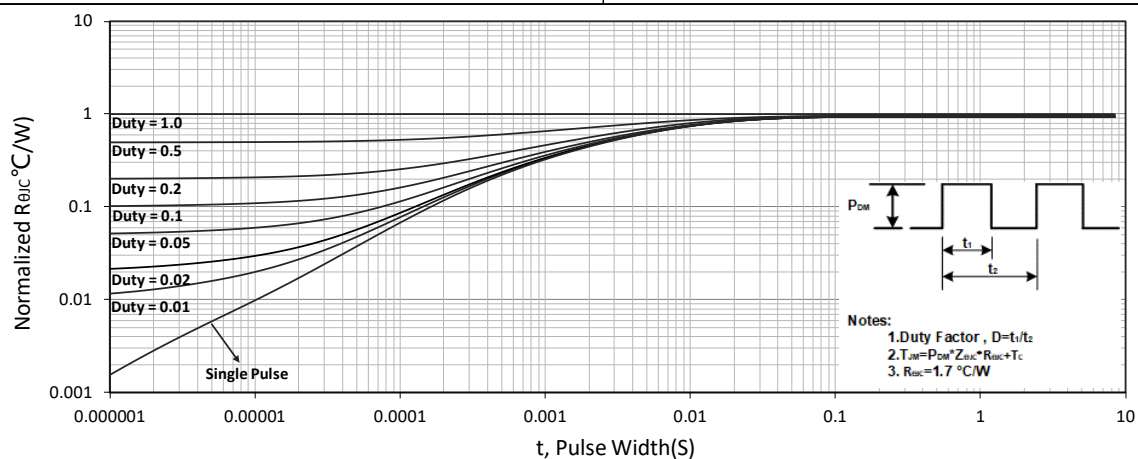


Figure 11. Normalized Maximum Transient Thermal Impedance

### Test Circuit

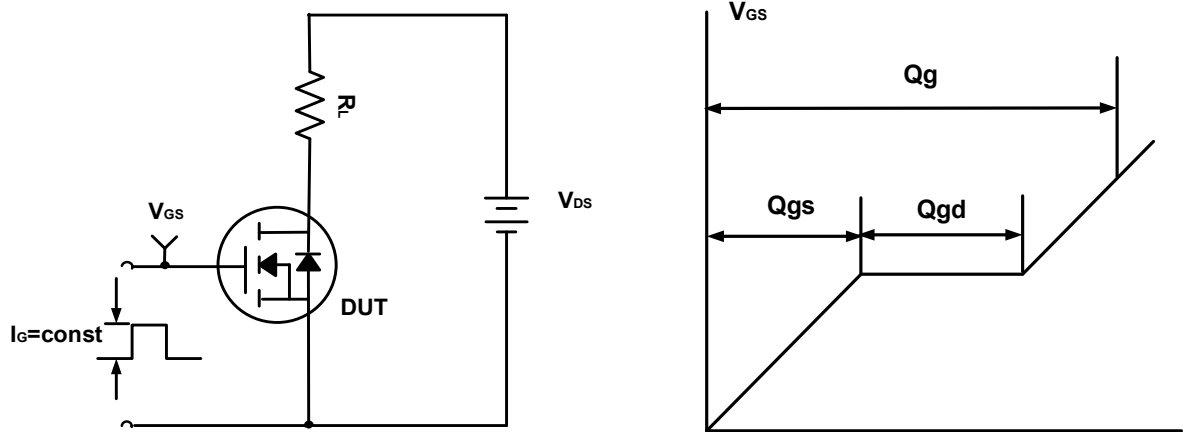


Figure A. Gate Charge Test Circuit & Waveforms

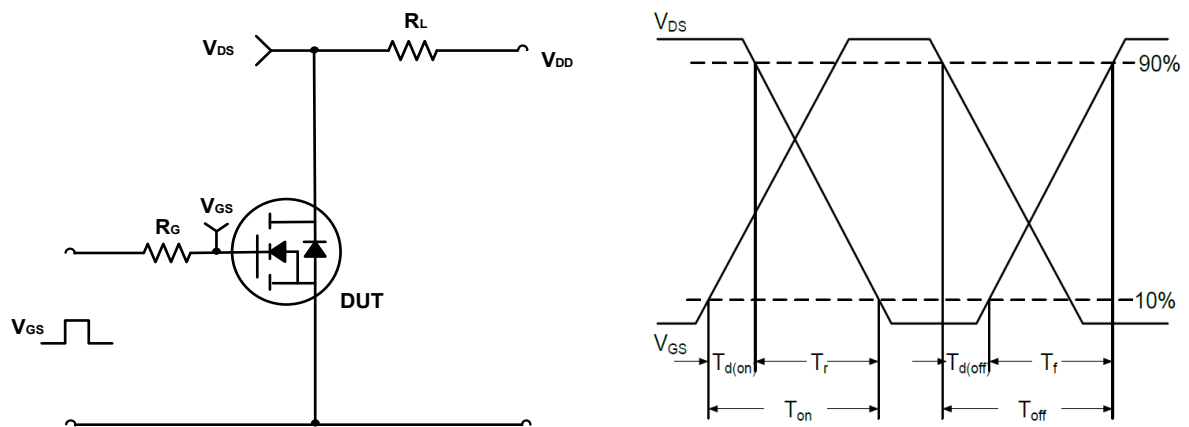


Figure B. Switching Test Circuit & Waveforms

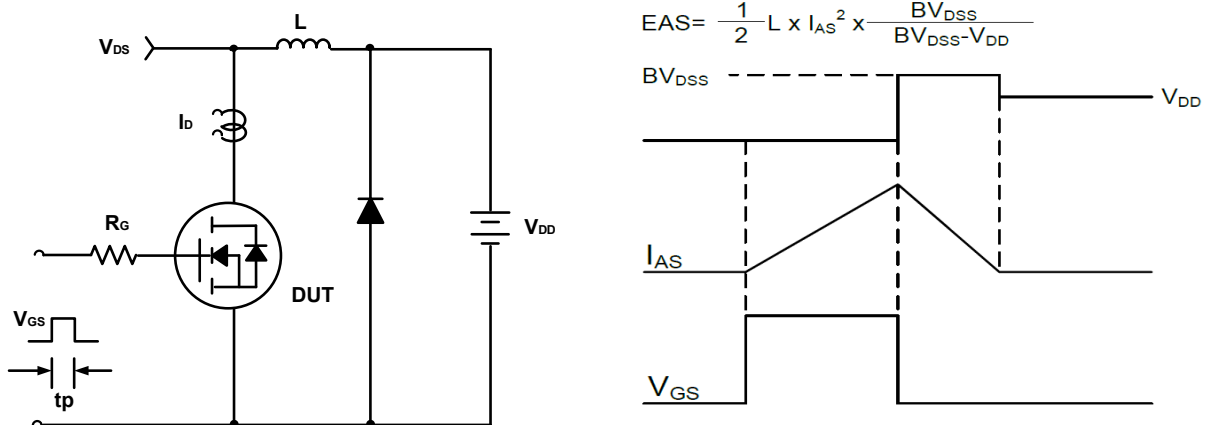
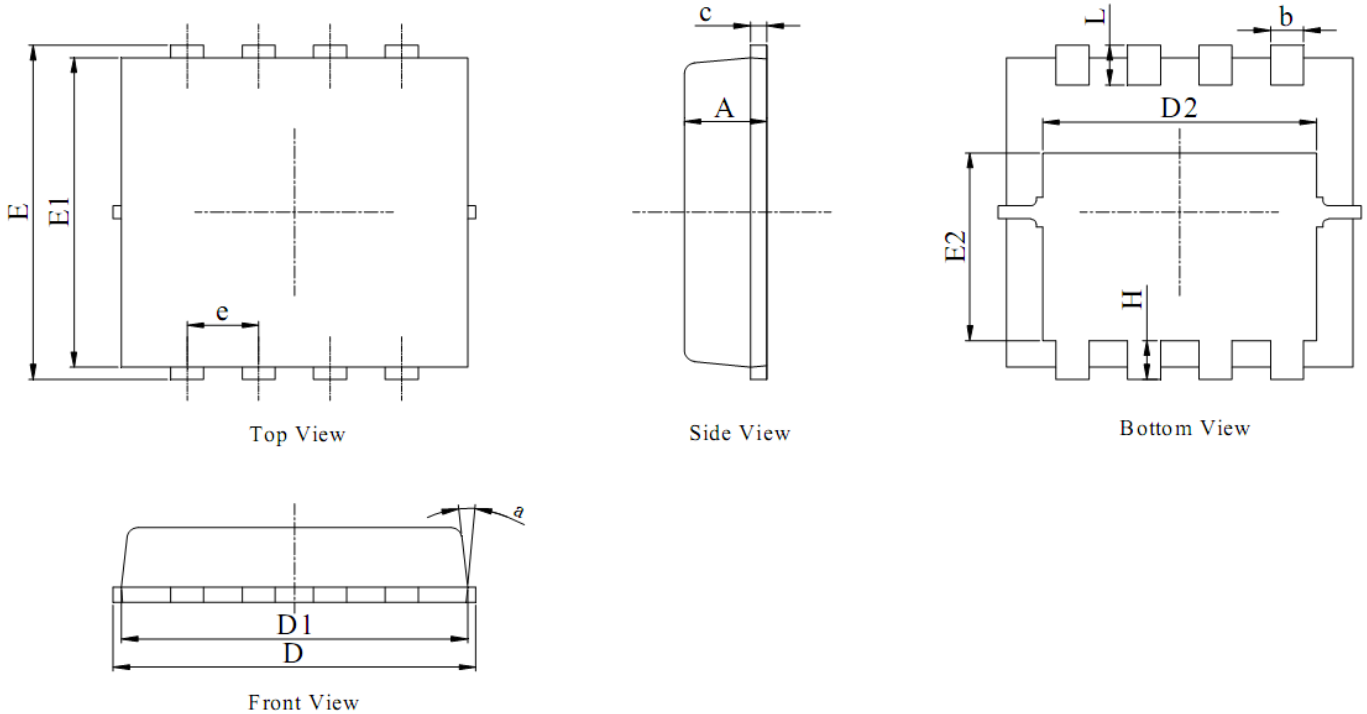


Figure C. Unclamped Inductive Switching Circuit & Waveforms

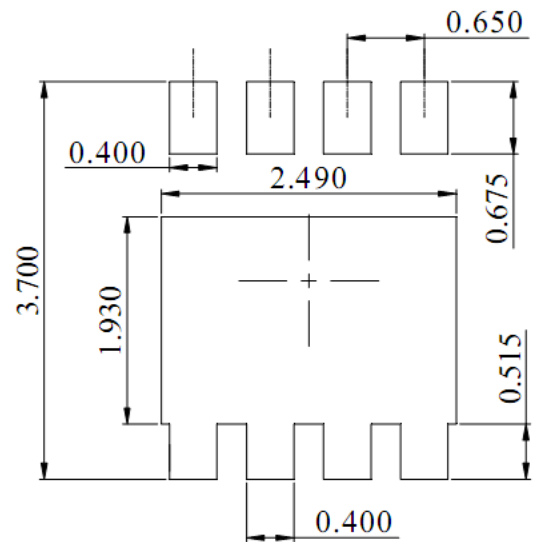
#### Package Mechanical Data-PDFN3333-8L-Single



#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. ALL DIMENSIONS IN MILLIMETER (ANNGLE IN DEGREE).
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM.	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.20	0.25
D	3.00	3.15	3.25
D1	2.95	3.05	3.15
D2	2.39	2.49	2.59
E	3.20	3.30	3.40
E1	2.95	3.05	3.15
E2	1.70	1.80	1.90
e	0.65 BSC		
H	0.30	0.40	0.50
L	0.25	0.40	0.50
a	---	---	15°



DIMENSIONS:MILLIMETERS