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cc Chuck Alpert/Austin/IBM@IBMUS, lou@cadence.com, sachin@mail.ece.umn.edu, Gi-Joon Nam/Austin/IBM@IBMUS

bcc

Subject ISPD 2005 Placement Contest Sample Benchmarks

Dear All,

First of all, thanks for your interest and registration for ISPD 2005 placement contest.
In this email, there are 4 important information:

1. Contest date Changes
2. Technical paper draft requirement
3. Co-author information
4. Sample benchmarks

1. Contest date changes:

Originally, it was posted that the contest starts on March 27th (Sunday) and ends at 5:00 PM on April 1st.
However, there are 9+ groups who want to participate in the contest so far and it might go up because the
registration deadline is Jan. 15th. Therefore, I'd like to allow myself more time to verify and measure your
solutions. Here is my suggested new dates:

March 20th Sunday 5:00 PM US Eastern time: 5 benchmarks will be posted at ISPD website
**March 25th Friday   5:00 PM US Eastern time: Your solutions (in bookshelf PL file format) should
be submitted to me by email (gnam@us.ibm.com)**

If you have any problem with the above schedule, please let me know as soon as possible.

2. Technical paper draft

One of the requirement for the registration was to write a 3 page technical paper on your placer. (The
other important requirement is to give a short (approximate 10 minutes) presentation at ISPD.) Since the
steering committee has to finish proceeding planning, please submit the draft of your technical paper by
Jan. 28th Friday. It should be an overview paper of your placer, No need for experimental results, just
tutorial style paper. It is a draft, not final version, yet we'd like to see how they look.

3. Co-author information

 Please send me the complete list of authors of your placers. The list should match the authors of your
technical paper. Those names will appear in ISPD 2005 advanced technical program.

4. Sample benchmarks

In the following emails, you will two sample benchmarks in bookshelf format. There are several questions
on Bookshelf format itself. By any means, I'm an expert on Bookshelf format, but I can explain what I did

to produce these bookshelf files from IBM internal format. If you have any question or problem with my interpretation, please let me know. This is the whole point of releasing sample benchmarks, to remove any potential miscommunication between you and me.

Assuming benchmark name is xxx,
(1) xxx.aux : denotes the set of input files. Usually looks like
        RowBasedPlacement : xxx.nodes xxx.nets xxx.wts xxx.pl xxx.scl

(2) xxx.nodes: specifies the set of objects. For each object,

        object_name   width   height   terminal

        keyword "terminal" appears only for fixed objects.

(3) xxx.nets: specifies the set of nets. For each net,
        "NetDegree : k net_name   用pin位置计算wire length?
                object_name   I : x_offset   y_offset   # input pin   pin offset is measured
from the center of corresponding object
                object_name   O: x_offset   y_offset   # output pin

(4) xxx.pl: specifies the location & orientation of objects. For each object,

        object_name   x_location   y_location   : N   # every object stands
straight. No rotation is applied. x_location & y_location are low_x and low_y of an object   左下角?
        object_name   x_location   y_location   : N   /FIXED   # fixed object

(5) xxx.scl: circuit row information. For each row,
        CoreRow Horizontal
         Coordinate   :   xxx   # row starts at coordinate xxx
         Height :   yyy   # row height is yyy
         Sitewidth :   1
         Sitespacing : 1   ?
         Siteorient : 1
         Sitesymmetry : 1
         SubrowOrigin : xxx   NumSites : zzz # you can specify sub rows within a row. In our
benchmarks, there would be only 1 sub-row per row. Thus, this basically says the row spans from xxx to
zzz with yyy height.

(6) xxx.wts: specifies weights for object and nets. But for our case, every object and net have the same weight. Thus, this file is empty.

The rest information should be trivial. For more information, please refer to Bookshelf website at:
http://vlsicad.eecs.umich.edu/BK

Please note:
(1) In two sample benchmarks, all the movable objects are standard cells and its height is same with circuit row height. I.e., there is no movable macros with all the macros fixed. FYI, we're planning to allow movable macros in benchmarks for the contest.

(2) Currently, every terminal (in NODE file) is also defined as "/FIXED" in PL file and there is no overlap among any types blocks. However, we'd like to allow some overlaps for IO blocks **in the future**. For example, in a design with area-array IOs, it is usual some objects sits on top of one of IO block. You might want to think that area-array IOs are at different layers, but their locations must be respected. To reflect this situation, I'd like to differentiate the following two types in NODE and PL file as:
        NODE file:
                object1 width   height   terminal
                object2 width   height   terminal

PL file:
```
object1 x_loc    y_loc    : N
object2 x_loc    y_loc    : N        /FIXED
```

In the example above, some other movable or FIXED objects CAN overlap with object1, but **no** overlap is allowed for object2. Again, this is the future item and I will send you separate versions with these definition.
If you have any concerns or question, please let me know. Have fun !!!

Regards,

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