ISPD 2015 Benchmarks with Fence Regions and Routing Blockages for Detailed-Routing-Driven Placement

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ABSTRACT

The ISPD 2015 placement-contest benchmarks include all the detailed pin, cell, and wire geometry constraints from the 2014 release, plus

(a) added fence regions and placement blockages,
(b) altered netlists including fixed macro blocks,
(c) reduced standard cell area utilization via larger floorplan outlines, and
(d) specified upper limits on local cell-area density.

Compared to the 2014 release, these new constraints add realism and increase the difficulty of producing detail-routable wirelength-driven placements.

Categories and Subject Descriptors

B.7.2 [**Integrated Circuits**]: Design Aids - Placement and Routing; D.2.8 [**Software Engineering**]: Metrics—*complexity measures, performance measures*

General Terms

Algorithms, Design

Keywords

Placement; routability; placement evaluation; global routing; detailed routing; fence regions

1. INTRODUCTION

The challenge of computing placements compatible with increasingly complex design rules enforced in detailed routing was taken up in the 2014 ISPD placement contest [17]. There, contestants from nine universities grappled with realistic constraints such as pin access, edge spacing, end of line, and other non-default rules for routing like double-width vias, for the first time in a publicly released suite of placement benchmarks.

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Winning solutions to the contest adapted techniques including detailed-routability enhanced look-ahead legalization [3] and placement migration [15] to produce placements that could be successfully detail-routed by a leading commercial tool [9].

While the ISPD 2014 benchmarks [17] do add important physical detail compared to that in previously released suites [12, 14], they lack the following features commonly seen in real industrial designs: (1) timing constraints, and (2) region placement constraints. Despite being routable, many of the winning placements in ISPD 2014 exhibit significantly higher local cell density than typical industrial solutions. We attribute a large part of this density disparity to the lack of timing constraints in the benchmarks and the resulting absence of a post-route timing-closure design stage including sizing and buffer insertion.

In order to address these shortcomings, the following enhancements have been added to these placement benchmarks for the 2015 ISPD contest:

1. maximum local logic-utilization (cell-density) constraints
2. region placement constraints ("region constraints")
3. diverse standard-cell utilizations ranging from 14.3% to 90.6%
4. placement and routing obstructions added to the Suite A benchmarks.

Although timing constraints are still not explicitly present, the limits on local cell density increase the difficulty of wirelength minimization and anticipate sizing and buffering operations.[1] Region constraints are used to support various design features such as voltage islands [8]. They are also common in top-level floorplans. The geometry of a region may vary from a simple rectangle to a complex, multiple-contour rectilinear shape. In practice, region constraints and large fixed obstructions in close proximity result in placement regions dominated by narrow channels and additional challenges in modeling the wirelength objective and cell density constraints.

In Section 2, we describe the ISPD 2014 detailed routing results and the relevance of global routing in assessing detailed routability. In Section 3, we discuss the importance of placement spreading and maximum utilization constraints. In Section 4, we describe our use of region constraints. The benchmarks are detailed in Section 5. Changes to the scoring for the ISPD 2015 placement contest are described in Section 6. We conclude in Section 7.

[1]However, such operations are not part of the contest evaluation.

2. THE ROLE OF GLOBAL ROUTING

A global routing (GR) is typically associated with a grid of global-routing cells called g-cells.[2] The capacity of g-cell edges is calculated from how many available routing tracks cross each edge. The GR edge-overflow percentage is the percentage of g-cell edges where the number of global-routing segments crossing an edge exceeds the edge capacity. Detailed routing (DR) can resolve minor edge overflows, but there will likely be DR violations[3] if there is significant GR congestion in an area, particularly for narrow routing channels between macros, routing blockages, and the floorplan boundary [9].

Several recent papers [16, 14, 17] have drawn attention to large and growing discrepancies between congestion predicted by GR and congestion encountered by DR on the same placement. The discrepancies are often not only in magnitude but also in the location of the congestion. Given the prominent role that GR has traditionally played in physical design, the observed GR-DR discrepancies raise the following questions regarding GR usage.

(1) Can GR be augmented without impairing its run time or scalability in such a way that significant discrepancies with DR are reduced or even eliminated?
(2) Assume GR is useful at coarser modeling stages but misleading at finer ones. As a placement algorithm incrementally increases its modeling resolution, at what point should its use of GR stop?
(3) What is the uncertainty of GR predictions? Specifically,
    (a) On a given placed design, *below* what level of maximum GR edge congestion can we be confident that DR *will* complete with an acceptably small number of violations?
    (b) On a given placed design, *above* what level of maximum GR edge congestion can we be confident that DR will *not* complete with an acceptably small number of violations?
(4) Is it feasible to generate detail-routable placements without *any* use of GR?

Question 1 has been considered in several recent papers [16, 18, 13, 7, 6], which have demonstrated significant reduction in the GR-DR gap but have not eliminated it. The ACE metric [16] introduced at the 2012 DAC placement contest was also used by one of the two winning teams in the ISPD 2014 placement contest. Both of these teams report using GR in global placement but not in legalization or detailed placement [3, 15]; we know of no study investigating whether replacing GR by more precise routability estimation *before* global placement completes can improve final detailed routability.

Questions 3 and 4 are open and do not appear to have simple answers. However, both in industry and in the ISPD 2014 and 2015 placement-contest evaluations (Section 6), a conservative upper limit for GR edge-congestion overflow is used to bail out early on unroutable designs, preventing long run time in DR with low probability of any ultimate success. Results from the ISPD 2014 contest described next suggest that the uncertainty in this estimated upper limit may be quite substantial and thus support the claim that a GR-free approach to efficient recognition of unroutability may be a better alternative [4].

Figure 1 illustrates how GR edge-congestion values over ISPD 2014 contest placements sometimes fail to show a clear trend in the subsequent number of DR violations. DR violations have been normalized by number of nets in a design, as the benchmarks vary significantly in size. A log scale[4] has been used on the axes to highlight that GR edge-overflow percentage does not correlate well with detailed routing violations.

We would typically consider a design with GR edge overflow of 0.02% or more to be difficult to route [9], but the data in Figure 1 show a wide range of detailed routing scores below 0.15% GR edge overflow. The `mgc_superblue19` design is very difficult to route, despite solutions with GR edge overflow of zero and 0.005%, which respectively had 1,587 and 7,532 detailed routing violations.

Global routing edge overflow does not consider usage of vias between metal layers. However, vias are a limited resource and also use up space that could be used instead by planar routing, and hence can significantly impact detailed routing. GR node congestion is a measure of via usage and planar routing resource usage internal to g-cells.

In particular, for the `mgc_fft_2` design, one solution had zero GR edge congestion but 67 routing violations, whereas another solution with "poor" GR edge overflow of 0.38% actually had only 55 DR violations. As shown in Figure 2, the GR edge overflow and node congestion are worse on both sides of the version of `mgc_fft_2` with even placement spread. However, there are actually more DR violations on the left and top of the version with uneven cell placement. There appears to be only a little GR node congestion at the top of the version of `mgc_fft_2` with even placement spread, but the majority of the DR violations are there. This motivates more careful consideration of GR node congestion or better metrics to identify and address such issues before they cause problems in detailed routing.

Design `mgc_superblue19` is a "blind" benchmark, unseen by the contestants during development of their placers, and not publicly released until after the ISPD 2015 contest.

3. LOCAL CELL-DENSITY CONSTRAINTS

Figure 3 shows global-routing congestion on two different placements of `mgc_superblue11`. The first placement was computed under a uniform-spread constraint equivalent to 65% cell density; the second, under a local cell density constraint of 95%. The second placement might appear unroutable, but, surprisingly, it is not! Some contest placements from the ISPD 2014 contests did complete detailed routing with reasonably low DR violation counts, even with local cell densities near or above 95%. We attribute these results to the use of a wirelength objective coupled with fine-grain design-constraint-aware look-ahead legalization.

Placement constraints on maximum utilization, i.e., local cell density, were imposed in the ISPD 2006 placement contest [10, 11] primarily as a proxy for routability. No routability proxy is needed for the ISPD 2015 placement contest, but there are no timing constraints included in our benchmarks. Realistic placements should still reserve space important for

[2]For the ISPD 2015 contest, a global-routing grid of 3x3 standard cell row heights is used.

[3]opens, shorts, blocked pins, insufficient spacing, etc. [17]

[4]The data have been shifted by 0.01 to avoid log(0).

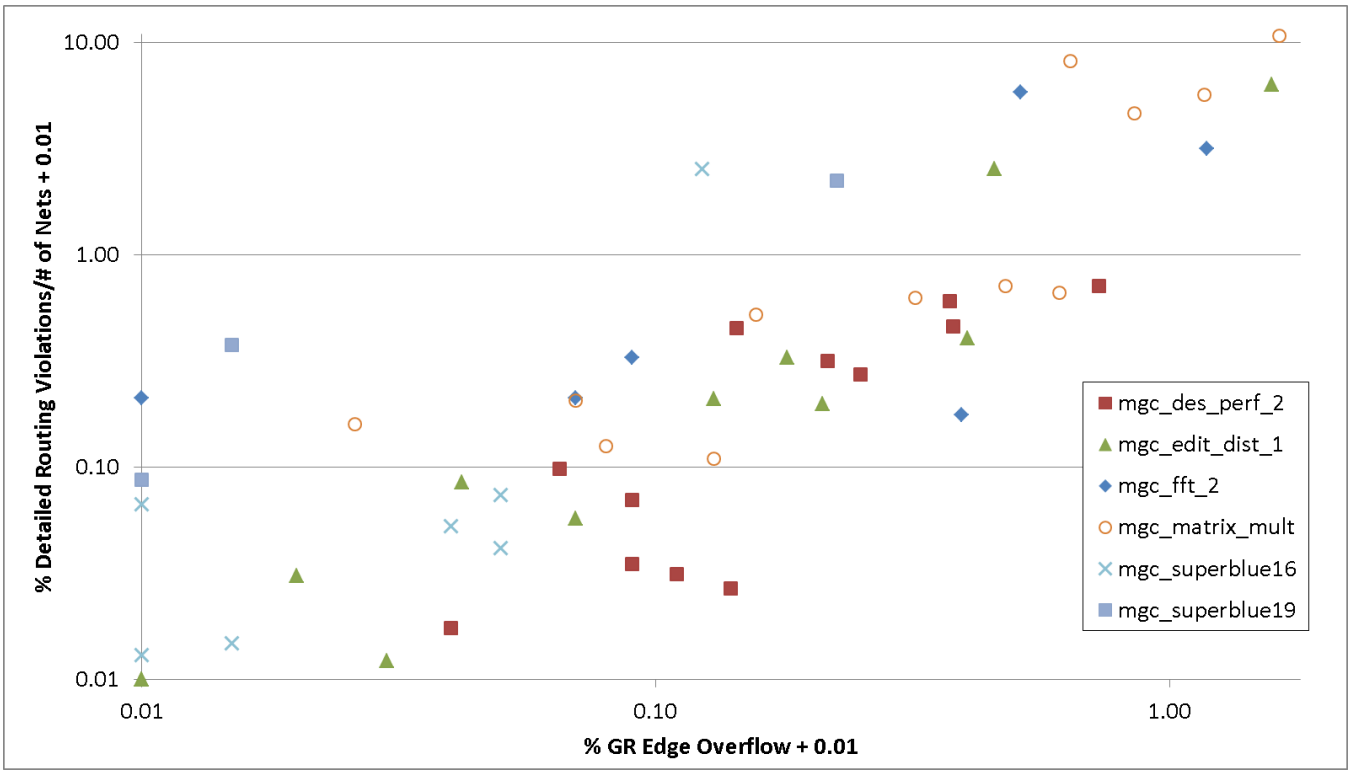

Figure 1: Log-scale DR violation counts normalized by net count vs. GR edge-congestion percentages, over placements from the ISPD 2014 contest.

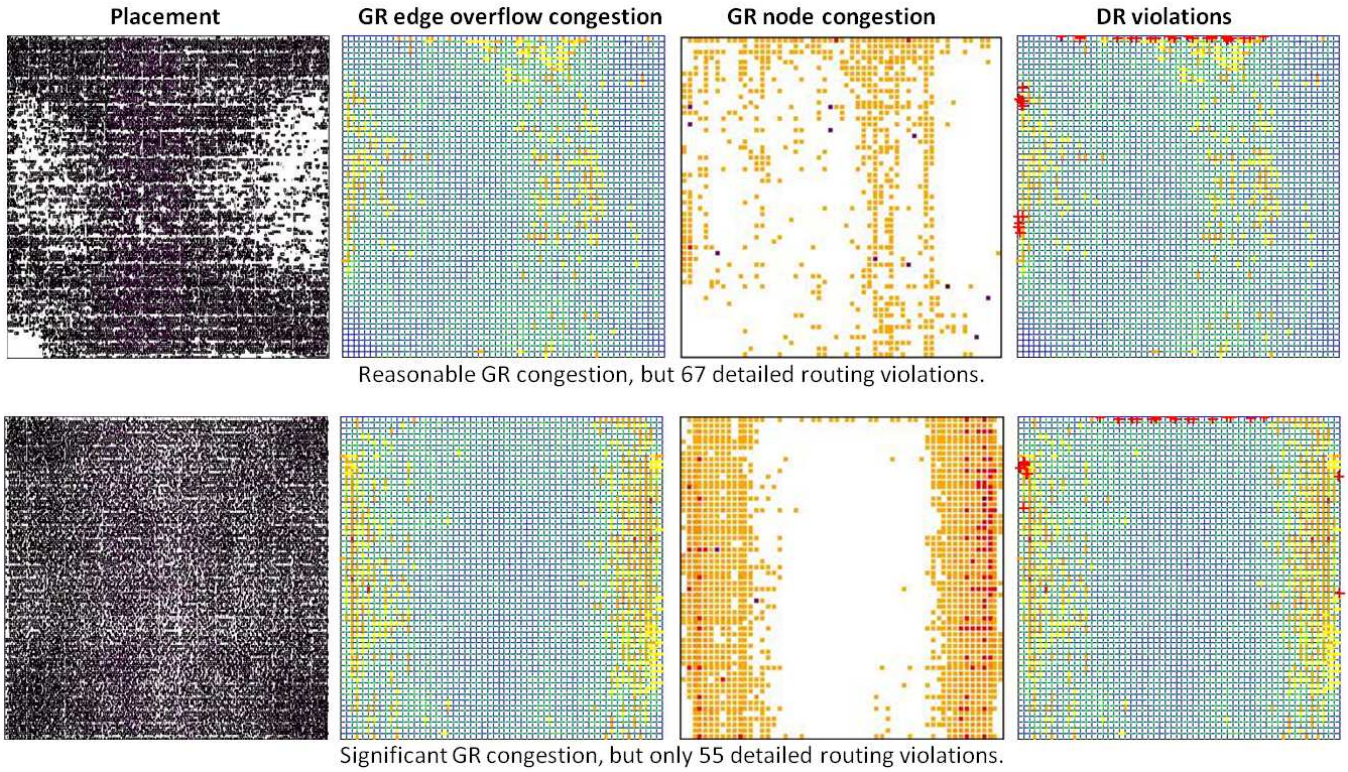

Figure 2: GR edge overflow and node congestion for two different placements of `mgc_fft_2`. The DR violations (red crosses), shown super-imposed on the GR edge overflow congestion map, do not correlate with the GR-congestion hot spots. The algorithm computing the upper placement may have been misled by GR congestion.

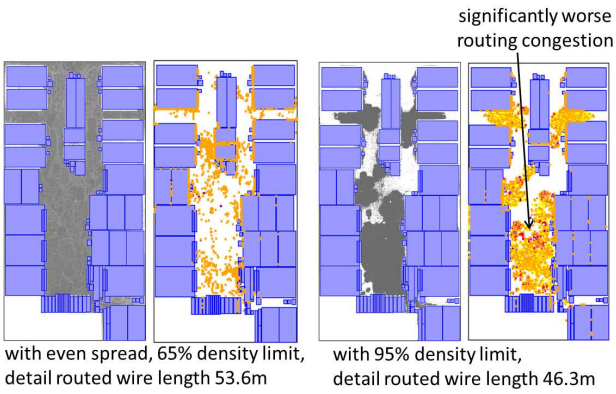

Figure 3: GR congestion maps for placements of mgc_superblue11 at 65% and 95% local cell-density limits.

subsequent timing-optimization operations such as sizing, buffering, and localized netlist remapping.

In the 2015 placement contest, a single local cell-density limit constraint is imposed uniformly on each design, irrespective of any region constraints (Section 4). If any region has a higher area utilization than the limit specified in the local cell-density constraint, the limit will be raised within that region to the region's native area utilization as defined in Section 5.1.

It is emphasized that these maximum-utilization constraints are to be interpreted as soft constraints rather than hard ones. Violations are expected, particularly on high design-utilization test cases where the limit is set to the native design utilization. The scoring penalty in Section 6 is formulated to allow contestants to trade limited violation of this cell-density constraint for significantly improved routability or wirelength.

4. REGION CONSTRAINTS

Placing cells with the same function contiguously in a confined subregion rather than scattering them haphazardly often improves important design characteristics. Region constraints are specified by designers to guide automatic place-and-route tools toward improved performance, power consumption, and/or manufacturability in various ways.

Power domains are used to simplify power/ground distribution and to isolate separate voltage regions. Space may also be reserved for power header/footer cells and always-on cells. Region constraints may be imposed at the block level to reserve whitespace in order to place global repeaters for routing top-level nets across the chip. Clock mesh distribution of clock signals periodically across chip motivates reserving space for the first level of clock buffers and clock gaters that connect to the bottom level of the mesh, in order to reduce clock wire load, which also decreases wire RC delay and hence reduces clock skew. Designers may also specify placement constraints for some datapath cells to improve the datapath placement quality, and for tightly clustering registers to reduce clock wire load and thus decrease clock power.

By definition [1], a *fence* region is *member-hard* and also *non-member-hard*: cells assigned to a fence region must be placed inside its boundary, and cells not assigned to it must be placed outside that boundary. Some tools support all four possible kinds of region membership based on independent settings of their boolean member-hard and non-member-hard properties. For instance, a region which is neither member-hard nor non-member-hard is sometimes called a *guide* region or *soft* region constraint.

All regions in every test case described here are fence regions. Fence-region constraints are hard constraints. Placements with cells even partially outside their assigned regions' boundaries are inadmissible and are not routed (Section 6).

Regions may overlap spatially in practice, but all distinct regions in the test cases here are defined so as to be spatially disjoint. However, any single region is not required to be contiguous or simply connected: it may consist of multiple spatially disjoint subregions, as shown in Figure 6.

5. BENCHMARKS

The ISPD 2015 test cases have been adapted from the ISPD 2014 test cases by expanding floorplan outlines, creating fixed macros from subnetlists, adding region constraints, and adding upper-limit constaints on local cell density.

5.1 Design utilizations

Design utilization or *area utilization* is the total area of all movable[5] standard cells divided by total available placement area for those standard cells.[6] *Available* area does *not* include the areas of placement obstructions like fixed macros. The test cases in this suite have been deliberately constructed to exhibit widely varying design utilizations. In practice, designs with tens or hundreds of millions of objects are typically partitioned into multiple *block-level* subdesigns or "blocks", which are ultimately reunited in the *top-level* design. Area utilization in each block may be pushed over 80% in order to shrink die size, whereas utilization of "glue logic" in the top level may be left well below 20%. Low utilization in the top level design allows for more aggressive post-placement optimization needed to complete longer timing paths around large obstructions.

5.2 Test case construction

The following scheme has been applied to construct realistic floorplans from some of the Suite A test cases originally without obstructions.

- With all cell sizes held fixed, each floorplan outline is enlarged to attain a distinct target design utilization.
- The outline-enlarged macro-free design is placed and routed in Olympus-SoC.
- Artificial macros are created from spatially localized cell subsets in the placed design as detailed below.
- Fence regions are defined in the placed design by both (a) boundary geometry and (b) cell membership.

Artificial macro construction proceeds as follows.

1. Temporary artificial fence regions are specified in the placed design by boundary geometry and cell members. Each such region has a simple rectangular boundary. A proper subset of cells ("members") inside each

[5] As the designs here have no fixed standard cells anyway, we may omit the word "movable."

[6] Tables 1 and 2 also list *total utilization*, i.e., total cell *and* fixed-macro area divided by total chip area.

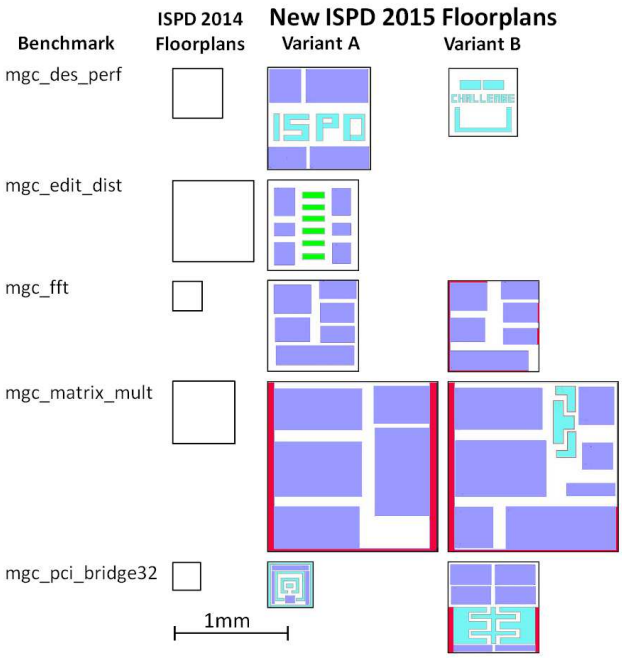

Figure 4: 2015 Suite A Floorplans vs. 2014 Suite A. See Legend in Figure 6.

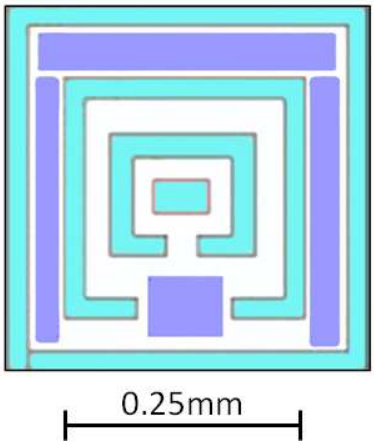

Figure 5: Close-up of mgc_pci_bridge32_a from Suite A. See Legend in Figure 6.

subregion boundary are assigned to the region; all other cells ("non-members") in the netlist are excluded from it.

2. A fresh placement is computed for the design subject to the fence-region constraints.
3. Each fence region is converted to a partition.
4. Each net containing both interior cells and exterior cells of any partition is associated with a single pin on the boundary of the partition.
5. In order to reduce congestion, the pin placement on each partition boundary is recomputed, consistently with the given cell placement.
6. Each partition is converted to a fixed macro with an associated routing blockage obstructing all routing layers over the macro.

Final floorplans for modified Suite A test cases are shown in Figures 4 and 5. Final floorplans for Suite B are shown in Figure 6. Placement blockages have been added to some of the modified Suite A benchmarks to show a common design technique used to avoid routing congestion due to placement of cells in narrow channels between macros and the floorplan boundary. Automating this approach in placement may help improve detailed routability for some designs.

5.3 Test case characteristics

Two separate benchmark suites,[7] A and B, have been adapted from the corresponding 2014 ISPD suites [17] in

[7]As of this writing, some specifications of these benchmarks are being adjusted and may still change, to provide an appropriate level of difficulty. Additional test-case variants are also being considered. All such changes and additional test cases, if any, will be collected and posted on the ISPD 2015 contest web site as an addendum to this article.

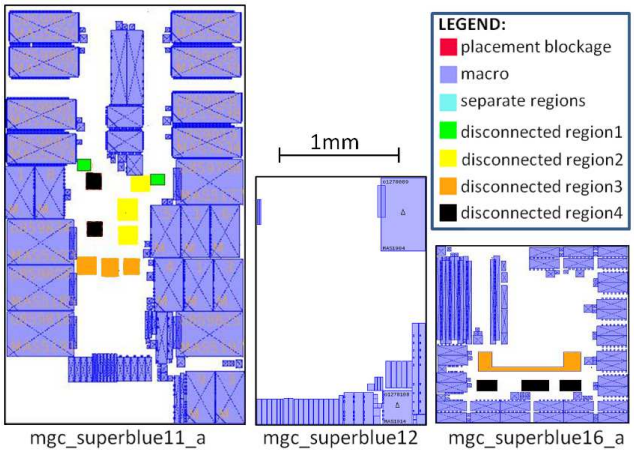

Figure 6: 2015 Suite B Floorplans

Table 3: Suite A PG-grid geometry (μm) by layer

	M1	M2	M3	M4	M5
rail width w_r	0.51	0.58	3.50	4.00	4.00
rail spacing s_r	1.49	20.0	14.0	20.0	14.0
track utilization	11%	6%	27%	24%	30 %

Table 4: Suite B PG-grid geometry (μm) by layer

	M2	M3	M4	M5	M6	M7
rail width w_r	0.10	0.86	0.80	0.90	0.90	1.0
rail spacing s_r	9.0	18.0	9.0	18.0	9.0	18.0
track utilization	1%	5%	8%	5%	9%	5%

LEF/DEF format [1]. As in the 2014 benchmarks, all standard-cell rows in each design are the same height. There are no fixed standard cells or movable macros in any of the test cases.

Suite A consists of twelve test cases adapted from benchmarks released by Intel Corporation for the ISPD 2013 discrete cell-sizing contest [12]. All movable objects are standard cells of comparable sizes. Each test case has 5 routing layers, all available for routing on every test case except `mgc_fft_2`, where routing on layer M5 is not allowed. Suite A PG grid geometry is listed in Table 3.

Suite B consists of three test cases adapted from benchmarks released by IBM Corporation for the DAC 2012 placement contest [14]. In contrast to the test cases in Suite A, the test cases in Suite B have many fixed macros and hence more complicated floorplan geometry. Fence regions have been added to `mcg_superblue11a` and `mgc_superblue16a` as shown in Figure 6. Each test case has 8 routing layers, but only `mgc_superblue16` allows routing on all 8; the others restrict routing to layers M1–M7. Suite B power/ground (PG) grid geometry is listed in Table 4. The standard cells in Suite B have been left at their given sizes.

Characteristic physical data and design rules for the benchmarks — cell geometry, pin geometry, routing pitch, routing track density, pin layer assignment, etc. — are unchanged from the ISPD 2014 [17] benchmarks except as noted herein.

Table 1 lists basic statistics for benchmark test cases unchanged from ISPD 2014 except for added limits on local cell density. These relatively unchanged test cases serve to control against overtuning for new benchmark features and facilitate comparisons between the 2014 and 2015 contest entries. Table 2 lists statistics for benchmark test cases revised from ISPD 2014 by resizing floorplan outlines and adding fixed macros and fence regions as described in Section 5.

6. PLACEMENT CONTEST EVALUATION

As in 2014, submitted DEF placement solutions are evaluated in the OLYMPUS-SOC^{TM} place and route system subject to system memory limits and a 24-hour run-time limit. A script is used to check the placed designs for the following invalidating features: cells out of bounds, including region bounds, if any; netlist changes; and movement of fixed objects. Valid placements are legalized and routed in OLYMPUS-SOC.

Each placement's score S is computed as a sum of four category scores: cell legalization displacement, detailed-routing violations, detail-routed wire length, and run time:

$$S = S_{dp} + S_{dr} + S_{wl} + S_{cpu}. \quad (1)$$

All 4 terms except wirelength S_{wl} are evaluated just as in 2014 [17], including normalizing each term to lie in $[0, 25]$. The better the placement, the *lower* the score. An invalid placement receives the worst possible score of $S = 100$.

Detailed routing is not attempted on placements exhibiting excessive GR edge congestion, as described in Question 3b of Section 2. The GR edge-congestion limit is estimated separately for each test case but is typically between 0.05 and 1.0%.

6.1 Adjusted Detail-Routed Wirelength Score

Unscaled score wl_u is simply the final detail-routed wirelength reported by the router. Before normalization, wirelength is penalized by any local maximum-utilization violations as below, following essentially the same formula[8] used in the ISPD 2006 placement contest [10, 11]:

$$\text{WL} = wl_u \left(1 + k f_{of}^2\right), \quad (2)$$

where k is a small constant,[9] and f_{of} is defined over square bins 8×8 standard-cell-row heights each, as follows. Denote the maximum allowed cell density by $d_{\max}$. Let single_bin_area denote the area of one unobstructed bin, i.e., 64 square cell heights. Let free_space(b) denote the total area of bin b *not* occupied by fixed macros or any other placement obstructions. For movable cells c in bin b,

$$\text{overflow}(b) = \left(\sum_{\text{movable } c \in b} \text{area}(c) \right) - \text{free\_space}(b) \times d_{\max},$$

where area(c) denotes the area of the portion of cell c overlapping with bin b. Then

$$\text{total\_overflow} = \sum_{\text{all bins } b} \text{overflow}(b).$$

The final factor f_{of} is then the above total_overflow expressed as a multiple of the minimum number of bins required by the design:

$$f_{of} = \frac{\text{total\_overflow} \times \text{single\_bin\_area} \times d_{\max}}{\sum_{\text{all movable cells } c} \text{area}(c)}$$

On a design with fence regions, the above formulation is applied separately to regions with native cell-area utilizations above $d_{\max}$. The final value of f_{of} used in (2) is then computed as the weighted average of the per-region f_{of} over the regions, using the total cell area of each region as its weight.

The same normalization used in 2014 is then applied to WL. Over all valid placements p on a benchmark with $S_{dp}(p) < 25$, let

$$\begin{aligned} wl_{med} &= \text{the median of the WL}(p). \\ wl_{min} &= \text{the minimum of the WL}(p). \end{aligned}$$

Then

$$S_{wl} = \begin{cases} f_{aff}(\text{WL}) & \text{if WL} < 1.5 \times wl_{med} \\ 25 & \text{if WL} \geq 1.5 \times wl_{med}, \end{cases}$$

[8] We use a slightly finer bin grid and a different constant k.

[9] As of this writing, k has yet to be determined.

Table 1: Benchmarks with floorplans unchanged from ISPD 2014

Design	#Macros	#Cells	#Nets	#Fence Regions	#I/O	%Area Utilization		Density Limit %
						Std Cell	Std Cell & Macro	
mgc_des_perf	0	112,644	112,880	0	374	90.6	Same	90.6
mgc_fft	0	32,281	33,307	0	3,010	83.5	Same	83.5
mgc_fft_2	0	32,281	33,307	0	3,010	49.9	Same	65.0
mgc_matrix_mult	0	155,325	158,529	0	4,802	80.2	Same	80.2
mgc_superblue12	89	1,286,948	1,293,436	0	5,908	44.0	57.0	65.0
mgc_superblue19	286	506,097	511,687	0	15,422	52.3	80.7	67.3

Table 2: Benchmarks with floorplans revised from ISPD 2014

Design	#Macros	#Cells	#Nets	#Fence Regions	#I/O	%Area Utilization		Density Limit %
						Std Cell	Std Cell & Macro	
mgc_des_perf_a	4	108,292	115,187	4	374	42.9	71.7	42.9
mgc_des_perf_b	0	112,679	122,951	12	374	49.7	49.7	49.7
mgc_edit_dist_a	6	127,414	134,051	1	2,574	45.5	61.6	45.5
mgc_fft_a	6	30,625	32,090	0	3,010	25.1	74.0	50.0
mgc_fft_b	6	30,625	32,090	0	3,010	28.2	74.0	60.0
mgc_matrix_mult_a	5	149,650	154,286	0	4,802	41.9	76.7	60.0
mgc_matrix_mult_b	7	146,438	154,213	3	4,802	30.9	72.6	60.0
mgc_pci_bridge32_a	4	29,533	34,058	3	361	38.4	40.8	38.4
mgc_pci_bridge32_b	6	28,932	32,546	3	361	14.3	50.6	14.3
mgc_superblue11_a	1,458	925,616	935,731	4	27,371	43.0	73.0	65.0
mgc_superblue16_a	419	680,456	717,046	2	17,498	47.6	73.9	55.0

where f_{aff} denotes simple affine scaling

$$t \to 25 \cdot (t-a)/(b-a)$$

from $[a,b] = [wl_{min},\ 1.5 \cdot wl_{med}]$ into $[0,25]$.

7. CONCLUSION

Region placement constraints are widely used in industry to support voltage regions, datapath placement, and other design features. As floorplan complexity grows, so does the number and complexity of these regions, as does the challenge of producing detail-routable placements following all region constraints.

The ultimate measures of a placement's quality are its timing performance and its detailed routability. While the benchmarks described here still lack timing constraints, their routability and region constraints are reasonably complete. They represent some of the harder design challenges faced by industry in the year 2015 and beyond.

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