Lab-3 Q1 Report

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1 Question

Design a 1-bit full-adder. ‘a’ and ‘b’ are the two 1-bit numbers that are to be added. ‘cin’ is the input carry that should be added with ‘a’ and ‘b’. ‘sum’ and ‘cout’ are the sum and carry outputs respectively. This can be designed only in a structural way using only 1-bit half-adders and OR gates. It is mandatory to use the 1-bit half-adder for designing (i.e. at least one instance of 1-bit half-adder must be used.) The 1-bit half-adder itself must be designed only in a structural way using any basic gates.

```
entity OnebitFullAdd is
    port ( a, b, cin : in std_logic;
    sum, cout: out std_logic);
end entity;
```

2 Approach

1. Write/Draw the truth table of the 1 bit Half Adder.

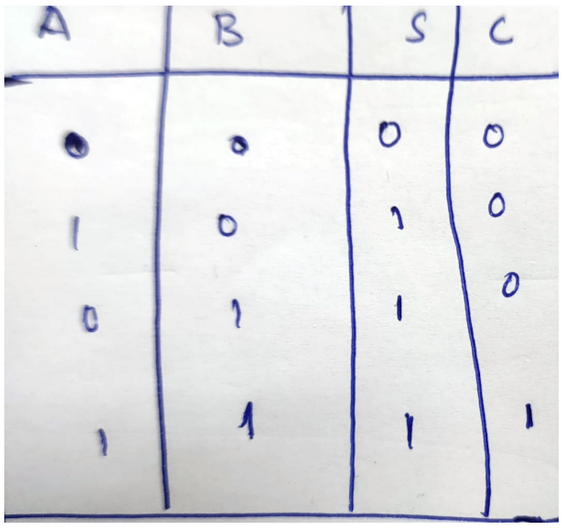


Figure 1: Half Adder Truth table

2. Figure out the logical expression for the outputs of the half adder.

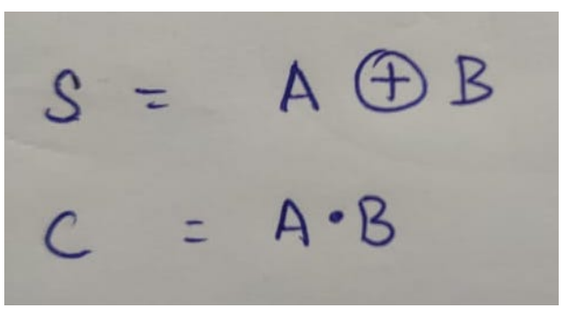
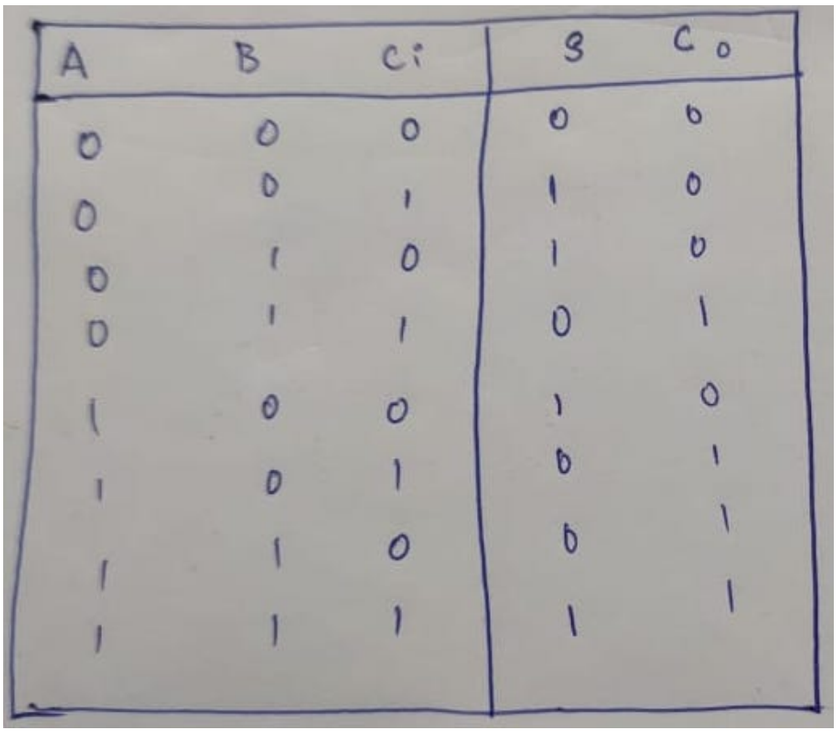


Figure 2: Half Adder Logic Expression

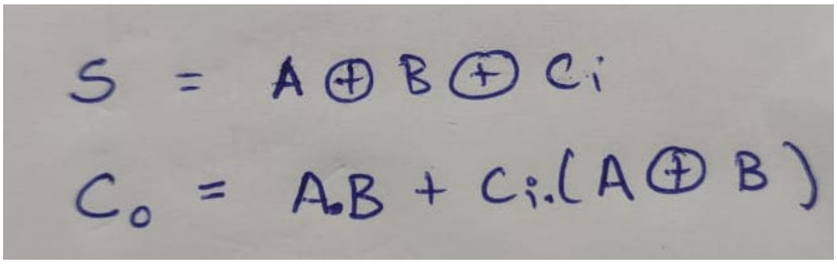
3. Write/Draw the truth table of the 1 bit Full Adder.



A	B	Ci	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Figure 3: Full Adder Truth table

4. Figure out the logical expression for the outputs of the full adder and simplify them.



$$S = A \oplus B \oplus C_i$$

$$C_o = A.B + C_i.(A \oplus B)$$

Figure 4: Full Adder Logic Expression

5. Figure out to use the half adders and OR gates to build a full adder. This is quite straightforward considering the form in which the expression was modified into.

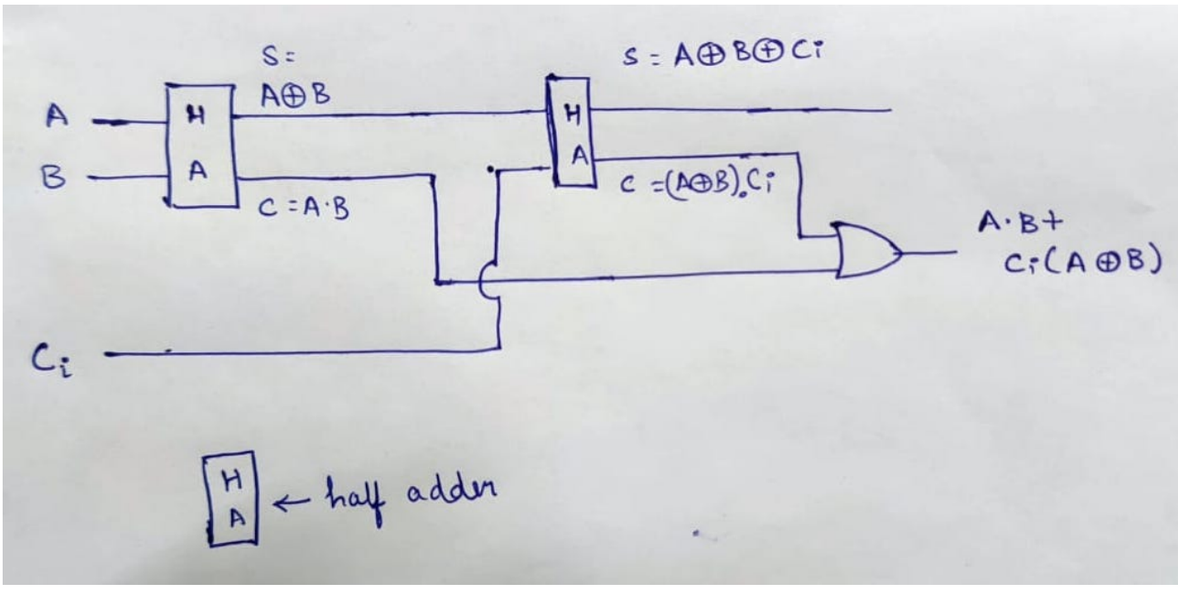


Figure 5: Full Adder using Half Adders

3 Details about Execution

- I created a 1-bit Half Adder out of basic gates as an individual component.
- Used two half adder instances and an OR gate to build the Full Adder component.(as shown in Fig 5)

4 Final Design

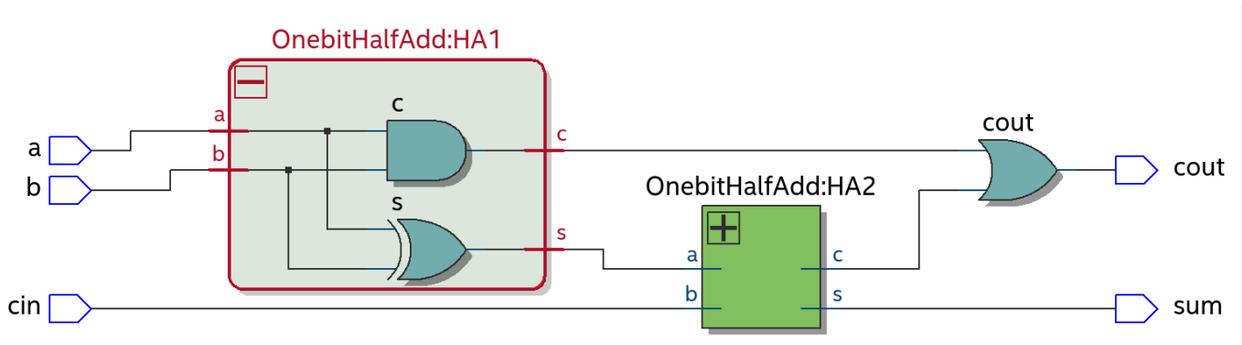


Figure 6: Full Adder

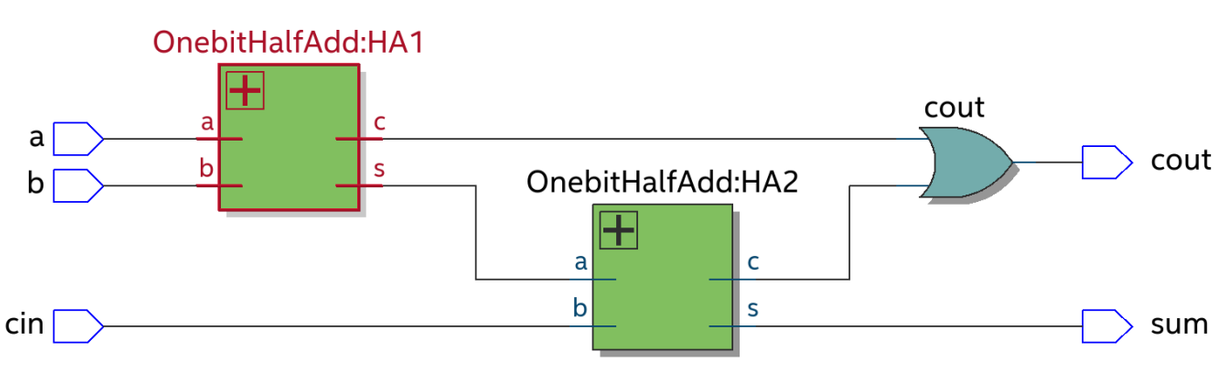


Figure 7: Full Adder

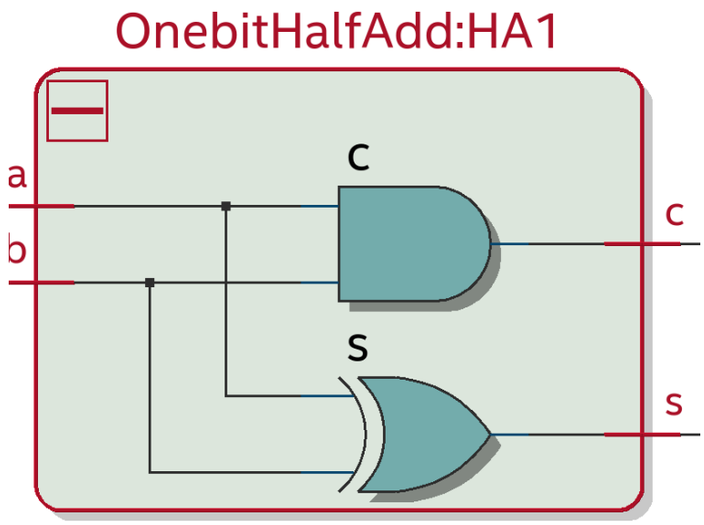


Figure 8: Half Adder Component

5 Waveform Outputs

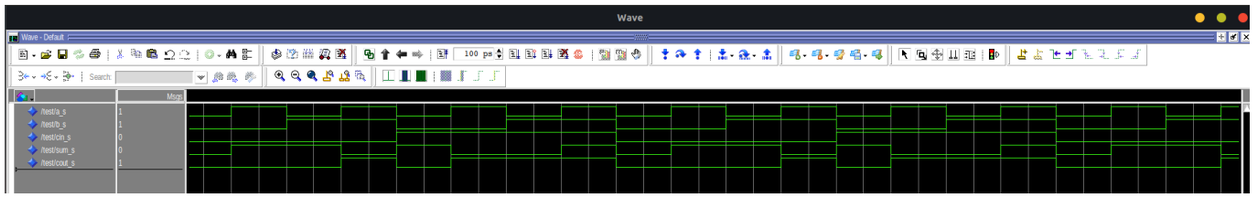


Figure 9: waveform image 1

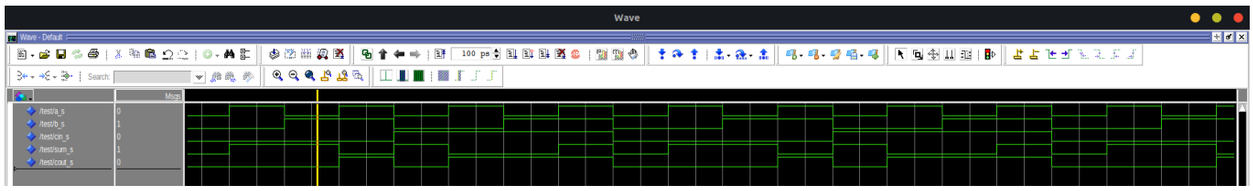


Figure 10: waveform image 2