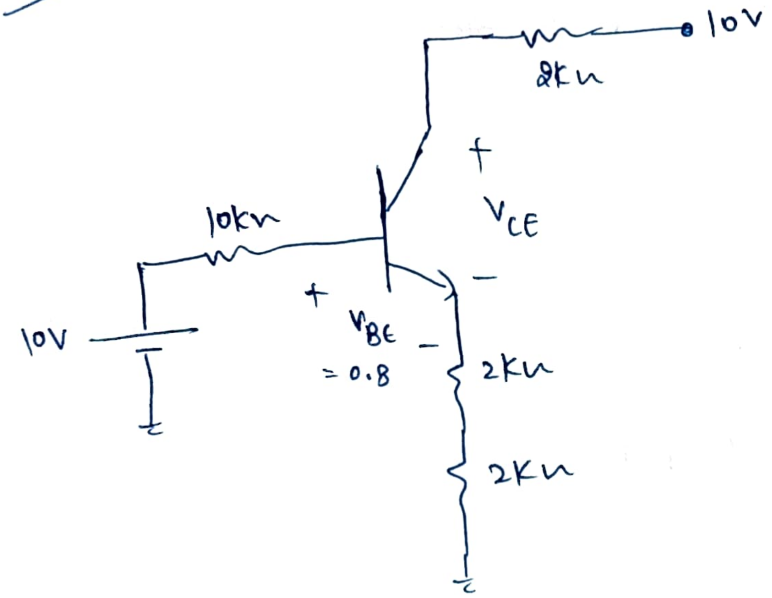
Q.1



Given, ~~Suppose~~ BJT is in the saturation region -

So, $V_{CE} = 0.2V$

By, applying KVL @ i/p loop -

$$-10 + 10K\, i_B + 0.8 + 4K\, i_E = 0$$

$$10K\, i_B + 4K(1+\beta)\, i_B = 9.2$$

$$i_B = \frac{9.2}{10K + 4K(1+\beta)}$$

And, $$i_{c\,active} = \beta i_B = \frac{9.2\beta}{10K + 4K(1+\beta)}$$

And By applying KVL @ o/p loop -

$$-10 + 2K\, i_{csat} + 0.2 + 4K(i_E) = 0$$

$$i_{csat} = \frac{9.8}{6K}$$

for BJT to be in the saturation -

$$\beta i_b > i_{c\,sat}.$$

$$\frac{9.2\beta}{10k + 4k(1+\beta)} > \frac{9.8}{6k}$$

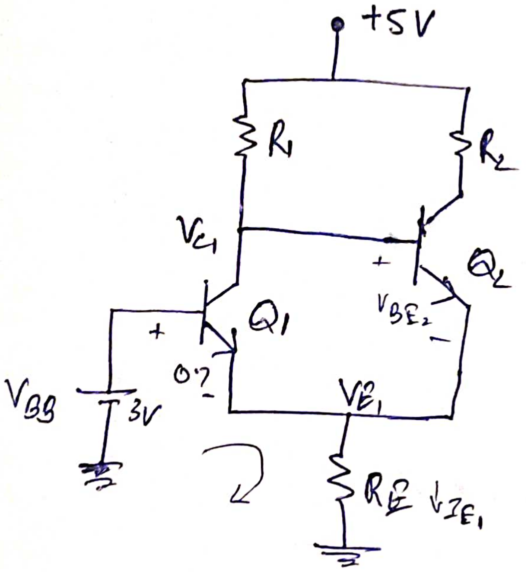
$$9.2\beta > 16.3 + 6.5(1+\beta)$$

$$2.7\beta > 22.8$$

$$\beta > 8.44 \quad (\text{or}) \quad \beta \cong 9$$

Q2) Given $V_{BB} = 3V$, $h_{fe} = 100$, Q_1 ON, Q_2 OFF

$R_1 = 4K\Omega$, $R_2 = 2.5K\Omega$



KVL at input of Q_1 :-

$$3 = 0.7 + V_{E_1} \Rightarrow V_{E_1} = 2.3V$$

$$I_{E_1} = \frac{2.3}{R_E}$$

$$V_{C_1} = 5 - \frac{2.3}{R_E} \times R_1 \quad — (1)$$

minimum voltage required to turn ON Q_2 is 3V

$$V_{BE_2} = V_{C_1} - V_{E_1}$$

$$0.7 = V_{C_1} - 2.3 \Rightarrow V_{C_1} = 3V$$

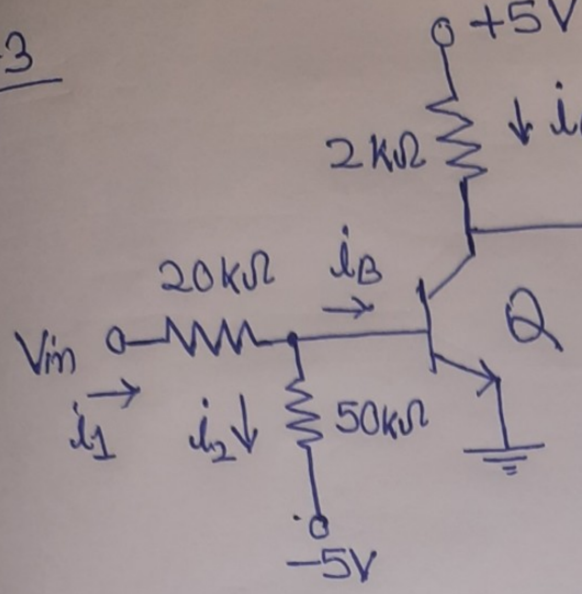
from eqn (1) –

$$5 - \frac{2.3}{R_E} \times R_1 < 3V$$

$$5R_E - 2.3 \times 4 < 3R_E$$

$$\therefore \boxed{R_E < 4.6K\Omega}$$

Sol-3



$\begin{bmatrix} V_{BE} = 0.8V \text{ for } V_o \text{ low} \\ V_{BE} = 0.5V \text{ for } V_o \text{ High} \end{bmatrix}$

npn BJT

low voltage = 0.2V ($V_{CE,sat}$)

high voltage = 5V (V_{CC})

(i) ~~Vi~~ if $V_{in} = 0.2V$

Assume Q - off $\Rightarrow I_B = 0$

$$\Rightarrow V_{BE} = \frac{V_{in} - (-5)}{20K + 50K} \times 50K + (-5) \simeq -1.286V$$

$V_{BE} < 0.5V$: Assumption correct

$I_C \simeq 0 \quad V_o \simeq 5V$

(ii) if $V_{in} = 5V$: ~~VBE~~

Assume Q-ON (saturation) : $V_{BE} = 0.8V$

$\cancel{I_B = 5 - 0}$. $\Rightarrow i_1 = i_2 + i_B$

$$i_1 = \cancel{\frac{V_{in} - (0.8)}{}} = \frac{V_{in} - 0.8}{20K} = \frac{5 - 0.8}{20K} = 0.21 \text{ mA} \quad \left(i_1 = \frac{V_{in} - V_{BE}}{20K} \right)$$

$$i_2 = \frac{0.8 - (-5)}{50K} = 0.116 \text{ mA} \quad \left(i_2 = \frac{V_{BE} - (-5)}{50K} \right)$$

$$i_B = i_1 - i_2 = 0.094 \text{ mA}$$

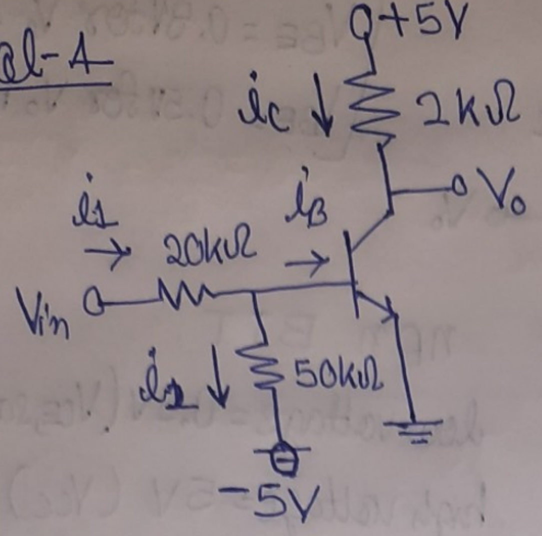
$$I_C = \frac{5 - 0.2}{2K} = 2.4 \text{ mA} \quad \left(I_C = \frac{5 - \overbrace{V_{CE,low}}^{0.2V}}{2K} \right)$$

$$\Rightarrow \frac{I_C}{I_B} = \frac{2.4}{0.094} \simeq 25.532$$

if $\beta > 25.532$ then assumption is correct

$$\Rightarrow V_o = V_{CE} = 0.2V$$

Sol-1



* KCL at Base

$$i_1 = i_2 + i_B$$

1) Solving for V_{iL} and V_{OH}

$V_{BE} = 0.5V$ (given)

$$\Rightarrow i_1 = \frac{V_{in} - V_{BE}}{20k} = \frac{V_{iL} - 0.5}{20k} \; ; \; i_2 = \frac{V_{BE} - (-5)}{50k} = \frac{0.5+5}{50K}$$

~~Assuming~~, for $V_{in} = V_{iL}$, $i_B \simeq 0$; $i_1 = i_2$

$$\Rightarrow \frac{V_{iL} - 0.5}{20K} = \frac{0.5+5}{50K} \Rightarrow V_{iL} = \frac{20}{50} \times 5.5 + 0.5 = 2.7V$$

$\Rightarrow V_{OH}$ will be 5V

2) Solving for V_{IH} and V_{OL}

$\Rightarrow V_{BE} = 0.8$ (given)

$$\Rightarrow i_1 = \frac{V_{in} - V_{BE}}{20K} = \frac{V_{iH} - 0.8}{20K} \; ; \; i_1 = \frac{V_{BE} - (-5)}{50K} = \frac{0.8+5}{50}$$

$$i_C = \frac{5 - 0.2}{2k} = \frac{5 - V_{CE,low}}{2k} = 2.4mA$$

$$\Rightarrow i_B = \frac{i_C}{\beta} = 0.024mA$$

$$\Rightarrow \frac{V_{iH} - 0.8}{20K} = \frac{0.8+5}{50k} + 0.024$$

$$V_{iH} = 20 \times 0.14 + 0.8 = 3.6$$

* input is sufficiently high, so $V_{OL} \simeq 0.2V$

* Noise margin

$NM_L = V_{iL} - V_{OL} = 2.7 - 0.2 = 2.5V$

$NM_H = V_{OH} - V_{iH} = 5 - 3.6 = 1.4V$

Tutorial 8 Solution

Q.5

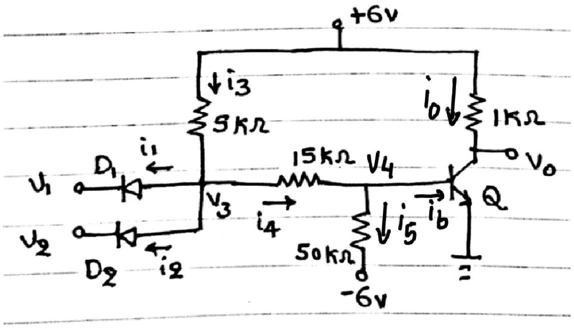


Fig. A DTL NAND gate

Find the power dissipation in the circuit (NAND gate)

For all the NAND gate input/output combinations shown below '1' logic is +6V and '0' logic is 0V

(Assuming all diodes and BJT are ideal)

Truth Table (NAND Gate)

V_1	V_2	V_0	
0	0	1	case 1
0	1	1	case 2
1	0	1	case 3
1	1	0	case 4

When case 1, case 2, case 3 is considered

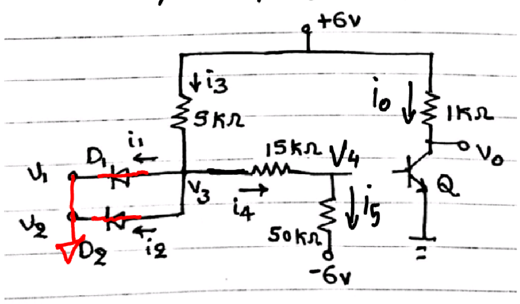


Fig. A DTL NAND gate

D_1 and D_2 will short circuit the $5k\Omega$ resistor to ground

BJT will be in cutoff. $(i_0 = 0) \rightarrow V_0 = +6V \rightarrow i_0 = 0\,mA$

KCL at $V_3 \rightarrow i_1 + i_2 = i_3$

$\therefore i_3 = \frac{6-0}{5k\Omega} = 1.2mA$

Power dissipated $P_1 = 6 \times i_3 = 7.2mW$

KCL at $V_4 \rightarrow i_4 = i_5$

$\therefore i_5 = \frac{0+6}{65k\Omega} = 0.092\,mA$

$P_2 = 6 \times i_5 = 6 \times 0.092 = 0.552\,mW$

Total power dissipated $= P = 7.2 + 0.552 = 7.752mW$

When Case 4 is considered

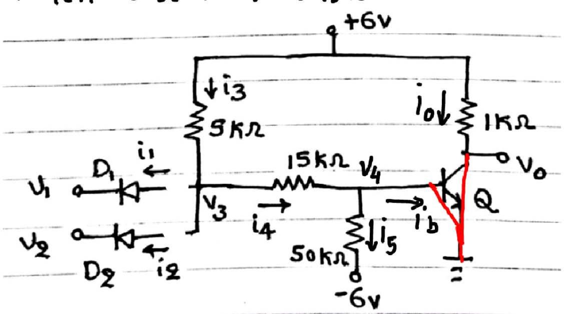


Fig. A DTL NAND gate

D_1 and D_2 will be open circuited

KCL at $V_3 \rightarrow i_3 = i_4$

$\therefore \frac{6 - V_4}{20k\Omega} = i_3$

$\therefore i_3 = 0.3mA$

$P_1 = 6 \times i_3 = 1.8mW$

BJT will be in saturation and act as short to the ground. $\rightarrow V_4 = V_0 = 0V$

$\frac{6 - V_0}{1k\Omega} = i_0$

$\therefore i_0 = 6mA$

$P_2 = 6 \times i_0 = 36mW$

KCL at V_4.

$i_4 = i_5 + i_b$

$\because i_5 = \frac{V_4 + 6}{50k\Omega} = 0.12mA$

$\therefore i_b = i_4 - i_5 = 0.3 - 0.12mA = 0.18mA$

$P_3 = 6 \times i_5 = 0.72mA$

$\therefore$ Total dissipated power

$P = P_1 + P_2 + P_3 = 1.8 + 36 + 0.72$

$\therefore P = 38.52\,mW$