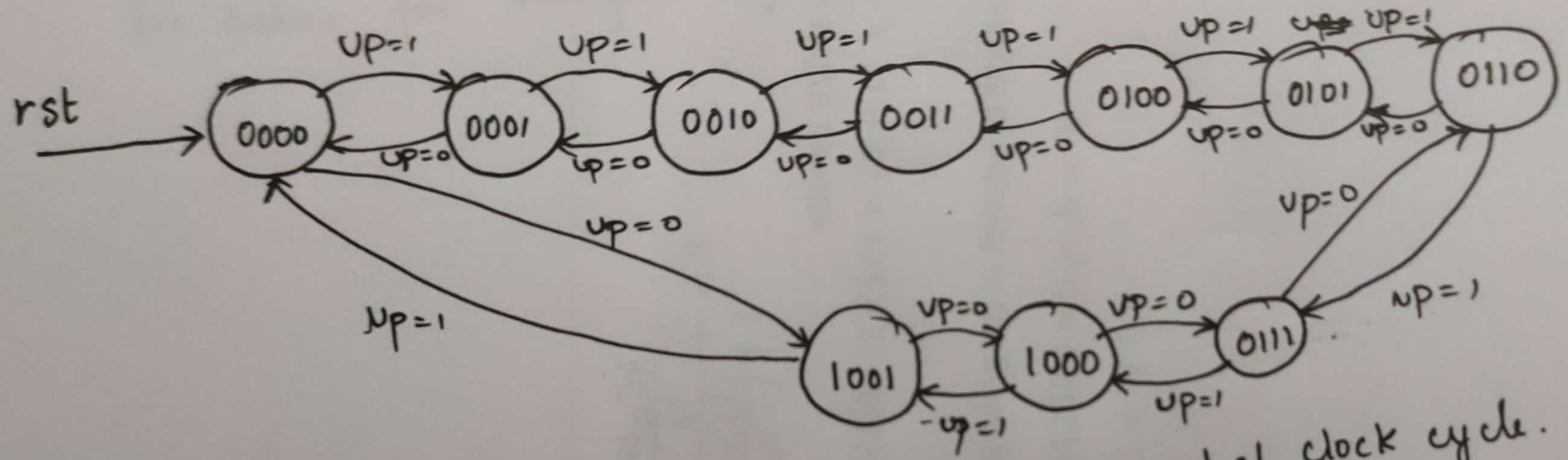
CS232 Lab 5 Q1

Mod 10 up-Down Counter



State Machine

if rst='1' then state will be zero at end of clock cycle.

if rst='0' ⟶ up='1' the state increases by 1

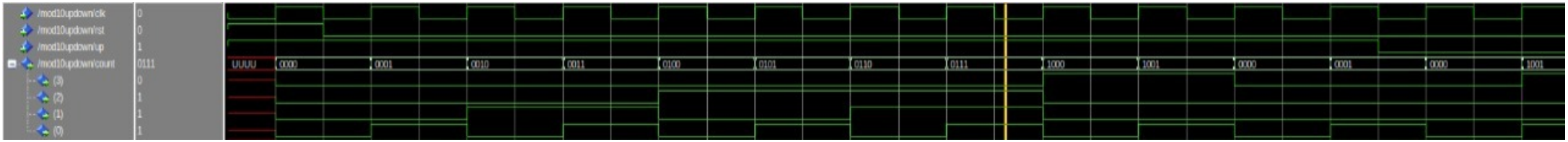
up='0' the state decreases by 1

How I achieve above state machine:

I use 2 processes.
The first one which is sensitive to clock and after every clock cycle, checks for the conditions given above and accordingly updates value of new state.

The second process updates the state and count signals to give the appropriate signals as output.

See below for waveform of output.


/mod10updown/clk
/mod10updown/rst
/mod10updown/up
/mod10updown/count
(3)
(2)
(1)
(0)
0
0
1
0111
0
1
1
1
UUUU
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
0000
0001
0000
1001