Handwritten Digit Recognition

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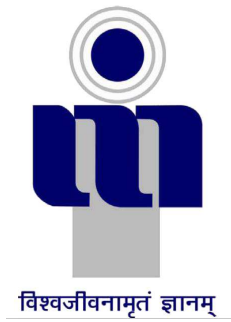

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Introduction

- **Handwritten digits recognition** in a computer vision system is a challenging task that is essential to many new applications. Researchers in computer vision and machine learning have utilised it extensively to build useful applications like **computerised bank check numbers reading**.

- Each digit is represented as an **image** and hence can be processed for finding **similar type of patterns** and hence can be used for classification.

Figure 1: Handwritten digits

Objective

- To train an ANN (Artificial Neural Network) model for prediction of handwritten digits.
- Defining the required hardware configuration for the same in the industry.

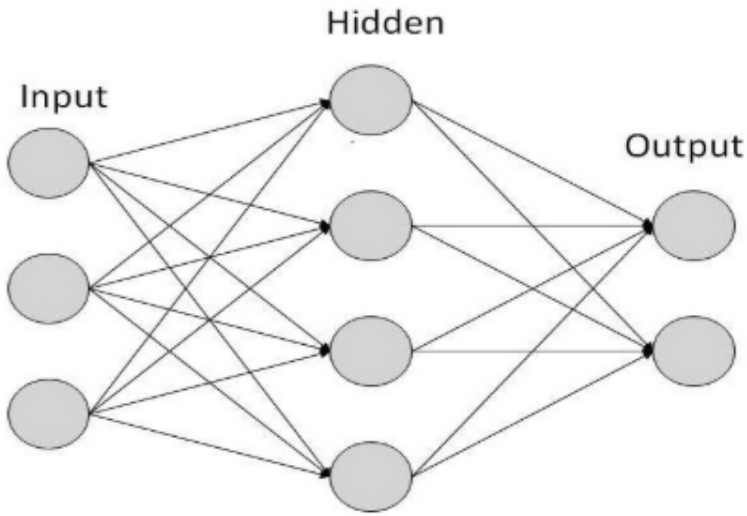

Figure 2: General ANN network

Experimental setup

Dataset Used:**MNIST**

- The MNIST database of handwritten digits, has a training set of 60,000 examples, and a test set of 10,000 examples. It is a subset of a larger set available from **NIST**. The digits have been size-normalized and centered in a fixed-size image.
- The **3 Densely layers: input, hidden, and output** performing computation and push the output forward with activation function set as 'Sigmoid' for all the layers.
- Output layer contains **10 neurons**, and is wrapped with 'Sigmoid' activation function.

Experimental setup

Dataset:**MNIST**

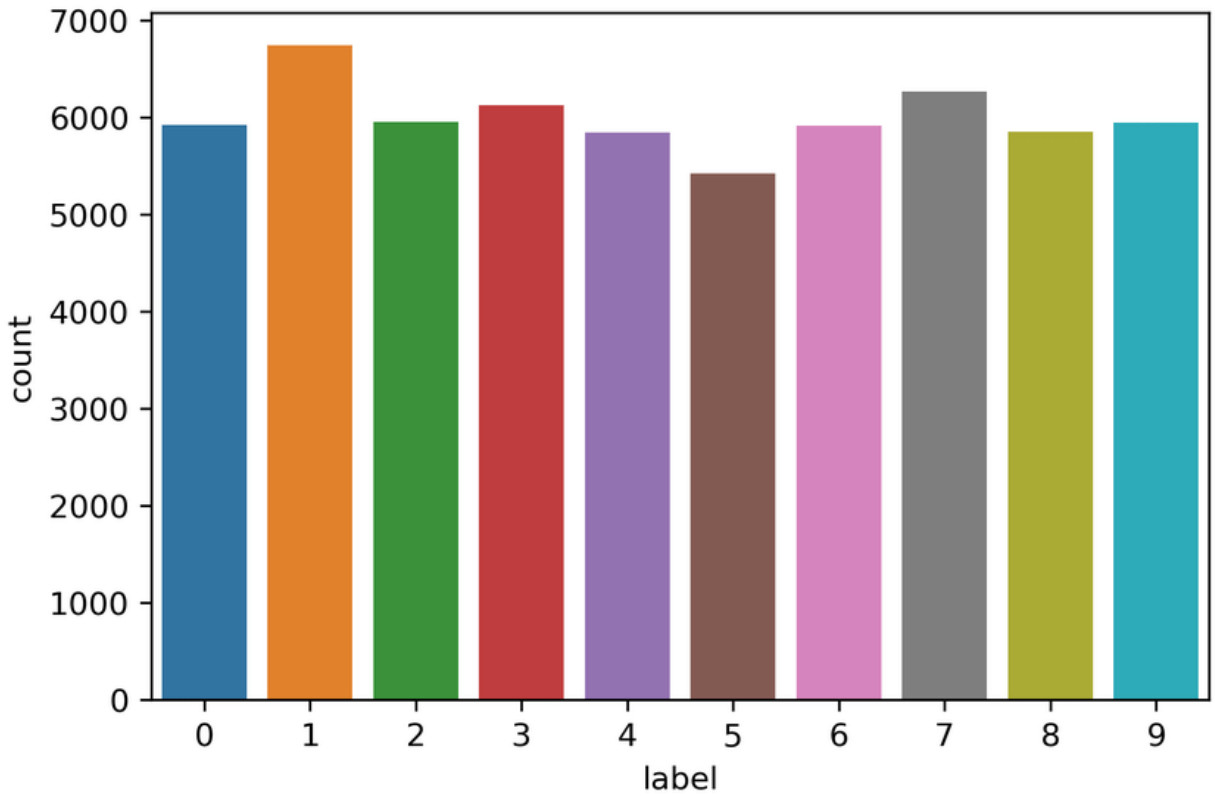

Figure 3: Distribution of Dataset

Model Function

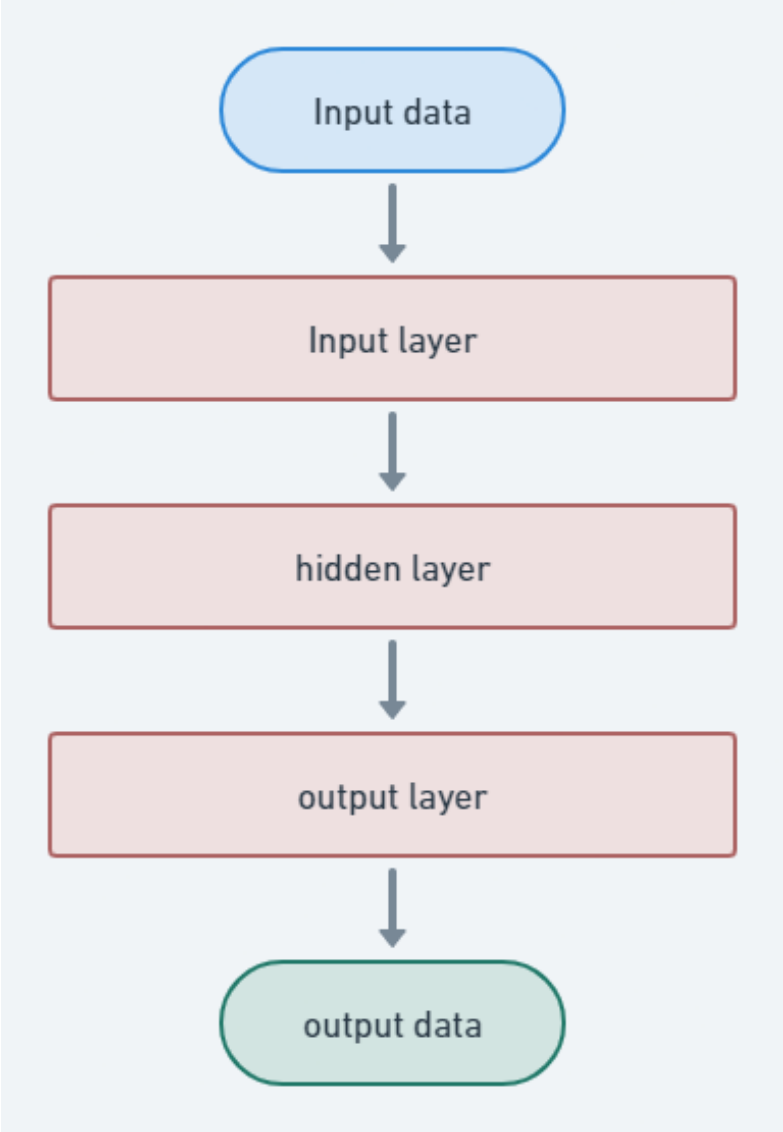

Figure 4: Technical Flowchart

Experimental result

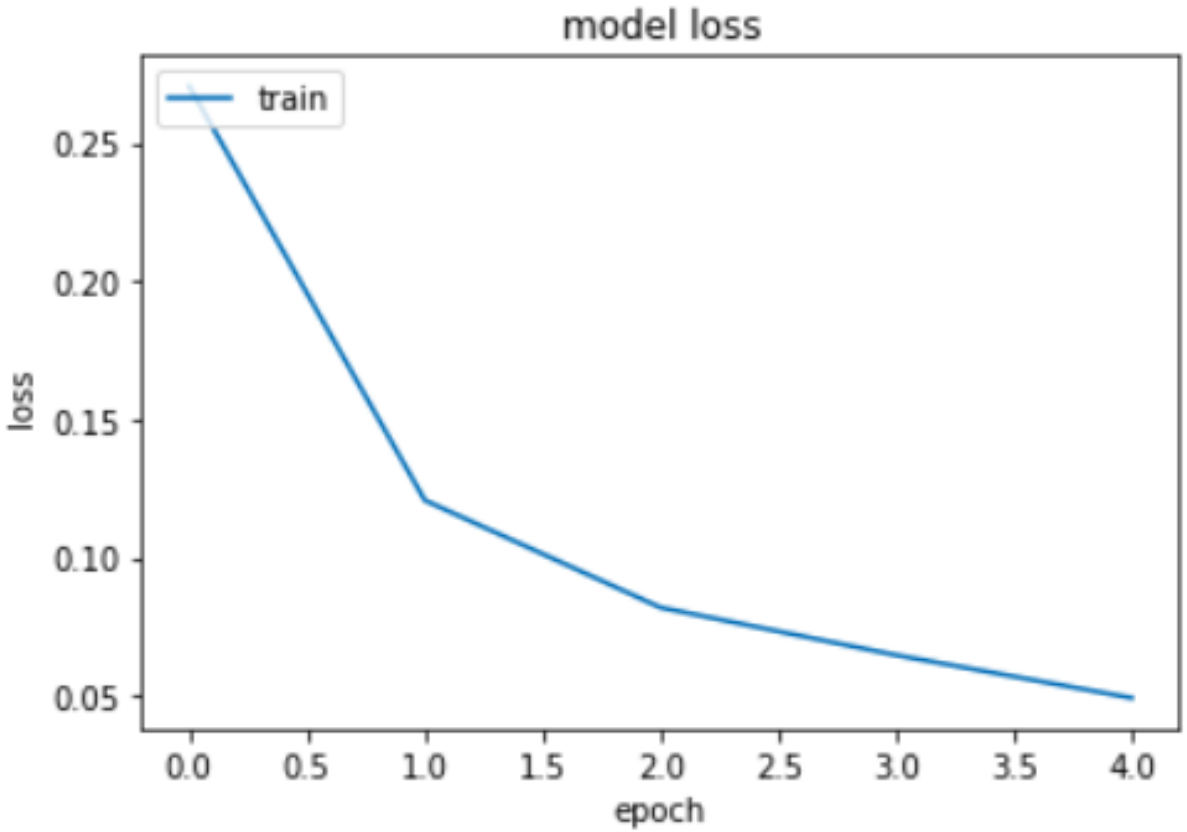

Figure 5: Train loss decreases as epochs increase

Experimental result

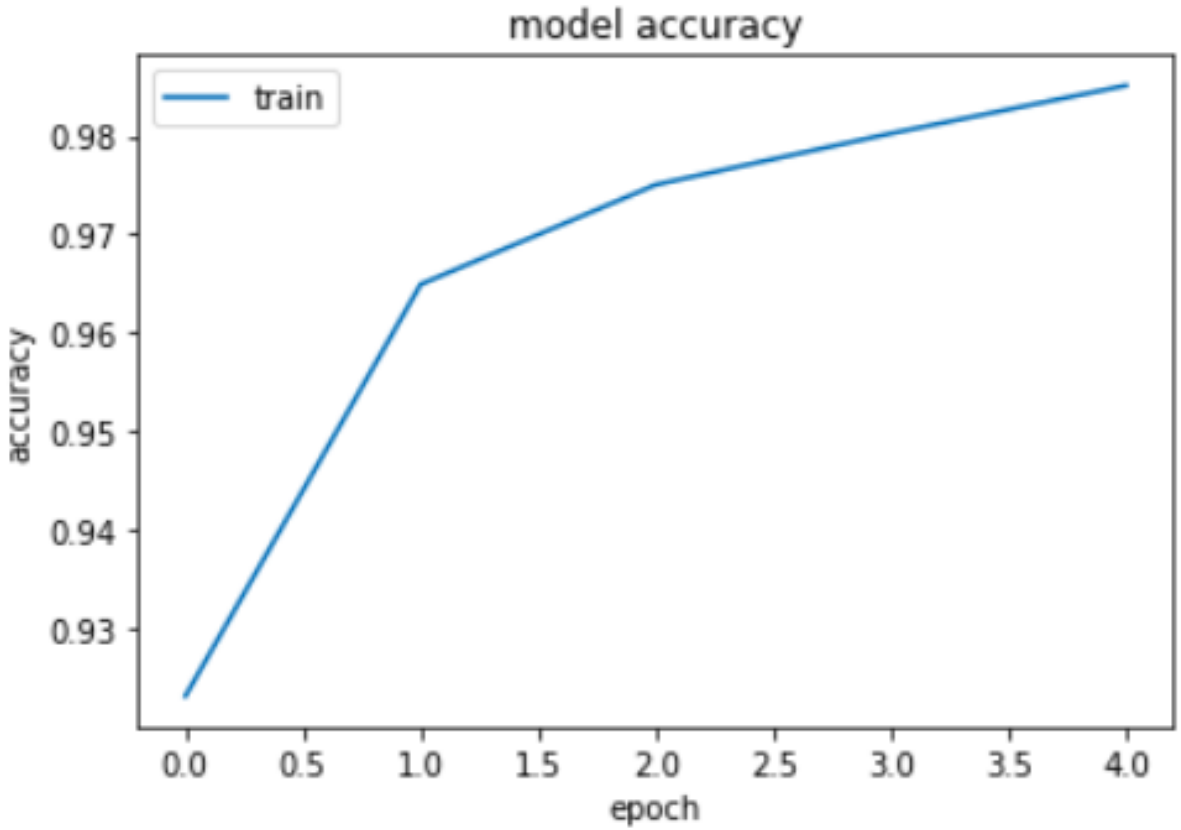

Figure 6: Train accuracy increases as epochs increases

Experimental result

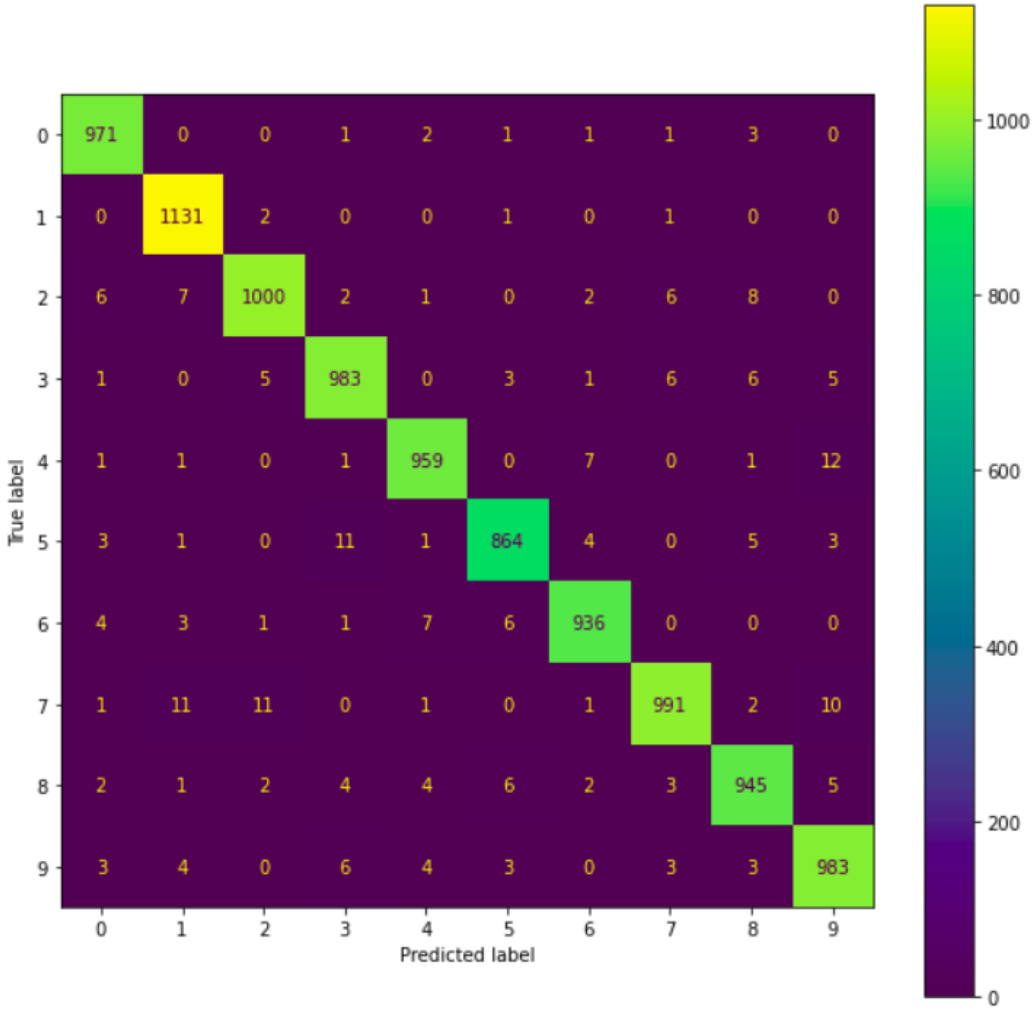

Figure 7: Confusion Matrix

Performance Estimates

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	8.451	1.25

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
1114548	1114548	1114548	1114548	none

Detail

Instance

N/A

Loop

	Latency			Initiation Interval			
Loop Name	min	max	Iteration Latency	achieved	target	Trip Count	Pipelined
- memcpy_lay1	156899	156899	1569	-	-	100	no
+ memcpy_lay1	1567	1567	2	-	-	784	no
- Loop 2	200	200	2	-	-	100	no
- Loop 3	945900	945900	9459	-	-	100	no
+ Loop 3.1	9408	9408	12	-	-	784	no
- Loop 4	11510	11510	1151	-	-	10	no
+ Loop 4.1	1100	1100	11	-	-	100	no

Figure 8: Performance Estimates

Memory

Detail

Instance

Instance	Module	BRAM_18K	DSP48E	FF	LUT
hand_written_digig8j_U1	hand_written_digig8j	0	2	205	390
hand_written_digihbi_U2	hand_written_digihbi	0	3	143	322
hand_written_digiibs_U3	hand_written_digiibs	0	0	128	284
hand_written_digijbC_U4	hand_written_digijbC	0	0	100	137
hand_written_digikbM_U5	hand_written_digikbM	0	0	66	239
hand_written_digilbW_U6	hand_written_digilbW	0	7	324	906
hand_written_digimb6_U7	hand_written_digimb6	0	3	509	1165
hand_written_digincg_U8	hand_written_digincg	0	0	3211	3644
hand_written_digiocq_U9	hand_written_digiocq	0	0	394	238
hand_written_digit_classification_CRTL_BUS_s_axi_U	hand_written_digit_classification_CRTL_BUS_s_axi	0	0	106	168
Total	10	0	15	5186	7493

DSP48

Memory

Memory	Module	BRAM_18K	FF	LUT	Words	Bits	Banks	W*Bits*Banks
hand_written_digit_c_1_U	hand_written_digibkb	256	0	0	78400	32	1	2508800
b1_0_U	hand_written_digicud	1	0	0	100	32	1	3200
lay21_U	hand_written_digidEe	2	0	0	1000	32	1	32000
lay1_U	hand_written_digieOg	256	0	0	78400	32	1	2508800
h1_U	hand_written_digifYi	1	0	0	100	32	1	3200
Total	5	516	0	0	158000	160	5	5056000

Figure 9: Memory

Utilization Estimates

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT
DSP	-	-	-	-
Expression	-	-	0	550
FIFO	-	-	-	-
Instance	0	15	5186	7493
Memory	516	-	0	0
Multiplexer	-	-	-	959
Register	-	-	1001	-
Total	516	15	6187	9002
Available	40	40	16000	8000
Utilization (%)	1290	37	38	112

Figure 10: Utilization Estimates

Vivado Results

Expression

Variable Name	Operation	DSP48E	FF	LUT	Bitwidth P0	Bitwidth P1
i_1_fu_502_p2	+	0	0	15	7	1
i_2_fu_575_p2	+	0	0	13	4	1
i_fu_479_p2	+	0	0	15	7	1
indvarinc1_fu_440_p2	+	0	0	17	10	1
indvarinc_fu_434_p2	+	0	0	15	7	1
j_2_fu_519_p2	+	0	0	17	10	1
j_3_fu_593_p2	+	0	0	15	7	1
next_mul2_fu_490_p2	+	0	0	24	17	10
next_mul4_fu_559_p2	+	0	0	17	10	7
next_mul_fu_428_p2	+	0	0	24	17	10
tmp_13_fu_534_p2	+	0	0	24	17	17
tmp_1_fu_450_p2	+	0	0	24	17	17
tmp_29_fu_608_p2	+	0	0	17	10	10
tmp_26_fu_705_p2	and	0	0	8	1	1
tmp_28_fu_711_p2	and	0	0	8	1	1
exitcond1_fu_569_p2	icmp	0	0	9	4	4
exitcond3_fu_513_p2	icmp	0	0	13	10	9
exitcond4_fu_496_p2	icmp	0	0	11	7	6
exitcond5_fu_473_p2	icmp	0	0	11	7	6
exitcond_fu_587_p2	icmp	0	0	11	7	6
notlhs8_fu_687_p2	icmp	0	0	11	8	2
notlhs_fu_669_p2	icmp	0	0	11	8	2
notrhs9_fu_693_p2	icmp	0	0	18	23	1
notrhs_fu_675_p2	icmp	0	0	18	23	1
tmp_2_fu_461_p2	icmp	0	0	13	10	9
tmp_3_fu_467_p2	icmp	0	0	11	7	6
tmp_24_fu_681_p2	or	0	0	8	1	1
tmp_25_fu_699_p2	or	0	0	8	1	1
mm_1_fu_723_p3	select	0	0	32	1	32
num_1_fu_716_p3	select	0	0	32	1	32
tmp_18_neg_fu_623_p2	xor	0	0	40	32	33
tmp_9_neg_fu_549_p2	xor	0	0	40	32	33
Total	32	0	0	550	324	264

Figure 11: Expressions

Vivado Results

Interface

Summary

RTL Ports	Dir	Bits	Protocol	Source Object	C Type
s_axi_CRTL_BUS_AWVALID	in	1	s_axi	CRTL_BUS	scalar
s_axi_CRTL_BUS_AWREADY	out	1	s_axi	CRTL_BUS	scalar
s_axi_CRTL_BUS_AWADDR	in	5	s_axi	CRTL_BUS	scalar
s_axi_CRTL_BUS_WVALID	in	1	s_axi	CRTL_BUS	scalar
s_axi_CRTL_BUS_WREADY	out	1	s_axi	CRTL_BUS	scalar
s_axi_CRTL_BUS_WDATA	in	32	s_axi	CRTL_BUS	scalar
s_axi_CRTL_BUS_WSTRB	in	4	s_axi	CRTL_BUS	scalar
s_axi_CRTL_BUS_ARVALID	in	1	s_axi	CRTL_BUS	scalar
s_axi_CRTL_BUS_ARREADY	out	1	s_axi	CRTL_BUS	scalar
s_axi_CRTL_BUS_ARADDR	in	5	s_axi	CRTL_BUS	scalar
s_axi_CRTL_BUS_RVALID	out	1	s_axi	CRTL_BUS	scalar
s_axi_CRTL_BUS_RREADY	in	1	s_axi	CRTL_BUS	scalar
s_axi_CRTL_BUS_RDATA	out	32	s_axi	CRTL_BUS	scalar
s_axi_CRTL_BUS_RRESP	out	2	s_axi	CRTL_BUS	scalar
s_axi_CRTL_BUS_BVALID	out	1	s_axi	CRTL_BUS	scalar
s_axi_CRTL_BUS_BREADY	in	1	s_axi	CRTL_BUS	scalar
s_axi_CRTL_BUS_BRESP	out	2	s_axi	CRTL_BUS	scalar
ap_clk	in	1	ap_ctrl_hs	hand_written_digit_classification	return value
ap_rst_n	in	1	ap_ctrl_hs	hand_written_digit_classification	return value
interrupt	out	1	ap_ctrl_hs	hand_written_digit_classification	return value
X_Addr_A	out	32	bram	X	array
X_EN_A	out	1	bram	X	array
X_WEN_A	out	4	bram	X	array
X_Din_A	out	32	bram	X	array
X_Dout_A	in	32	bram	X	array
X_Clk_A	out	1	bram	X	array
X_Rst_A	out	1	bram	X	array

Figure 12: Interface

Vivado Results

Multiplexer

Name	LUT	Input Size	Bits	Total Bits
ap_NS_fsm	725	165	1	165
grp_fu_350_p0	15	3	32	96
grp_fu_355_p0	15	3	32	96
grp_fu_355_p1	15	3	32	96
grp_fu_370_p1	15	3	32	96
h1_address0	21	4	7	28
h1_d0	21	4	32	128
i1_reg_235	9	2	7	14
i2_reg_246	9	2	7	14
invdar1_reg_224	9	2	10	20
invdar_reg_200	9	2	7	14
j_1_reg_339	9	2	7	14
j_reg_269	9	2	10	20
lay1_address0	15	3	17	51
mm_reg_303	9	2	32	64
num_2_reg_292	9	2	4	8
num_reg_280	9	2	32	64
phi_mul1_reg_257	9	2	17	34
phi_mul3_reg_315	9	2	10	20
phi_mul_reg_212	9	2	17	34
tmp_14_reg_327	9	2	32	64
Total	959	214	377	1140

Figure 13: Multiplexers

Vivado Results

- **Register**

Name	FF	LUT	Bits	Const Bits
X_load_reg_817	32	0	32	0
ap_CS_fsm	164	0	164	0
h1_addr_1_reg_794	7	0	7	0
i1_reg_235	7	0	7	0
i2_reg_246	7	0	7	0
i_1_reg_789	7	0	7	0
i_2_reg_850	4	0	4	0
i_reg_766	7	0	7	0
indvarinc1_reg_741	10	0	10	0
indvarinc_reg_736	7	0	7	0
invdar1_reg_224	10	0	10	0
invdar_reg_200	7	0	7	0
j_1_reg_339	7	0	7	0
j_2_reg_802	10	0	10	0
j_3_reg_858	7	0	7	0
j_reg_269	10	0	10	0
lay1_load_reg_822	32	0	32	0
lay21_load_reg_878	32	0	32	0
mm_reg_303	32	0	32	0
next_mul2_reg_781	17	0	17	0
next_mul4_reg_837	10	0	10	0
next_mul_reg_731	17	0	17	0
num_2_cast2_reg_842	4	0	32	28
num_2_reg_292	4	0	4	0
num_reg_280	32	0	32	0
phi_mul1_reg_257	17	0	17	0
phi_mul3_reg_315	10	0	10	0
phi_mul_reg_212	17	0	17	0
reg_385	32	0	32	0
reg_390	32	0	32	0
reg_396	32	0	32	0
reg_402	32	0	32	0
reg_407	64	0	64	0
reg_412	64	0	64	0
reg_417	64	0	64	0
reg_422	32	0	32	0
tmp_14_reg_327	32	0	32	0
tmp_18_neg_reg_873	32	0	32	0
tmp_27_reg_888	1	0	1	0
tmp_2_reg_756	1	0	1	0
tmp_31_cast_reg_746	17	0	64	47
tmp_4_reg_771	7	0	64	57
tmp_9_neg_reg_827	32	0	32	0
Total	1001	0	1133	132

Experimental conclusion

Following are the conclusions drawn from the experiments:

1) The model performs quite well with an accuracy about 97

2) We have also defined for the necessary hardware configurations, its utilisation and the interface it provides.

Thank You