


Cypress_DVT_Adapter_RP01

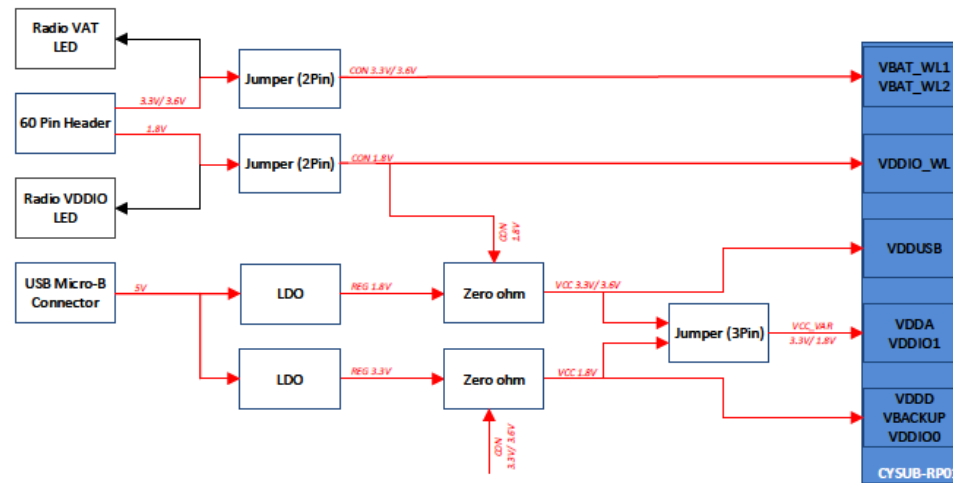
CONTENTS	
PAGE	DESCRIPTION
01	Title, Table of Contents & Drawing Numbers
02	Block Diagram
03	Power Supply - 1
04	Module RP01
05	60-Pin Connector (SDIO)
06	SWD/JTAG Header & Strapping Options
07	Revision History

Drawing Numbers

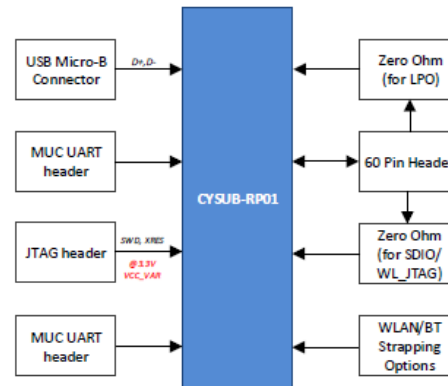
PCBA	121-ZET0007-01
PCB	600-ZET0007-01
FAB DRW	610-ZET0007-01
ASSY DRW	620-ZET0007-01
SCH DRW	630-ZET0007-01

		CYPRESS SEMICONDUCTOR 198 CHAMPION COURT SAN JOSE, CA 95134 (408) 943-2600					
CYPRESS SEMICONDUCTOR © 2019							
SCH Title : Cypress_DVT_Adapter_RP01							
Page Title :Title Page							
Size B	Document Number 630-ZET0007-01	Drawn By SANJEEVI	Approved By <Approved>	Rev 0.1			
Date:	Friday, July 26, 2019		Sheet	1 of 7			

Block Diagram



Functional



CYPRESS SEMICONDUCTOR
 198 CHAMPION COURT
 SAN JOSE, CA 95134
 (408) 943-2600

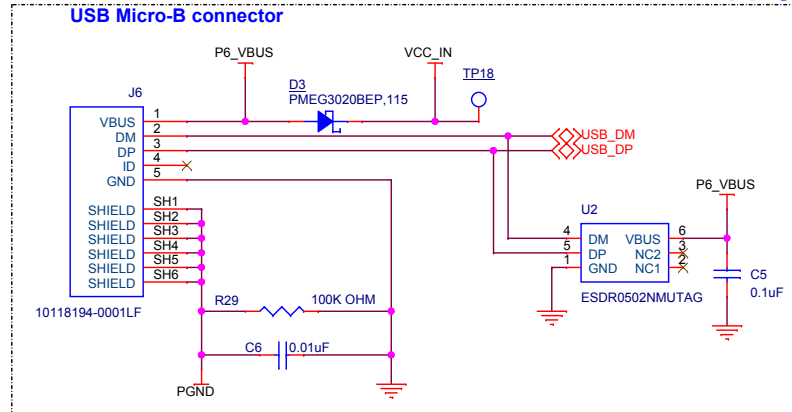
CYPRESS SEMICONDUCTOR © 2019

SCH Title : Cypress_DVT_Adapter_RP01

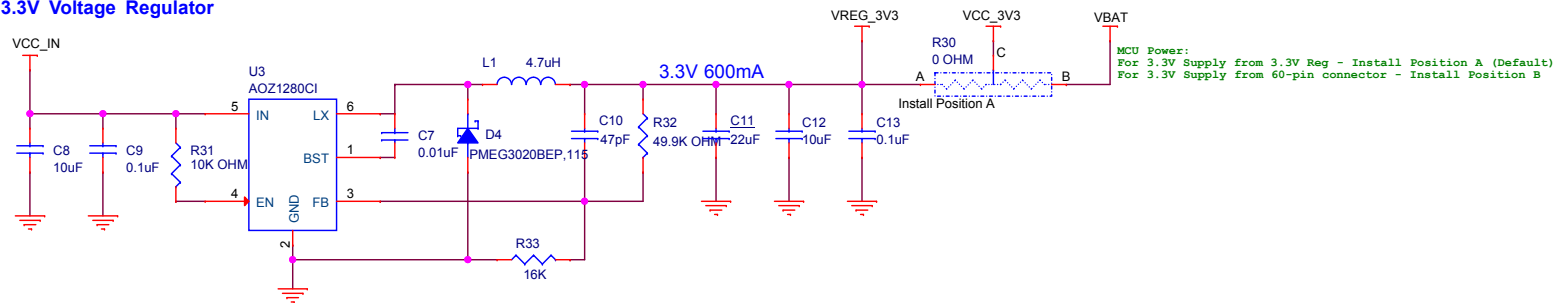
Page Title :Block Diagram

Size	Document Number	Drawn By	Approved By	Rev
B	630-ZET0007-01	SANJEEVI	<Approved>	0.1
Date:	Friday, July 26, 2019		Sheet	2 of 7

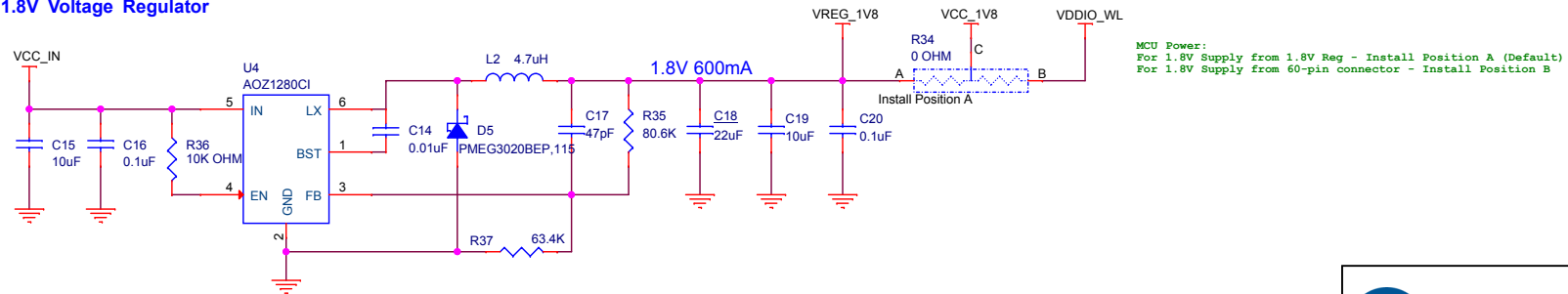
Power Supply - 1



3.3V Voltage Regulator



1.8V Voltage Regulator



CYPRESS SEMICONDUCTOR © 2019

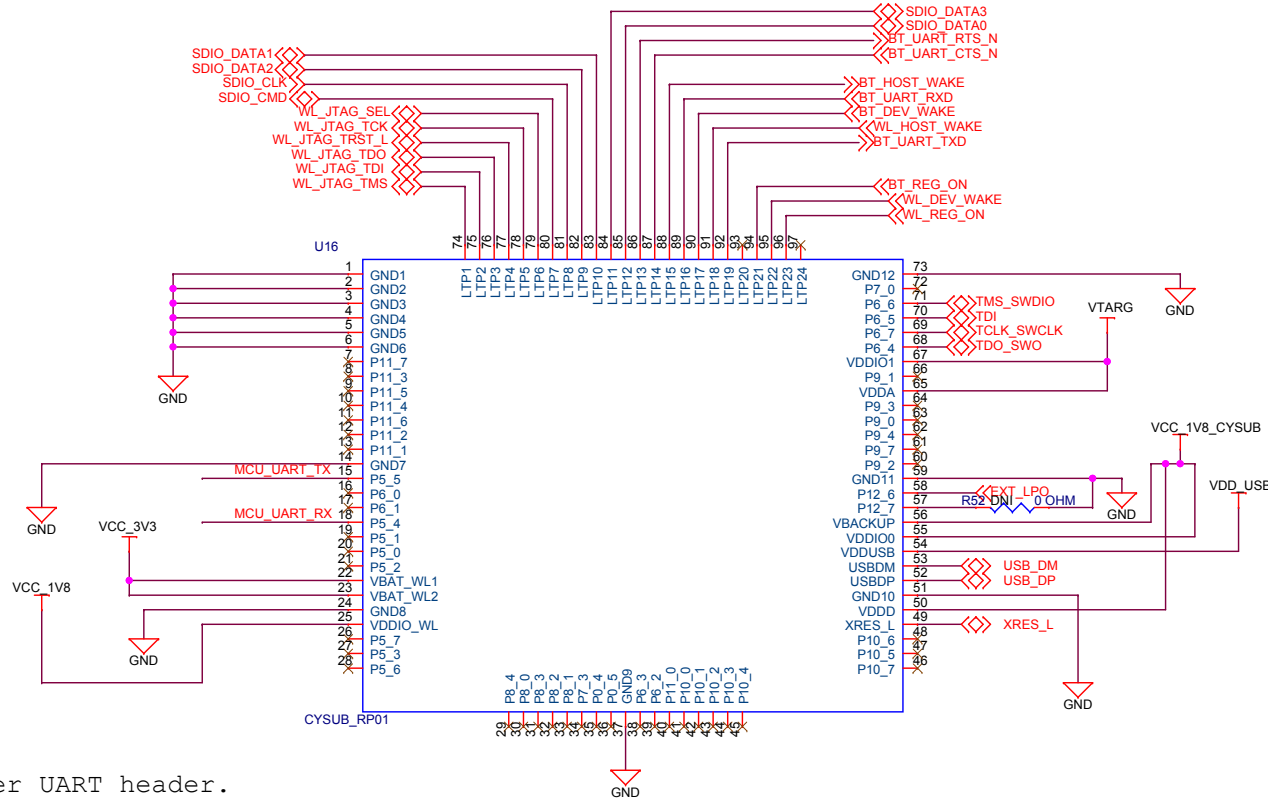
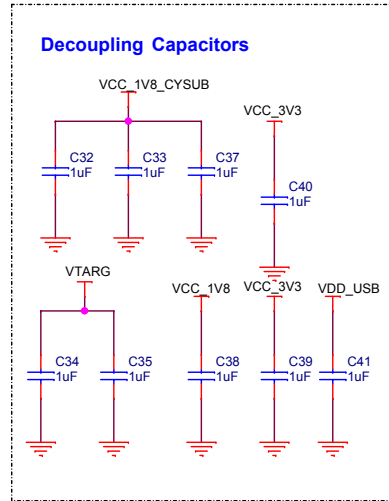
SCH Title : Cypress_DVT_Adapter_RP01

Page Title :Power Supply - 1

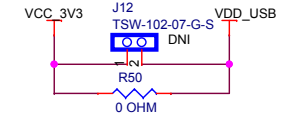
Size	Document Number	Drawn By	Approved By	Rev
B	630-ZET0007-01	SANJEEVI	<Approved>	0.1
Date:	Friday, July 26, 2019		Sheet	3 of 7

CYSUB_RP01

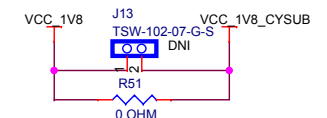
Decoupling Capacitors



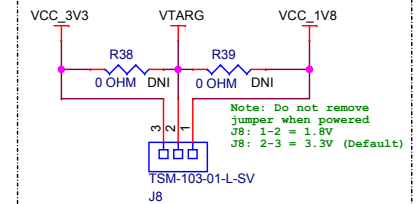
VDDUSB Current Measurement



VCC_1V8_CYSUB Current Measurement

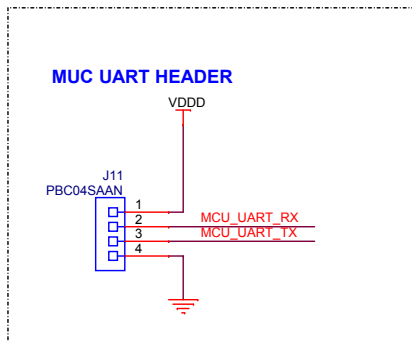


MCU Voltage Selection

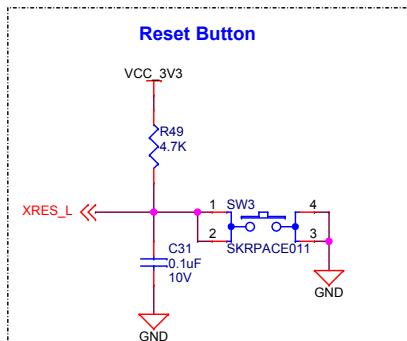


Block Diagram shows another UART header.
Where this need to get connected?

MUC UART HEADER



Reset Button



CYPRESS SEMICONDUCTOR © 2019

SCH Title : Cypress_DVT_Adapter_RP01

Page Title :Module RP01

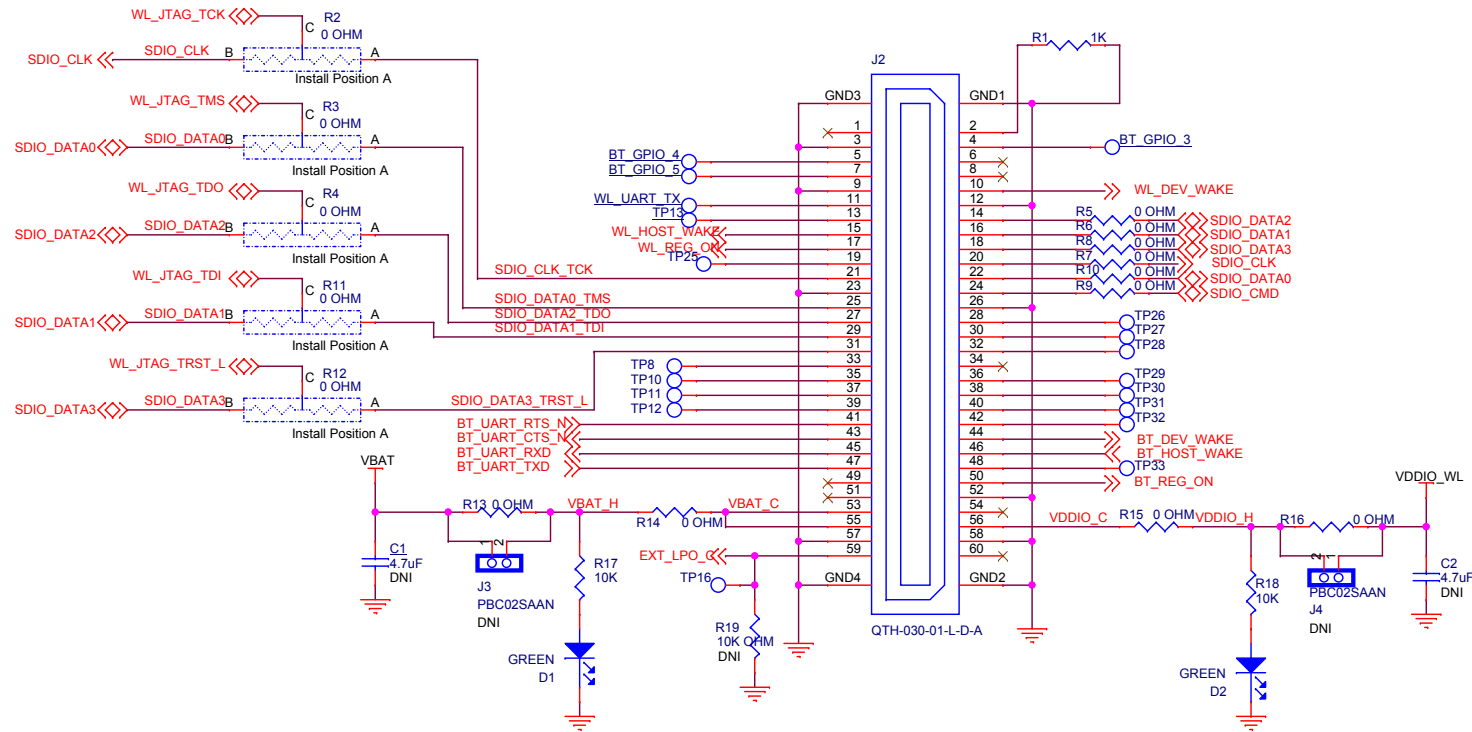
Size	Document Number	Drawn By	Approved By	Rev
B	630-ZET0007-01	SANJEEVI	<Approved>	0.1

Date: Friday, July 26, 2019

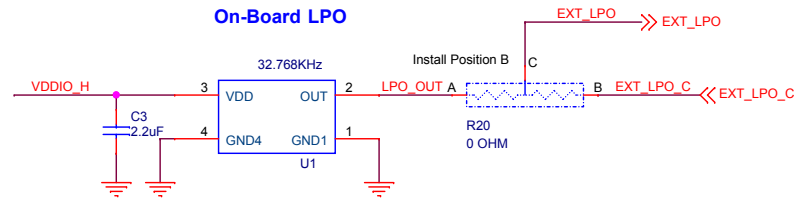
Sheet 4 of 7

60-Pin Connector (SDIO)

For JTAG:
Resistors R2, R3, R4, R11, R12:
For 43012: Install Position A
For 4343x: Install Position B (For JTAG over SDIO option)



On-Board LPO



CYPRESS SEMICONDUCTOR
198 CHAMPION COURT
SAN JOSE, CA 95134
(408) 943-2600

CYPRESS SEMICONDUCTOR © 2019

SCH Title : Cypress_DVT_Adapter_RP01

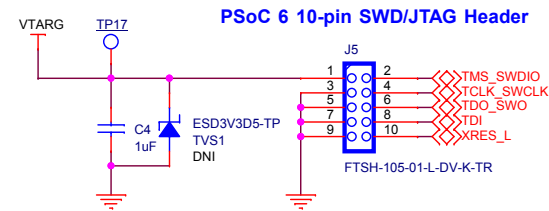
Page Title : 60-Pin Connector (SDIO)

Size	Document Number	Drawn By	Approved By	Rev
B	630-ZET0007-01	SANJEEVI	<Approved>	0.1

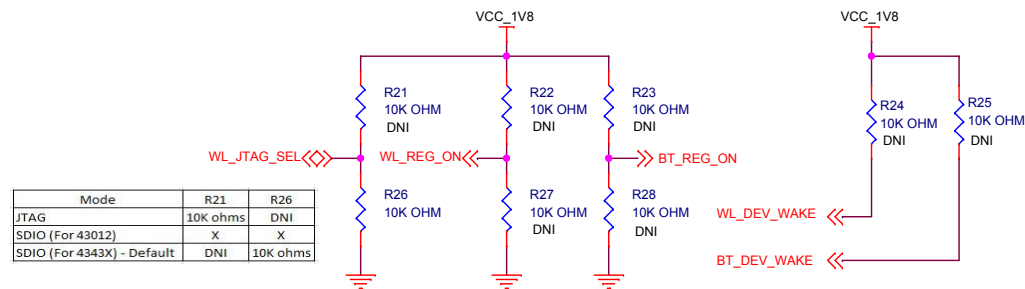
Date: Friday, July 26, 2019

Sheet 5 of 7

SWD/JTAG Header & Strapping Options



WLAN/BT Strapping Options



Mode	R21	R26
JTAG	10K ohms	DNI
SDIO (For 43012)	X	X
SDIO (For 4343X) - Default	DNI	10K ohms



CYPRESS SEMICONDUCTOR
 198 CHAMPION COURT
 SAN JOSE, CA 95134
 (408) 943-2600


CYPRESS SEMICONDUCTOR © 2019

SCH Title : Cypress_DVT_Adapter_RP01

Page Title :SWD/JTAG Header & Strapping Options

Size	Document Number	Drawn By	Approved By	Rev
B	630-ZET0007-01	SANJEEVI	<Approved>	0.1
Date:	Friday, July 26, 2019	Sheet	6 of 7	

REVISION HISTORY		
REV	DESCRIPTION OF CHANGE	DATE
0.1	Initial Release	26/07/2019



CYPRESS
EMBEDDED IN TOMORROW™

CYPRESS SEMICONDUCTOR
198 CHAMPION COURT
SAN JOSE, CA 95134
(408) 943-2600

CYPRESS SEMICONDUCTOR © 2019

SCH Title : Cypress_DVT_Adapter_RP01

Page Title :Revision History

Size B	Document Number 630-ZET0007-01	Drawn By SANJEEVI	Approved By <Approved>	Rev 0.1
Date:	Friday, July 26, 2019	Sheet	7	of 7