國立清華大學

Analog Circuit Design

國立清華大學
NATIONAL TSING HUA UNIVERSITY

Homework 4

Two-Stage OPA

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目錄

(a) Operation point

1. Please DESIGN your bias (Mb1- Mb3) and amplifier (M1 – M5) size to make the gain at DC larger than 60dB.

表格 **1 MOS size**

	W/L(μm/μm)	**m**
Mb1(pmos)	20/0.18	1
Mb2(pmos)	10/0.18	1
Mb3(pmos)	10/0.18	1
M1(pmos)	10/0.4	1
M2(pmos)	10/0.4	1
M3(nmos)	10/0.8	1
M4(nmos)	10/0.8	1
M5(nmos)	27.5/0.4	1

2. Print out the results from .op command. And make sure all the devices are properly biased.

**** mosfets

subckt								
element	0:mb1	0:mb2	0:mb3	0:m3	0:m4	0:mm1	0:mm2	0:m5
model	0:p_18.1	0:p_18.1	0:p_18.1	0:n_18.1	0:n_18.1	0:p_18.1	0:p_18.1	0:n_18.1
region	Saturation	Saturation	Saturation	Saturation	Saturation	Saturation	Saturation	Saturation
id	-100.0000u	-31.4780u	-44.2051u	15.7390u	15.7390u	-15.7390u	-15.7390u	44.2051u
ibs	9.559e-21	3.153e-21	4.427e-21	-2.547e-21	-2.547e-21	1.576e-21	1.576e-21	-6.707e-21
ibd	544.5851a	65.7418a	305.8655a	-365.1456a	-365.1456a	430.5029a	430.5029a	-1.8924f
vgs	-592.5381m	-592.5381m	-592.5381m	469.3420m	469.3420m	-613.4546m	-613.4546m	469.3420m
vds	-592.5381m	-136.5454m	-635.2596m	469.3420m	469.3420m	-894.1125m	-894.1125m	864.7404m
vbs	0.	0.	0.	0.	0.	0.	0.	0.
vth	-511.8655m	-524.0868m	-520.7778m	402.6254m	402.6254m	-508.7514m	-508.7514m	456.8274m
vdsat	-143.6360m	-135.0348m	-137.4774m	98.8056m	98.8056m	-137.3087m	-137.3087m	78.7924m
vod	-80.6726m	-68.4513m	-71.7603m	66.7166m	66.7166m	-104.7032m	-104.7032m	12.5147m
beta	12.9675m	6.3669m	6.3733m	3.9300m	3.9300m	1.8956m	1.8956m	24.7437m
gam eff	557.0846m	557.0846m	557.0846m	507.4460m	507.4460m	557.0846m	557.0846m	507.4460m
gm	1.3390m	421.3208u	615.5177u	257.1132u	257.1132u	204.1590u	204.1590u	875.2120u
gds	43.0482u	69.5846u	18.4967u	3.3270u	3.3270u	1.6168u	1.6168u	14.7371u
gmb	394.5544u	124.1025u	179.9585u	52.3678u	52.3678u	60.2327u	60.2327u	162.8779u
cdtot	23.2689f	13.5122f	11.6118f	13.9282f	13.9282f	11.1135f	11.1135f	38.6263f
cgtot	36.2227f	18.0572f	17.9060f	53.1474f	53.1474f	27.8915f	27.8915f	71.6704f
cstot	50.6197f	24.8541f	25.0556f	60.4859f	60.4859f	35.4176f	35.4176f	88.5196f
cbtot	44.2775f	23.6867f	22.1920f	34.5609f	34.5609f	24.5192f	24.5192f	80.1173f
cgs	26.2682f	12.8747f	12.8501f	44.6522f	44.6522f	22.3486f	22.3486f	49.2129f
cgd	7.0826f	3.7395f	3.5420f	3.6010f	3.6010f	3.5887f	3.5887f	11.1682f

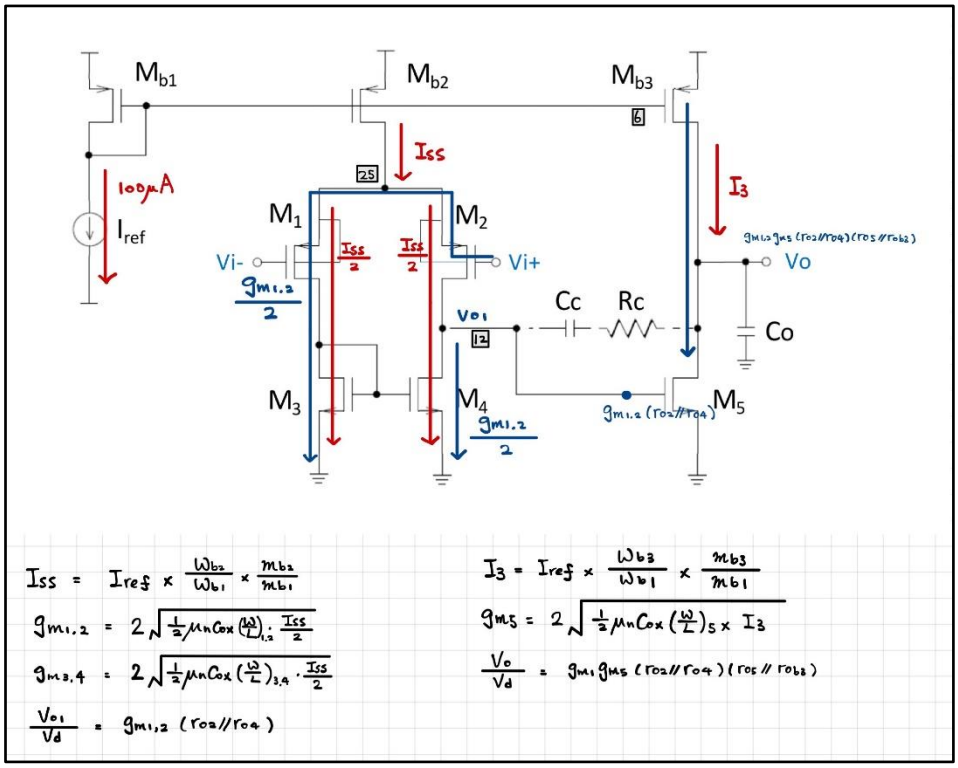
圖 1 lis file result(.op)

3. Use .tf command to print out the voltage gain.

```
****     small-signal transfer characteristics

     v(vout)/vac                                =     1.0787k
     input resistance at              vac       =   1.000e+20
     output resistance at v(vout)               =    30.0937k
```

圖 2 lis file result(.tf)

4. Verify your DC gain with hand calculation.



根據上頁.op result，可得:

ro2=618.506K ; ro4=300.571K ;

ro5=67.856K ; rob3=54.064K

$$\frac{Vo}{Vac} = gm1gm5(ro2 \parallel ro4)(ro5 \parallel rob3)$$

$$= 204.159\mu \times 875.212\mu \times 202.273K \times 30.09K$$

$$= 1.0875K\ V/V$$

誤差值$=\frac{1.0875-1.0787}{1.0787} = 0.816\%$

(b) AC response before compensation

1. Please simulate and plot the frequency response (magnitude and phase) of your design in (a). Mark the (i) DC gain (ii) unity gain frequency, and (iii) phase margin on figure.

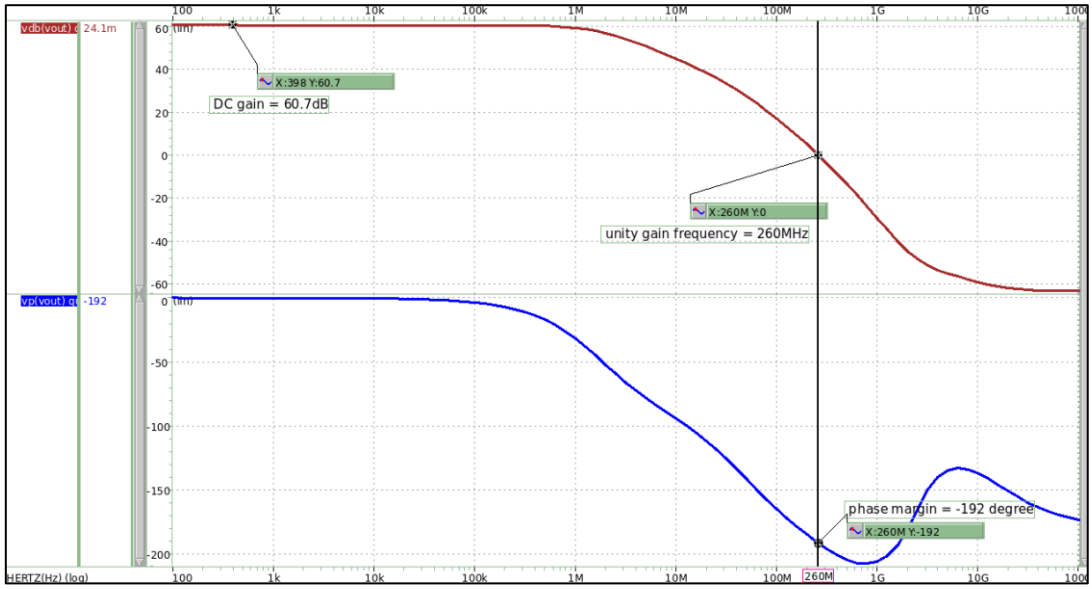


圖 3 frequency response

```
****** ac analysis tnom=  25.000 temp=  25.000 ******
phase=-191.6099
phase_margin= -11.6099
gmax=  60.6578
bw=   1.7072x
unit_gain_frequency= 261.2712x
```

DC gain=60.7dB ;

unity gain frequency=261.27MHz ;

Phase margin=-12 degree

2. Use .pz to identify the poles and zeros, and mark them on bode plot.

```
******   pole/zero analysis


  input =  0:vac          output = v(vout)

     poles (rad/sec)                poles ( hertz)
real            imag            real            imag
-10.7673x       0.              -1.71366x       0.
-275.740x       0.              -43.8854x       0.
-2.40375g       0.              -382.569x       0.
-5.63484g       0.              -896.812x       0.
-17.5327g       0.              -2.79042g       0.

     zeros (rad/sec)                zeros ( hertz)
real            imag            real            imag
-4.37480g       0.              -696.272x       0.
-9.39933g       11.9207g        -1.49595g       1.89724g
-9.39933g       -11.9207g       -1.49595g       -1.89724g
-13.1761g       0.              -2.09704g       0.
84.7344g        0.              13.4859g        0.
```

圖 4 .pz result

First pole	Second pole	Zero
1.714MHz	43.89MHz	13.485GHz

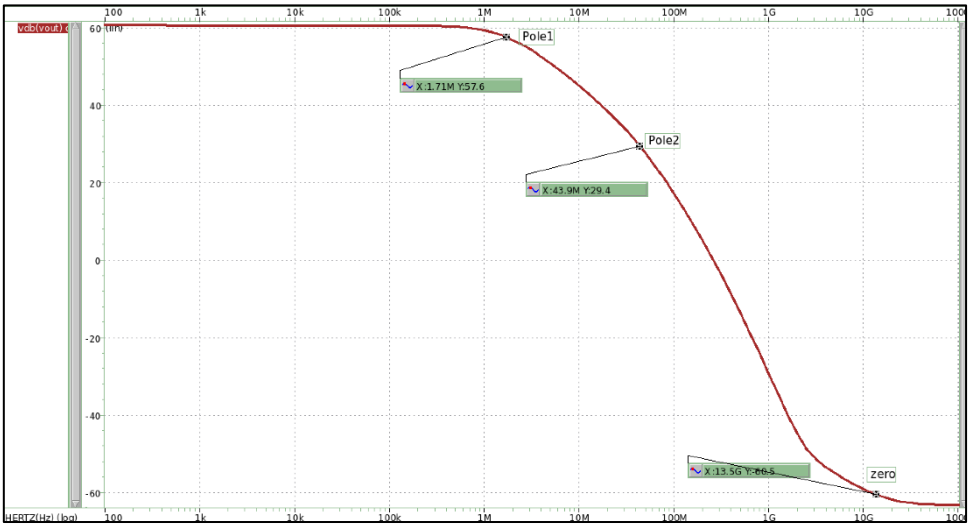
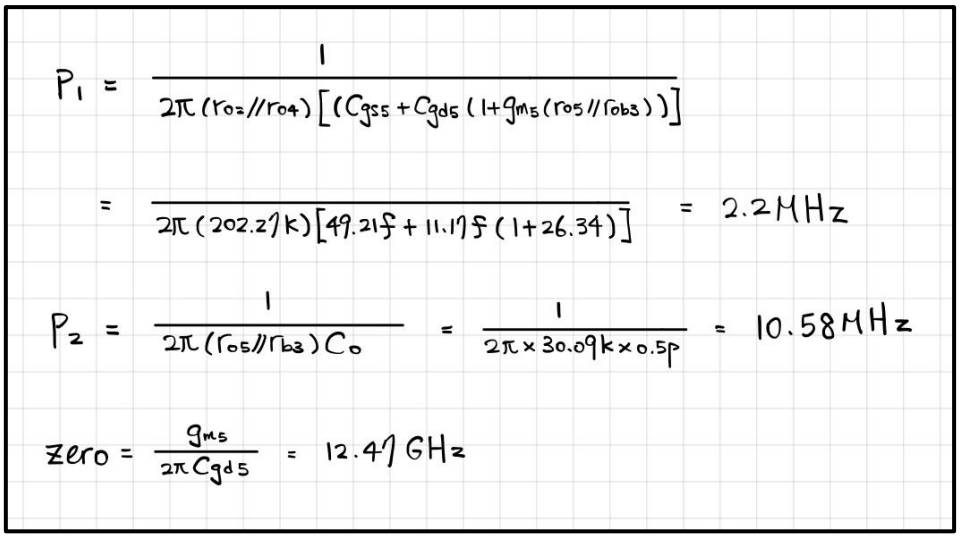


圖 5 bode plot

3. Verify the first and second dominant poles and first RHP zeros with hand calculation.



	Simulation	Hand Calculate	誤差值
Pole1	1.7MHz	2.2MHz	29%
Pole2	43.9MHz	10.58MHz	76%
zero	13.49GHz	12.47GHz	7.5%

(c) AC response after Cc compensation

1. Please design your value of Cc and simulate the AC response in (b). (please note, your Cc must be smaller than 10pF, and the phase margin must larger than 0 in this case).

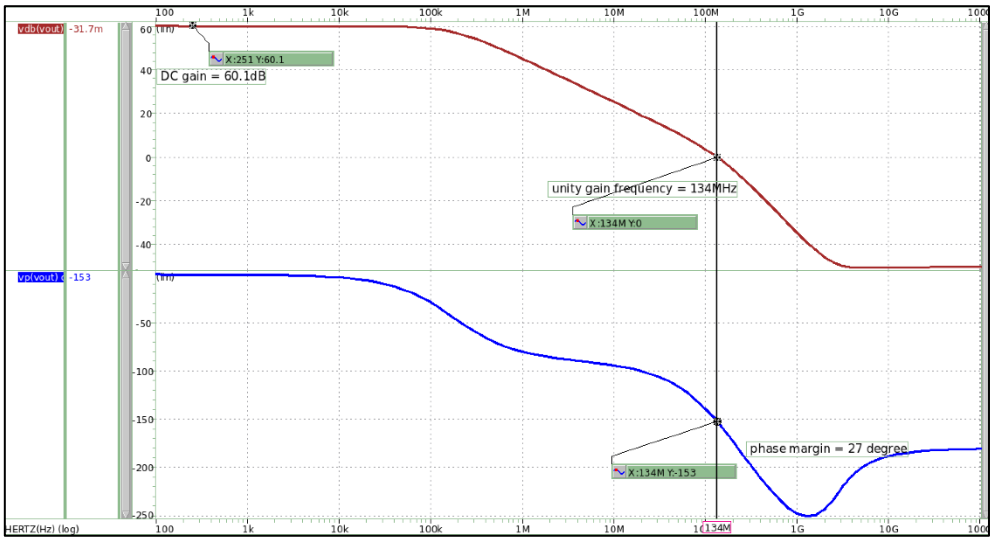


圖 6 frequency response

```
****** ac analysis tnom=  25.000 temp=  25.000 ******
phase=-152.4286
phase_margin=  27.5714
gmax=  60.1145
bw= 181.7721k
unit_gain_frequency= 134.3915x
```

Design Cc=0.15pf, phase margin=27.57° →meet the requirement

2. Please print .pz output of the new poles (first and second dominant) and zeros (first RHP), and mark them on bode plot.

```
  ******   pole/zero analysis


   input =  0:vac          output = v(vout)

      poles (rad/sec)                 poles ( hertz)
real            imag            real            imag
-1.14491x       0.              -182.217k       0.
-970.035x       0.              -154.386x       0.
-2.34178g       0.              -372.706x       0.
-5.76619g       0.              -917.717x       0.
-17.5381g       0.              -2.79127g       0.

      zeros (rad/sec)                 zeros ( hertz)
real            imag            real            imag
-4.36085g       0.              -694.052x       0.
5.30708g        0.              844.648x        0.
-10.9830g       12.5556g        -1.74799g       1.99828g
-10.9830g       -12.5556g       -1.74799g       -1.99828g
-13.6191g       0.              -2.16755g       0.
```

First pole	Second pole	Zero1
182.217kHz	154.386MHz	844.65MHz

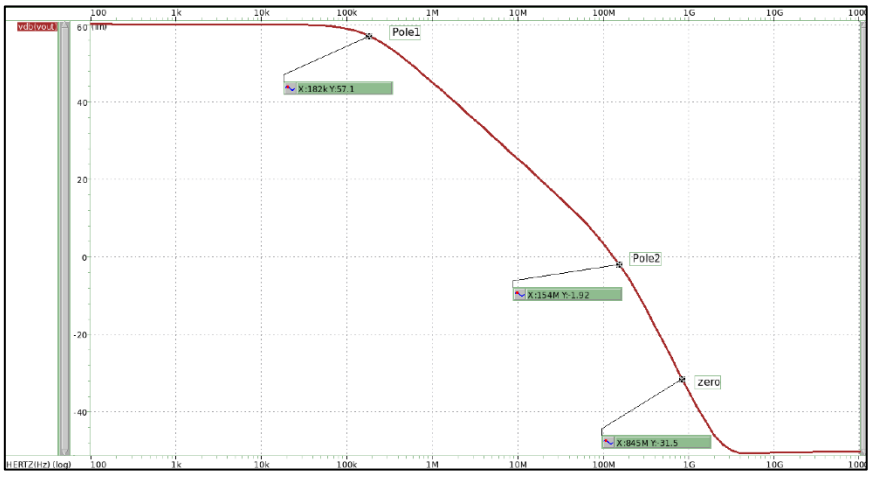
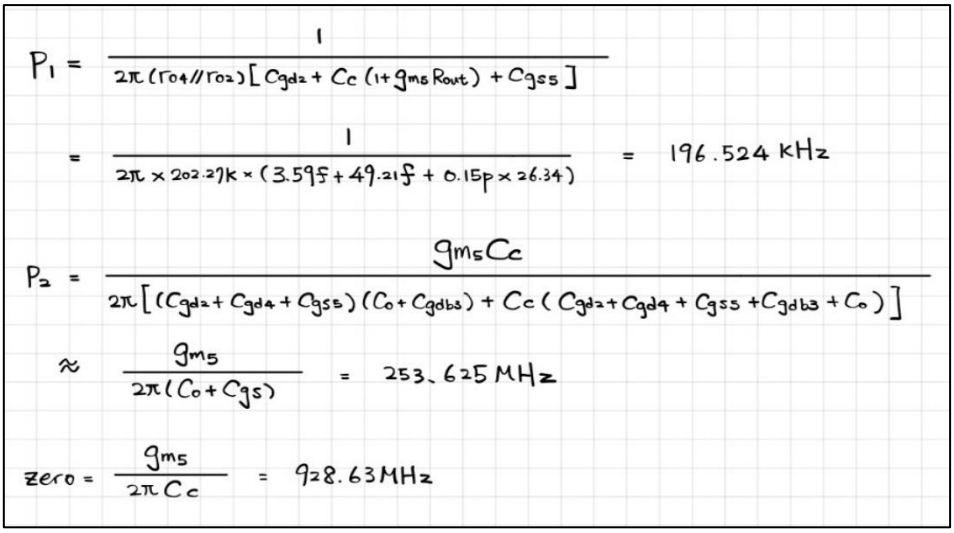


圖 7 bode plot

3. Verify the compensation with hand calculation.



	Simulation	Hand Calculate	誤差值
Pole1	182.217KHz	196.254KHz	7.7%
Pole2	154.386MHz	253.625MHz	64.3%
zero	844.65MHz	928.63MHz	10%

(d) AC response after Cc-Rc compensation

1. Please design your value of Rc to shift the RHP zero and simulate the AC response in (c). (please note, your unity gain frequency must be larger than 50MHz and phase margin must larger than 45 in this case).

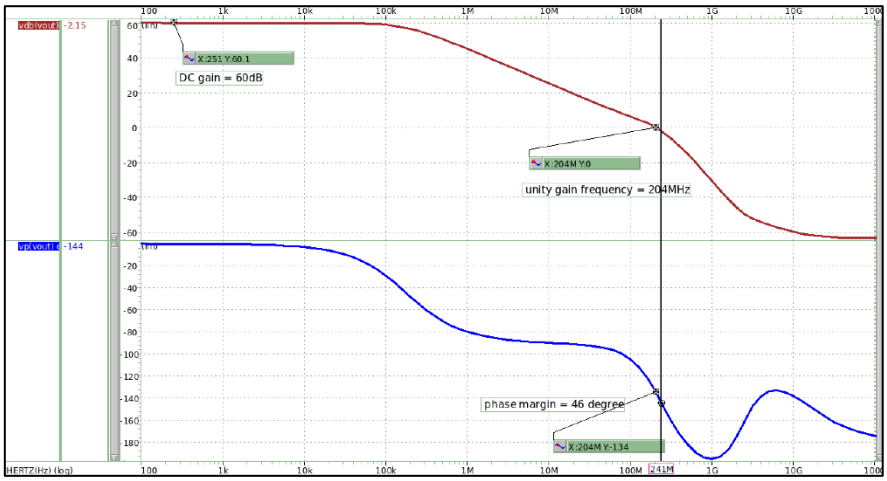


圖 8 frequency response

```
****** ac analysis tnom=  25.000 temp=  25.000 ******
phase=-134.3518
phase_margin=  45.6482
gmax=  60.1145
bw= 181.5066k
unit_gain_frequency= 204.5289x
```

Cc=0.15pf and Rc=9.5K, unit gain frequency=204.53MHz ;

phase margin=45.65° →meet the requirement

2. Please print .pz output of the new poles and zeros, and mark them on bode plot as (c).

```
******   pole/zero analysis


   input =  0:vac          output = v(vout)

      poles (rad/sec)                 poles ( hertz)
real             imag             real             imag
-1.14322x        0.               -181.950k        0.
-1.12921g        785.509x         -179.719x        125.018x
-1.12921g        -785.509x        -179.719x        -125.018x
-2.51954g        0.               -400.998x        0.
-5.54682g        0.               -882.804x        0.
-17.5336g        0.               -2.79056g        0.

      zeros (rad/sec)                 zeros ( hertz)
real             imag             real             imag
120.704k         0.               19.2106k         0.
-123.456k        0.               -19.6486k        0.
1.76212g         0.               280.451x         0.
```

First pole	Second pole	Zero
181.95kHz	401MHz	280.45MHz

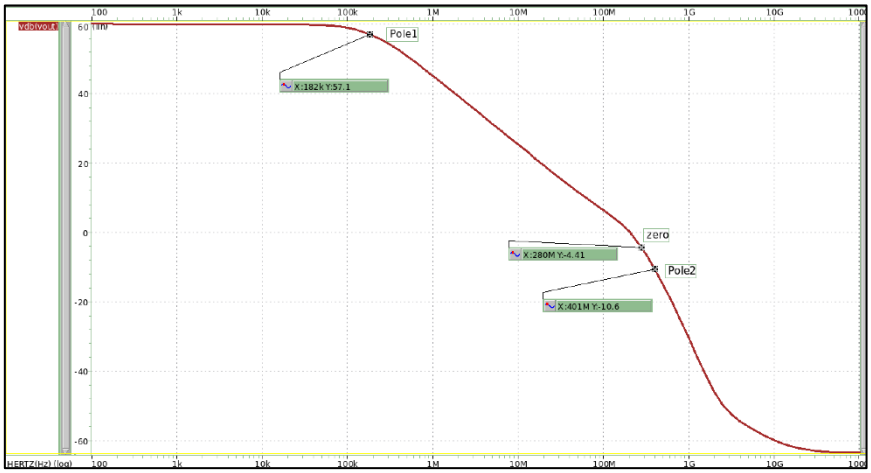
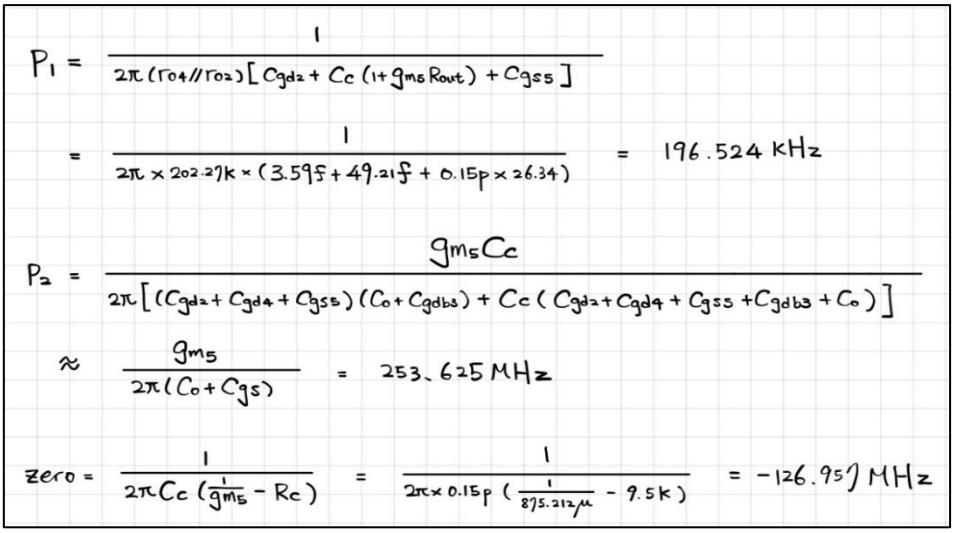


圖 9 bode plot

3. Verify the compensation with hand calculation.



	Simulation	Hand Calculate	誤差值
Pole1	182.217KHz	196.254KHz	7.7%
Pole2	401MHz	253.625MHz	36.75%
zero	280.45MHz	126.957MHz	54.73%

(e) Closed-loop transfer function

1. Please simulation the closed-loop DC transfer curve when input from 0 to 1.5V, and plot the closed-loop gain and mark the slope.

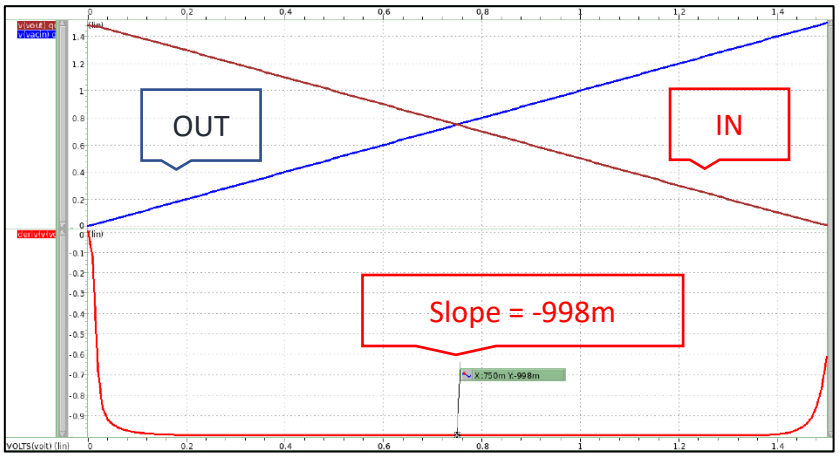


圖 10 DC transfer curve

2. Print .tf output to discuss the gain and input/output impedance.

```
****     small-signal transfer characteristics

    v(vout)/vacin                                = -997.6507m
    input resistance at              vacin       =  100.1176k
    output resistance at v(vout)                 =   54.4978
```

3. Please calculate the closed-loop DC gain with the real op-amp gain in your design.

$$V_o = \left(V_i \times \frac{R_f}{R_i + R_f} + V_o \times \frac{R_i}{R_i + R_f}\right) \times (-A_o)$$

$$\Rightarrow V_o = \left(\frac{V_i}{2} + \frac{V_o}{2}\right) \times 1078.1$$

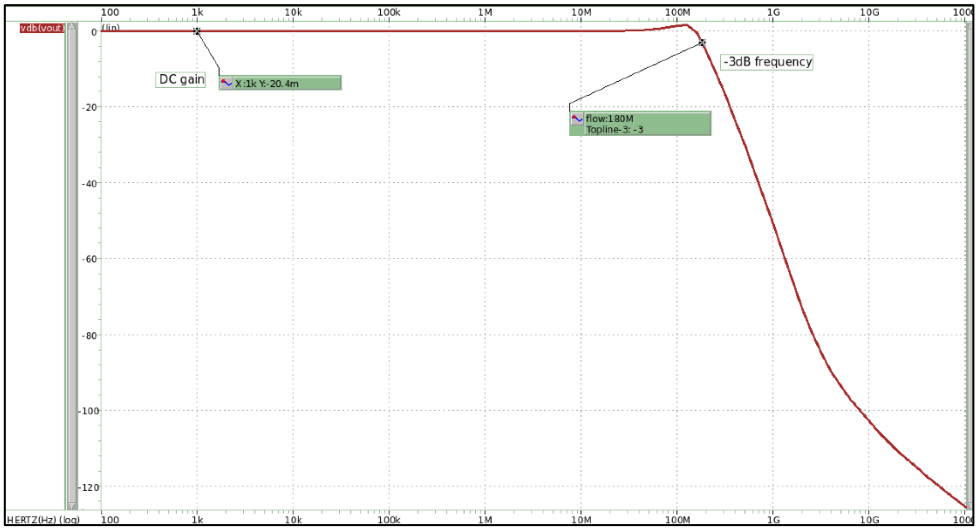
$$\Rightarrow 539.35\, V_i = -538.35\, V_o$$

$$\Rightarrow \frac{V_o}{V_i} = -0.9981$$

Simulation	Hand Calculate	誤差值
-0.9977	-0.9981	0.05%

(f) Closed-loop AC response

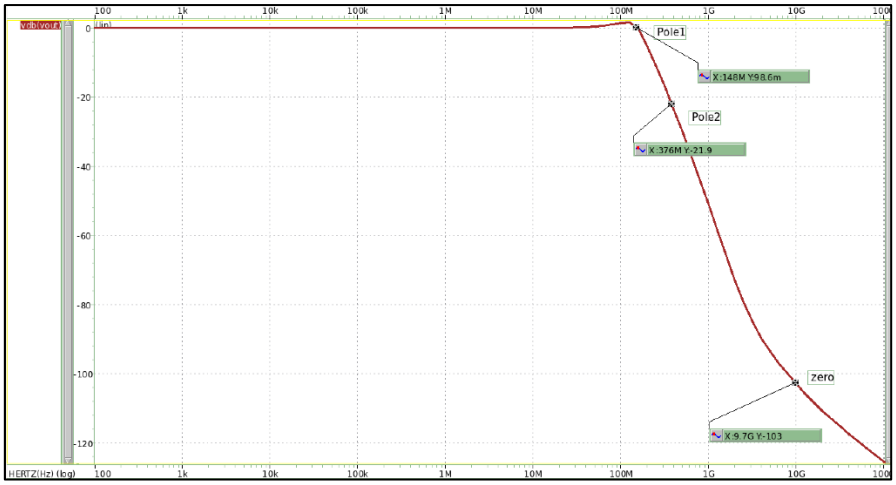
1. Please simulation the closed-loop AC response. Draw the bode plot and mark its DC gain and-3dB frequency.



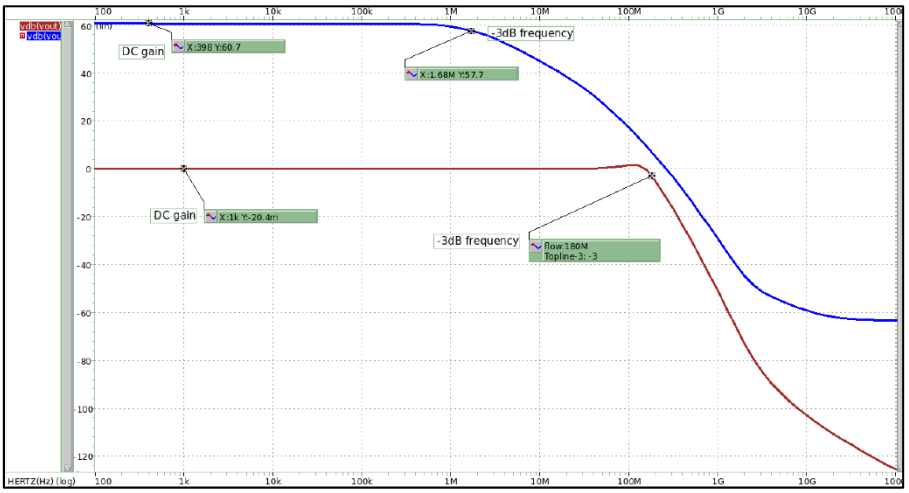
DC gain = -20.4mdB ; -3db frequency = 180MHz

```
******   pole/zero analysis

  input =  0:vacin          output = v(vout)

     poles (rad/sec)                poles ( hertz)
real             imag          real             imag
-356.552x        858.783x      -56.7471x        136.680x
-356.552x        -858.783x     -56.7471x        -136.680x
-681.861x        0.            -108.522x        0.
-2.25902g        699.509x      -359.534x        111.330x
-2.25902g        -699.509x     -359.534x        -111.330x
-4.90037g        0.            -779.918x        0.
-17.6823g        0.            -2.81423g        0.

     zeros (rad/sec)                zeros ( hertz)
real             imag          real             imag
-798.275x        0.            -127.049x        0.
-4.36580g        0.            -694.839x        0.
-11.9162g        13.8639g      -1.89652g        2.20651g
-11.9162g        -13.8639g     -1.89652g        -2.20651g
-12.1972g        0.            -1.94124g        0.
61.2050g         0.            9.74108g         0.
```

First pole	Second pole	Zero
148MHz	376MHz	9.7GHz



2. Put this bode plot with open-loop response and compare the results.



	DC gain	-3DB frequency
Closed loop	-20.4mdB	180MHZ
Open loop	60.7dB	1.68MHz

(g) Closed-loop linearity response

1. Please simulation the closed-loop THD when input with 0.7Vpp 10kHz sinusoidal waveform. (THD has to be smaller than-60dB).

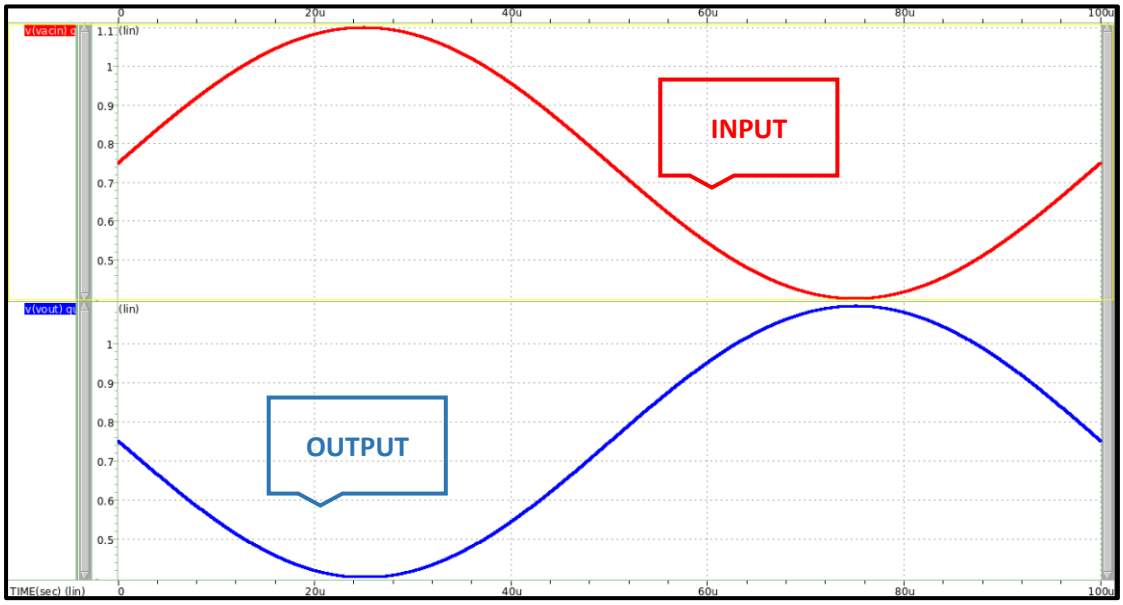
harmonic no	frequency (hz)	fourier component	normalized component	phase (deg)	normalized phase (deg)
1	10.0000k	349.1586m	1.0000	89.9937	0.
2	20.0000k	26.7238u	76.5378u	497.4838m	-89.4963
3	30.0000k	6.7526u	19.3397u	91.8743	1.8805
4	40.0000k	520.6543n	1.4912u	-179.4715	-269.4653
5	50.0000k	283.6153n	812.2822n	-121.6149	-211.6087
6	60.0000k	147.6689n	422.9279n	179.9770	89.9832
7	70.0000k	153.1823n	438.7182n	175.6610	85.6673
8	80.0000k	152.6075n	437.0721n	179.9997	90.0060
9	90.0000k	152.4715n	436.6827n	-179.7252	-269.7189

total harmonic distortion = 0.00789664 percent

圖 11 THD result

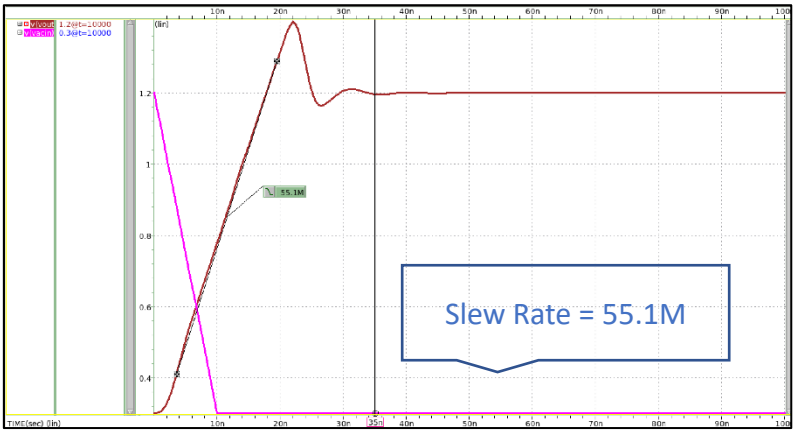
THD = -83.1dB

2. Please plot the input and output waveforms.

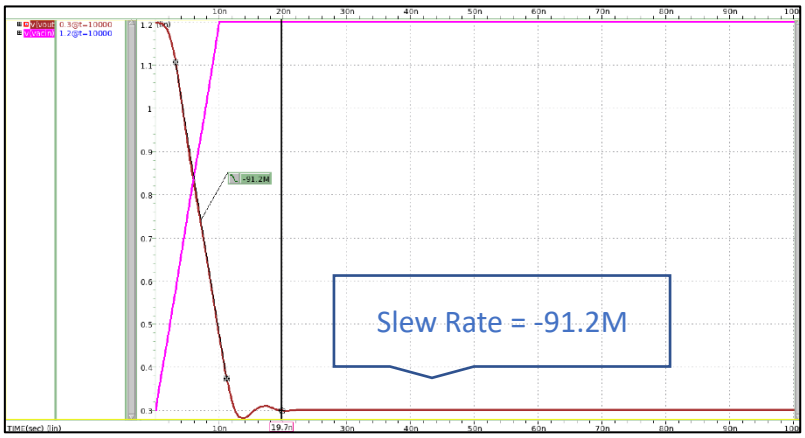


(h) Closed-loop step response

1. Please plot the output waveform when input with a step- from 0.3V to 1.2V, and a step+ from 1.2V to 0.3V, with rise/fall time of 10ns.
2. Please mark slew rate (slope between 10%- 90% of final value), and the settling time (to within 10mV error) on your step+ and step- responses.



$$\frac{I_{ss}}{Cc} = \frac{31.478\mu}{0.15p} = 209.85M$$



$$-\frac{\min(I5, I_{b2})}{Cc} = \frac{-31.48\mu}{0.5p} = -62.96M$$

3. Compare slew rate simulation results with hand calculation.

	Simulation	Hand Calculate	誤差值	settle time
$SR^+ (\frac{V}{\mu s})$	55.1M	209.85M	280.85%	35ns
$SR^- (\frac{V}{\mu s})$	-91.2M	-62.96M	30.96%	19.7ns

(i) Closed-loop transfer function with diff R

1. Print .tf output to discuss the gain and input/output impedance

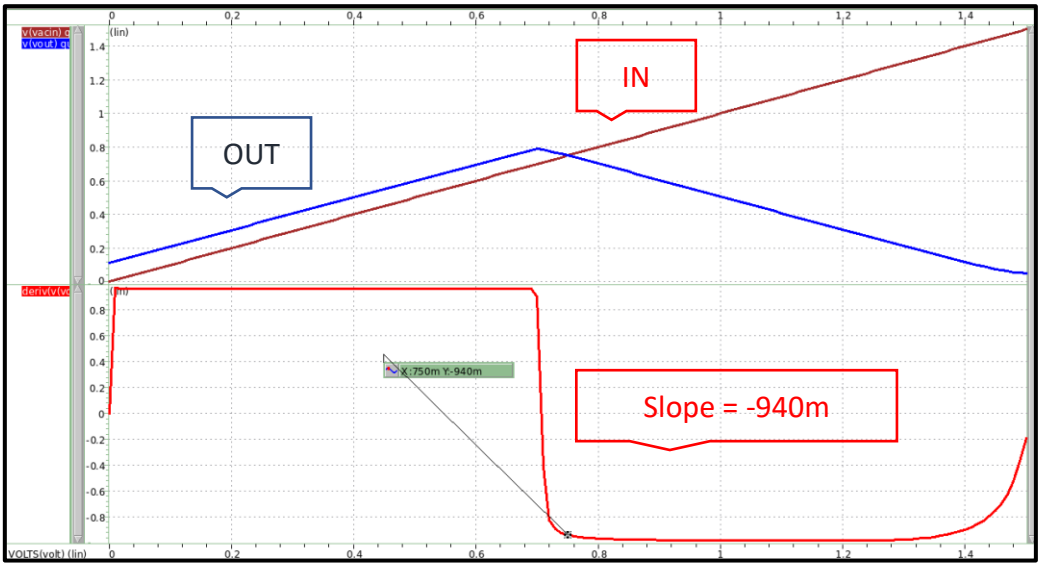


圖 12 transfer curve

2. Please discuss the difference.

Ri、Rf 為 1k 時，Vout transfer curve 與 Ri、Rf 為 100k 時不同，在 Vin=0-0.75 間，無法上升到 VDD。

推測是因放大器回授增益因 Ri、Rf 電阻降低而降低，表現較不理想。

回授增益 A_f = Ao/1+Ao β ，而其中 β =1/Rf，若 Rf 不夠大，將導致 A_f =1/ β ，會變成與 open loop 無關，直接由 β 決定電路回授增益。

(j) Discussion

1. **Please fill the following table. and discuss your design for frequency compensation and for best FoM.**

V_{DD}	1.5V	
I_{DD} (total current exclude of I_{mb1}) *1	75.683 μA	
I_{mb2},I_{mb3}	31.478 μA	44.205 μA
Rc, Cc(<10pF)	9.5K	0.15pF
Open-loop performance(after final compensation)		
DC gain(>60dB)	60.1dB	
Unity gain frequency *2	204.53MHz	
Phase margin	45.65	
Closed-loop performance(after final compensation)		
T.H.D	-83.1dB	
S.R.+ *3	55.1 V/ μS	
S.R.- *4	-91.2V/ μS	
Settling time	35ns	
Figure of merit(after final compensation)		
*2/*1	2.7	
*3/*1	0.73	
*4/*1	1.21	

這次主要分為 slew rate、unity gain frequency、IDD 三者關係去調便 FOM。
調大 slew rate 方法為小 Cc 和大電流，Cc 小有助於 slew rate 的表現，但會使得 phase margin 表現變差，較容易使電路不穩定。而大電流就要看到底是 slew rate 成長幅度較大還是電流下降程度較多。

至於 Rc 的功能，是用於使零點頻率更大，zero = $\frac{1}{Cc(\frac{1}{gm}-Rc)}$，Rc 越大，便可使 zero 落在左半平面，phase margin 會更穩定;反之若 zero 落在右半平面，會使電路不穩定，輸出將有可能發散。
實際測試幾組下來，發現此次作業的電流太小，弊大於利。固本次作業在做取捨時選擇捨棄電流，採取大電流大頻寬大 slew rate 的設計方向設計。