

國立清華大學

Analog Circuit Design



國立清華大學

NATIONAL TSING HUA UNIVERSITY

Homework 5

Common Mode Feedback

學號:111063548

姓名:蕭方凱

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Operation point for CKT B

- (a) Please design your amplifier M1, M2, M3, M4, RF, and input common mode level to achieve differential mode DC gain of 35(V/V), common mode DC gain smaller than 0.05 (V/V), and the output common mode level of 1.0V.

	W/L(μm/μm)	m
M1	15/0.5	1
M2	15/0.5	1
M3	40/1.2	5
M4	40/1.2	5
MS	4.7/1	2
RF	305K	
Common model level	0.78V	

電壓大小設計：

在設計時，我先決定好 V_X 電壓，為使 MS 操作在飽和區，電壓不可小於 **0.52**，否則 **MS** 將截止；至於 V_X 最大值的設計，因 V_X 越大，MOS size 就要越小，以滿足 $\text{tail current} = 30\mu\text{A}$ 的條件，若 mos size 太小將影響到其他 mos 可調整的彈性，故在設計 V_X 值時，我並沒有設計太大，約落在 0.53 到 0.6 之間去做設計調整。

決定好 V_X 後，接著是調整 MS size 使 $\text{tail current} = 30\mu\text{A}$ ，便可開始決定 common mode level，其值不可小於 MS 的 **drain voltage + V_{t1}** ，否則 M1、M2 將截止，同時也不可太大，太大的話將導致 M1、M2 進入線性區。

Gain 調變：

需同時考慮 differential mode 和 common mode，兩個 gain 公式分別如下：

$$A_d = g_{m1}(r_{o1} // r_{o3} // R_F)$$

$$A_{cm} = \frac{r_{o1}(1 - M) // 2r_{os}}{\frac{1}{g_{m1}} + [r_{o1}(1 - M) // 2r_{os}]} \times \frac{1}{\frac{g_{m3}}{2r_{os}}}$$

g_{m1} 越大，可使 A_d 變大， A_{cm} 變小。而 r_{o1} 越小對 A_{cm} 越好，但會使 A_d 變小，且因電流固定故調整空間不大，在設計時，先滿足使 $A_{cm} < 50\text{m(V/V)}$ ，再調變 R_F 使 $A_d = 35\text{(V/V)}$ ，會較有效率。

- (b) Print out the small signal parameters using .op command.

```
**** mosfets

subckt
element 0:mm1      0:mm2      0:mms      0:mm3      0:mm4
model    0:n_18.1  0:n_18.1  0:n_18.1  0:p_18.1  0:p_18.1
region   Saturation Saturation Saturation Saturation Saturation
id       15.2825u   15.2825u   30.5650u  -15.2825u  -15.2825u
ibs      -317.5867a -317.5867a -5.468e-21 1.426e-21  1.426e-21
ibd      -1.1357f   -1.1357f   -227.0980a 4.4451f    4.4451f
vgs      499.1011m  499.1011m  530.0000m -495.4698m -495.4698m
vds      723.6313m  723.6313m  280.8989m -495.4698m -495.4698m
vbs      -280.8989m -280.8989m 0.         0.         0.
vth      490.0938m  490.0938m  389.9428m -491.9445m -491.9445m
vdsat    75.6823m   75.6823m   144.3693m -67.1407m  -67.1407m
vod       9.0073m   9.0073m   140.0572m -3.5253m   -3.5253m
beta      9.7579m   9.7579m    2.9264m   12.2982m   12.2982m
gam_eff   514.7790m  514.7790m  507.4461m  557.0847m  557.0847m
gm        312.8165u  312.8165u  347.9333u  306.8623u  306.8623u
gds       4.7862u    4.7862u    7.2409u   849.9654n  849.9654n
gmb       49.7346u   49.7346u   70.1168u   92.8660u   92.8660u
cdtot     18.9741f   18.9741f   14.3627f   236.6894f   236.6894f
cgtot     40.7648f   40.7648f   64.9068f   1.0902p    1.0902p
cstot     46.2977f   46.2977f   72.5653f   1.0853p    1.0853p
cbtot     39.0047f   39.0047f   36.4631f   814.4105f   814.4105f
cgs       28.6368f   28.6368f   56.5248f   760.8266f   760.8266f
cgd       5.5571f    5.5571f    3.5656f    71.8642f    71.8642f
```

Tail current=30 μ A ➡ meet the requirement

- (c) Please use .tf command to simulate the differential and common mode gain, and print out the results.

```
****      small-signal transfer characteristics

v(out1,out2)/vac      = -35.0886
input resistance at   vac      = 1.000e+20
output resistance at v(out1,out2) = 224.3517k
```

圖 1 differential mode gain

Gain = 35.088(V/V)

```
****      small-signal transfer characteristics

v(out2)/vac      = -9.9192m
input resistance at   vac      = 1.000e+20
output resistance at v(out2) = 57.7126k
```

圖 2 common mode gain

Gain = 9.92m (V/V)

- (d) Please calculate the differential mode and common mode gains with the small-signal model.

```
**** mosfets

subckt
element 0:mm1      0:mm2      0:mms      0:mm3      0:mm4
model    0:n_18.1  0:n_18.1  0:n_18.1  0:p_18.1  0:p_18.1
region   Saturation Saturation Saturation Saturation Saturation
id       15.2825u  15.2825u  30.5650u  -15.2825u  -15.2825u
ibs      -317.5867a -317.5867a -5.468e-21 1.426e-21 1.426e-21
ibd      -1.1357f  -1.1357f  -227.0980a 4.4451f 4.4451f
vgs      499.1011m 499.1011m 530.0000m -495.4698m -495.4698m
vds      723.6313m 723.6313m 280.8989m -495.4698m -495.4698m
vbs      -280.8989m -280.8989m 0. 0. 0.
vth      490.0938m 490.0938m 389.9428m -491.9445m -491.9445m
vdsat    75.6823m 75.6823m 144.3693m -67.1407m -67.1407m
vod       9.0073m 9.0073m 140.0572m -3.5253m -3.5253m
beta     9.7579m 9.7579m 2.9264m 12.2982m 12.2982m
gam_eff  514.7790m 514.7790m 507.4461m 557.0847m 557.0847m
gm       312.8165u 312.8165u 347.9333u 306.8623u 306.8623u
gds      4.7862u 4.7862u 7.2409u 849.9654n 849.9654n
gmb      49.7346u 49.7346u 70.1168u 92.8660u 92.8660u
cdtot    18.9741f 18.9741f 14.3627f 236.6894f 236.6894f
cgtot    40.7648f 40.7648f 64.9068f 1.0902p 1.0902p
cstot    46.2977f 46.2977f 72.5653f 1.0853p 1.0853p
cbtot    39.0047f 39.0047f 36.4631f 814.4105f 814.4105f
cgs      28.6368f 28.6368f 56.5248f 760.8266f 760.8266f
cgd      5.5571f 5.5571f 3.5656f 71.8642f 71.8642f
```

$$ro1 = ro2 = 208.934K$$

$$ro3 = ro4 = 1176.518K$$

$$ros = 138.104K$$

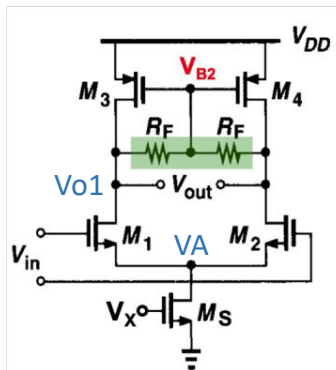
$$gm1 = gm2 = 312.8165\mu$$

$$gm3 = gm4 = 306.8623\mu$$

Differential gain:

$$\begin{aligned} A_d &= -gm_1(ro_1//ro_3//R_F) \\ &= -312.8165\mu \times (208.934K^{-1} + 1176.518K^{-1} + 305K^{-1}) \\ &= -312.8165\mu \times 112.172K \\ &= -35.0893\left(\frac{V}{V}\right) \end{aligned}$$

Common gain:



$$\begin{aligned} M &= \frac{Vo1}{VA} = -\frac{\frac{1}{gm3}}{2ros} = -0.0118 \\ A_{CM} &= \frac{\frac{ro1}{(1-M) // 2ros}}{\frac{1}{gm1} + [\frac{ro1}{(1-M) // 2ros]}} \times M \\ &= \frac{118.185K}{3.197K + 118.185K} \times (-0.0118) \\ &= -0.0115 \end{aligned}$$

	Simulation	Hand calculates	Error
Differential gain	35.0886	35.0893	0.00002%
Common gain	0.0099	0.0115	16.16%

Operation point for CKT A

- (e) Based on the design in (a), please design the bias voltage VB1 to achieve the output common mode level of 1.0V.

VB1 Design:

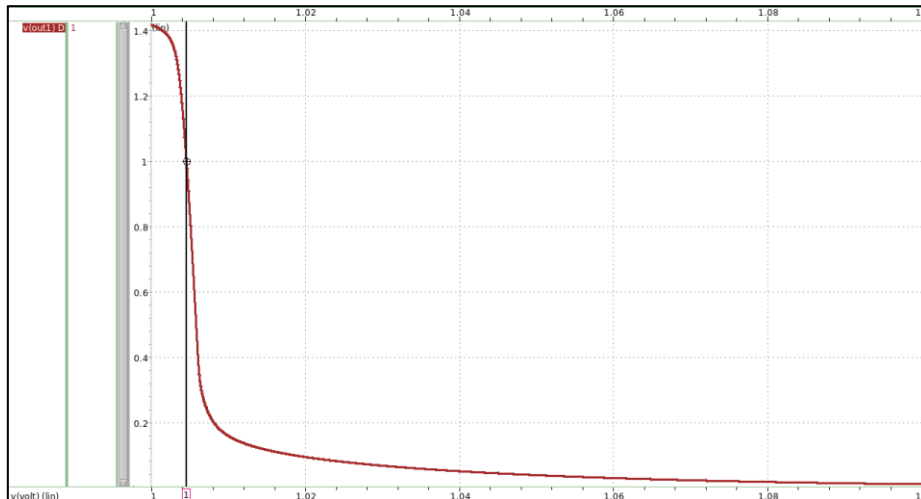
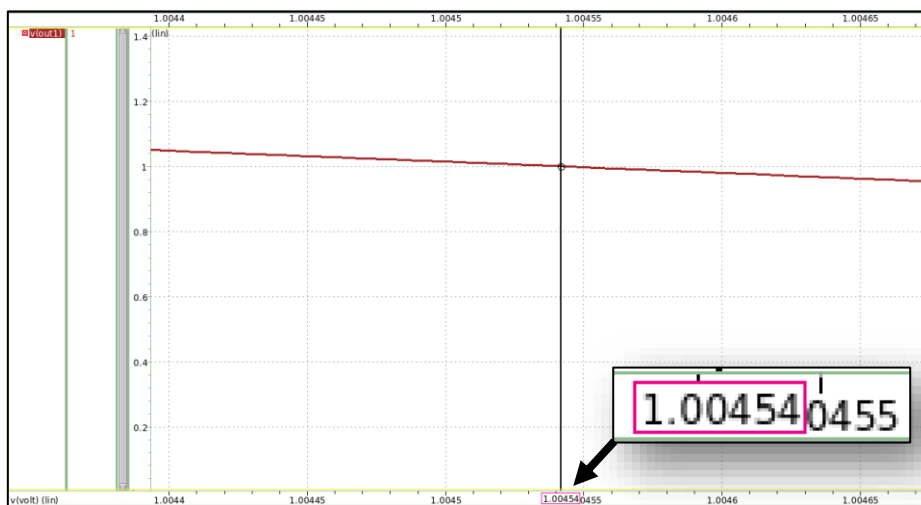


圖 3 sweeping VB1 to find the value

利用 sweep VB1 變數，找出 output common mode level = 1V 時的 VB1 值。



得到當 VB1=1.0051，output common mode level = 1V。

+0:in	= 0.	0:net15	= 205.8884m	0:net18	= 1.0051
+0:node1	= 780.0000m	0:node2	= 780.0000m	0:out1	= 1.0065
+0:out2	= 1.0065	0:vcm	= 780.0000m	0:vdd	= 1.5000
+0:vss	= 0.	0:vx	= 530.0000m		

模擬後，結果為 output common mode level = 1V。

- (f) Please compare the feedback voltage VB1 with the bias voltage VB2 in (B).

Net18 = VB1(circuit A) = 1.0045

+0:in	=	0.	0:net15	=	280.8989m	0:net18	=	1.0045
+0:node1	=	780.0000m	0:node2	=	780.0000m	0:out1	=	1.0045
+0:out2	=	1.0045	0:vcm	=	780.0000m	0:vdd	=	1.5000
+0:vss	=	0.	0:vx	=	530.0000m			

Net18 = VB2(circuit B) = 1.0045

+0:in	=	0.	0:net15	=	280.8558m	0:net18	=	1.0045
+0:node1	=	780.0000m	0:node2	=	780.0000m	0:out1	=	1.0012
+0:out2	=	1.0012	0:vcm	=	780.0000m	0:vdd	=	1.5000
+0:vss	=	0.	0:vx	=	530.0000m			

Circuit B 因有 RF，而 gate 端電流為 0，故兩端電壓相等，output voltage = pmos gate voltage (VB2)= 1.0045。

而 Circuit A 因沒有 RF，output voltage 並不會等於 pmos gate voltage (VB1)，但很剛好的是，上題利用 dc sweep 找出的 VB1，恰好等於 Circuit B output voltage 的值，且在設計 VB1 過程，發現只要調變一點點，Output voltage 就會改變很多。

- (g) Please use .tf command to simulate the differential and common mode gain, and print out the results.

Differential gain:

**** small-signal transfer characteristics			
v(out1,out2)/vac			= -55.4953
input resistance at		vac	= 1.000e+20
output resistance at v(out1,out2)			= 354.8421k

Common gain:

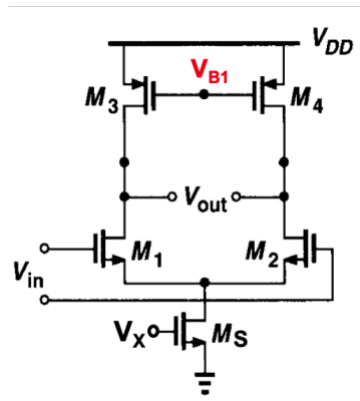
**** small-signal transfer characteristics			
v(out2)/vac			= -3.4160
input resistance at		vac	= 1.000e+20
output resistance at v(out2)			= 648.1103k

- (h) Please calculate the differential mode and common mode gains with the small-signal model.

Differential gain:

$$\begin{aligned}
 A_d &= -gm_1(ro_1//ro_3) \\
 &= -312.8165\mu \times (208.934K^{-1} + 1176.518K^{-1}) \\
 &= -312.8165\mu \times 177.426K \\
 &= -55.501\left(\frac{V}{V}\right)
 \end{aligned}$$

Common gain:



$$M = \frac{V_{o1}}{V_A} = -\frac{ro_3}{2ros} = -\frac{1176.518K}{276.208K} = -4.26$$

$$\begin{aligned}
 A_{CM} &= \frac{ro_1(1 - M)//2ros}{\frac{1}{gm_1} + [ro_1(1 - M)//2ros]} \times M \\
 &= \frac{118.953K}{3.197K + 118.953K} \times (-4.26) \\
 &= -4.15
 \end{aligned}$$

	Simulation	Hand calculates	Error
Differential gain	-55.495	-55.501	0.01%
Common gain	-3.416	-4.15	21.49%

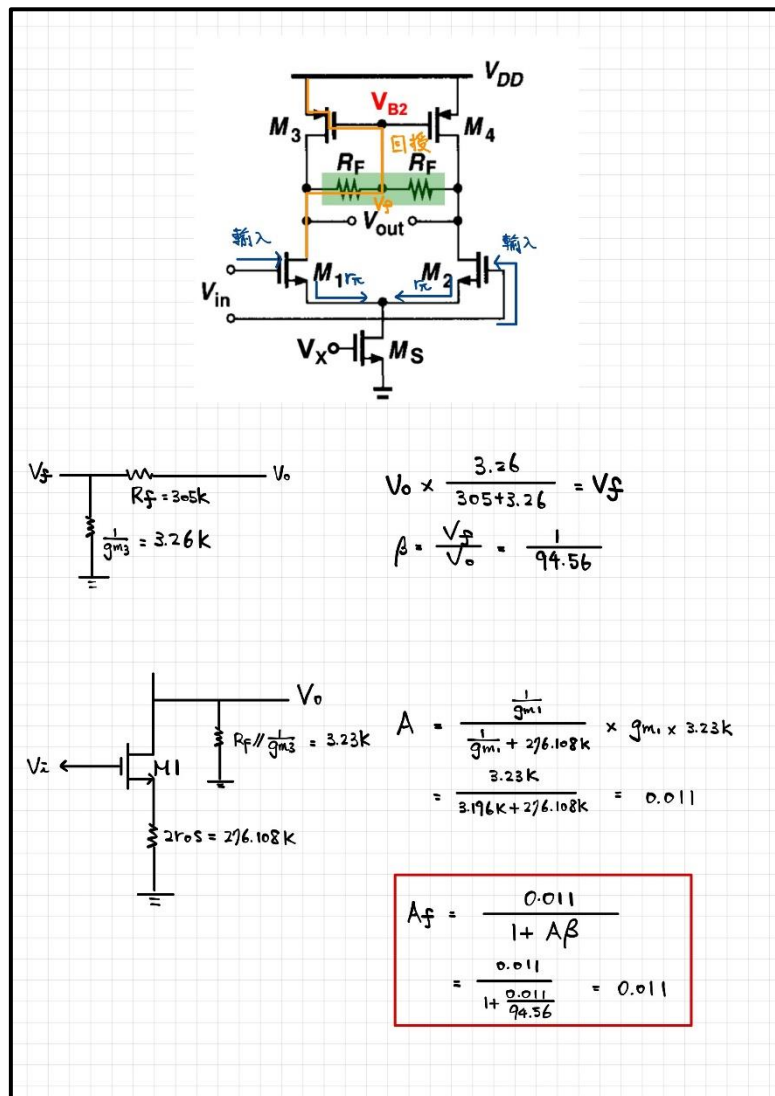
Discussion

- (i) Please discuss the precision requirement for the bias voltage VB1.

加入 VB1 的目的，是為了穩定直流點。若直流工作點不穩定，將導致小訊號參數、小訊號增益等誤差很大，無法預測電路行為，故需要加入 VB1 穩定 common output level。在設計時，通常欲加入的直流電壓會剛好等於有 feedback resistance 時的該點電位。

加入適當的 VB1 雖可使 common output voltage 趨近於 1V，但仍無法像有 feedback 的電路一樣完全相等，

- (j) Please also use the feedback concept to calculate this common mode gain.



Working item	specification	Simulation result	Hand calculation
Vdd	1.5V		
Tail current I_{ss}	30 μ A	30.565 μ	
Output common mode	1.0V	1.0045	
Differential voltage gain(V/V)	35	35.089	
Common voltage gain (V/V) w/o CMFB		3.416	4.15
Common voltage gain (V/V) wi CMFB	<0.05	0.0092	0.0115
$M_s(W/L_N \times m)$		4.7 μ /1 $\mu \times 2$	
$M_1, M_2(W/L \times m)$		15 μ /0.5 $\mu \times 1$	
$M_3, M_4(W/L \times m)$		40 μ /1.2 $\mu \times 5$	
R_F	Kohm	305	
V_{B1}	V	1.0045	
V_{B2}	V	1.0045	