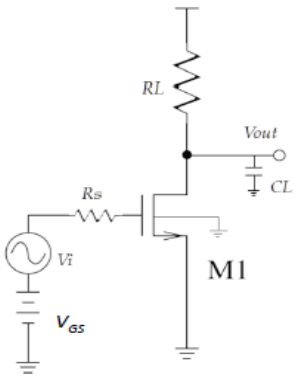
Homework I – Common Source
Due Time : 2022. 10. 13 10:00pm
First release : 2022. 9. 29

This homework is for you to design a **common source** stage. The results should include HSPICE simulations and hand calculations. The SPICE model is cic018.l. Please use the parameters from HSPICE simulation results for hand calculations.

Please note again:

1. Please hand in your report using eeclass system.
2. 若無於繳交期限前，先行向老師說明並獲許可，作業一律不同意補交!
3. 嚴禁抄襲(參考)!
4. Please generate your report with pdf format. At first page please add your student ID and name. Try to make the information "readable". (Note: Don't use black color in background for your screen capture figures). (Without performance table, -10pt)
5. Please hand in the spice code file (.sp) for each item of work. Do not include output file.
6. Please fill the number into HW1.xls. (Without excel file, -20pt)
7. Please do not zip your report.
8. Please write down the "values" associated with each variable in the equations. Do not just give answer directly.

In this common source, please use V_{DD}=1.5V.



The source impedance Rs is assumed 10Kohm and the loading capacitance C_L is 0.5pF.

Please design the bias voltage (V_{GS}), device size (W/L) of M1, and load resistor (R_L), to make M1 overdrive voltage (V_{GS}-V_t, Vod in HSPICE) larger than 0.15V. The small signal voltage gain (v_{out}/v_i) must be **larger** than 5.0 (V/V), at the same time the small signal -3dB bandwidth has to be **larger** than 30MHz.

Please try to design your circuit to achieve the large bandwidth (MHz) with small current (mA).

(operation point)

(a) Please design the device size of M_1, load resistance R_L, and the bias voltage V_{GS}, to make the small signal voltage gain (v_{out}/v_i) equal to 5.0 (V/V).

(b) Please use .op command to print out its small signal parameters.

(c) Please hand-calculate the gain value using SPICE parameters.

(d) Please sweep the gate DC voltage to draw its DC transfer curve. And find the slope at the selected V_{GS}.

(frequency response)

(e) Please plot the frequency response of this gain stage. And mark the poles and zeros on this curve. (Try to use .pz command (p.42 in tutorial) in SPICE).

(f) Compared and simulated poles/zeros with hand calculation.

(discussion)

(g) We will use the bandwidth (MHz) / current consumption (μA) as the figure of merit (FoM). Try to make it large, and then fill the table below.

(h) Please discuss how to achieve best FoM.

Parameter		Result
Supply Vdd	1.5V	
M_1 Device size (W/L x m)		
M_1 V_{GS} (mV)		
M_1 Bias Current (μA)	As small as possible	
M_1 Overdrive Voltage (mV)	Vod > 0.15V	
M_1 V_{DS} Saturation Voltage (mV)	vdsat	
M_1 Transconductance (μA/V)	gm	
Load R (Kohm)		
Voltage Gain (V/V)	> 5.0 V/V	
Bandwidth (MHz)	> 30 MHz	
FoM (BW (MHz) / Bias Current (μA))	As large as possible	

(a) 參考指令

```
.op                                          $operation point
.tf v(vout) vi                               $transfer function
.DC vi 0 1.5 0.001
.probe v(vout)
.probe d_gain=deriv('v(vout)')               $find gain using the first derivative
.meas DC d_av find deriv('v(vout)') when v(vin)=XXX
                                  $find gain at the bias condition using the first derivative
```

(e) 參考指令

```
.ac dec 10 1 10g
.pz v(vout) vi                               $find pole & zero (p42 in tutorial)
.probe vdb(vout) vp(vout)                    $plot AC gain and phase responses
.meas AC gmax MAX vdb(vout)                  $find max AC gain
.meas AC BW when vdb(vout)='gmax-3'          $find bandwidth
```