國立清華大學

Analog Circuit Design

國立清華大學
NATIONAL TSING HUA UNIVERSITY

Homework 1

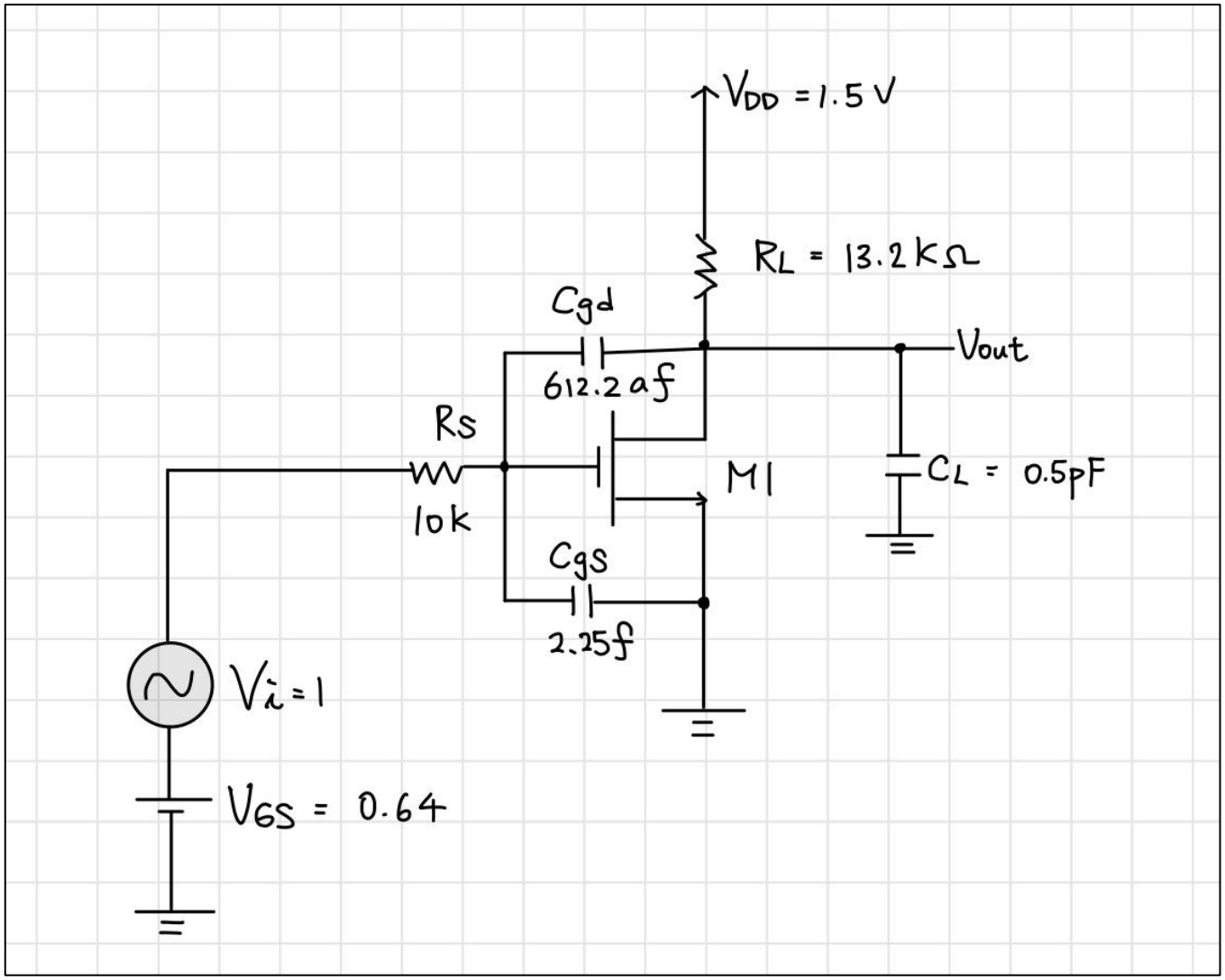
Common Source Mosfet

學號:111063548

姓名:蕭方凱

目錄

電路設計圖


VDD = 1.5 V
RL = 13.2 kΩ
Cgd
612.2 af
Vout
RS
10k
M1
CL = 0.5pF
Cgs
2.25f
Vi = 1
VGS = 0.64

Operation Points

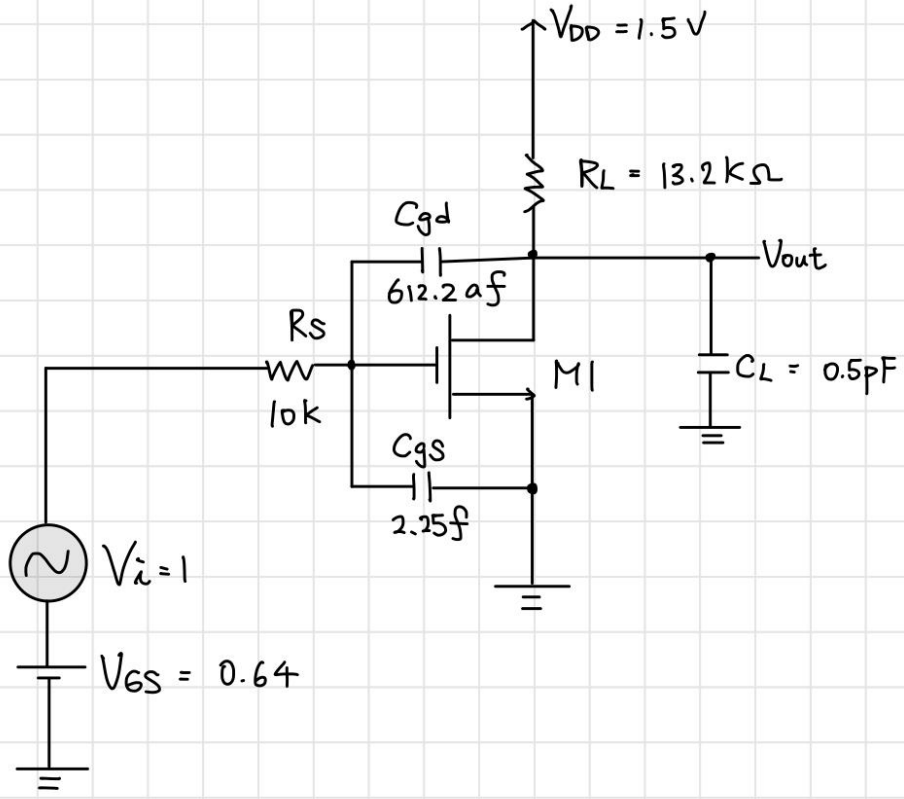
a. Please design the device size of M1, load resistance RL, and the bias voltage VGS, to make the small signal voltage gain (vout /vi) equal to 5.0 (V/V)

Design parameters	VGS	W	L	m	RL
Design value	0.64	0.85u	0.18u	2	13.2K

b. Please use .op command to print out its small signal parameters.

```
subckt
element  0:m1
model    0:n_18.1
region   Saturation
 id        54.2179u
 ibs     -1.761e-20
 ibd     -208.2076a
 vgs      640.0000m
 vds      784.3231m
 vbs        0.
 vth      488.9080m
 vdsat    170.8435m
 vod      151.0920m
 beta       3.4042m
 gam eff  507.4478m
 gm       489.4182u
 gds       22.0461u
 gmb       66.0537u
 cdtot      2.4369f
 cgtot      3.1495f
 cstot      4.7434f
 cbtot      4.5459f
 cgs        2.2454f
 cgd      612.1795a
```

c. Please hand-calculate the gain value using SPICE parameters



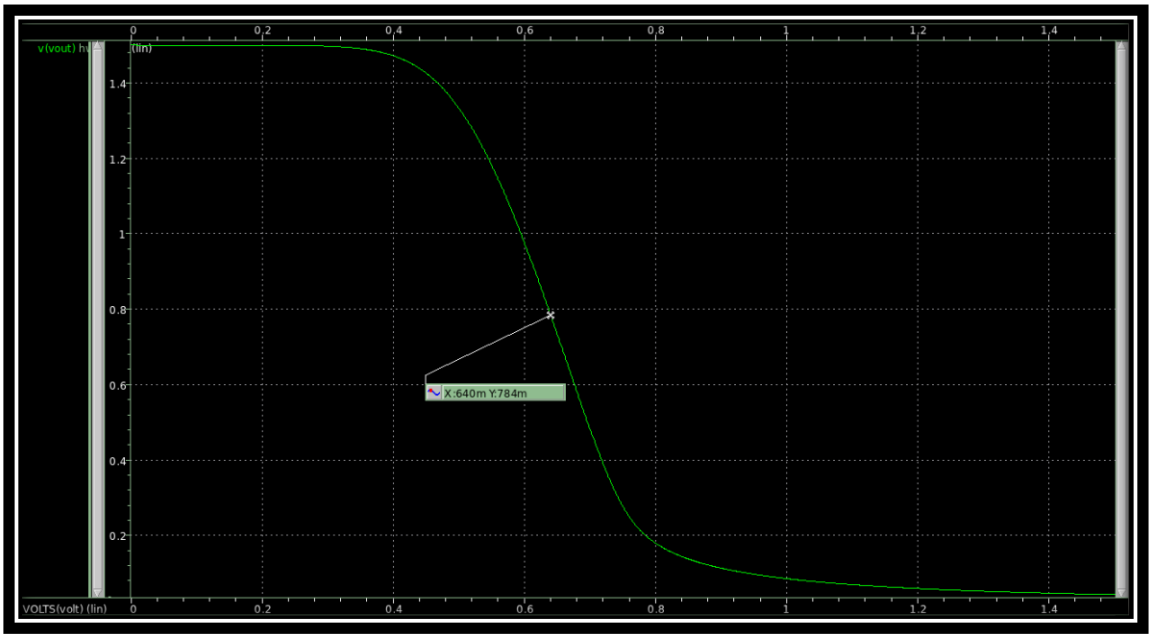
$g_m = 489.418\ \mu A/V$

$R_{out} = r_o // R_L = 10.2263\ k\Omega$

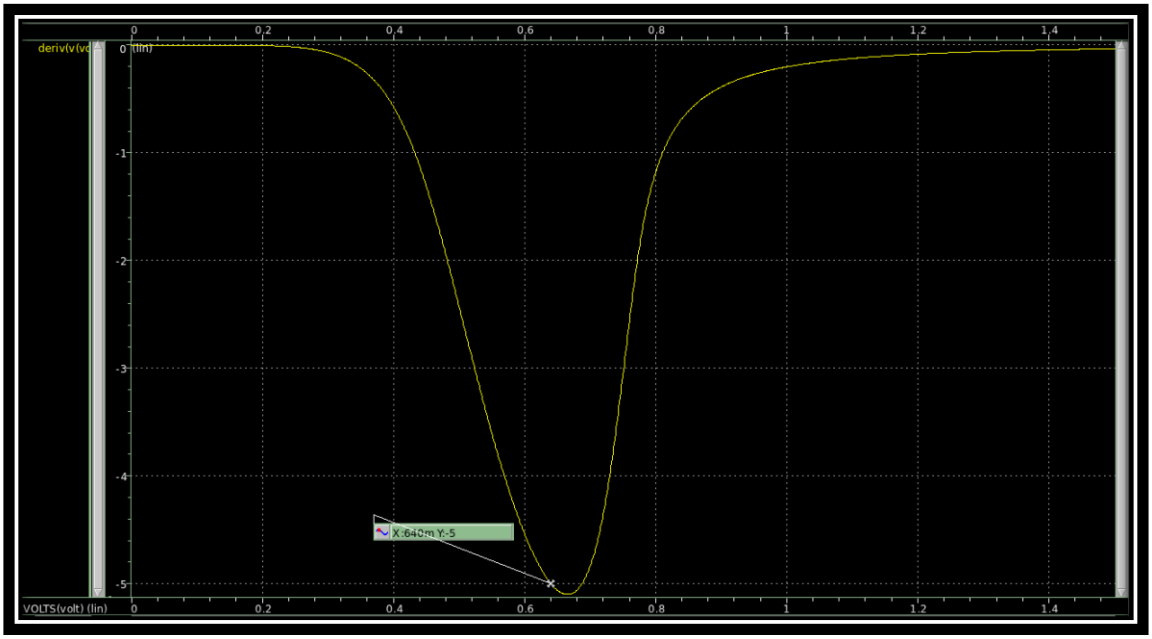
$gain = \frac{V_{out}}{V_{in}} = -g_m R_{out} = -5.0049$

DC Sweep

d. Please sweep the gate DC voltage to draw its DC transfer curve. And find the slope at the selected VGS



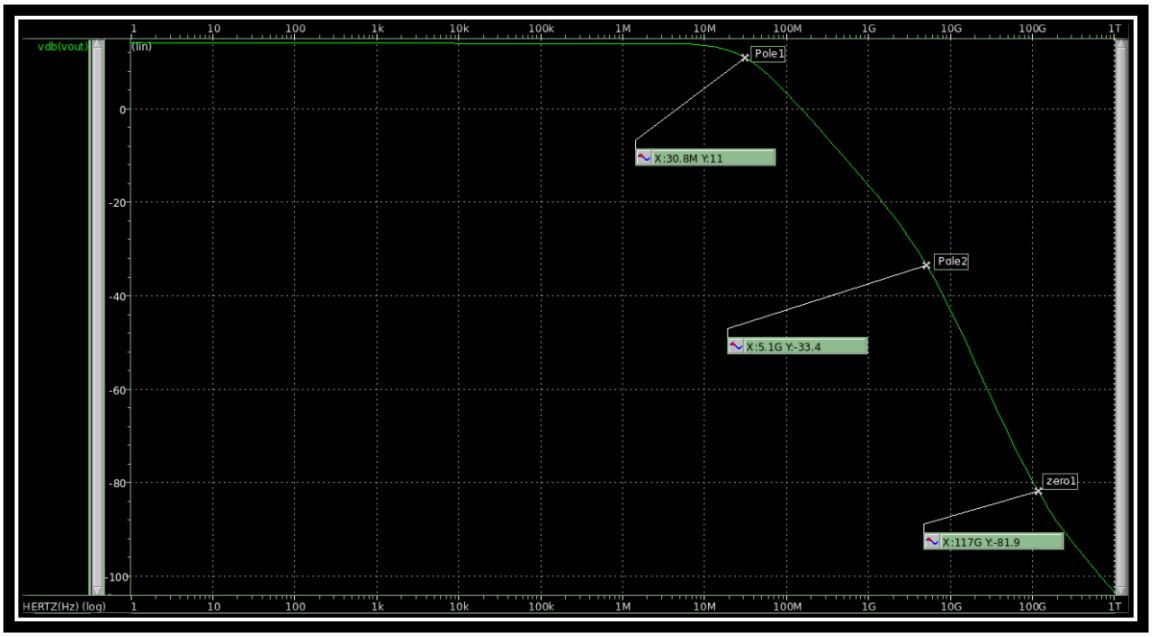
Transfer curve: Vo=0.784V, VGS=0.64V



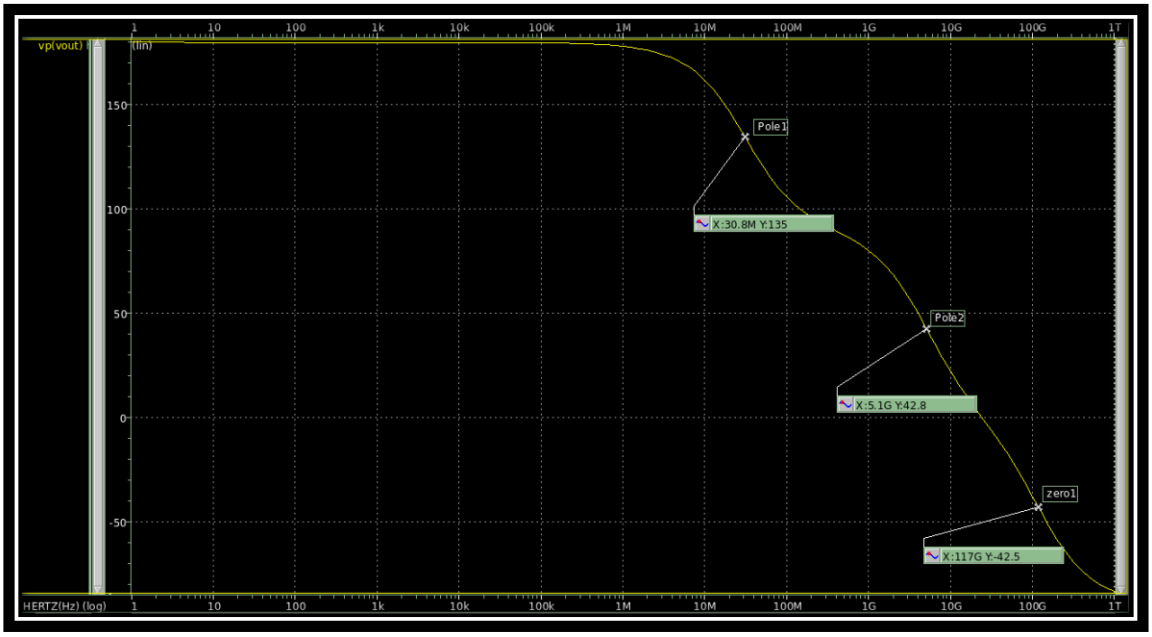
Vo/Vi transfer curve slope: the slope Vo/Vi= -5 at VGS=0.64V

AC Sweep

e. Please plot the frequency response of this gain stage. And mark the poles and zeros on this curve. (Try to use .pz command (p.42 in tutorial) in SPICE)



Frequency response(Gain)

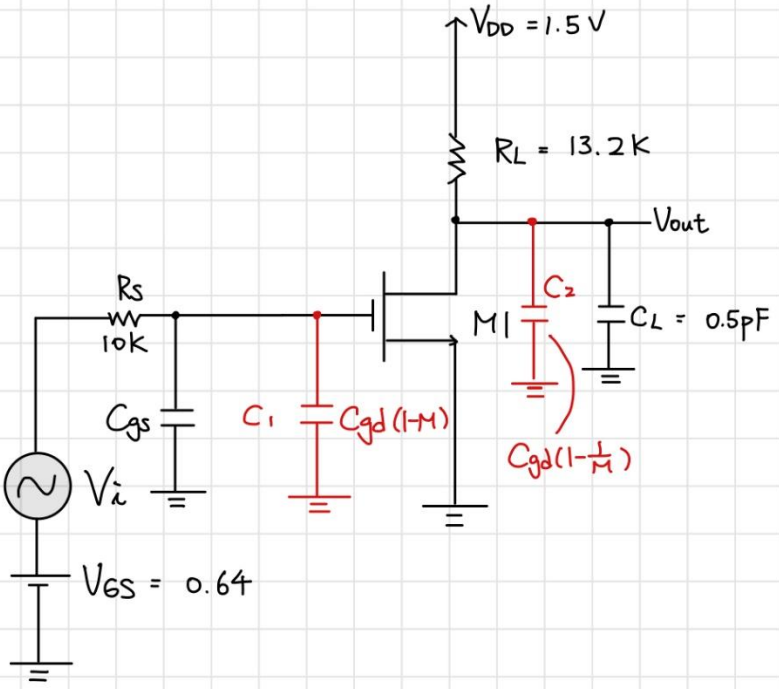


Frequency response(Phase)

f. Compared and simulated poles/zeros with hand calculation

gain = −5.0012 = $\frac{V_o}{V_i}$ = M (Miller 係數)

將原圖米勒拆橋後，可得：



$C_1 = C_{gd}(1-M) = 3673.81\ af$

$C_2 = C_{gd}(1-\frac{1}{M}) = 734.59\ af$

$a = 10^{-18}$, $f = 10^{-15}$

pole1 :

$$\frac{1}{(r_o // R_L)\times(C_2 // C_L)} = \frac{1}{10.2263k\times(734.59a+0.5p)}$$

$= 1.953\times10^{8}\ rad/s$

$= 3.108\times10^{7}\ Hz = 31.08\ MHz$

pole 2 :

$$\frac{1}{R_S\times(C_{gs} // C_1)} = \frac{1}{10k\times(2.25f+3673.81a)}$$

$= 1.688\times10^{10}\ rad/s$

$= 2.687\times10^{9}\ Hz = 2.69\ GHz$

zero1 :

$$\frac{g_m}{C_{gd}} = \frac{489.42\mu}{612.18a}$$

$= 799.47\times10^{9}\ rad/s$

$= 127.24\times10^{9}\ Hz$

$= 127.24\ GHz$

Discussion

g. We will use the bandwidth (MHz) / current consumption (μA) as the figure of merit (FoM). Try to make it large, and then fill the table below

Parameter		Result
Supply Vdd	1.5V	1.5V
M1 Device size (W/L x m)		0.85u/0.18u x 2
M1 VGS (mV)		0.64V
M1 Bias Current (μA)	As small as possible	54.28
M1 Overdrive Voltage (mV)	Vod > 0.15V	151.092
M1 VDS Saturation Voltage (mV)	vdsat	170.844
M1 Transconductance (μA/V)	gm	489.418
Load R (Kohm)		13.2
Voltage Gain (V/V)	> 5.0 V/V	5.001
Bandwidth (MHz)	> 30 MHz	30.712
FoM (BW (MHz) / Bias Current (μA))	As large as possible	0.57

h. Please discuss how to achieve best FoM.

FoM=BW/Id，BW = $\frac{1}{2\pi}\frac{1}{(ro//RL)x(C2//CL)}$(Hz)，Id=$K(VGS-Vth)^2$，其中 K 正比於 W/L，故提高 FoM，需將 BW 提高，Id 降低。

1. Id 下降: Id=$K(VGS-Vth)^2$，K 和 Vth 為製程參數，故調整 VGS 來調整 Id，調整方法為將 VGS 降低，但仍需使 VOV 大於 0.15(題目要求)。
2. BW 提高: BW = $\frac{1}{2\pi}\frac{1}{(ro//RL)x(C2//CL)}$(Hz)，其中 C2 為 atto 等級(10 的-18 次方)非常小，影響不大，而 CL 為題目給定，故不適用改變電容大小來改變頻寬。此題著重在 ro//RL 之調整，ro= VA/Id；RL 為自己設計，將 Id 變大或 RL 變小，都可使 BW 變寬，
   Id 提高時，雖 BW 提高，但 FoM=BW/Id，故很難保證 FoM 會變大。
   而 RL 降低時，雖 BW 提高但整體 gain 下降，為防止 gain 因 RL 下降甚至低於 5，本題嘗試提高 gm 值，gm=$\frac{2Id}{VOV}$=$2\sqrt{KId}$，在不調整 Id 情況下，盡量使 VOV 越小越好。

總結，使 VOV 等於 0.15，是提高 FoM 的一大原則。