| **Term Project – A Fully-Differential Two-Stage Op-Amp** |
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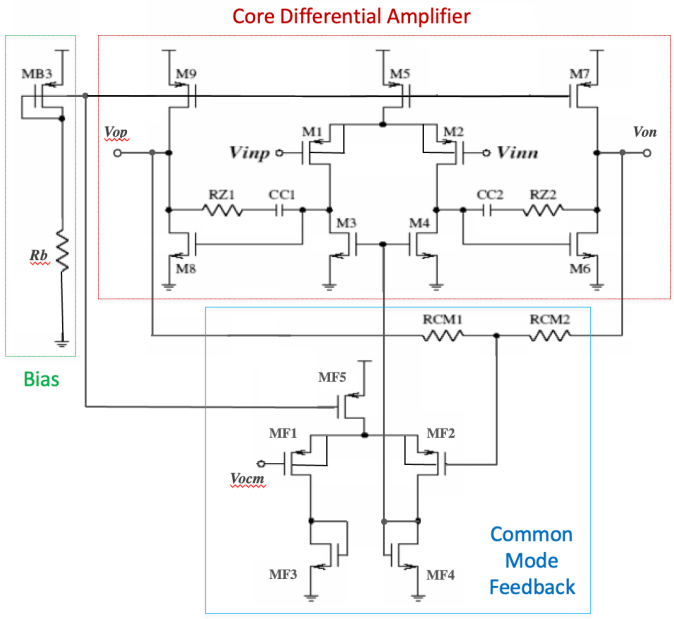
| Due date : 2023. 1. 16. 10:00am |
| First release : 2023. 1. 5. |

In this term project you have to fine-tune a fully differential operational amplifier based on the reference design. You have to submit three files with exact file name.

- term-a1234567.pdf (report file with ID#)
- op.sp (amplifier spice file).
- Term.xlsx (performance in excel file)

Please note again:

1. Please hand in your report using eeclass system.
2. 一律不同意補交!
3. 嚴禁抄襲(參考), 違者校規議處!
4. Please generate your report with pdf format. At first page please add your student ID and name. Try to make the information "readable". (Note: Don't use black color in background for your screen capture figures). (without performance table, -20pt)
5. Please hand in the spice code file (.sp) for each item of work. Do not include output file.
6. Please do not zip your report.
7. Please write down the "values" associated with each variable in the equations. Do not just give answer directly.



| Design Items | Specifications | Ref Work | My Work |
|---|---|---|---|
| Technology | CIC pseudo 0.18um technology | | |
| Supply voltage | **1.5V** | **1.8V** | **1.5V** |
| Vicm, Vocm | **0.75V, 0.75V** | **0.9V, 0.9V** | **0.75V, 0.75V** |
| Supply current | **< 5mA** including bias ckt | 1.136 mA | |
| Loading | **5pF / 25KΩ (for each output)** | **5pF / 10KΩ** | **5pF / 25KΩ** |
| Compensation R, C, | Rc < 10KΩ , Cc < 10pF | Rc=0.5KΩ , Cc=3pF | |
| Open-loop simulation | | | |
| DC gain | **> 60dB**, as large as possible | 70.6 dB | |
| G-BW (ft) * | **> 30MHz**, as large as possible | 64.1 MHz | |
| P.M. | **> 45 o** | 54.8 o | |
| C.M.R.R. @10KHz | > 90dB | 100.6 dB | |
| P.S.R.R.+ @10KHz | > 90dB | 102.0 dB | |
| P.S.R.R.- @10KHz | > 90dB | 103.9 dB | |
| Closed-loop simulation | | | |
| Differential swing of 1.0 -V (step or sinusoidal) | | | |
| Closed-loop gain | > -0.1dB @ 10KHz | -0.005 dB | |
| S.R.+ (10% ~ 90%)* | > 15 V/μs (single-ended output) | 18.9 V/μs | |
| S.R.- (90% ~ 10%)* | > 15 V/μs (single-ended output) | 22.7 V/μs | |
| T.H.D. (1.0Vpp@100kHz Sin)* | **< - 60 dB** | -59 dB | |
| Settling+ (1.0Vstep to 0.5%)* | **< 150ns** | 240ns | |
| Settling- (1.0Vstep to 0.5%)* | **< 150ns** | 250ns | |
| **FoM:** | | | |
| GxBW / total bias I | MHz / mA | **56.4** | |
| 1 / (Settling+)(total bias I) | 1000 / nsec x mA | **3.67** | |
| 1/(Settling-)(total bias I) | 1000 / nsec x mA | **3.52** | |

note1: all the devices are assumed to be with no body effect.

note2: the current consumption includes all the circuits.

*Report: (Please mark each item clearly in your report)*

1. Schematic

Please draw the schematic of your circuit.

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Fig.1* marks each *active device dimension*, *passive component value*, *node voltage* and *branch current*.

List.1* print all the small signal parameters of each devices from .op command in report.

2. Spice Code

Please pack your circuits as a sub-circuit in a file named "**op.sp**" and print it in your report. The format in HSPICE "must" follow the definition as:

```
.param vdd=1.5V     *Your positive supply voltage
.param vss=0V       *Your negative supply voltage
.param vocm=0.75V   *Your output common mode voltage (for CMFB)

                positive input
                  |   nagtive input
                  |    |   supply
                  |    |    |   gnd
                  |    |    |    |  positive output
                  |    |    |    |    |  negative output
                  |    |    |    |    |    |  output common mode V
                  V    V    V    V    V    V     V
.subckt my_op  vip  vin  vdd  vss  vop  von  vocm
  circuit body
.ends
```

List.2* print all the codes of your op.sp in report.

3. Simulations and Calculations

Please check the test circuits packed for this term project, and do the simulations and compare the results with hand calculations.

### 3.1 Open-loop differential mode AC response

Fig. 3.1(a)* Please plot the AC magnitude and phase responses of differential mode gain.
Mark the DC gain (dB), unity-gain frequency (Hz), and phase margin (degree) in this figure.

Tab. 3.1(b) Please print the gain and impedance from .tf command.

Tab. 3.1(c) Please print the poles and zeros from .pz command.

Dis. 3.1* Please check the results with your hand calculations.
Discussion the movement of poles/zeros after compensation.
(gain, p1, p2, zero – after frequency compensation)

### 3.2 Open-loop differential mode DC sweep

Fig. 3.2(a) Please draw the test circuit with your input source and load.

Fig. 3.2(b)* Please plot the single-ended (Vop and Von separately) and differential (Vop-Von) outputs for inputs with differential signals. (zoom-in the operation range). Mark the slope to make sure the gain is like AC response.

### 3.3 Open-loop common mode AC response

Fig. 3.3(a) Please draw the test circuit with your input source and load.

Fig. 3.3(b)* Please plot the magnitude response of common mode gain. Mark the DC gain (dB) and poles and zeros in this figure.

Tab. 3.3(c) Please print the gain and impedance from .tf command.

Tab. 3.3(d) Please print the poles and zeros from .pz command.

Dis. 3.3* Please check the results with your hand calculations. (gain, and low frequency zero)

### 3.4 Open-loop common mode DC sweep

Fig. 3.4(a) Please draw the test circuit with your input source and load.

Fig. 3.4(b)* Please plot the single-ended (Vop or Von) Mark the slope to make sure the gain is like AC response.

### 3.5 Open-loop power supply+ AC response

Fig. 3.5(a) Please draw the test circuit with your input source and load.

Fig. 3.5(b) Please plot the magnitude response of power supply+ gain. Mark the DC gain (dB) in this figure.

### 3.6 Open-loop power supply- AC response

Fig. 3.6(a) Please draw the test circuit with your input source and load.

Fig. 3.6(b) Please plot the magnitude response of power supply- gain. Mark the DC gain (dB) in this figure.

### 3.7 Closed-loop differential mode AC response

Fig. 3.7(a) Please draw the test circuit with your input source and load.

Fig. 3.7(b)* Please plot the AC magnitude and phase responses of differential mode gain. Mark the DC gain (dB) and -3dB freq (Hz) in this figure. Compare the results with hand calculations.

Fig. 3.7(c)* Please print the input and output node voltages from .op. Check if these values are reasonable.

Tab. 3.7(d) Please print the values from .tf command.

Dis. 3.7(e) Please check the results with your hand calculations.

### 3.8 Closed-loop differential mode DC sweep

Fig. 3.8(a) Please draw the test circuit with your input source and load.

Fig. 3.8(b)* Please plot the single-ended (Vop and Von separately) and differential (Vop-Von) outputs for inputs with differential signals. Mark the slope and compare it with gain in AC response.

### 3.9 Closed-loop distortion simulation

Fig. 3.9(a) Please draw the test circuit with your input source and load.

Fig. 3.9(b)* Please plot the single-ended (Vop and Von separately) and differential (Vop-Von) outputs for 100KHz sinusoidal inputs with differential peak-to-peak signal of 1.0V. The THD must be less than -60dB.

### 3.10, 3.11 Closed-loop step response

Fig. 3.10(a) Please draw the test circuit with your input source and load.

Fig. 3.10(b)* Please plot the single-ended (Vop and Von separately) and differential (Vop-Von) outputs for 1.0V differential step inputs.

Fig. 3.10(c)* Please mark the slew rate+ (10% to 90%) and settling+ time (to 0.5% error) in the figure. Compare with the hand calculations.

Fig. 3.11(a)* Please mark the slew rate- (90% to 10%) and settling- time (to 0.5% error) in the figure. Compare with the hand calculations.

Fig. 3.10(d)* Please plot the common mode sensing node waveform.

Fig. 3.10(e)** Try to improve the common model settling time. And discuss the CMFB operation during step transient.

## 4. Performance Table

Please fill your performance into the summary table and proj.xlsx.

## 5. Design Concerns

Briefly express your design consideration and optimization during your design.

(a) Operation point selection.

(b) Compensation. Please especially address your placement of unity frequency (ft), first non-dominant pole (p2), and zero (LHP or RHP).

(c) Feedback loop of common mode stabilization. Please compare the loop performance of the common mode and the differential mode signals.

(d) How to achieve better FoMs.

## 6. Discussions

Dis 6.1. Discuss your *experience* on this project and the *problem* during design.

Dis 6.2. Please *conclude* what you get and *suggest* for this course.

Reference Reading:


- P. Allen and D. Holberg, *CMOS Analog Circuit Design,* 2e, Oxford, 2002.
  *Chap 6.6* there are many examples of application circuit for each specification (it is a single-ended case).
- R. Gregorian, *Introduction to CMOS OP-Amp and Comparator*, Wiley, 1999.
  *Chap 8.2* there are a complete design flow for an two-stage op-amp (it is also a single-ended case)