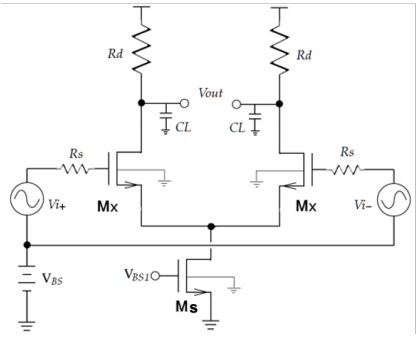
Homework II – Differential Pair
Due date : 2022. 11. 03 10:00pm
First release : 2022. 10. 20

This homework is for you to design a **source-coupled pair**. The problem sets include HSPICE simulations and hand calculations. The SPICE model is cic018.l. Please use the parameters from HSPICE simulation results for hand calculations.

Please note again:

1. Please hand in your report using eeclass system.
2. 若無於繳交期限前，先行向老師說明並獲許可，作業一律不同意補交!
3. 嚴禁抄襲(參考)!
4. Please generate your report with pdf format. At first page please add your student ID and name. Try to make the information "readable". (Note: Don't use black color in background for your screen capture figures). (Without performance table, -10pt)
5. Please hand in the spice code file (.sp) for each item of work. Do not include output file.
6. Please fill the number into HW2.xls. (Without excel file, -20pt)
7. Please do not zip your report.
8. Please write down the "values" associated with each variable in the equations. Do not just give answer directly.

In this differential pair circuit, please use V_{DD}=1.5V.



The source impedance Rs is assumed 10Kohm and the loading capacitance is assumed 0.5pF.

Please design the bias voltage (V_{BS1}) and device size (W/L) of Ms, to generate the tail current (Ms drain current).

Please design the differential mode small signal voltage gain (v_{out}/v_i) larger than 6.0 (V/V), under its small signal -3dB bandwidth larger than 30MHz.

We will find the best **figure of merit (FoM)** value as "bandwidth (MHz) x linear range (mV) / current consumption (μA)".

(operation point)

(a) Please design the device size of Mx, Ms, load resistance Rd, and the bias voltage V_{BS} and V_{BS1}, to make the small differential signal voltage gain (vout/vi) larger than 6.0 (V/V). (Please note, since Ms serves as a current source, Ms must stay in the saturation region).

(b) Please print out the small signal parameters of active devices from list file.

(Transfer curves of differential mode and common mode)

(c) Under the operation condition in (a), please run .DC then plot the **differential input – differential output** transfer curve (as in slide 6). Try to plot and measure its small signal differential mode gain.

(d) Compare the gain value with hand calculation using the small signal parameters from (b).

(e) Like (c) please also run .DC to plot the **common-mode input – common-mode output** transfer curve (as in slide 6). Try to plot and measure its small signal common mode gain.

(f) And compare the gain value with hand calculation using the small signal parameters from (b).

(frequency response)

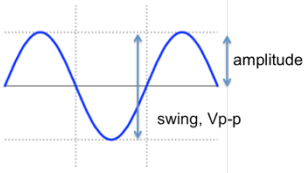
(g) The small signal -3dB bandwidth of differential mode signal has to be larger than 30MHz. Please simulate and plot the differential mode frequency response of this gain stage.

(h) Use .pz to simulate and mark the poles/zeros on this curve.

(i) Compare with hand calculations.

(linearity)

(j) Please input differential sinusoidal waveforms to estimate the harmonic distortion. Please use .four to simulate the THD performance. And also use .tran to plot the maximum output differential voltage waveforms that achieve -60dB THD at 1MHz. The single-ended input amplitude value is defined as the linear range in this homework. The linear range must be larger than 10mV.



(k) Please print out the .THD results.

(l) Compare the simulated input amplitude with the hand calculation.

(m) Under this amplitude please also simulate the THD performance under 100KHz and 10MHz respectively.
(set DELMAX < 1e-9 in .option for higher accuracy in THD simulation)

(Figure of Merit)

(n) We will use the "bandwidth (MHz) x linear range (mV) / current (μA)" as the figure of merit (FoM). Please try to make this FoM maximal.

(o) Please use your design equations to explain how to achieve max FOM.

Working Item	Specification	Simulation	calculation
Vdd	1.5-V		
Tail current	As small as possible (μA) (#3)		
Differential gain	> 6 (V/V)		
Input common mode	Open for design (V_{BS}, V)		
Tail current bias	Open for design (V_{BS1}, V)		
Common-mode gain	Open for design (V/V)		
Input size Mx	Open for design (W/L), m		
Differential gm	Open for design (mA/V)		
Load R	Open for design (Kohm)		
Bandwidth	>30MHz (#1)		
Linear range output -60dB THD @1MHz	Single-ended input amplitude >10mV (#2)		
FoM	(#1 x #2 / #3)		

DC/AC 參考指令

…

```
Vac    in gnd ac 1                    $generate the differential signals
Eac1 vi1 vdc in gnd 0.5               $with two voltage-controlled voltage source
E
Eac2 vi2 vdc in gnd -0.5
…
.op                                   $operation point
.ac dec 10 100 1g
.tf v(vo1,vo2) Vac                    $calculate input to output transfer function
```

THD 參考指令

```
.option ABSTOL=1e-7 RELTOL=1e-7 POST=1 CAPTAB ACCURATE=1 DELMAX=1e-9
…                                     $increase the accuracy
.op                                   $operation point
.tran  0.1us 100us
.four  1x v(vo1)                      $simulate the single-ended output THD
.four  1x v(vo1,vo2)                  $simulate the differential output THD
.probe v(vo1,vo2)
```