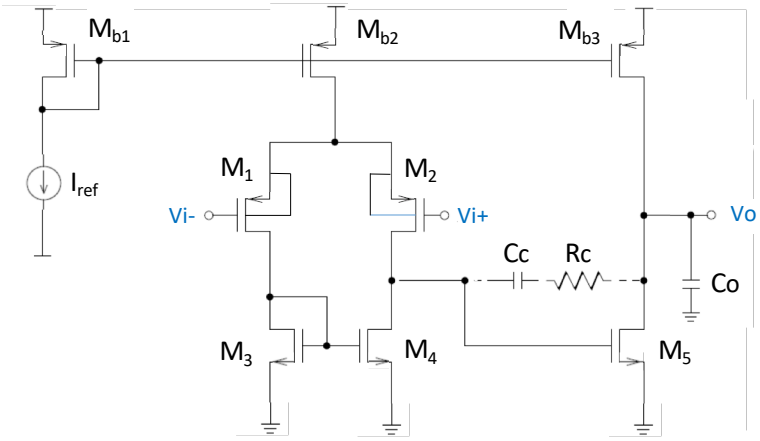
Homework IV – Two-Stage Operational Amplifier
Due date : 2022. 12. 15. 10:00pm
First release : 2022. 12. 01.

This homework is a single-ended CMOS two-stage operational amplifier. The problem set includes HSPICE simulations and hand calculations. The SPICE model is cic018.l. Please use the parameters from HSPICE simulation results for hand calculations.

Please note again:

1. Please hand in your report using eeclass system.
2. 若無於繳交期限前，先行向老師說明並獲許可，作業一律不同意補交!
3. 嚴禁抄襲(參考)!
4. Please generate your report with pdf format. At first page please add your student ID and name. Try to make the information "readable". (Note: Don't use black color in background for your screen capture figures). (Without performance table, -10pt)
5. Please hand in the spice code file (.sp) for each item of work. Do not include output file.
6. Please fill the number into HW4.xls. (Without excel file, -20pt)
7. Please do not zip your report.
8. Please write down the "values" associated with each variable in the equations. Do not just give answer directly.

In this two-stage op-amp circuit, please use V_{DD}=1.5V, V_{icm}=0.75V, V_{ocm}=0.75V, I_{ref} = 100μA, C_o= 0.5pF



In this design, the DC gain has to be larger than 60dB, unity gain frequency larger than 50MHz, phase margin larger than 45^0. Our target is to achieve *maximum unity gain frequency* and *maximum slew rate* with *minimum current.*

(a) Operation point

1. Please DESIGN your bias (M_{b1} - M_{b3}) and amplifier (M_1 – M_5) size to make the *gain at DC larger than 60dB*.
2. Print out the results from **.op** command. And make sure all the devices are properly biased.
3. Use **.tf** command to print out the voltage gain.
4. Verify your DC gain with hand calculation.

(b) Before compensation

1. Please simulate and plot the frequency response (magnitude and phase) of your design in (a). Mark the (i) DC gain (ii) unity gain frequency, and (iii) phase margin on figure.
2. Use **.pz** to identify the poles and zeros, and mark them on bode plot.
3. Verify the first and second dominant poles and first RHP zeros with hand calculation.

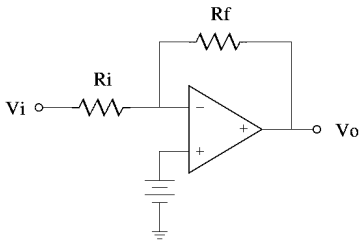
(c) with compensation capacitor Cc

1. Please design your value of Cc and simulate the AC response in (b). (please note, your *Cc must be smaller than 10pF, and the phase margin must larger than 0^0 in this case*).
2. Please print **.pz** output of the new poles (first and second dominant) and zeros (first RHP), and mark them on bode plot.
3. Verify the compensation with hand calculation.

(d) with compensation capacitor Cc in (c) and nulling resistor Rc

1. Please design your value of Rc to shift the RHP zero and simulate the AC response in (c).
   (please note, your *unity gain frequency must be larger than 50MHz* and *phase margin must larger than 45^0 in this case*).
2. Please print **.pz** output of the new poles and zeros, and mark them on bode plot as (c).
3. Verify the compensation with hand calculation.

Now, we apply this op-amp to an inverting type configuration. The closed-loop gain should be -1, with the feedback resistors Ri=Rf=100kΩ.



The closed-loop total harmonic distortion (THD) has to be smaller than -60dB, when input with *0.7Vpp 10kHz* sinusoidal waveform.

(e) Closed-loop transfer curve

1. Please simulation the closed-loop DC transfer curve when input from 0 to 1.5V, and plot the closed-loop gain and mark the slope.
2. Print **.tf** output to discuss the gain and input/output impedance.
3. Please calculate the closed-loop DC gain with the real op-amp gain in your design.

(f) Closed-loop AC response

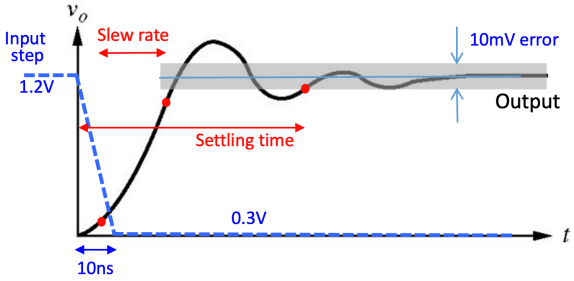
1. Please simulation the closed-loop AC response. Draw the bode plot and mark its DC gain and -3dB frequency.
2. Put this bode plot with open-loop response and compare the results.

(g) Closed-loop linearity response

1. Please simulation the closed-loop *THD* when input with *0.7Vpp 10kHz* sinusoidal waveform. (*THD has to be smaller than -60dB*).
2. Please plot the input and output waveforms.

(h) Closed-loop large-signal step response

1. Please plot the output waveform when input with a step- from *0.3V to 1.2V*, and a step+ from *1.2V to 0.3V,* with rise/fall time of *10ns*.
2. Please mark slew rate (slope between 10% - 90% of final value), and the settling time (to within 10mV error) on your step+ and step- responses.
3. Compare slew rate simulation results with hand calculation.



(i) Please change the feedback resistors Ri=Rf=1kΩ. Repeat the closed-loop transfer curve as (e).

1. Print **.tf** output to discuss the gain and input/output impedance
2. Please discuss the difference.

(j) Please fill the following table. and discuss your design for frequency compensation and for best FoM.

V_{DD}	1.5V	
I_{DD} (total current exclude of I_{Mb1}) (*1)	μA	
I_{Mb2}, I_{Mb3}	____ μA	____ μA
Rc, Cc *(<10pF)*		
Open-loop performance (after final compensation)		
DC gain *(> 60dB)*	dB	
Unity gain frequency *(1pF load) (> 50MHz)* (*2)	MHz	
Phase margin *(> 45⁰)*	degree	
Closed-loop performance (after final compensation)		
T.H.D. (0.3V-1.1V, 10KHz test) *(THD < -60dB)*	dB	
S.R.+ (Vo 0.3V-1.2V, slope from 10%-90%) (*3)	V/μs	
S.R.- (Vo 1.2V-0.3V, slope from 90%-10%) (*4)	V/μs	
Settling time (Vo 0.3-to-1.2V within 10mV error)	ns	
Figure of Merit (after final compensation)		
$\frac{*2_{(MHz)}}{*1_{(uA)}}$		
$\frac{*3_{(V/us)}}{*1_{(uA)}}$		
$\frac{*4_{(V/us)}}{*1_{(uA)}}$		