國立清華大學

Analog Circuit Design

國立清華大學
NATIONAL TSING HUA UNIVERSITY

Term Project

Fully-Differential Two-Stage Op-Amp

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目錄

1. Schematic

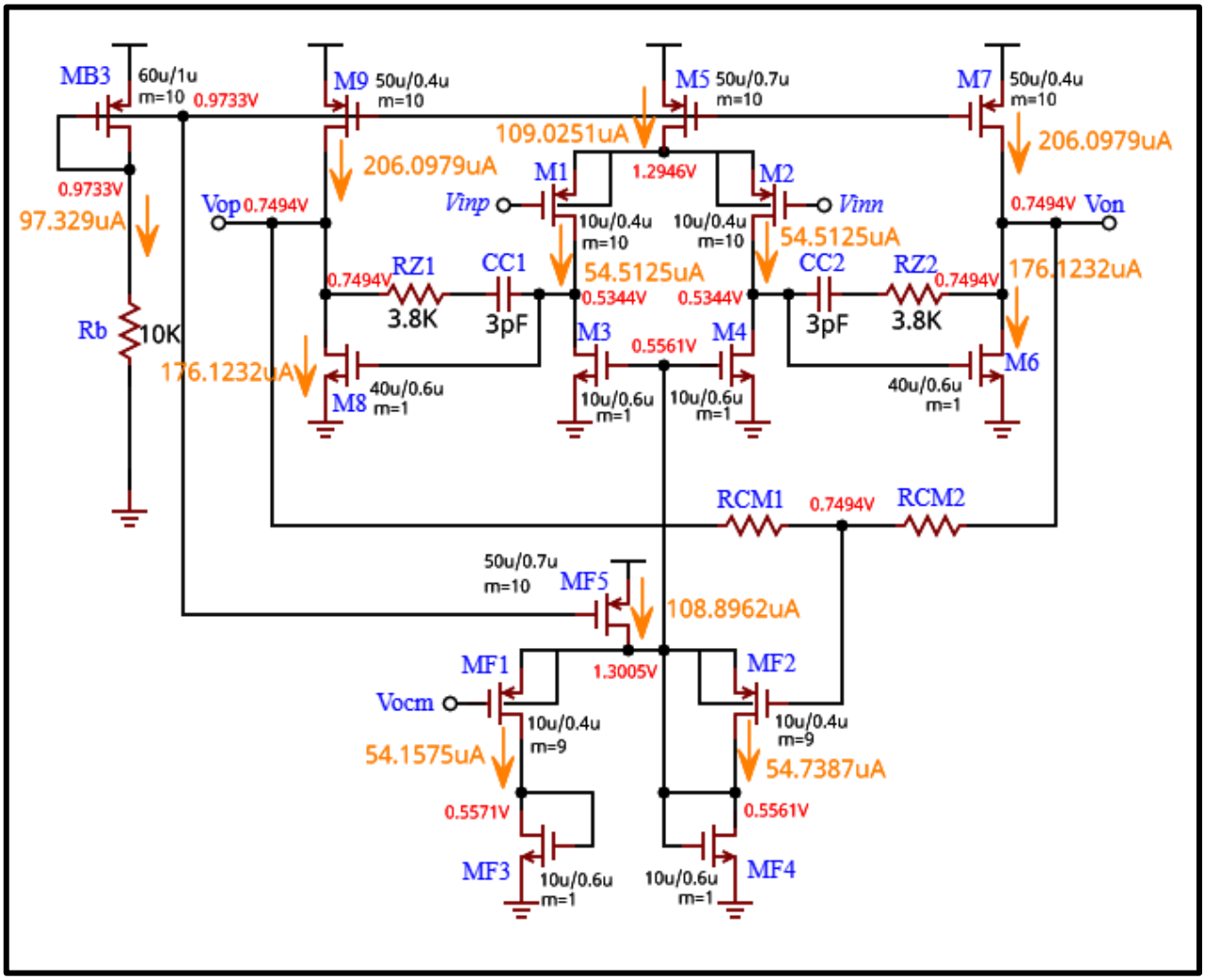


Fig 1 marks each active device dimension, passive, component value, node voltage and branch current

MOS	W/L	m	MOS	W/L	m
MB3	60μ/1μ	10	**M8**	40μ/0.6μ	4
M1	10μ/0.4μ	10	**M9**	50μ/0.4μ	10
M2	10μ/0.4μ	10	**MF1**	10μ/0.4μ	9
M3	10μ/0.6μ	1	**MF2**	10μ/0.4μ	9
M4	10μ/0.6μ	1	**MF3**	10μ/0.6μ	1
M5	50μ/0.7μ	10	**MF4**	10μ/0.6μ	1
M6	40μ/0.6μ	4	**MF5**	50μ/0.7μ	10
M7	50μ/0.4μ	10			

subckt	xop	xop	xop	xop	xop	xop
element	1:mmb3	1:mm1	1:mm2	1:mm3	1:mm4	1:mm5
model	0:p_18.1	0:p_18.1	0:p_18.1	0:n_18.1	0:n_18.1	0:p_18.1
region	Saturation	Saturation	Saturation	Saturation	Saturation	Saturation
id	-97.3290u	-54.5125u	-54.5125u	54.5125u	54.5125u	-109.0251u
ibs	9.007e-21	5.459e-21	5.459e-21	-8.821e-21	-8.821e-21	1.012e-20
ibd	14.0604f	3.6605f	3.6605f	-415.7584a	-415.7584a	4.5832f
vgs	-526.7099m	-544.6486m	-544.6486m	557.0528m	557.0528m	-526.7099m
vds	-526.7099m	-760.2435m	-760.2435m	534.4052m	534.4052m	-205.3514m
vbs	0.	0.	0.	0.	0.	0.
vth	-494.5476m	-508.7508m	-508.7508m	426.0395m	426.0395m	-498.7058m
vdsat	-80.9129m	-92.1796m	-92.1796m	144.4753m	144.4753m	-81.3192m
vod	-32.1623m	-35.8979m	-35.8979m	131.0133m	131.0133m	-28.0041m
beta	44.2081m	19.2239m	19.2239m	5.3354m	5.3354m	53.1577m
gam eff	557.0847m	557.0846m	557.0846m	507.4462m	507.4462m	557.0847m
gm	1.7719m	951.7299u	951.7299u	638.6526u	638.6526u	1.9991m
gds	6.0900u	6.7264u	6.7264u	10.0813u	10.0813u	21.5511u
gmb	532.7554u	279.5343u	279.5343u	125.1393u	125.1393u	595.4033u
cdtot	704.9396f	113.5490f	113.5490f	13.7523f	13.7523f	642.1155f
cgtot	3.2327p	245.7591f	245.7591f	42.8508f	42.8508f	1.9055p
cstot	3.5348p	304.5474f	304.5474f	50.9072f	50.9072f	2.1387p
cbtot	2.2087p	246.7450f	246.7450f	30.9055f	30.9055f	1.5801p
cgs	2.5323p	180.3048f	180.3048f	35.9871f	35.9871f	1.4399p
cgd	215.6714f	35.8878f	35.8878f	3.6068f	3.6068f	182.6962f

subckt	xop	xop	xop	xop	xop	xop
element	1:mm6	1:mm7	1:mm8	1:mm9	1:mmf1	1:mmf2
model	0:n_18.1	0:p_18.1	0:n_18.1	0:p_18.1	0:p_18.1	0:p_18.1
region	Saturation	Saturation	Saturation	Saturation	Saturation	Saturation
id	176.1232u	-206.0979u	176.1232u	-206.0979u	-54.1575u	-54.7387u
ibs	-2.650e-20	1.914e-20	-2.650e-20	1.914e-20	5.424e-21	5.482e-21
ibd	-2.1683f	16.7533f	-2.1683f	16.7533f	3.2255f	3.2216f
vgs	534.4052m	-526.7099m	534.4052m	-526.7099m	-550.4845m	-551.1167m
vds	749.3678m	-750.6322m	749.3678m	-750.6322m	-744.3281m	-743.4317m
vbs	0.	0.	0.	0.	0.	0.
vth	422.1286m	-506.6094m	422.1286m	-506.6094m	-508.7508m	-508.7508m
vdsat	132.6323m	-83.3168m	132.6323m	-83.3168m	-95.4769m	-95.8410m
vod	112.2766m	-20.1005m	112.2766m	-20.1005m	-41.7337m	-42.3658m
beta	21.3469m	97.8938m	21.3469m	97.8938m	17.2838m	17.2818m
gam eff	507.4462m	557.0847m	507.4462m	557.0847m	557.0846m	557.0846m
gm	2.2695m	3.8155m	2.2695m	3.8155m	925.1859u	932.8627u
gds	30.4439u	26.4198u	30.4439u	26.4198u	6.6942u	6.7641u
gmb	445.2691u	1.1301m	445.2691u	1.1301m	271.7178u	273.9719u
cdtot	52.4646f	562.9819f	52.4646f	562.9819f	102.4752f	102.4912f
cgtot	170.2289f	1.1582p	170.2289f	1.1582p	225.3656f	225.7989f
cstot	202.0596f	1.4101p	202.0596f	1.4101p	280.3598f	281.0088f
cbtot	120.9560f	1.2195p	120.9560f	1.2195p	222.4825f	222.5120f
cgs	142.3153f	810.9613f	142.3153f	810.9613f	167.7166f	168.2802f
cgd	14.3969f	179.4349f	14.3969f	179.4349f	32.3000f	32.3001f

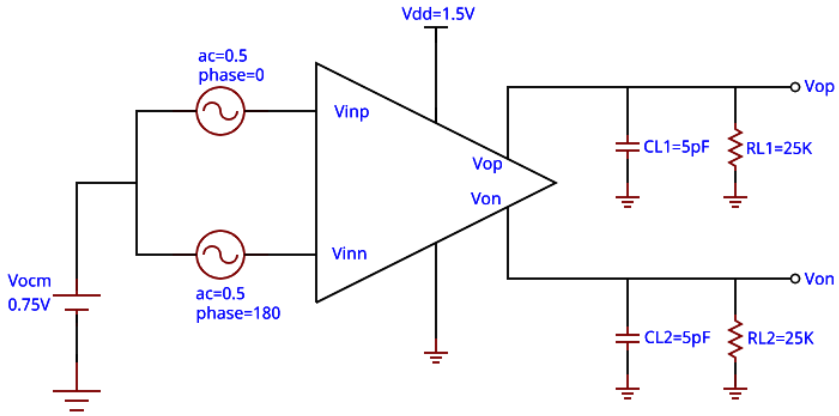
subckt	xop	xop	xop
element	1:mmf3	1:mmf4	1:mmf5
model	0:n_18.1	0:n_18.1	0:p_18.1
region	Saturation	Saturation	Saturation
id	54.1575u	54.7387u	-108.8962u
ibs	-8.764e-21	-8.858e-21	1.011e-20
ibd	-432.6809a	-433.3782a	4.4530f
vgs	556.1564m	557.0528m	-526.7099m
vds	556.1564m	557.0528m	-199.5155m
vbs	0.	0.	0.
vth	425.7977m	425.7877m	-498.7058m
vdsat	144.0214m	144.6498m	-81.3191m
vod	130.3587m	131.2650m	-28.0041m
beta	5.3353m	5.3354m	53.1577m
gam eff	507.4462m	507.4462m	557.0847m
gm	636.7014u	640.6390u	1.9963m
gds	9.8309u	9.9014u	22.6307u
gmb	124.7137u	125.4560u	594.5576u
cdtot	13.6895f	13.6873f	643.8714f
cgtot	42.8425f	42.8493f	1.9059p
cstot	50.8996f	50.9091f	2.1385p
cbtot	30.8487f	30.8451f	1.5812p
cgs	35.9745f	35.9839f	1.4401p
cgd	3.6049f	3.6049f	182.9781f

2. Spice Code

```
*Final Project - A Fully-Differential Two-Stage Op-Amp

.param vdd=1.5V
.param vss=0V
.param vocm=0.75V

.SUBCKT my_op Vinp Vinn vdd vss vop von vocm

*Bias
MMB3 net5 net5 VDD VDD p_18 W=60u L=1u m=10

*Core Differential Amplifier
MM1 net41 Vinp net16 net16 p_18 W=10u L=0.4u m=10
MM2 net47 Vinn net16 net16 p_18 W=10u L=0.4u m=10
MM3 net41 net53 VSS VSS n_18 W=10u L=0.6u m=1
MM4 net47 net53 VSS VSS n_18 W=10u L=0.6u m=1
MM5 net16 net5 VDD VDD p_18 W=50u L=0.7u m=10
MM6 Von net47 VSS VSS n_18 W=40u L=0.6u m=1
MM7 Von net5 VDD VDD p_18 W=50u L=0.4u m=10
MM8 Vop net41 VSS VSS n_18 W=40u L=0.6u m=1
MM9 Vop net5 VDD VDD p_18 W=50u L=0.4u m=10

*Common Mode Feedback
MMF1 net55 VOCM net36 net36 p_18 W=10u L=0.4u m=9
MMF2 net53 net33 net36 net36 p_18 W=10u L=0.4u m=9
MMF3 net55 net55 VSS VSS n_18 W=10u L=0.6u m=1
MMF4 net53 net53 VSS VSS n_18 W=10u L=0.6u m=1
MMF5 net36 net5 VDD VDD p_18 W=50u L=0.7u m=10

*Bias
Rb net5 VSS 10K

*Core Differential Amplifier
RZ1 Vop net1 3.8K
CC1 net1 net41 3pF
RZ2 Von net2 3.8K
CC2 net2 net47 3pF

*Common Mode Feedback
RCM1 Vop net33 50K
RCM2 Von net33 50K

.ENDS
```

3. Simulations and Calculations

3.1 Open-loop differential mode AC response



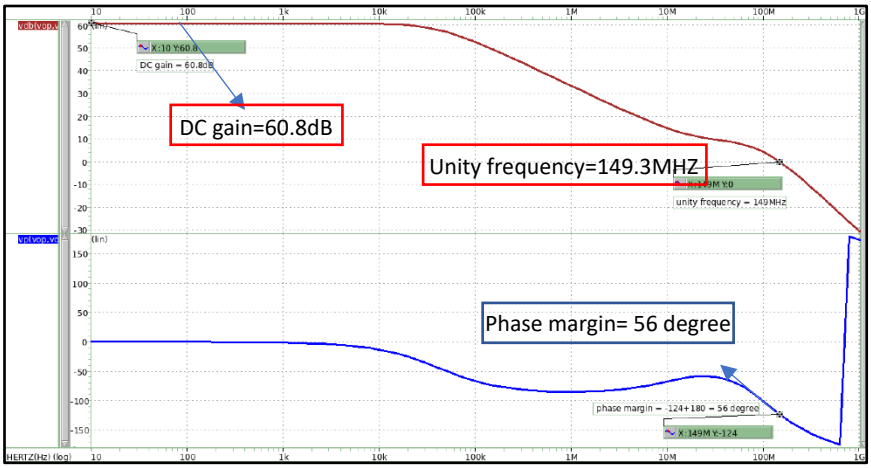


Fig 2 AC response

```
****** ac analysis tnom=  25.000 temp=  25.000 ******
dcgain_in_db=  60.8249      at=  10.0000
            from=  10.0000      to=   1.0000g
dcgain=   1.0996k     at=  10.0000
            from=  10.0000      to=   1.0000g
unity_frequency= 149.3282x
phase=-123.3693
phase_margin=  56.6307
```

Fig 3 ac command result

```
****      small-signal transfer characteristics

     v(vop,von)/vinp                           =    1.0996k
     input resistance at              vinp     =  1.000e+20
     output resistance at v(vop,von)           =   17.1147k
```

Fig 4 .tf command result

input = 0:vac output = v(vop,von)

poles (rad/sec)		poles (hertz)	
real	imag	real	imag
-265.858k	0.	-42.3126k	0.
-71.4383x	0.	-11.3698x	0.
-173.386x	440.615x	-27.5953x	70.1260x
-173.386x	-440.615x	-27.5953x	-70.1260x
-174.997x	0.	-27.8516x	0.
-555.540x	281.577x	-88.4170x	44.8144x
-555.540x	-281.577x	-88.4170x	-44.8144x
-1.14315g	-575.912x	-181.938x	-91.6592x
-1.14315g	575.912x	-181.938x	91.6592x
-1.19201g	0.	-189.715x	0.
-3.74192g	173.940x	-595.545x	27.6835x
-3.74192g	-173.940x	-595.545x	-27.6835x

zeros (rad/sec)		zeros (hertz)	
real	imag	real	imag
-71.2974x	0.	-11.3473x	0.
-99.2178x	0.	-15.7910x	0.
-173.720x	-440.956x	-27.6484x	-70.1803x
-173.720x	440.956x	-27.6484x	70.1803x
-174.097x	440.857x	-27.7084x	70.1646x
-174.097x	-440.857x	-27.7084x	-70.1646x
-174.715x	47.8862k	-27.8067x	7.62133k
-174.715x	-47.8862k	-27.8067x	-7.62133k
-1.14281g	574.974x	-181.883x	91.5099x
-1.14281g	-574.974x	-181.883x	-91.5099x
-1.14589g	-575.568x	-182.374x	-91.6044x
-1.14589g	575.568x	-182.374x	91.6044x
-1.19220g	0.	-189.744x	0.
-3.74198g	174.062x	-595.555x	27.7028x
-3.74198g	-174.062x	-595.555x	-27.7028x
-3.74208g	-174.218x	-595.570x	-27.7276x
-3.74208g	174.218x	-595.570x	27.7276x
26.4238g	0.	4.20548g	0.
127.687g	0.	20.3221g	0.

Fig 5 poles and zeros

Discussion the movement of poles/zeros after compensation.

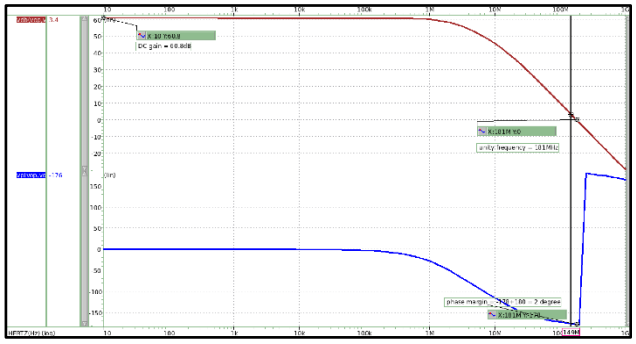


Fig 7 before compensation

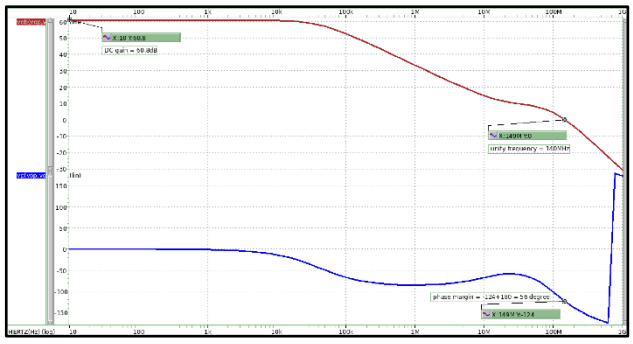


Fig 6 after compensation

上面兩張圖，左圖為 compensation 前，右圖為 compensation 後。
從這兩張圖的差別可看出，未補償前的 unity frequency 較大，相應的 phase margin 也非常小(發散邊緣)，只有 1degree。而補償後的圖，整體 poles and zeros 往左移，主極點的位置更靠左邊，雖然 unity frequency 變小了，但 phase margin 變大許多，使電路處於穩定的狀態，達到補償目的。

Hand Calculation:

gm1	**951.7299μ**
ro1	**148.668K**
ro3	**99.194K**
gm8	**2.2695m**
ro8	**32.847K**
ro9	**37.85K**
R_L	**25K**
R_{CM}	**50K**
RZ1	**3.8K**

$$A_d = gm1 \times (ro1//ro3) \times gm8 \times (ro8//ro9//R_L//R_{CM})$$

$$= 951.7299\mu \times 59.496K \times 2.2695m \times 8.557K = 1.0996K(\frac{V}{V})$$

$$pole1 = \frac{1}{2\pi \times (ro1//ro3) \times gm8 \times (ro8//ro9//R_L) \times C_C}$$

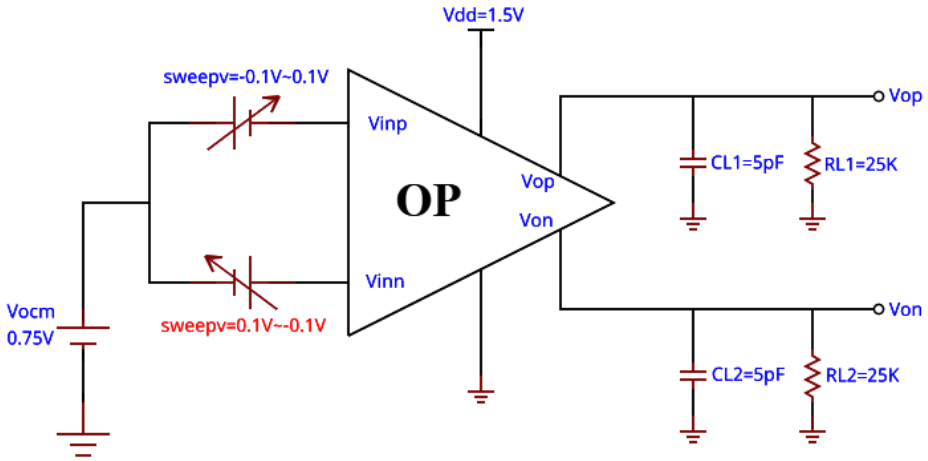
$$= \frac{1}{2\pi \times 36.248K \times 6.105m \times 5.348K \times 5p} = 38.058KHz$$

$$pole2 = \frac{1}{2\pi C_L \times (ro8//ro9//R_L//R_{CM})} = \frac{1}{2\pi \times 5p \times 8.557K} = 37.2MHz$$

$$zero = \frac{1}{2\pi \times C_C \times (\frac{1}{gm8} - RZ1)} = \frac{1}{2\pi \times 3.8p \times (-3.359K)} = -15.792MHz$$

	Simulation	**Hand Calculate**	**error**
Ad(V/V)	1.0996K	1.0996K	0%
Pole1(Hz)	42.313K	38.058K	10.056%
Pole2(Hz)	27.85M	37.2M	33.57%
Zero(Hz)	15.79M	15.792M	0.013%

3.2 Open-loop differential mode DC sweep



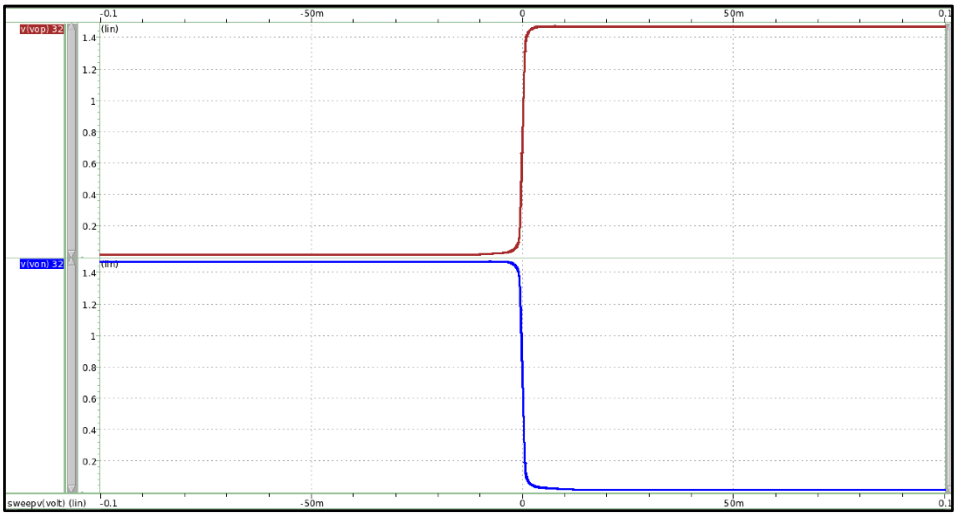


Fig 8 Vop&Von seperate dc sweep waveview

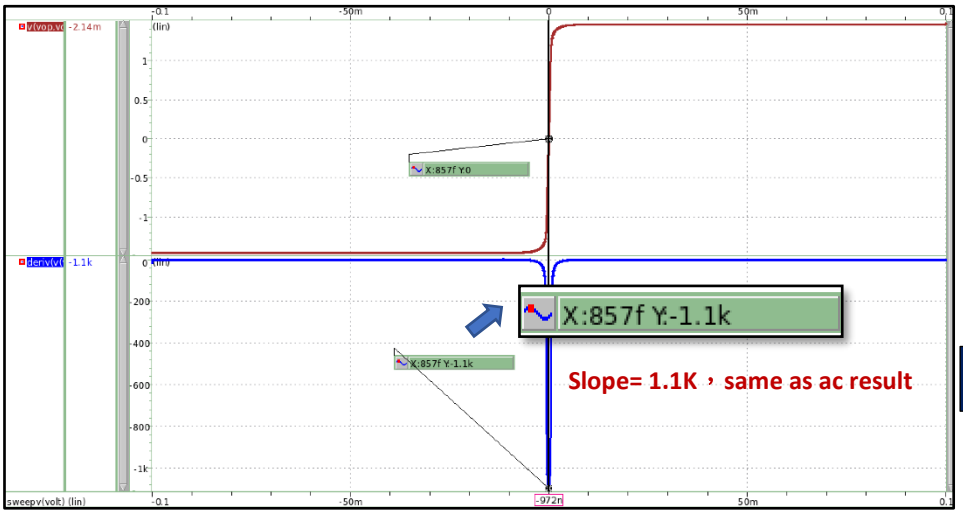
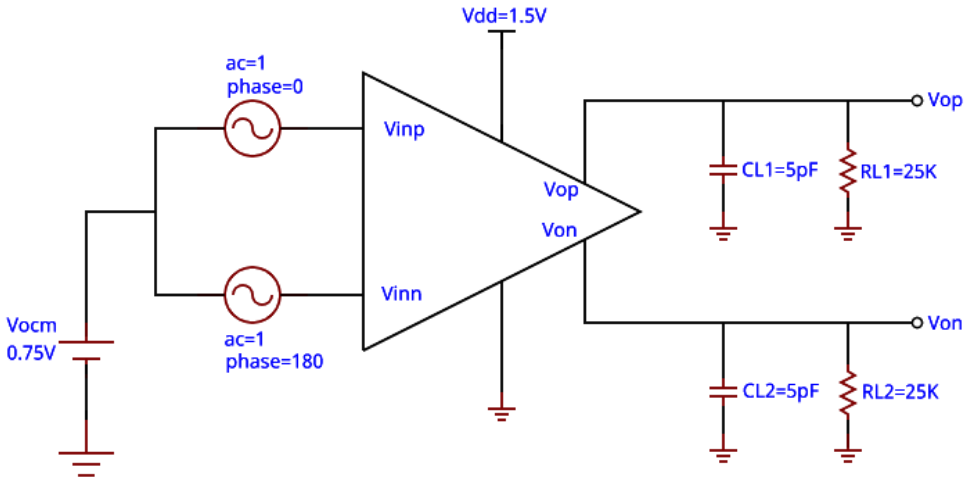


Fig 9 differential output and its derivation

3.3 Open-loop common mode AC response



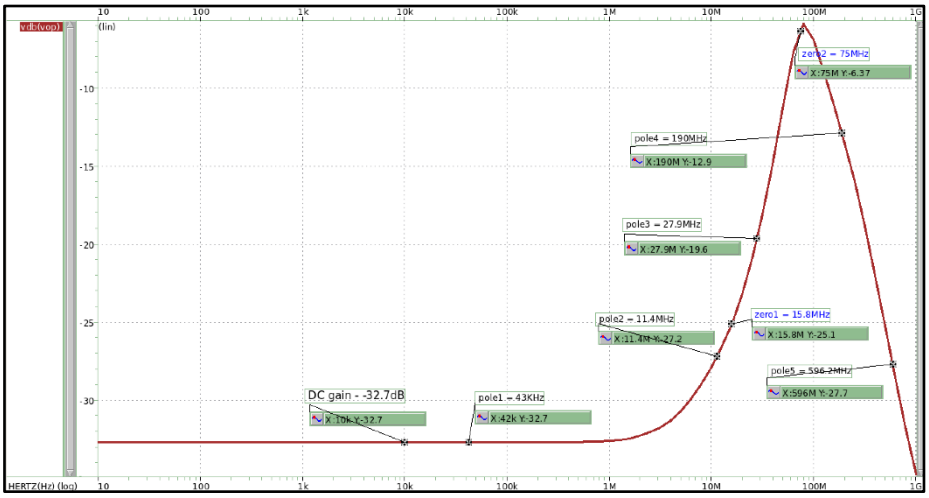


Fig 10 magnitude response with poles and zeros

```
****     small-signal transfer characteristics

    v(vop)/vac                                =    23.1406m
    input resistance at              vac      =   1.000e+20
    output resistance at v(vop)               =     4.2836k
```

Fig 11 tf command result

Acm= -32.7dB

$$CMRR = 60.8 + 32.7 = 93.5dB$$

input = 0:vac output = v(vop,von)

poles (rad/sec)		poles (hertz)	
real	imag	real	imag
-265.858k	0.	-42.3126k	0.
-71.4383x	0.	-11.3698x	0.
-173.386x	440.615x	-27.5953x	70.1260x
-173.386x	-440.615x	-27.5953x	-70.1260x
-174.997x	0.	-27.8516x	0.
-555.540x	281.577x	-88.4170x	44.8144x
-555.540x	-281.577x	-88.4170x	-44.8144x
-1.14315g	-575.912x	-181.938x	-91.6592x
-1.14315g	575.912x	-181.938x	91.6592x
-1.19201g	0.	-189.715x	0.
-3.74192g	173.940x	-595.545x	27.6835x
-3.74192g	-173.940x	-595.545x	-27.6835x

zeros (rad/sec)		zeros (hertz)	
real	imag	real	imag
-270.154k	-1.24763k	-42.9963k	-198.567
-270.154k	1.24763k	-42.9963k	198.567
-35.5110x	0.	-5.65176x	0.
-109.129x	54.7419x	-17.3684x	8.71244x
-109.129x	-54.7419x	-17.3684x	-8.71244x
-109.153x	-54.8990x	-17.3722x	-8.73744x
-109.153x	54.8990x	-17.3722x	8.73744x
-424.285x	18.6718x	-67.5270x	2.97172x
-424.285x	-18.6718x	-67.5270x	-2.97172x
-550.110x	-269.308x	-87.5527x	-42.8617x
-550.110x	269.308x	-87.5527x	42.8617x
-553.869x	281.560x	-88.1510x	44.8117x
-553.869x	-281.560x	-88.1510x	-44.8117x
-1.15385g	854.505k	-183.641x	135.999k
-1.15385g	-854.505k	-183.641x	-135.999k
-3.70805g	-124.596x	-590.155x	-19.8301x
-3.70805g	124.596x	-590.155x	19.8301x
-3.70826g	124.792x	-590.188x	19.8612x
-3.70826g	-124.792x	-590.188x	-19.8612x
6.61732g	-392.496k	1.05318g	-62.4677k
6.61732g	392.496k	1.05318g	62.4677k
96.3919g	-171.006x	15.3413g	-27.2165x
96.3919g	171.006x	15.3413g	27.2165x

Fig 12 .pz command result

Hand Calculation:

$$\text{Acm} = \text{A1} \times \text{A2} = -\frac{\text{ro4}}{2\text{ro5} + \frac{1}{\text{gm2}}} \times (-\text{gm6} \times (\text{ro9}//\text{ro8}//\text{Rcm}//\text{R}_\text{L}))$$

$$= -1.057 \times 19.42 = 20.527\text{V/V}$$

$$\text{Acms} = \frac{1}{\frac{1}{\text{g}_{\text{m,MF1}}} + (\text{r}_{\text{o,MF5}}//\frac{1}{\text{g}_{\text{m,MF2}}})} \times \frac{1}{\text{g}_{\text{m,MF2}}}$$

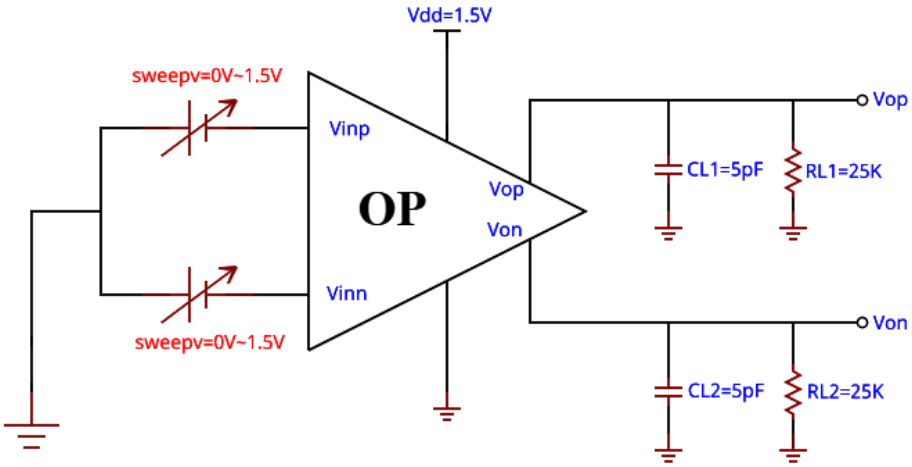
$$= \frac{1}{1.0809\text{K} + (44.188\text{K}//1.072\text{K})} \times 1.072\text{K} = 0.5039\text{V/V}$$

$$\text{Acmc} = 0.5 \times \text{gm5} \times \text{ro4} \times \text{A2} = 1925.47\text{V/V}$$

$$\textbf{common mode gain} = \frac{\textbf{Acm}}{\textbf{1} + \textbf{Acmc} \times \textbf{Acms}} = \textbf{21.1347mV/V}$$

$$\boldsymbol{zero} = \frac{\textbf{1}}{\boldsymbol{2\pi \times ro5 \times Css}} = \textbf{17.43}\boldsymbol{MHz}$$

3.4 Open-loop common mode DC sweep



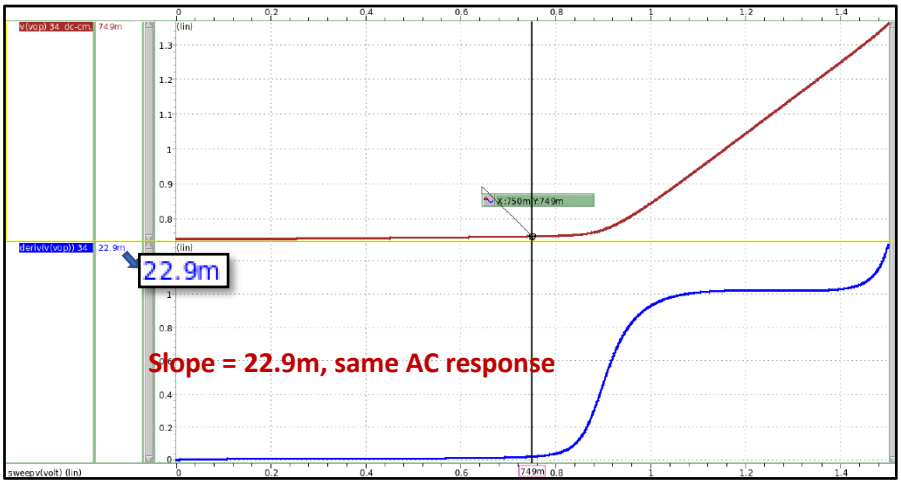
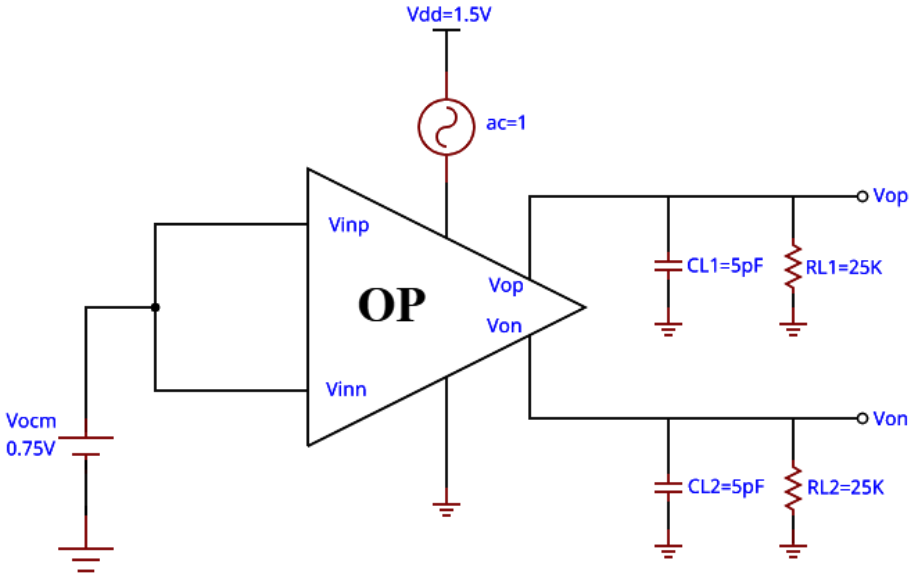


Fig 13 dc sweep

Vinp sweep to 0.75 時，slope = 22.9m，與 AC response 結果相近。

3.5 Open-loop power supply+ AC response



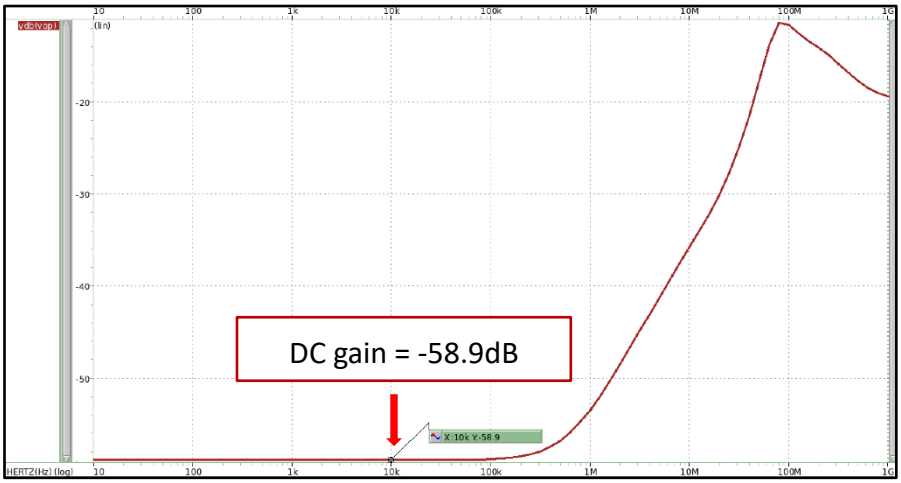
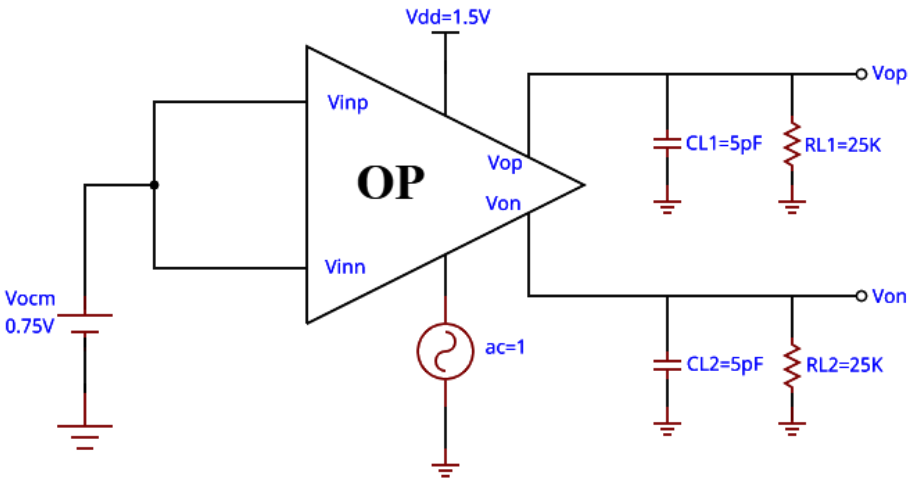


Fig 14 magnitude response of power supply+ gain

DC gain = -58.9dB

$$PSRR+= \frac{A_{dm}}{Avdd} = 60.8dB + 58.9dB = 119.7dB$$

3.6 Open-loop power supply- AC response



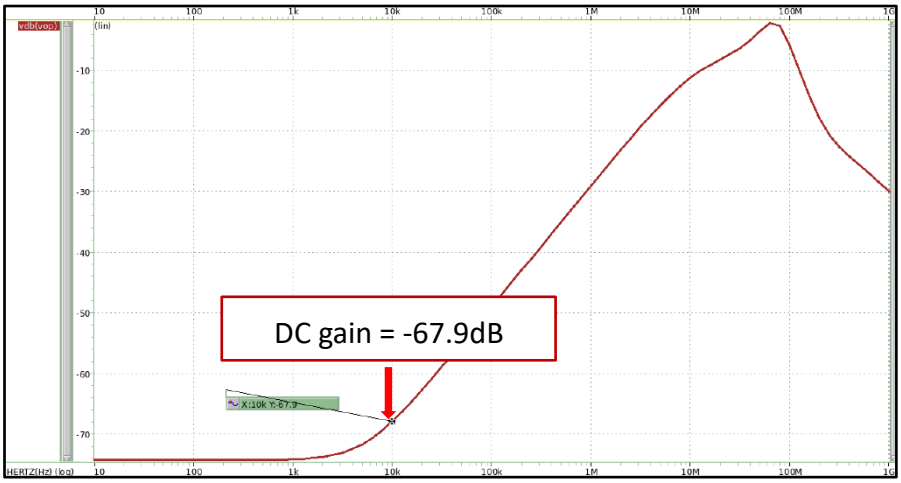
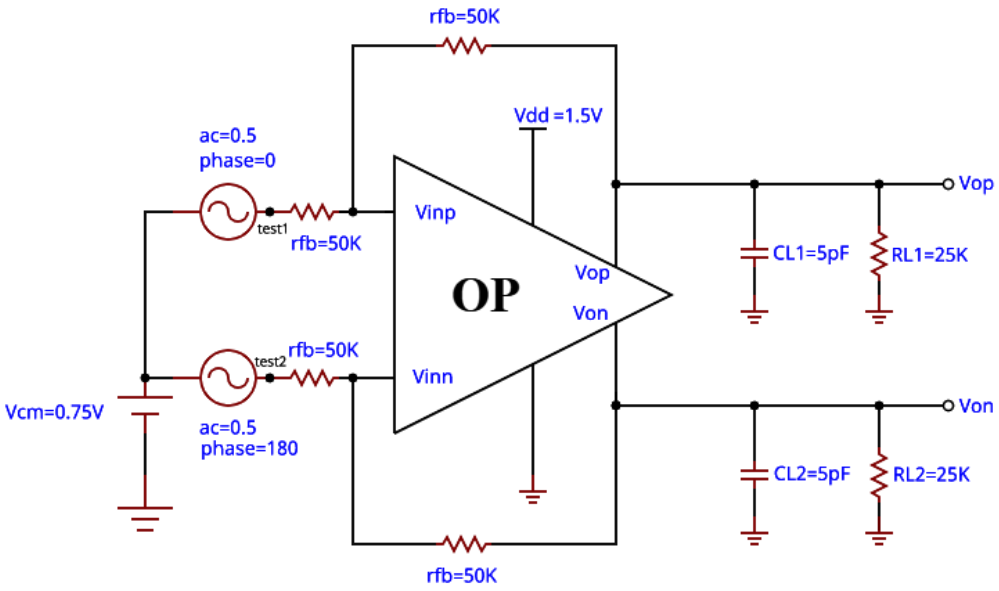


Fig 15 magnitude response of power supply- gain

DC gain = -67.9dB

$$\mathrm{PSRR}-=\frac{\mathrm{A_{dm}}}{\mathrm{Avss}}=60.8\mathrm{dB}+67.9\mathrm{dB}=128.7\mathrm{dB}$$

3.7 Closed-loop differential mode AC response



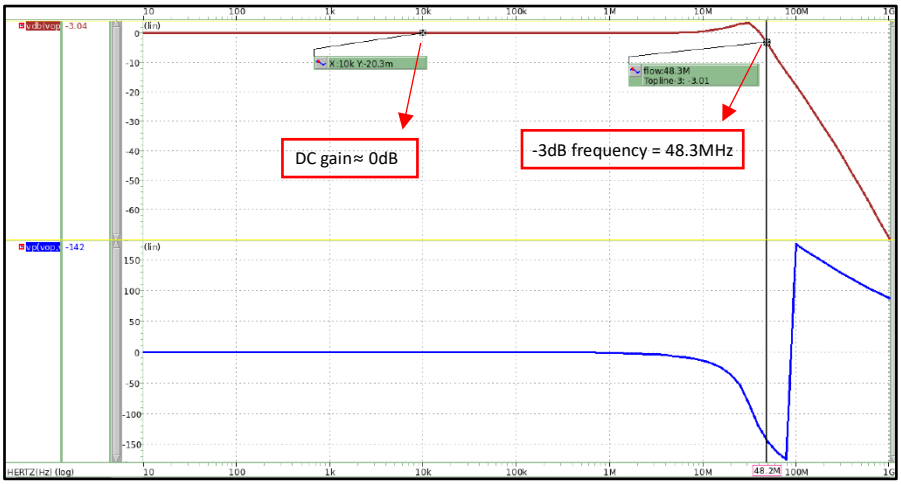


Fig 16 AC magnitude and phase responses

$$Av = \frac{\frac{R_f}{R_i}}{1 + \frac{\frac{R_f}{R_i} + 1}{Ao}} = \frac{1}{1 + \frac{2}{1.0996K}} = 998.184mV/V \approx 0dB$$

$$-3dB\ frequency = -3dBfrequency_{open-loop} \times \left(1 + \beta \times A_{open-loop}\right)$$
$$= 27.8K \times \left(1 + \frac{50K}{50K + 50K} \times 1.8346K\right) = 25.5MHz$$

```
+0:test1    = 750.0000m 0:test2    = 750.0000m 0:vdd      =   1.5000
+0:vinn     = 749.6803m 0:vinp     = 749.6803m 0:vocm     = 750.0000m
+0:von      = 749.3605m 0:vop      = 749.3605m 0:vss      =   0.
+1:net16    =   1.2943  1:net33    = 749.3605m 1:net36    =   1.3005
+1:net41    = 534.4083m 1:net47    = 534.4083m 1:net5     = 973.2901m
+1:net53    = 557.0580m 1:net55    = 556.1512m
```

Fig 17 node voltages

```
****      small-signal transfer characteristics

     v(vop,von)/vac                                =  997.8740m
     input resistance at                vac        =  1.000e+20
     output resistance at v(vop,von)               =   31.0685
```

Fig 18 .tf command result

Discussion:

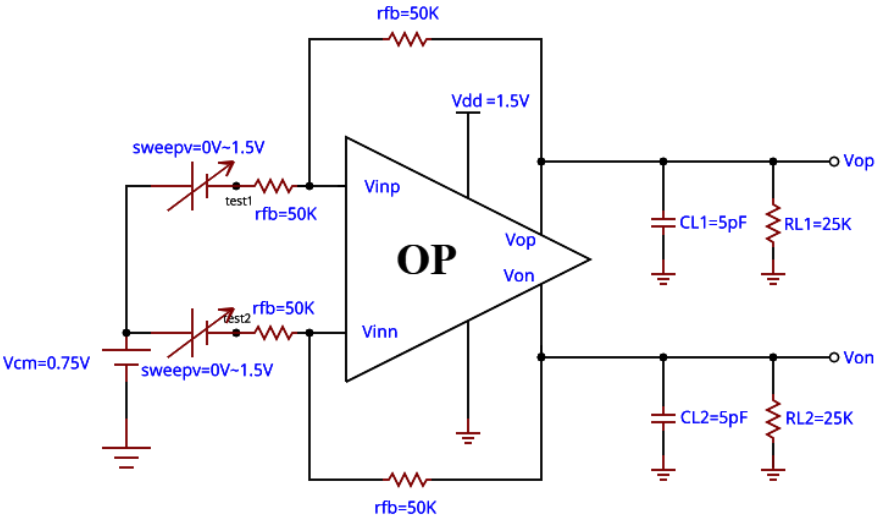
$$Av = \frac{\frac{R_f}{R_i}}{1 + \frac{\frac{R_f}{R_i} + 1}{Ao}} = \frac{1}{1 + \frac{2}{1.0996K}} = 998.184mV/V$$

$$-3dB\ frequency = -3dBfrequency_{open-loop} \times \left(1 + \beta \times A_{open-loop}\right)$$

$$= 42.2K \times \left(1 + \frac{50K}{50K + 50K} \times 1.0996K\right) = 23.24MHz$$

	Simulation	Hand Calculate	Error
Av	997.874m	998.184mV	0.031%
-3dB frequency	48.3MHz	23.24MHz	51.88%

3.8 Closed-loop differential mode DC sweep



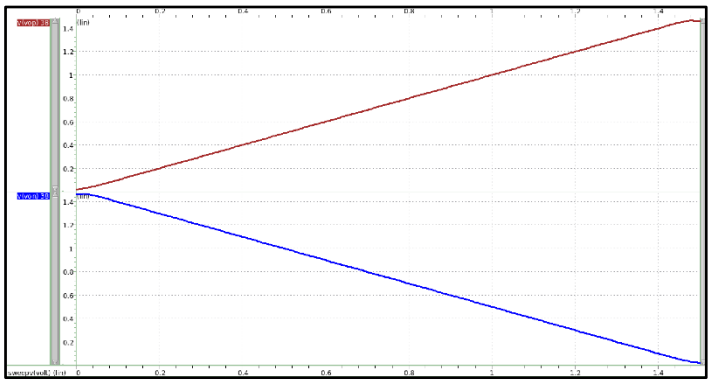


Fig 19 single-ended output vop and von

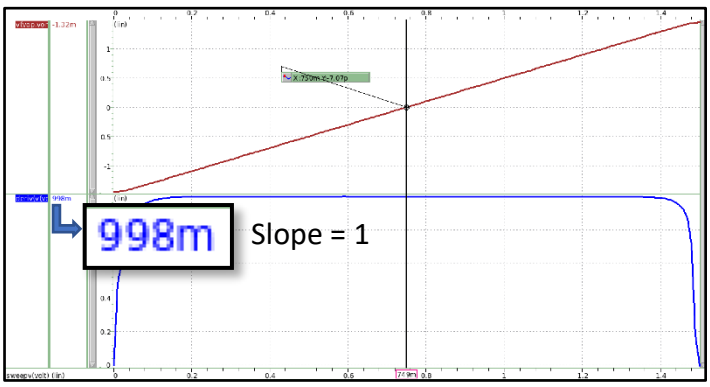


Fig 20 differential output and its derivation

Compare gain with AC response:

AC response gain = 998mV/V，same as the slope value。

3.9 Closed-loop distortion simulation

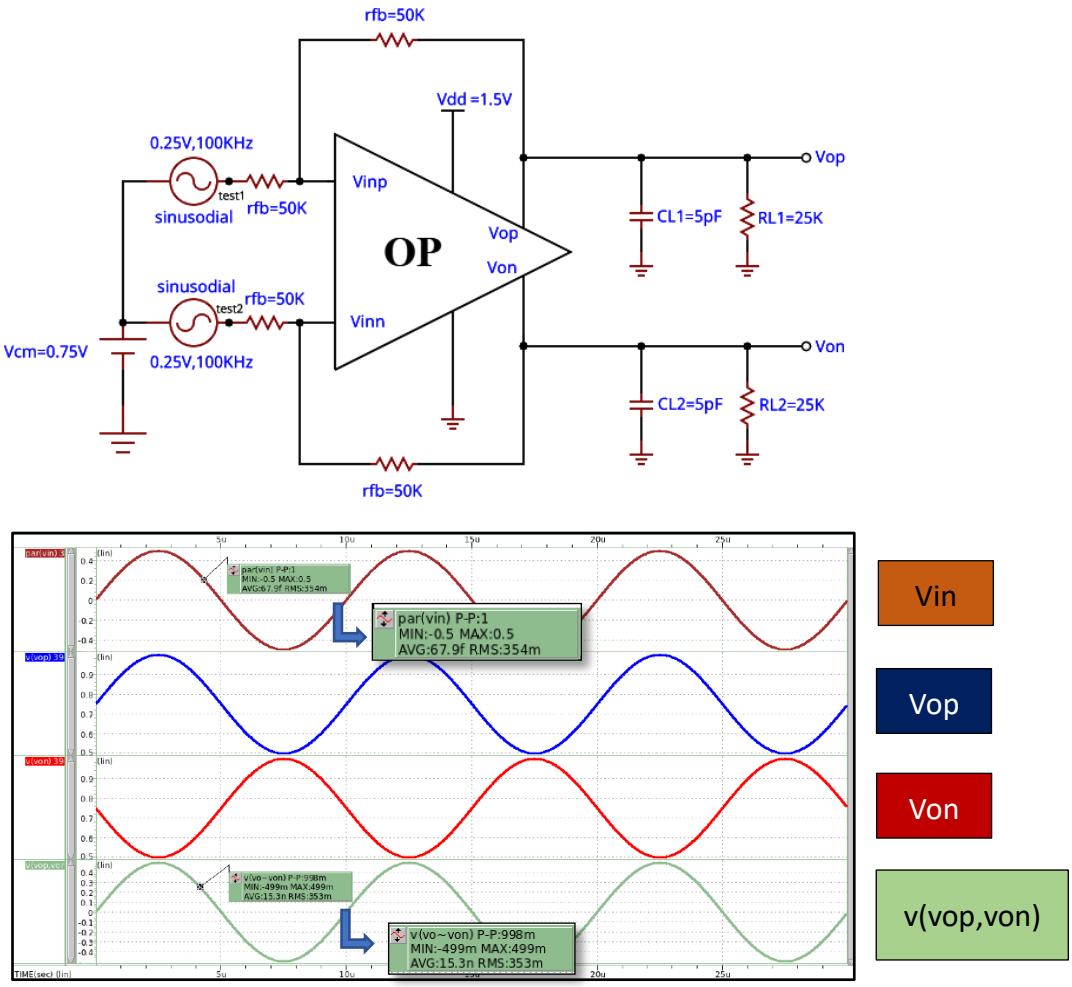


Fig 21 single-ended and differential output

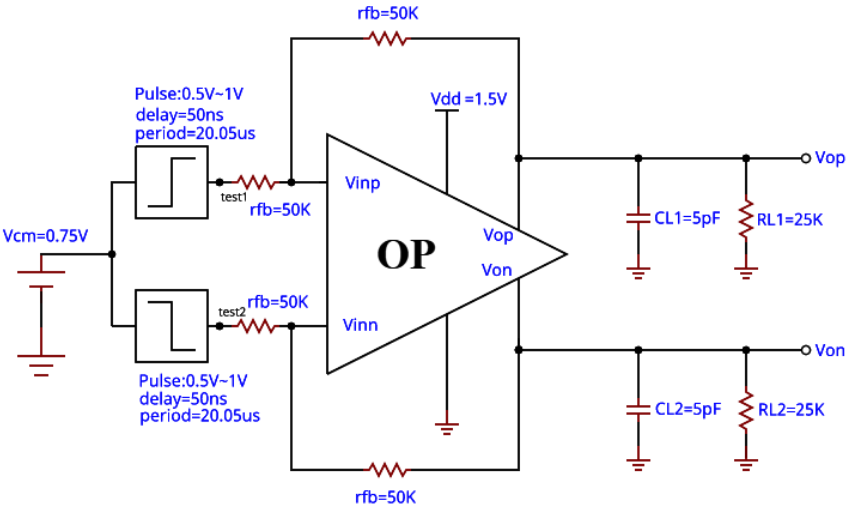
Closed loop gain = 1，所以當輸入一 1V differential step inputs 訊號時，output 輸出 peak to peak 也會是 1V，上圖結果 OUTPUT 訊號 peak to peak 為 999mV。

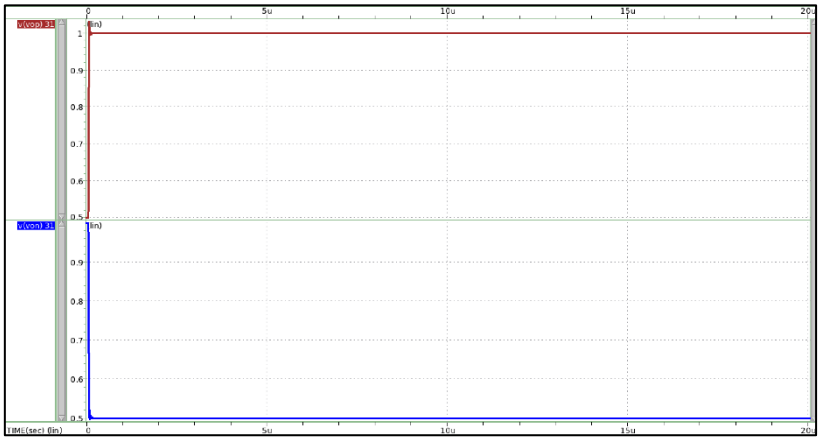
```
fourier components of transient response v(vop,von)
dc component =  -78.3234p

harmonic frequency  fourier    normalized phase      normalized
no       (hz)       component  component  (deg)      phase (deg)
1         100.0000k  498.9225m    1.0000   -90.2521     0.
2         200.0000k  151.6860p  304.0273p  -11.8053    78.4468
3         300.0000k    3.6679u    7.3517u  -63.2540    26.9981
4         400.0000k  153.5593p  307.7820p  153.0875   243.3395
5         500.0000k   84.5843n  169.5340n  127.0400   217.2921
6         600.0000k  162.1264p  324.9530p  -33.4215    56.8306
7         700.0000k    4.5108n    9.0411n  -62.9249    27.3272
8         800.0000k  184.6616p  370.1207p  142.5667   232.8188
9         900.0000k    2.1194n    4.2480n   93.0135   183.2656

total harmonic distortion =   0.000735368  percent
```

Fig 22 THD result of differential output

THD=0.0007% = -102.67dB

3.10 Closed-loop step response

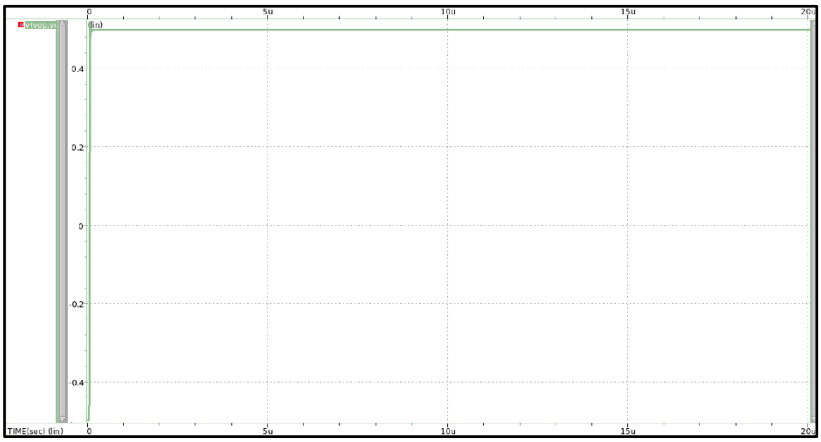




Vop

Von

Fig 23 single-ended output



v(vop,von)

Fig 24 differential output

➢ Slew Rate+ and Settling time+:

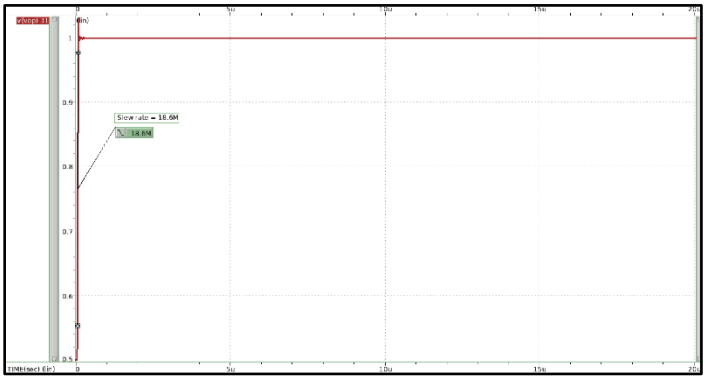


Fig 25 Vop output

```
final1= 998.8299m
hlimit1=   1.0038
llimit1= 993.8357m
htime1=  89.7971n
ltime1=  79.2510n
pos_settling=  39.7971n
```

Fig 26 settling+ time

```
begin1= 499.8851m
srp_v1= 549.7796m
srp_v2= 948.9354m
srp_time=  21.0666n  targ=  76.1640n   trig=  55.0973n
srp_diff= 399.1558m
srp=  18.9473x
```

Fig 27 slew rate+

Slew rate+ = 18.9473M ; Settling time = 39.7971ns

Hand Calculate(slew rate+):

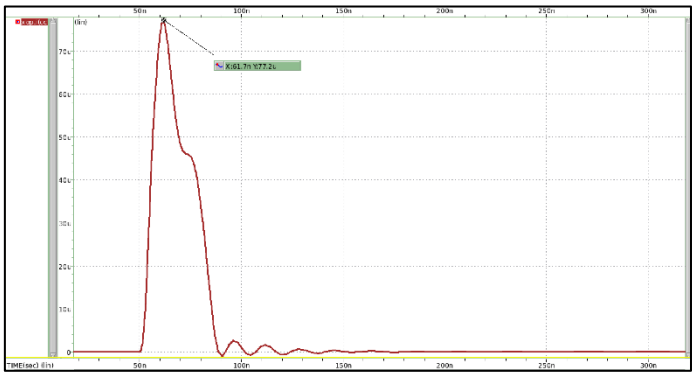


Fig 28 Cc1 上流經電流

$$Slew\ Rate = \frac{77.2\mu}{3p} = 25.73V/\mu s$$

➢ Slew Rate – and Settling time –:

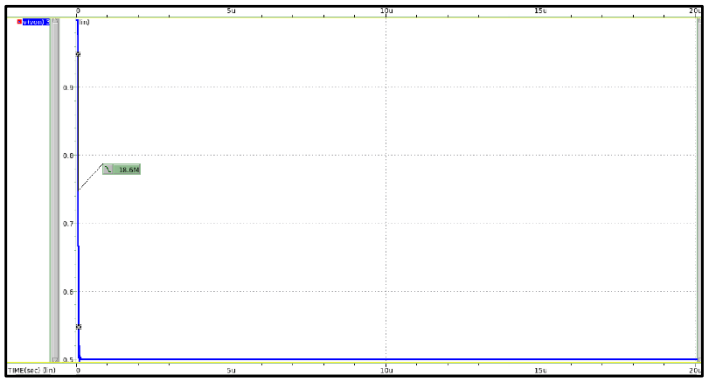


Fig 30 Von output

```
final2= 499.9192m
hlimit2= 502.4188m
llimit2= 497.4196m
htime2= 118.4551n
ltime2=  90.7159n
neg_settling=  68.4551n
```

Fig 29 settling- time

```
begin2= 998.8090m
srn_v1= 948.9200m
srn_v2= 549.8082m
srn_time=  21.1300n  targ=  75.4113n   trig=  54.2813n
srn_diff= 399.1119m
srn=  18.8884x
```

Fig 31 slew rate-

Slew Rate- = 18.8884M ; settling time = 68.4551ns

Hand Calculate(slew rate-):

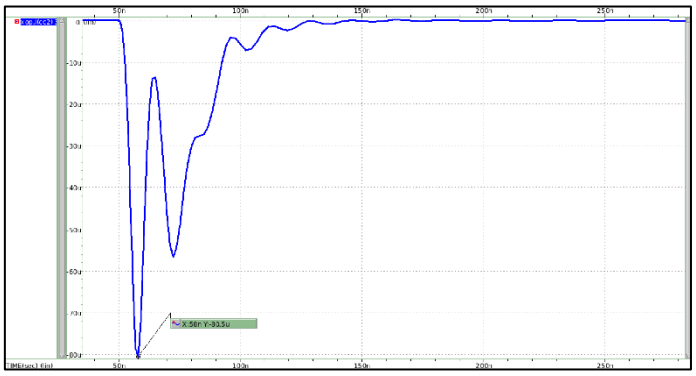
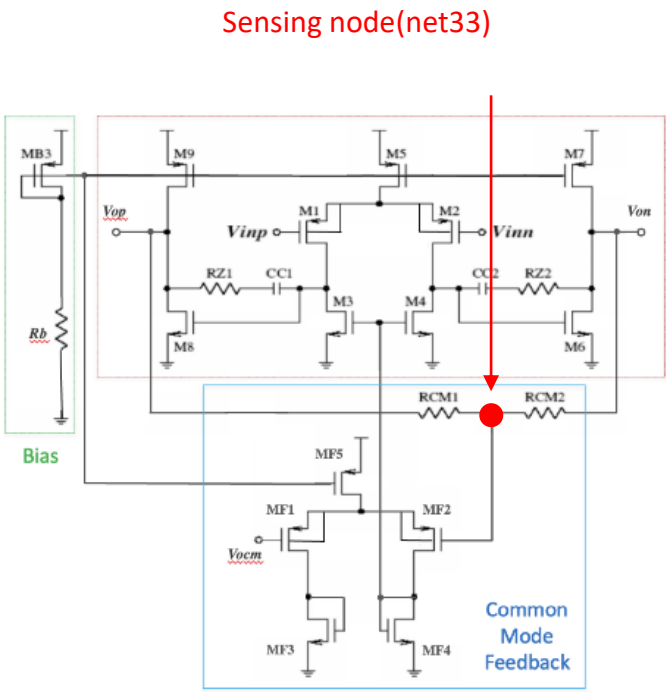


Fig 32 Cc2 上流經電流

$$Slew\ Rate = \frac{-80.5\mu}{3p} = -26.83V/\mu s$$

➢ common mode sensing node waveform:



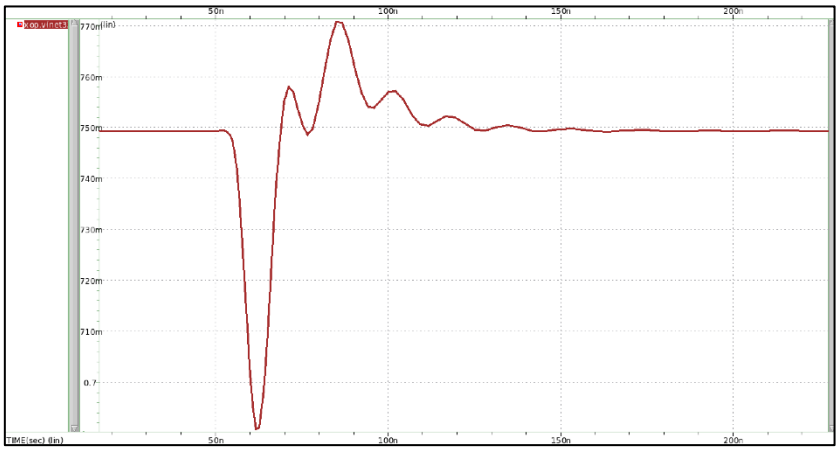
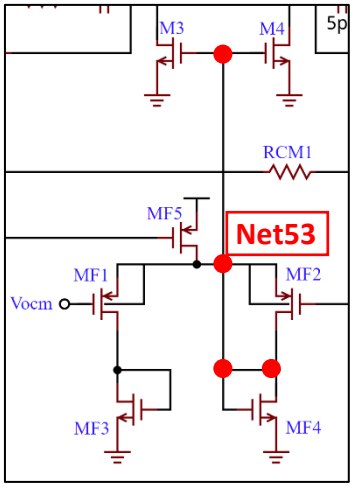


Fig 33 common mode sensing node waveform

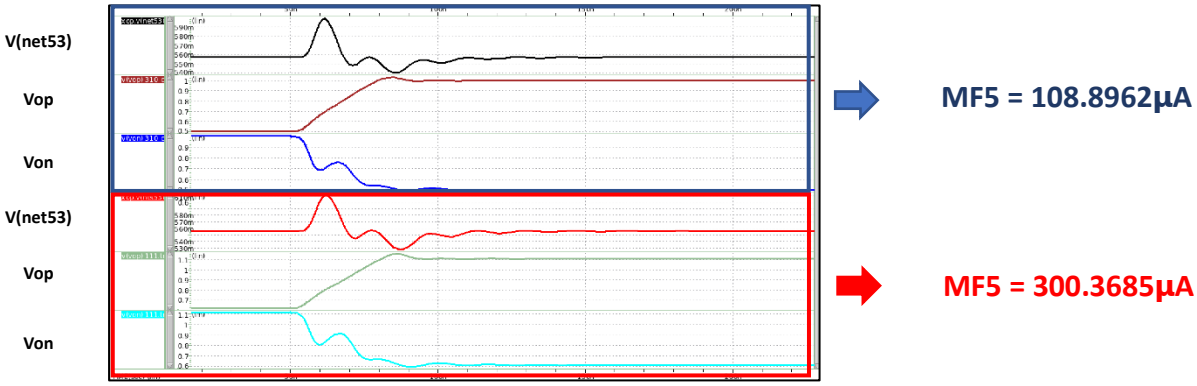
➢ Try to improve the common model settling time. And discuss the CMFB operation during step transient.

Vinn and Vinp 以差模訊號形式輸入進 OP，產生一 differential output，使 sensing node V(net33)在大訊號圖上產生一震盪，從 0.747V(無小訊號輸入時的電壓值)變化一個量值，最終回到穩定。這段震盪時間與 settling time 有關。



左圖為 op 內部 common feedback circuit 的電路，MF4 和 MF2 的電流被上面 M3, M4 的 gate 端電壓控制，所以若提高 feedback circuit MF5 的電流，將全部由 MF1 及 MF3 吸收，電流越大，除非調整上方 M3, M4 的 gate 端電壓，否則將導致電流不均，使其中一端輸出(Vop or Von)的 settling time increase。

下圖為兩種電流大小對應其電壓波形圖:



當電流變大，V(net53)回到穩定的時間更長，進而影響到 Von 的 settling time，也變得更長，在調整過程，Vop 的 settling time 幾乎沒什麼變化，變化的都是 Von，推測原因是提高電流本身並不會對 settling time 有不好的影響，會讓 Von settling time 提高的原因是因兩條電流不平均。

所以，盡可能使 CMFB circuit 左右兩條電流平均，也許是 improve settling time 的方法之一。

4. Performance Table

Design Items	Specifications	Ref Work	My Work
Technology	CIC pseudo 0.18um technology		
Supply Voltage	**1.5V**	**1.8V**	**1.5V**
Vicm,Vocm	**0.75V, 0.75V**	**0.9V, 0.9V**	**0.75V, 0.75V**
Supply current	**<5mA** including bias ckt	1.136mA	0.7274mA
Loading	**5pF/25KΩ (for each output)**	**5pF/10KΩ**	**5pF/25KΩ**
Compensation R, C,	Rc<10KΩ, Cc<10pF	Rc=0.5KΩ, Cc=3pF	Rc=3.8K, Cc=3pF
Open-loop simulation			
DC gain	>60dB,as large as possible	70.6dB	60.8B
G-BW(ft)	>30MHz,as large as possible	64.1MHz	149.3MHz
P.M.	>45 °	54.8 °	56.6 °
C.M.R.R.@10KHz	> 90dB	100.6dB	93.5dB
P.S.R.R.+10KHz	> 90dB	102.0dB	119.7dB
P.S.R.R.-10KHz	> 90dB	103.9dB	128.7dB
Closed-loop simulation			
Differential swing of 1.0 -V (step or sinusoidal)			
Closed loop gain	>-0.1dB @ 10KHz	-0.005dB	-0.018dB
S.R.+(10%~90%)	>15V/μs(single-ended output)	18.9 V/μs	18.9 V/μs
S.R.-(90%~10%)	>15V/μs(single-ended output)	22.7 V/μs	18.9 V/μs
T.H.D.(1.0Vpp@100KHz Sin)	< -60dB	-59dB	-102.67dB
Settling+ (1.0Vpp to 0.5%)	<150ns	240ns	39.8ns
Settling- (1.0Vpp to 0.5%)	<150ns	250ns	68.5ns
FoM:			
GxBW / total bias I	MHz/ mA	56.4	205.4
Settling+ / total bias I	1000 / nsec x mA	3.67	34.6
Settling- / total bias I	1000 / nsec x mA	3.52	20.07

5. Design Concerns

(a) Operation point selection.

因負責提供電的 mos，其 gate 全都與 MB3 的 gate 相接，故第一件事便是決定此點電壓。提高 Rb 時將使 gate 端電壓提高，在設計 Rb 大小時只需防止 MB3 截止，因 MB3 不可能進入 linear region，至於 MB3 的 size，直覺上調大會使流變大，但因調大 size 時，變大的不是只有電流，因為電流變大同時，gate 端電壓也會一起上升(Rb 不變)，根據電流公式會發現，當 pmos VG 上升，其電流會下降，經過幾組數據測試發現普遍調大 size 時，MB3 電流不升反降。考慮到整體電流不宜過大，在設計 Ibias 時，選擇使其小於 0.1mA。

設計完 bias part，便可以開始設計 core differential part 和 common feedback part，以下分別探討:

1. Core differential part:

因題目有指定 RL=25K 掛在輸出端上，根據前面 Ad 公式，ro8、ro9 再大也沒用，因為最後會因與 RL 並聯而整體電阻下降，故在設計時，採用 M6~M9 負責提供大 gm，M1~M4 負責提供大 ro (小 gds)，這樣設計的原因是大 gm 必定搭配大 gds，要同時擁有大 gm 及大 ro 相當困難，且考慮到 supply current 不可太大的關係，本專題選擇此設計方向，最終輸出增益為 65.3dB。

2. common feedback part:

共模增益越小越好，其實設計到夠大的差模增益就是一個很好的兩全其美方式了，因為共模增益公式$\frac{\mathbf{Acm}}{\mathbf{1+Acmc\times Acms}}$ 中，Acm 和差模增益成正比，故越大的差模增益可一定程度上抑制共模增益，而$Acms = \frac{1}{\frac{1}{g_{m,MF1}}+(r_{o,MF5}//\frac{1}{g_{m,MF2}})} \times \frac{1}{g_{m,MF2}}$，在設計時使 $g_{m,MF2} > g_{m,MF1}$，意即 MF2 流經電流大於 MF1 便可使共模增益變小，因 MF2 由 core differential part 的 M3,M4 gate 端電壓決定，因此設計 MF5 size 變得非常重要，應該使 MF5 電流不超過兩倍 MF2 電流為原則下進行設計，以避免 $g_{m,MF2} < g_{m,MF1}$。

(b) Compensation. Please especially address your placement of unity frequency (ft), first non-dominant pole (p2), and zero (LHP or RHP).

電路還未加入補償電阻電容時，其主極點很大，與 first non-dominant pole (p2)很靠近，unity frequency 也很大，雖然 unity frequency 大是好事，但對應的 phase margin 只有 1，使電路非常不穩定，需要靠補償電容和電阻將主極點往左拉，first non-dominant pole 則往右邊拉，避免 unity frequency 因主極點往左移動下降過多。

至於加入的補償電阻及電容應該設計多大可以達到目的，理論上因主極點與電容成反比關係，設計越大的補償電容可使主極點變小許多，但太大的話會影響 slew rate 的表現，可以順便得知 slew rate 與 phase margin 是一個 tradeoff。

考量 slew rate 的關係，電容不可設計太大，若導致補償效果降低的話，這時候變再加入一補償電阻 RZ，但與電容的概念不同，電容是分離主極點與 first non-dominant pole，電阻的功能則是將 zero 移到左半平面，使電路恢復穩定，此補償電阻 RZ 需設計得比$\frac{1}{gm8}$大，才可達到增加 phase margin 的目的，使電路回到穩定狀態。

poles (rad/sec)		poles (hertz)	
real	imag	real	imag
-14.2267x	0.	-2.26425x	0.
-82.6387x	0.	-13.1524x	0.
-178.676x	0.	-28.4372x	0.
215.864x	454.865x	34.3558x	72.3940x
215.864x	-454.865x	34.3558x	-72.3940x
-1.03670g	240.950x	-164.997x	38.3484x
-1.03670g	-240.950x	-164.997x	-38.3484x
-1.22159g	0.	-194.423x	0.
-3.73412g	165.761x	-594.304x	26.3817x
-3.73412g	-165.761x	-594.304x	-26.3817x

Fig 35 before compensation

poles (rad/sec)		poles (hertz)	
real	imag	real	imag
-265.858k	0.	-42.3126k	0.
-71.4383x	0.	-11.3698x	0.
-173.386x	440.615x	-27.5953x	70.1260x
-173.386x	-440.615x	-27.5953x	-70.1260x
-174.997x	0.	-27.8516x	0.
-555.540x	281.577x	-88.4170x	44.8144x
-555.540x	-281.577x	-88.4170x	-44.8144x
-1.14315g	-575.912x	-181.938x	-91.6592x
-1.14315g	575.912x	-181.938x	91.6592x
-1.19201g	0.	-189.715x	0.
-3.74192g	173.940x	-595.545x	27.6835x
-3.74192g	-173.940x	-595.545x	-27.6835x

Fig 34 after compensation

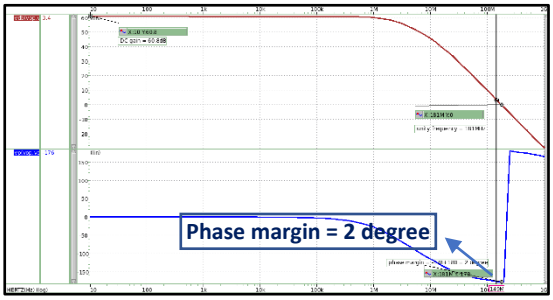


Fig 37 before compensation

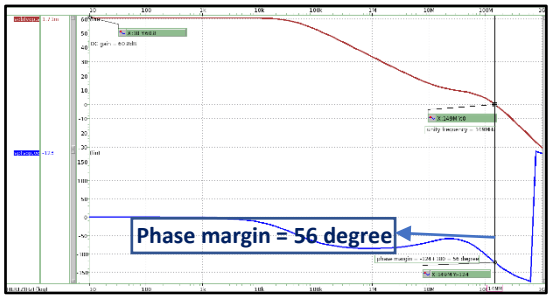


Fig 36 after compensation

左圖為補償前，pole1 and pole2 分別為 2.26MHz 和 13.15MHz，相當靠近，導致其 phase margin 非常小，使電路處於隨時發散的狀態;而右圖為補償後，pole1 and pole2 分別為 42.3KHz 和 11.37MHz，相距很遠，phase margin 也變大許多。

(c) Feedback loop of common mode stabilization. Please compare the loop performance of the common mode and the differential mode signals.

當輸入為 common input 時，決定 CMFB 的電流值及每個 mos 的 size 變得非常重要，其內部有許多小參數會影響共模增益，比方說: $g_{m,MF2}$ 應大於 $g_{m,MF1}$ 以抑制共模增益。

當輸入為 differential input 時，CMFB 在小訊號分析上除了 RCM 的值以外，下方的 circuit 皆對 differential gain 沒有影響，但仍與大訊號分析的 settling time 及 slew rate 有關，在前面也提到過 CMFB 電流分配的重要性，若使 MF1、MF2 兩端電流差距過大，將導致 Von 的 settling time increase。至於 slew rate 的影響，使 CMFB 電流提高原則上可以增加 Slew rate，但代價就是功耗變大，或是增加補償電阻大小也可以提高 slew rate，但會降低 settling time，由此可知 slew rate 與 settling time 也是一個 tradeoff。

(d) How to achieve better FoMs.

增加 FoMs 有幾個要素，降低 supply current 當然是其中一個，還有增加 unity frequency、減少 settling time 也可以提高 FoMs。

Decrease Supply current:

降低 supply current 很直覺也沒什麼其他調整方法，就是縮小每個 mos 的 size 便可使電流變小，但電流變小有許多缺點，最基本的 differential gain 有可能因此過低，或是 slew rate 不夠大等 tradeoff。降低 supply current 到非常低又要確保 OP 的功能性是非常困難的一件事。

Increase unity frequency:

有幾個方法可以提高 unity frequency，其中一個方法是不加入補償電容或是將補償電容設計的小一點，但代價是有可能使電路處於發散邊緣，無法收斂的放大器就是一個震盪器，就如 3.5、3.6 的 PSRR，電路抑制雜訊能力表現將會非常差，使 OP 無法在很多情況運作。另一個方法便是增加電流，靠提高電流強行維持增益同時使 unity frequency 在一定的值以上，代價便是整體功耗增加。

Decrease settling time:

降低 settling 的方法為增加補償電容的大小，但也有代價，無論是 slew rate 還是 unity frequency 都會下降，三者要同時取得平衡，達到最好的總體表現也是需要不斷的調整最終找出最佳的設計。

6. Discussions

6.1 Discuss your experience on this project and the problem during design.

不只是這份project,每次作業要同時滿足老師給予的spec都會發現許多tradeoff,除了第一次作業，其他次作業都不是一次到位。
這份 project 當然是這堂課最難的一次設計，同時符合大訊號與小訊號的 spec，小訊號內部又是這麼多的 tradeoff，要如何設計這麼大的電路，differential gain 夠大、common gain 盡可能的小，同時注意 phase margin 以避免電路發散，每個 mos 都需處於 saturation region，光是小訊號分析就已經很多低方要不斷調整以符合每個條件要求，同時還有大訊號需要考量。令我印象最深刻的是大訊號的 settling time 竟然與小訊號的 phase margin tradeoff，如何設計補償電容值絕對是一大重點，既然加入了補償電容，補償電阻肯定也無法不考慮，光是這兩個元件的 optimize 就花了一段時間。
做完整份 project，我認為我的 supply current 還可以再減少也不至於使電路功能不符合 spec。整體來說有幾個我覺得設計得不錯的地方，包括我的 Vop、Von node level 非常接近 0.5VDD，使得我的 dc transfer curve 非常好看，幾乎是對稱且 reach VDD and gnd，還有 sensing node 的圖形也是非常漂亮，沒有甚麼雜訊感，是一個很漂亮的弦波。

6.2 Please conclude what you get and suggest for this course.

過去大學已經上了許多電子學的課程內容，其中當然包含 OP，在設計 differential gain、common gain、bandwidth、phase margin 等都算是孰悉的，但這學期所學的類比電路除了小訊號的部分，還有大訊號的層面要考慮，使整體設計難度提升，但同時也讓我知道原來 OP 不是只有小訊號，放大能力很強，頻寬非常大就是一個好的 OP，也許 settling time 表現很差導致訊號回到穩定的時間很久，另外，之前完全沒接觸過的就是 T.H.D.，記得當初作業要求電路符合 Total Harmonic Distortion，要不是有上課完全不知道從何下手，記得老師那時候是以音響為例，表示擁有好的放大能力卻沒有好的雜訊抑制能力，音響便會動不動就破音，讓我更加體會市面上真正在販售的產品與目前所學的電路設計也是有許多相關之處，比起大學，修讀研究所課程很大的一個差別是更加了解為何這樣設計?為何要符合這些 spec?而不是背公式算答案這樣抽象的電路概念。