**國立清華大學**

**Analog Circuit Design**



Homework 1

Common Source Mosfet

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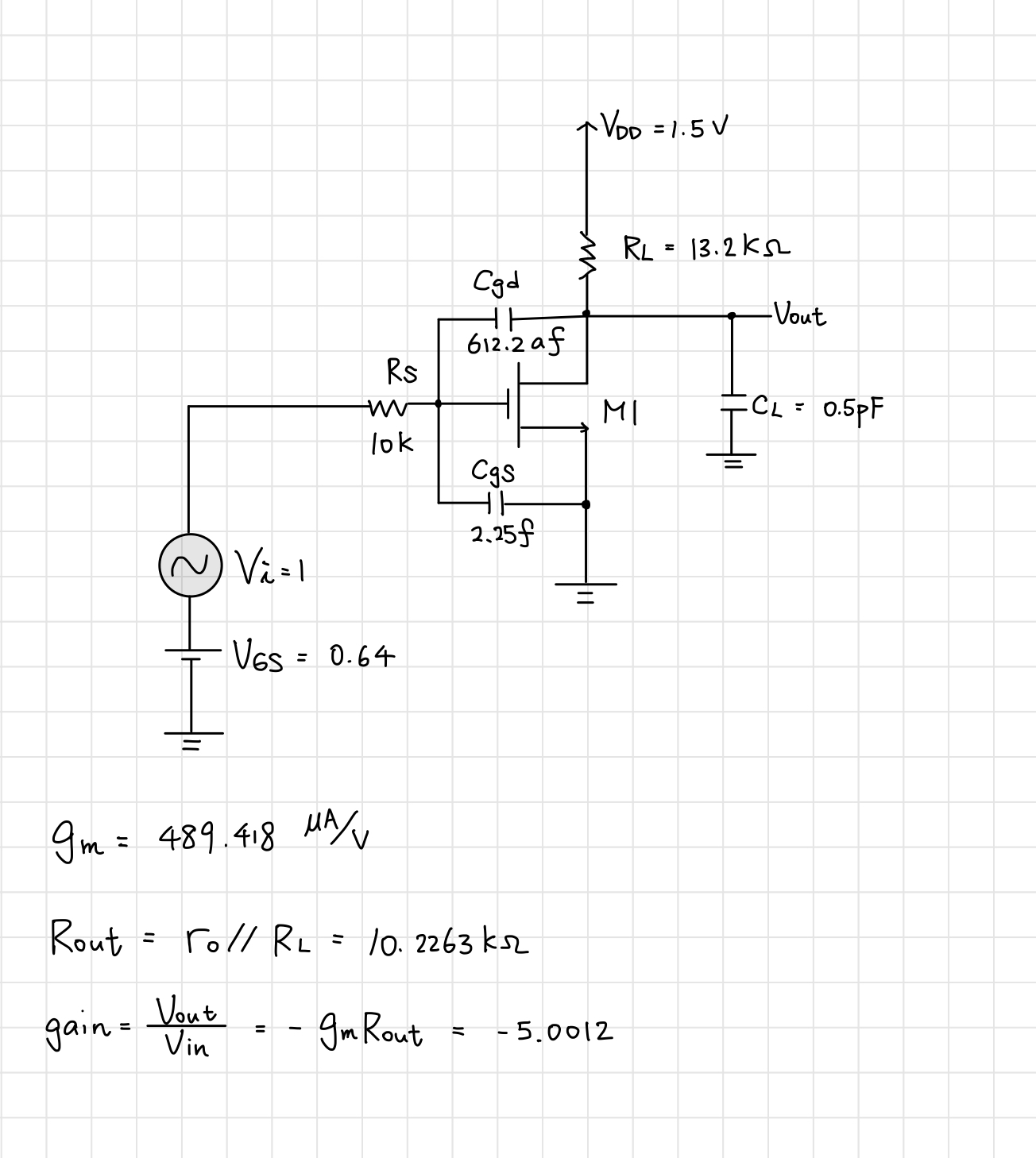
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電路設計圖

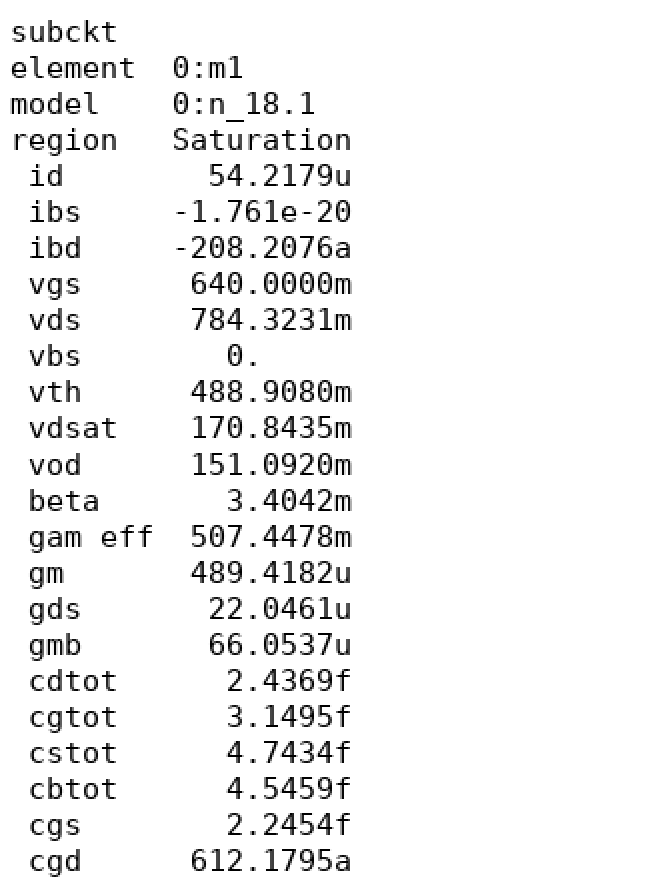


Operation Points

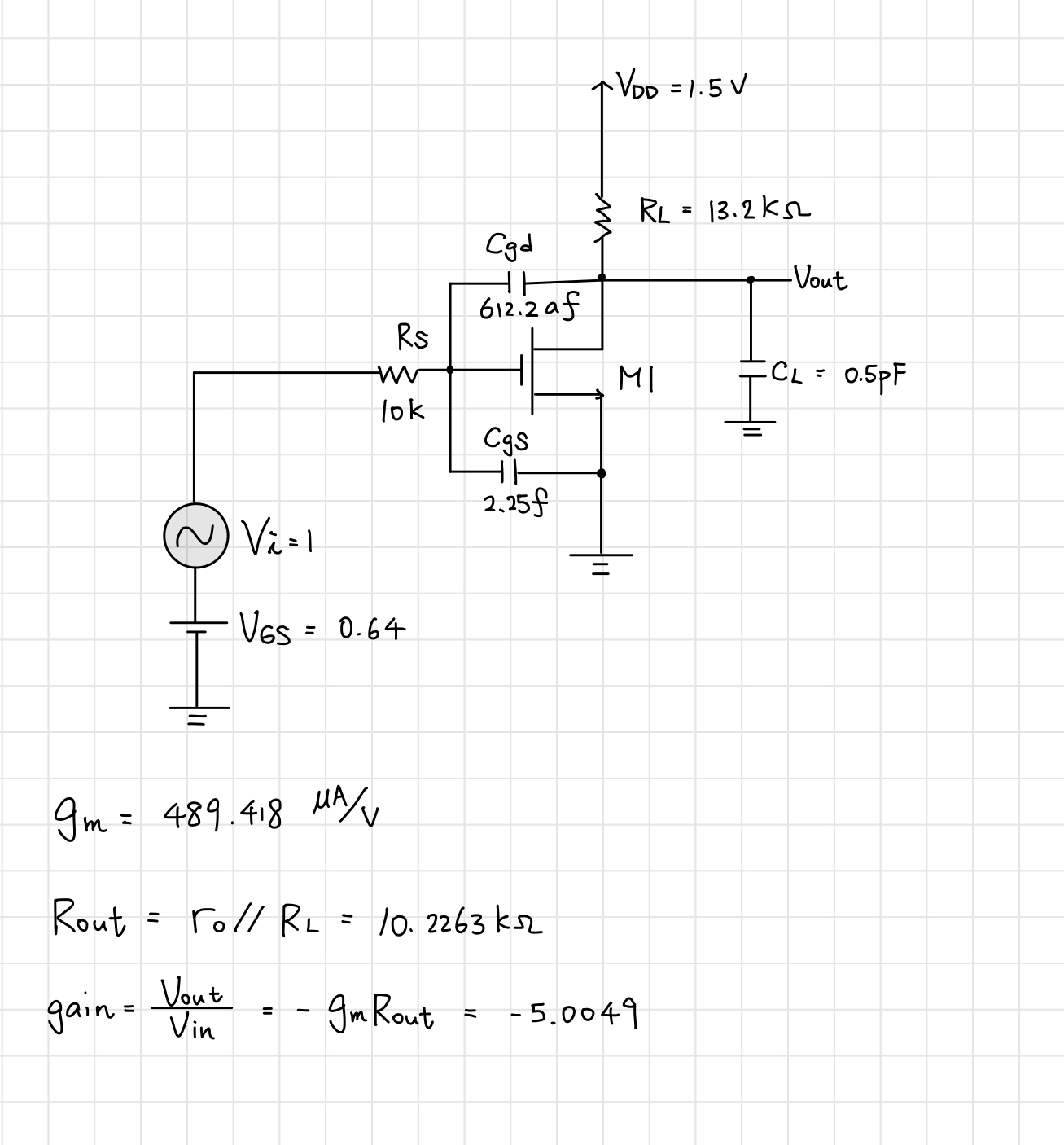
## Please design the device size of M1, load resistance RL, and the bias voltage VGS, to make the small signal voltage gain (vout /vi) equal to 5.0 (V/V)

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Design parameters | VGS | W | L | m | RL |
| Design value | 0.64 | 0.85u | 0.18u | 2 | 13.2K |

## Please use .op command to print out its small signal parameters.

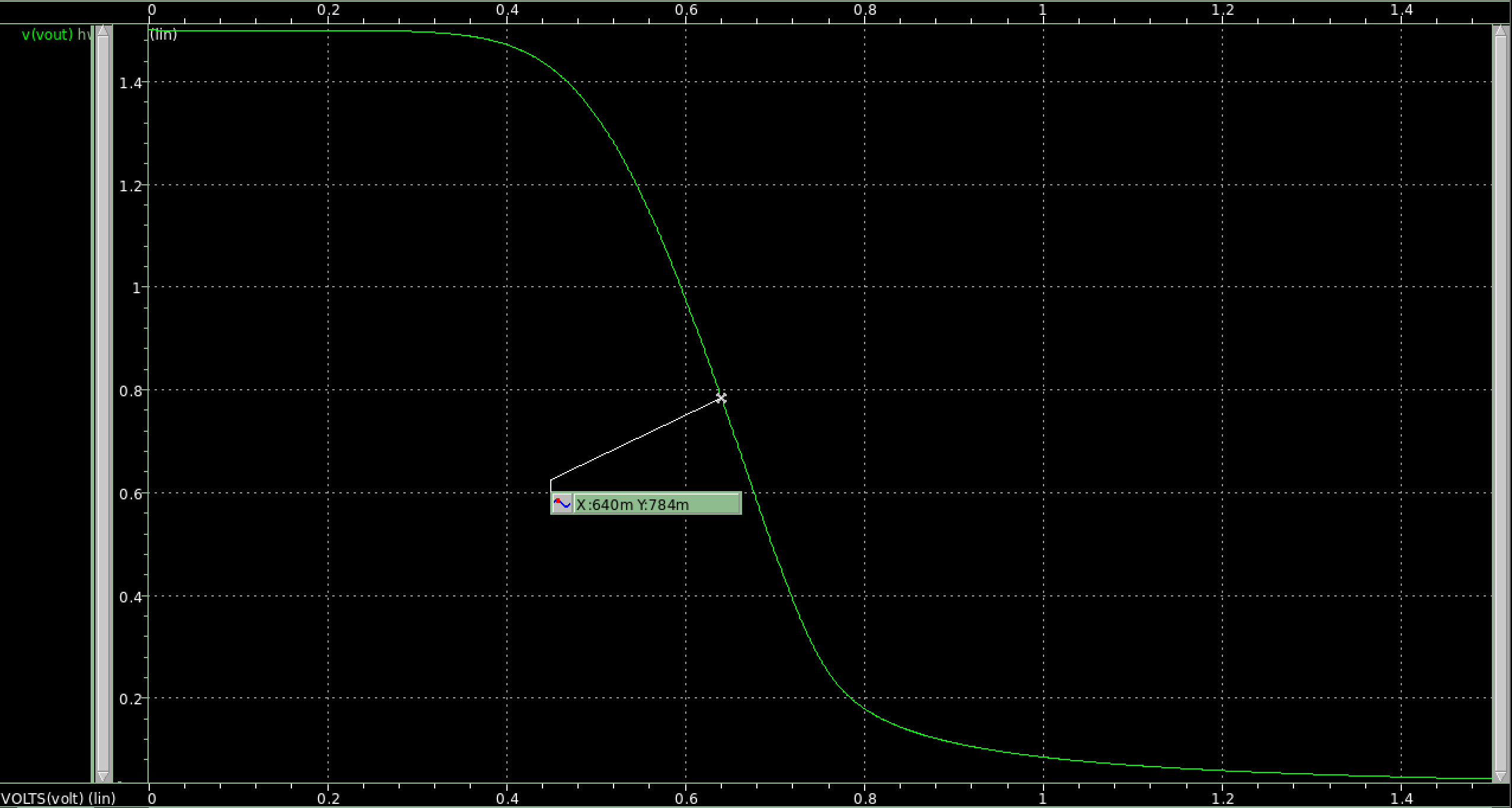


## Please hand-calculate the gain value using SPICE parameters

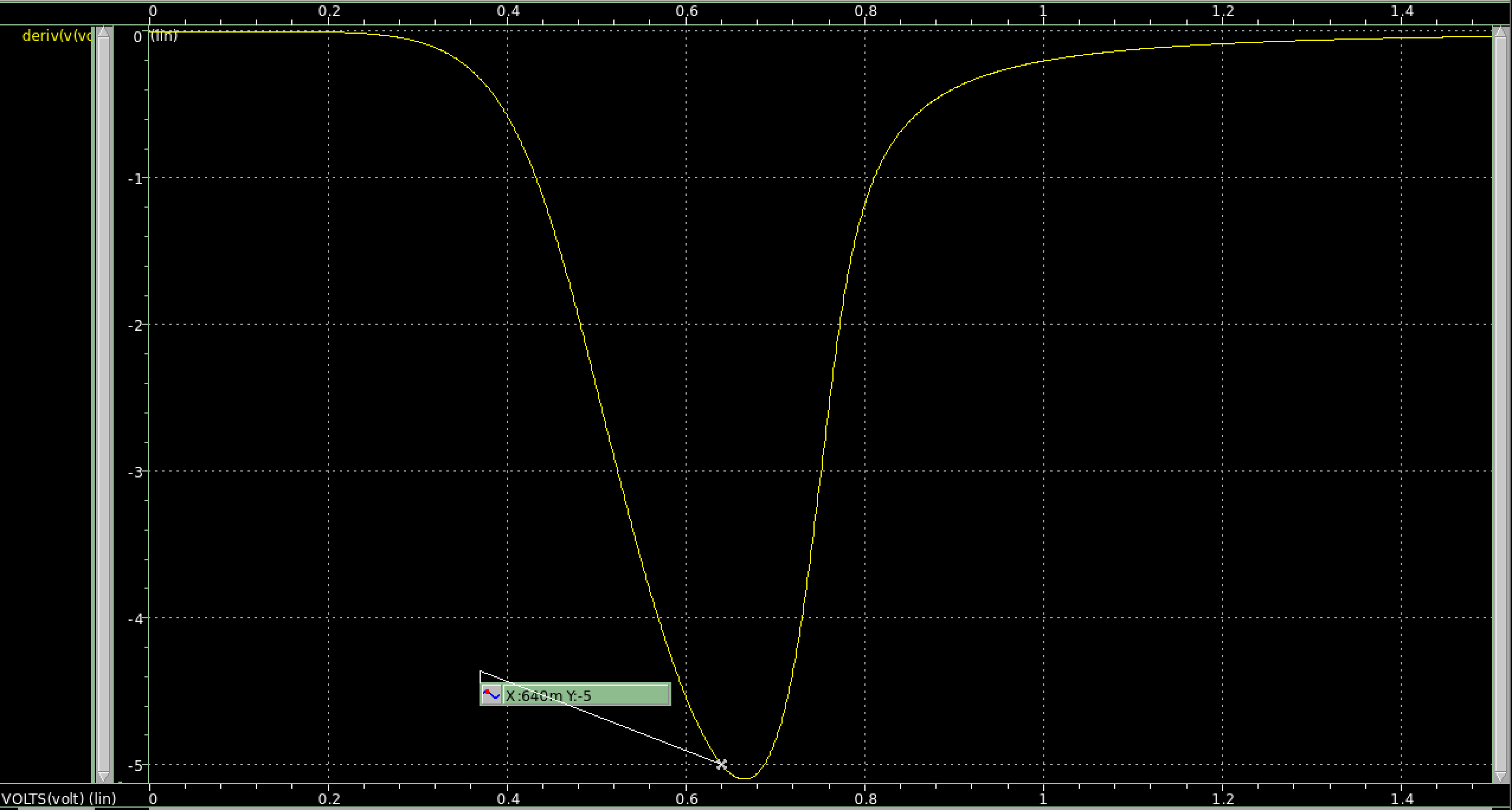


DC Sweep

## Please sweep the gate DC voltage to draw its DC transfer curve. And find the slope at the selected VGS



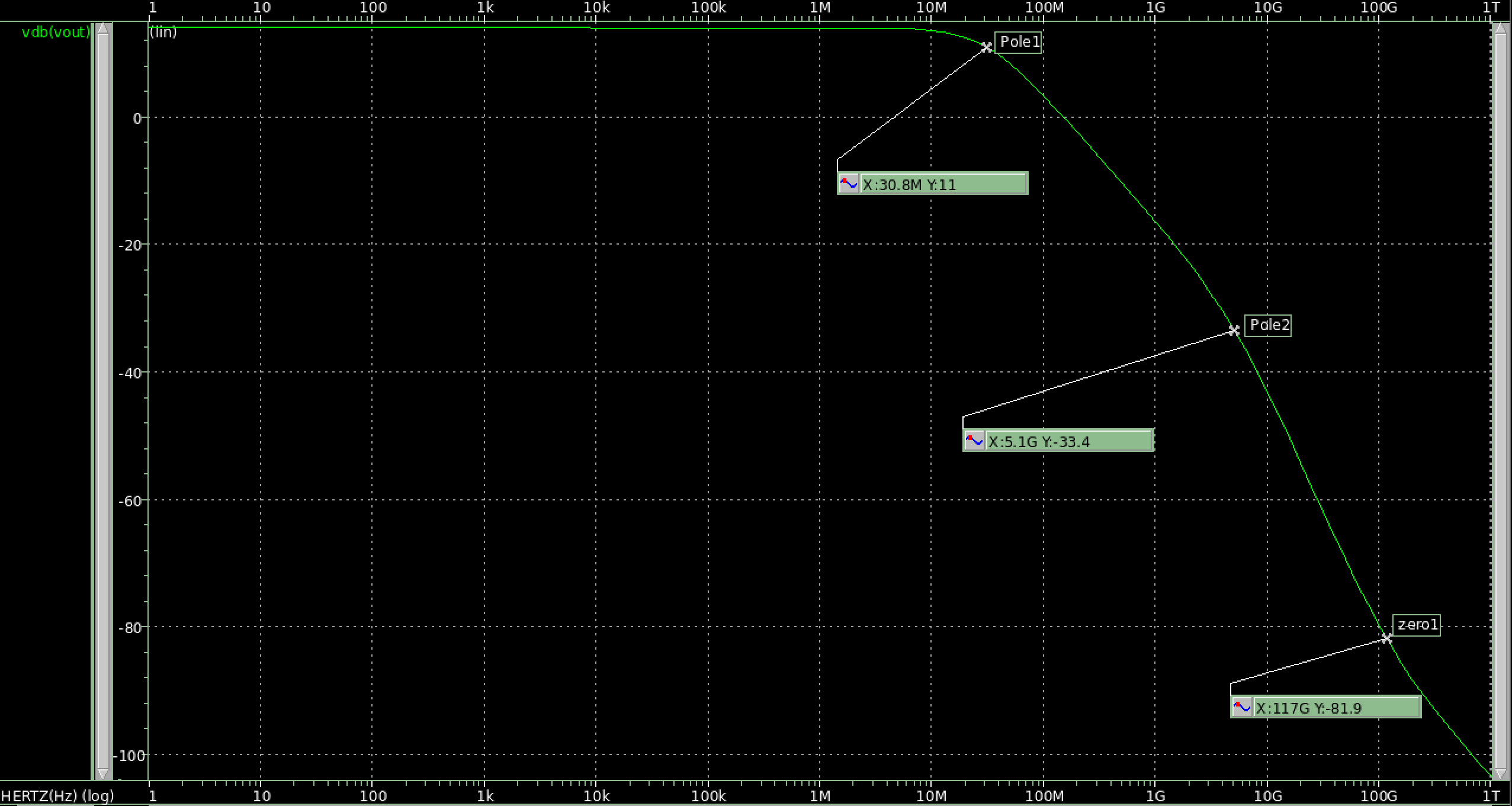
Transfer curve: Vo=0.784V, VGS=0.64V

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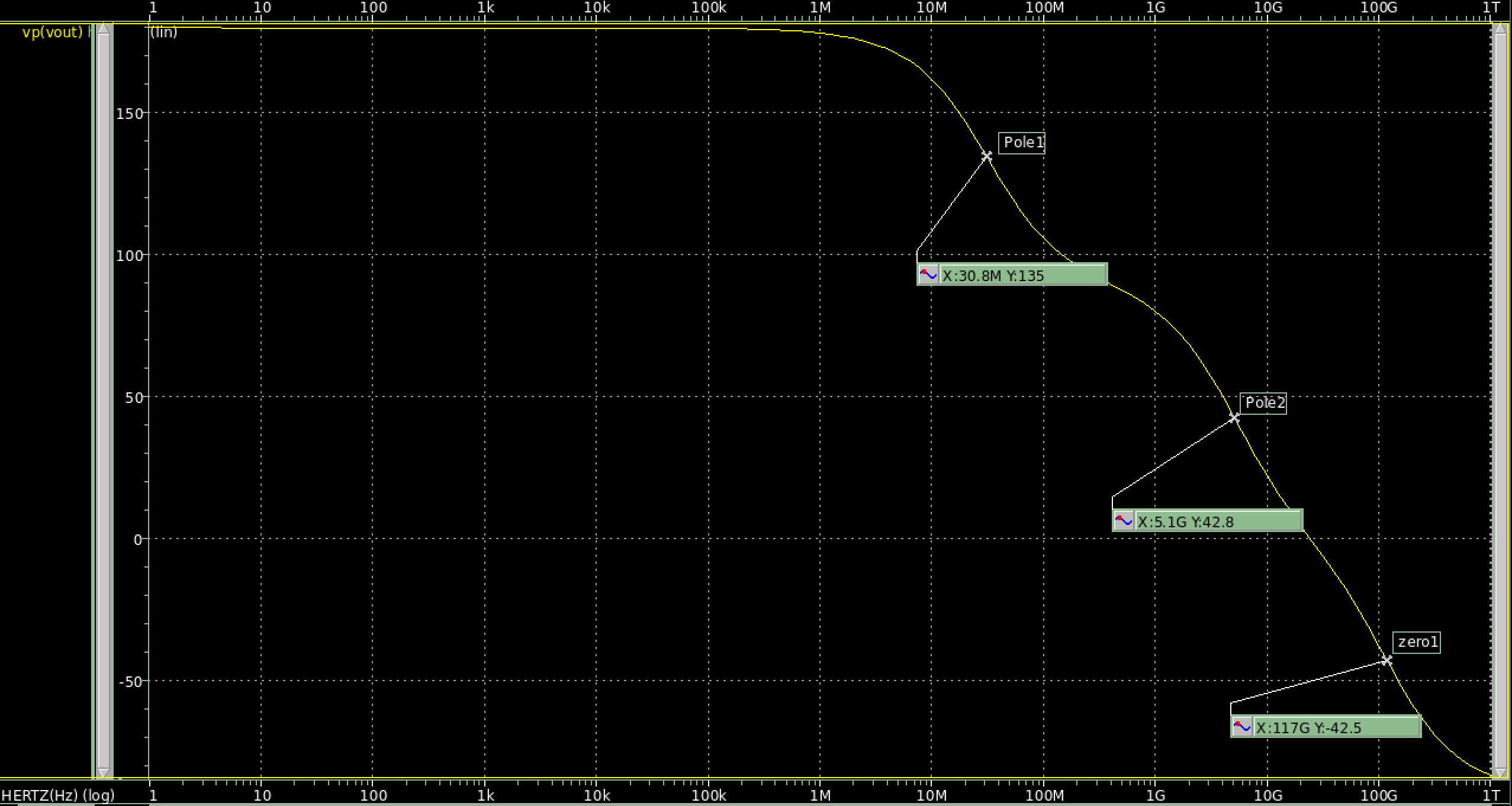
Vo/Vi transfer curve slope: the slope Vo/Vi= -5 at VGS=0.64V

AC Sweep

## Please plot the frequency response of this gain stage. And mark the poles and zeros on this curve. (Try to use .pz command (p.42 in tutorial) in SPICE)



Frequency response(Gain)



Frequency response(Phase)

## Compared and simulated poles/zeros with hand calculation

Discussion

## We will use the bandwidth (MHz) / current consumption (μA) as the figure of merit (FoM). Try to make it large, and then fill the table below

|  |  |  |
| --- | --- | --- |
| Parameter |  | Result |
| Supply Vdd | 1.5V | 1.5V |
| M1 Device size (W/L x m) |  | 0.85u/0.18u x 2 |
| M1 VGS (mV) |  | 0.64V |
| M1 Bias Current (μA) | As small as possible | 54.28 |
| M1 Overdrive Voltage (mV) | Vod > 0.15V | 151.092 |
| M1 VDS Saturation Voltage (mV) | vdsat | 170.844 |
| M1 Transconductance (μA/V) | gm | 489.418 |
| Load R (Kohm) |  | 13.2 |
| Voltage Gain (V/V) | > 5.0 V/V | 5.001 |
| Bandwidth (MHz) | > 30 MHz | 30.712 |
| FoM ( BW (MHz) / Bias Current (μA) ) | As large as possible | 0.57 |

## Please discuss how to achieve best FoM.

FoM=BW/Id，BW = (Hz)，Id=，其中K正比於W/L，故提高FoM，需將BW提高，Id降低。

1. Id下降: Id=，K和Vth為製程參數，故調整VGS來調整Id，調整方法為將VGS降低，但仍需使VOV大於0.15(題目要求)。
2. BW提高: BW = (Hz)，其中C2為atto等級(10的-18次方)非常小，影響不大，而CL為題目給定，故不適用改變電容大小來改變頻寬。此題著重在ro//RL之調整，ro= VA/Id；RL為自己設計，將Id變大或RL變小，都可使BW變寬，

Id提高時，雖BW提高，但FoM=BW/Id，故很難保證FoM會變大。

而RL降低時，雖BW提高但整體gain下降，為防止gain因RL下降甚至低於5，本題嘗試提高gm值，gm==，在不調整Id情況下，盡量使VOV越小越好。

**總結，使VOV等於0.15，是提高FoM的一大原則。**