**國立清華大學**

**Analog Circuit Design**



**Homework 2**

**Differential Pair**

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Operation point

# Please design the device size of Mx, Ms, load resistance Rd, and the bias voltage VBS and VBS1, to make the small differential signal voltage gain (vout/vi) larger than 6.0 (V/V). (Please note, since Ms serves as a current source, Ms must stay in the saturation region).

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Mx size | Ms size | RD | VBS | VBS1 |
| W=0.31u  L=0.18u  m=10 | W=0.51u  L=0.18u  m=10 | 14.3K | 0.65V | 0.61V |

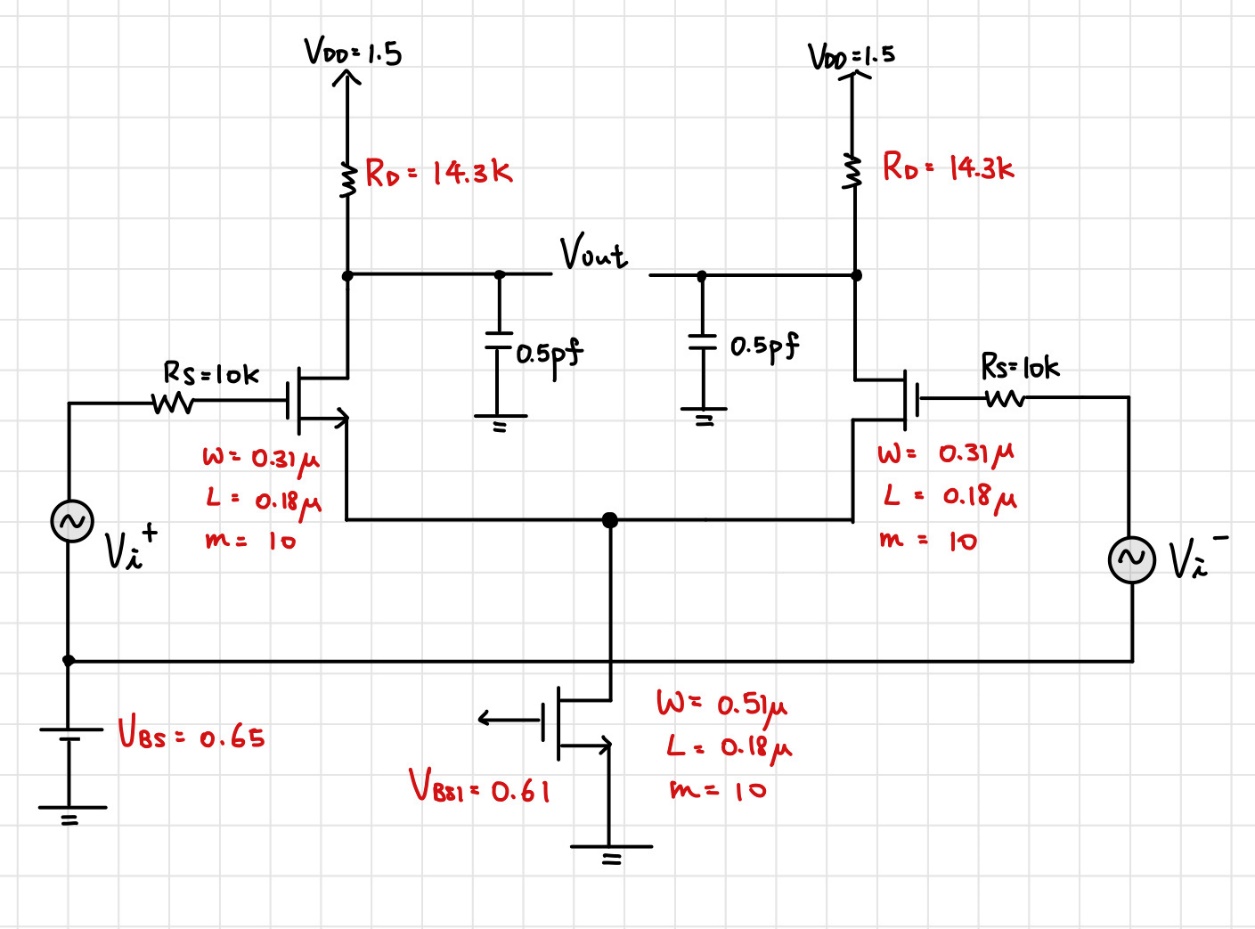
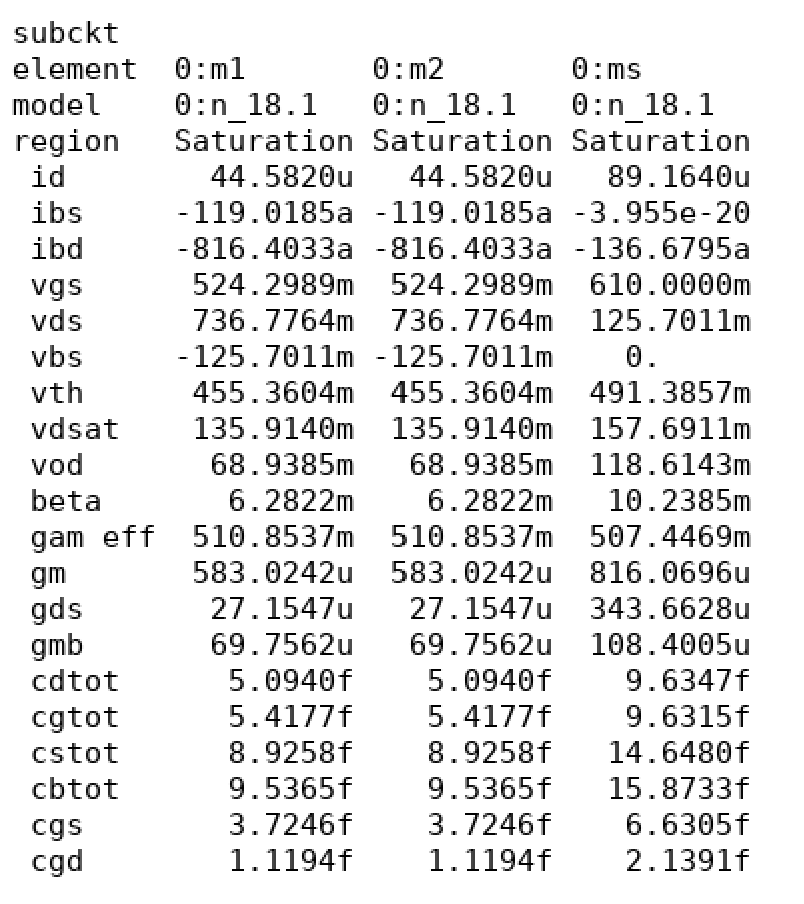
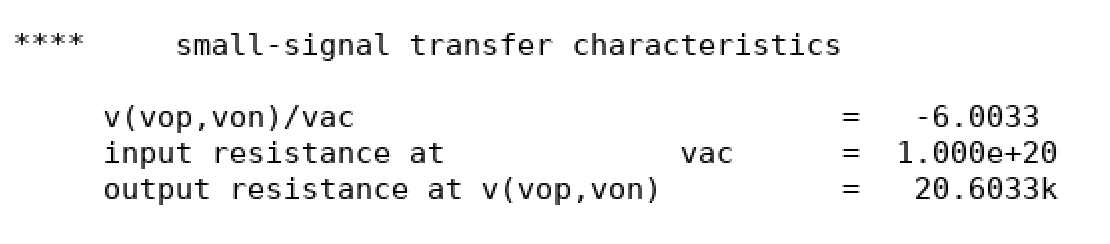


圖 1 電路設計圖

# Please print out the small signal parameters of active devices from list file.





# Under the operation condition in (a), please run .DC then plot the differential input – differential output transfer curve (as in slide 6). Try to plot and measure its small signal differential mode gain.

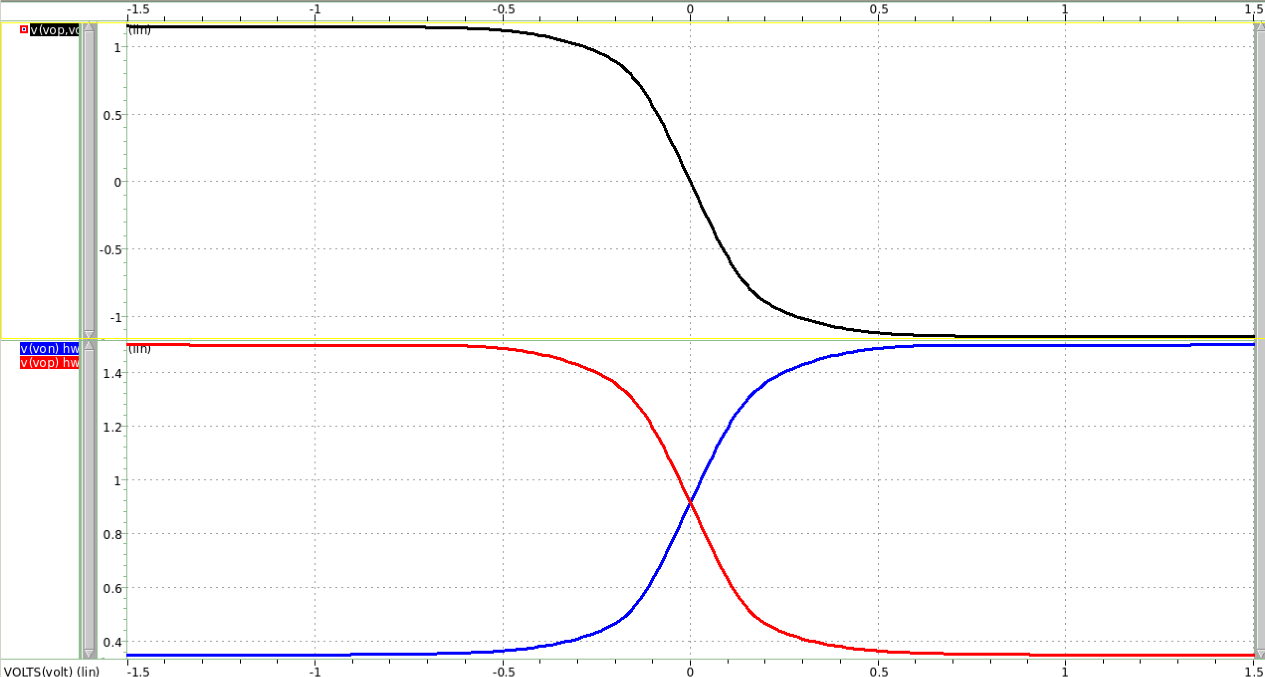


圖 2 differential output-input Transfer curve

上圖是雙端輸出，下圖是兩單端輸出

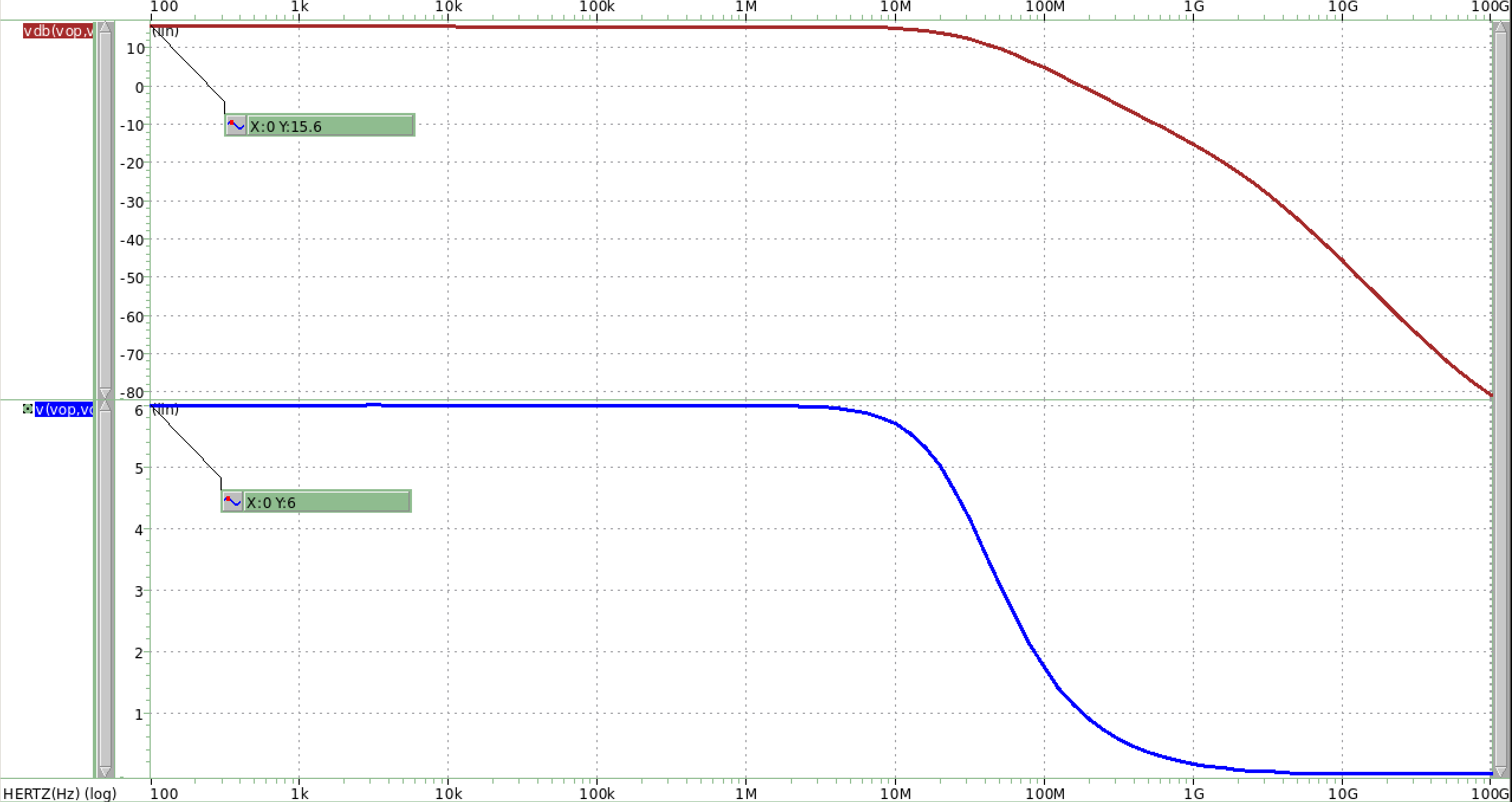


圖 3 measure differential mode gain

上圖為db為縱軸，下圖則為gain為縱軸(V/V)

# Compare the gain value with hand calculation using the small signal parameters from (b).

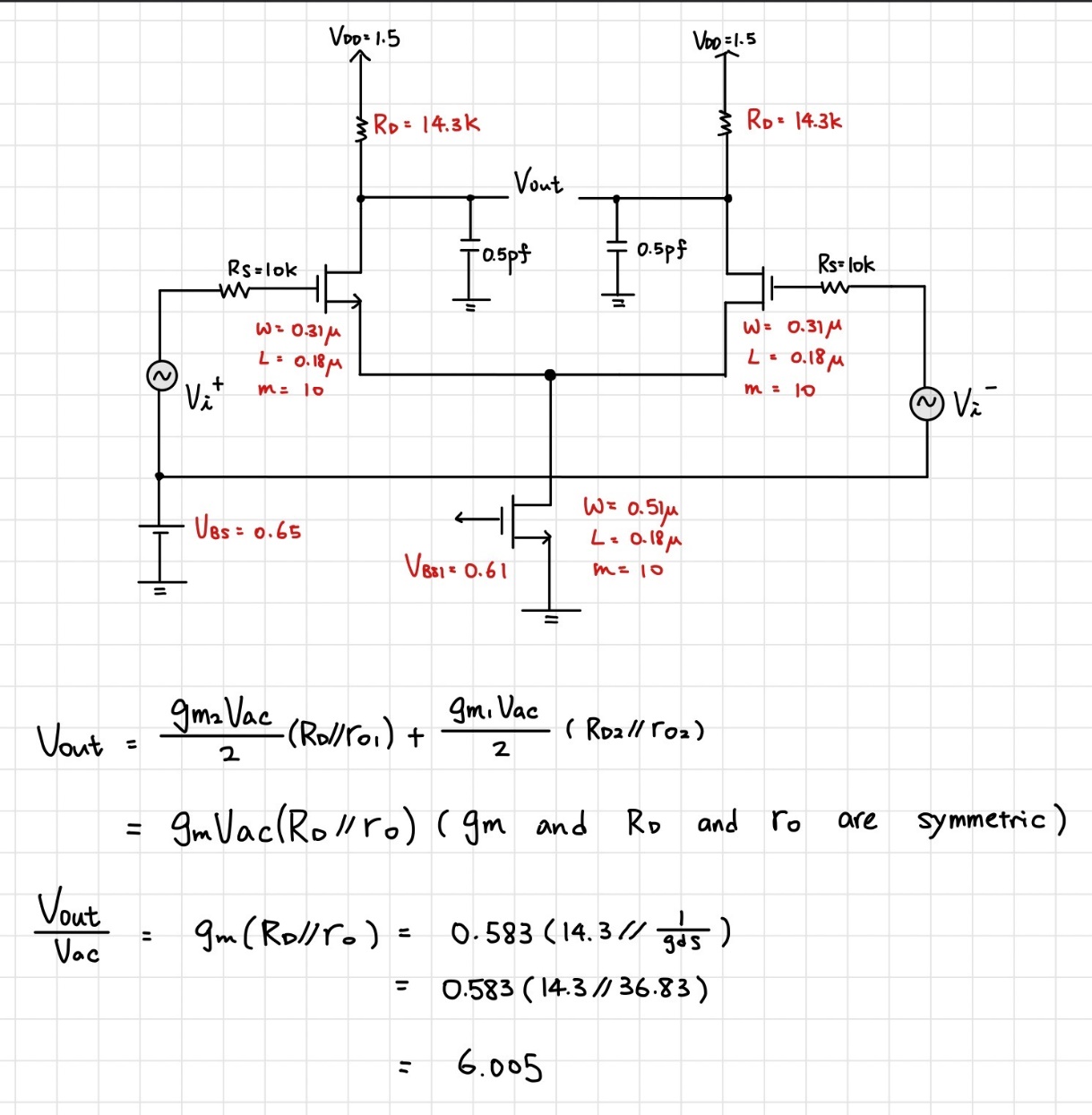


圖 4 hand calculate gain(differential mode)

Hand calculate值:6.005

Simulation gain value:6.003

誤差值:0.03%

Differential input signal一正一負，套用在spice上打的架構，將這裡的正負輸入訊號指定成Vac/2。

# Like (c) please also run .DC to plot the common-mode input – common-mode output transfer curve (as in slide 6). Try to plot and measure its small signal common mode gain.



圖 5 common mode input-output transfer curve

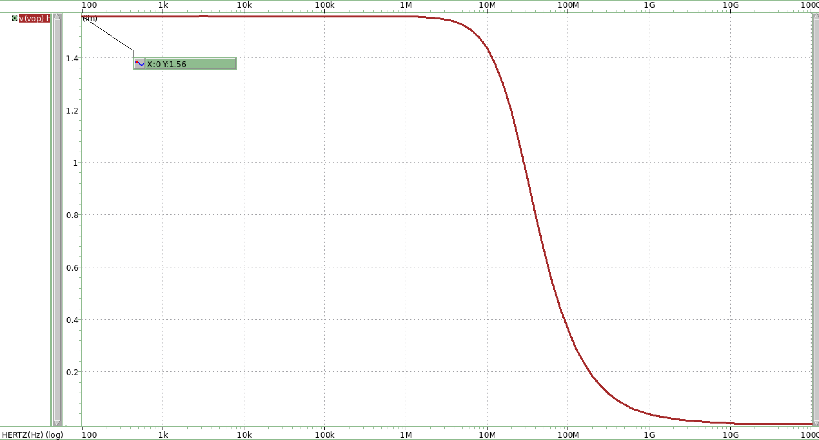


圖 6 measure common gain

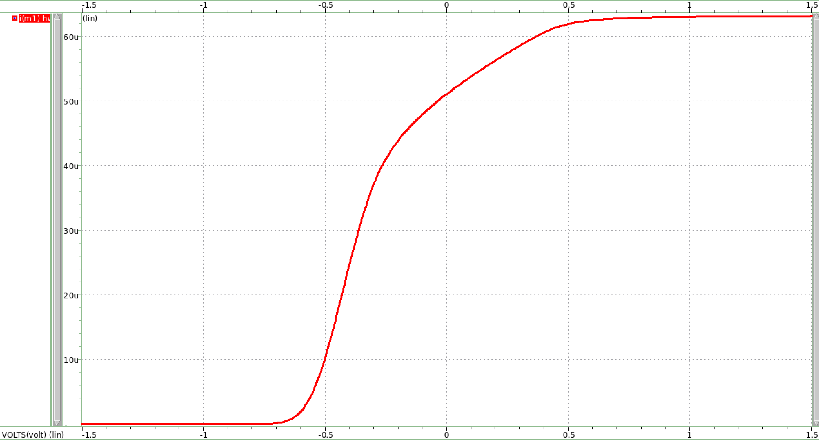


圖 7 output current transfer curve

# And compare the gain value with hand calculation using the small signal parameters from (b).

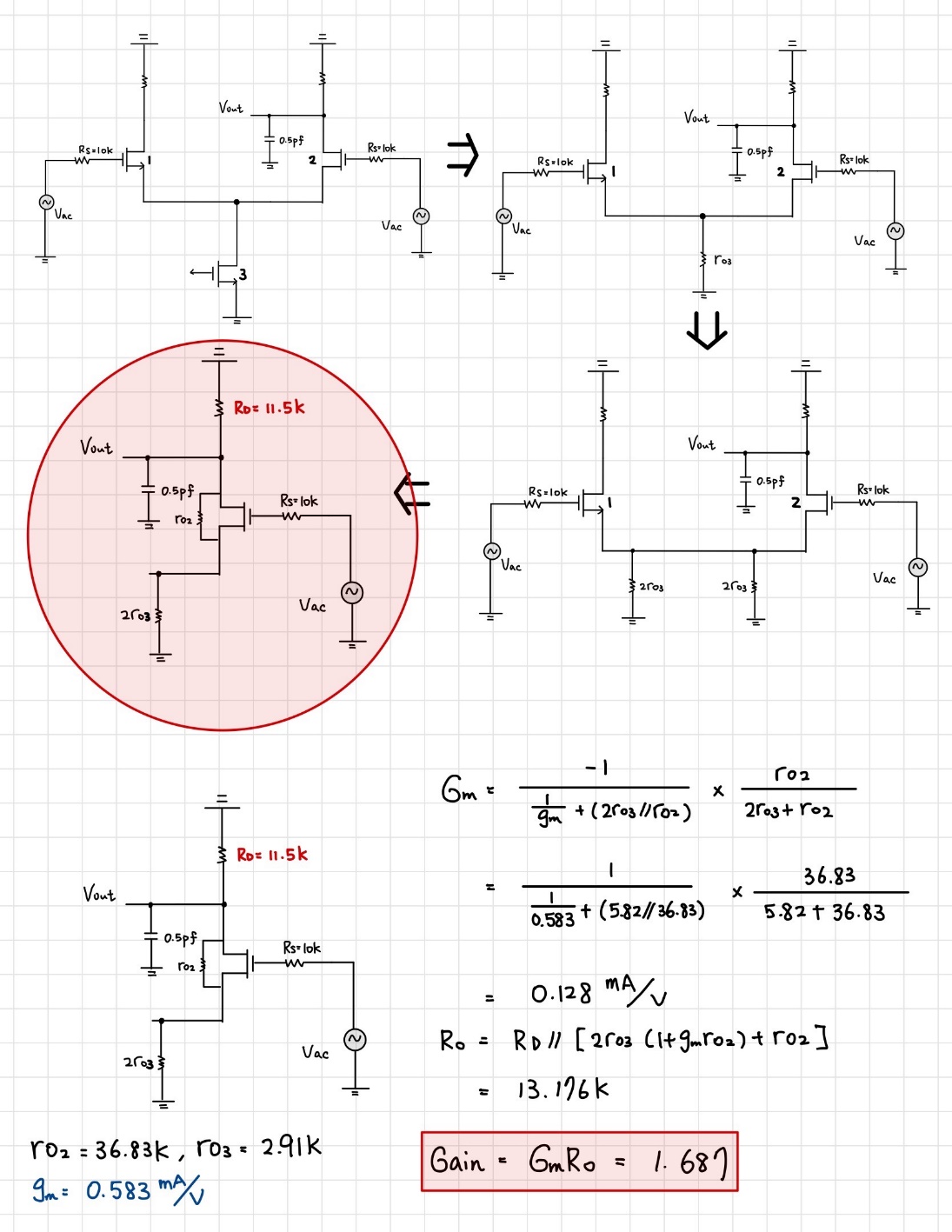


圖 8 hand calculate gain(differential mode)

Hand calculate值:1.687,

Simulation gain value:1.56

誤差值:8.14%

Frequency response

# The small signal -3dB bandwidth of differential mode signal has to be larger than 30MHz. Please simulate and plot the differential mode frequency response of this gain stage.



圖 9 frequency response

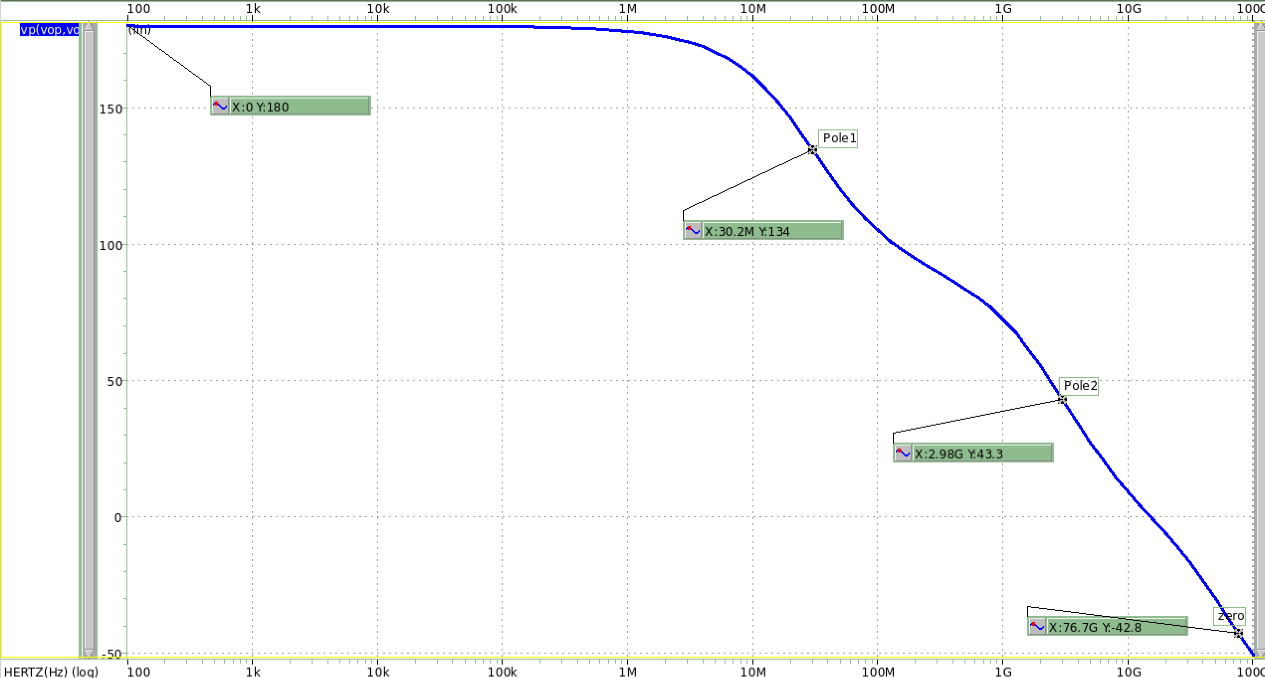


圖 10 phase response

# Use .pz to simulate and mark the poles/zeros on this curve.

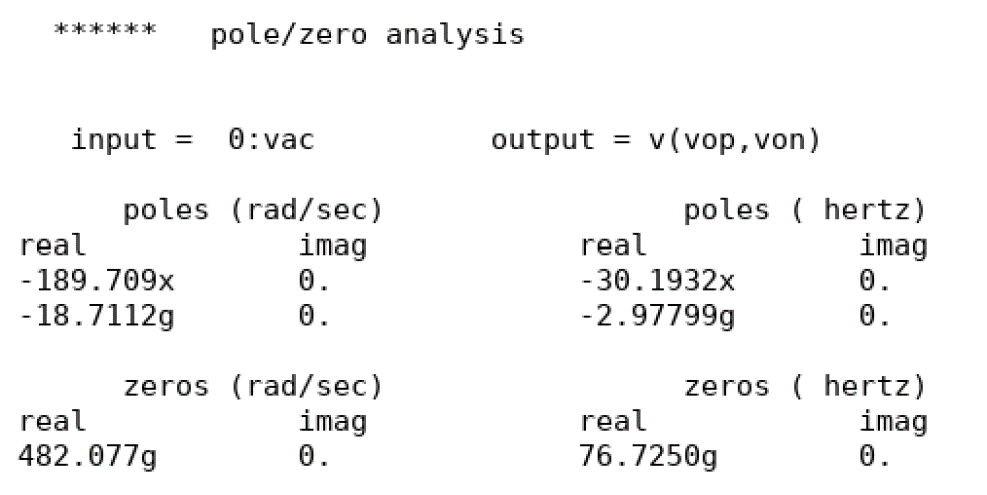


圖 11 pole&zero (.pz)

# Compare with hand calculations

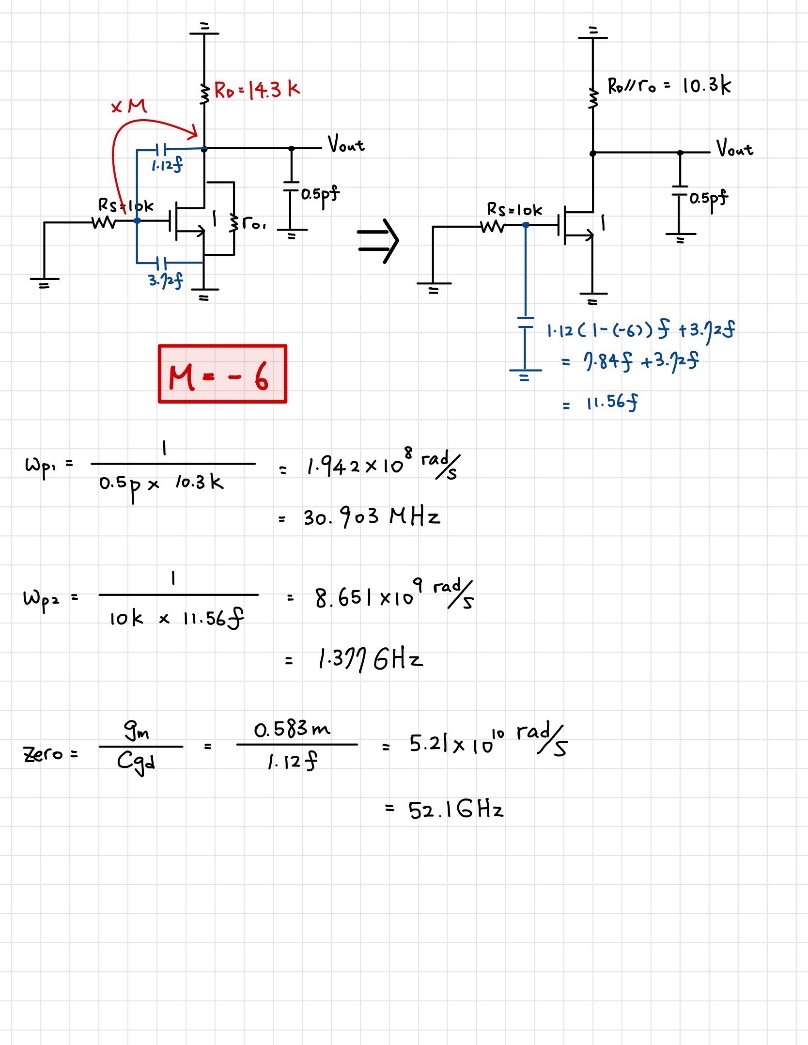


圖 12 pole&zero hand calculation

Pole1誤差值:2.31%

Pole2誤差值:53.7%

Zero誤差值:32.1%

Linearity

# Please input differential sinusoidal waveforms to estimate the harmonic distortion. Please use .four to simulate the THD performance. And also use .tran to plot the maximum output differential voltage waveforms that achieve -60dB THD at 1MHz. The single-ended input amplitude value is defined as the linear range in this homework. The linear range must be larger than 10mV.

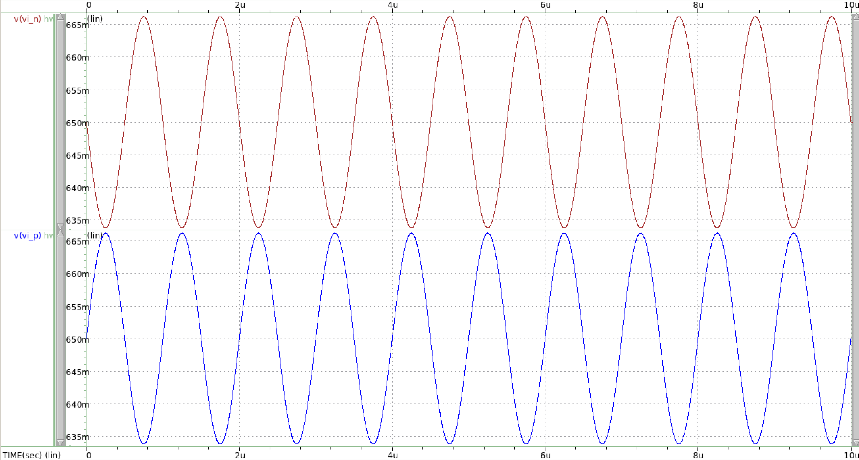


圖 13 differential sinusoidal input(linear range=16.25mv)

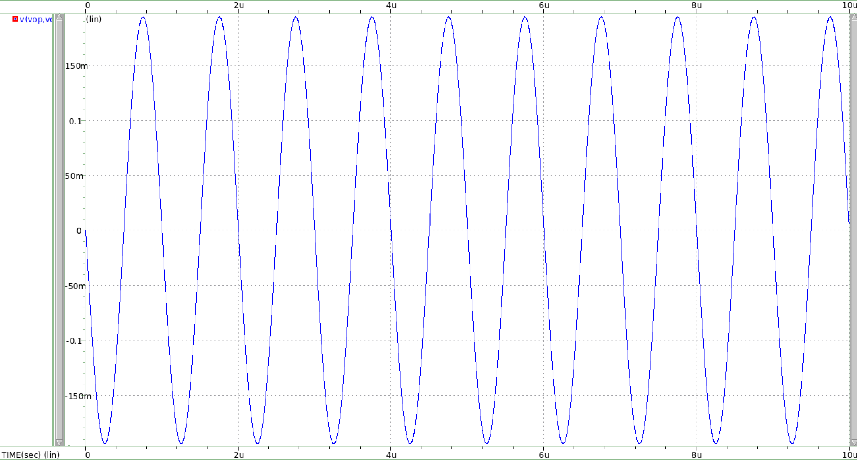


圖 14 maximum output differential voltage waveforms

# Please print out the .THD results.

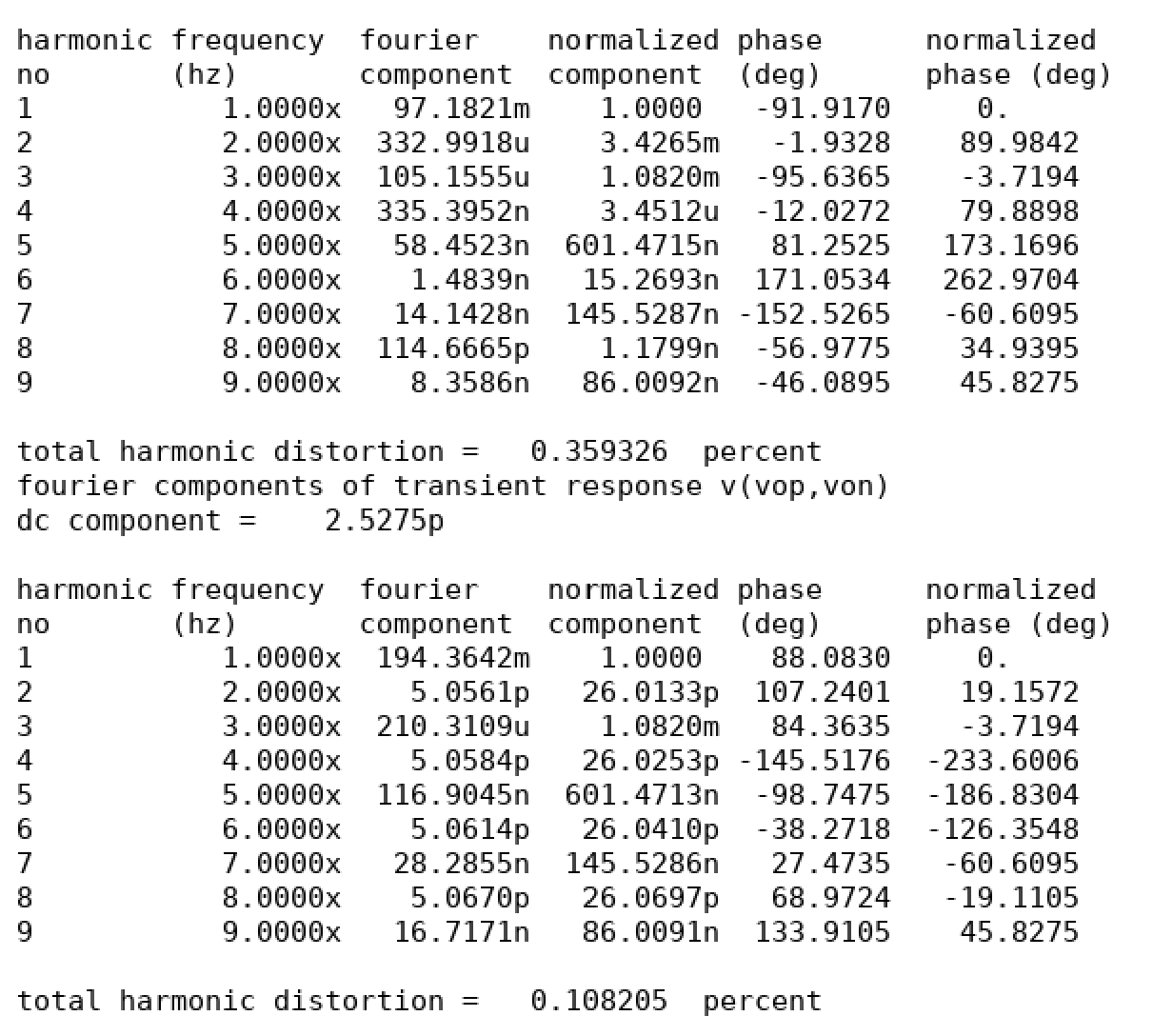
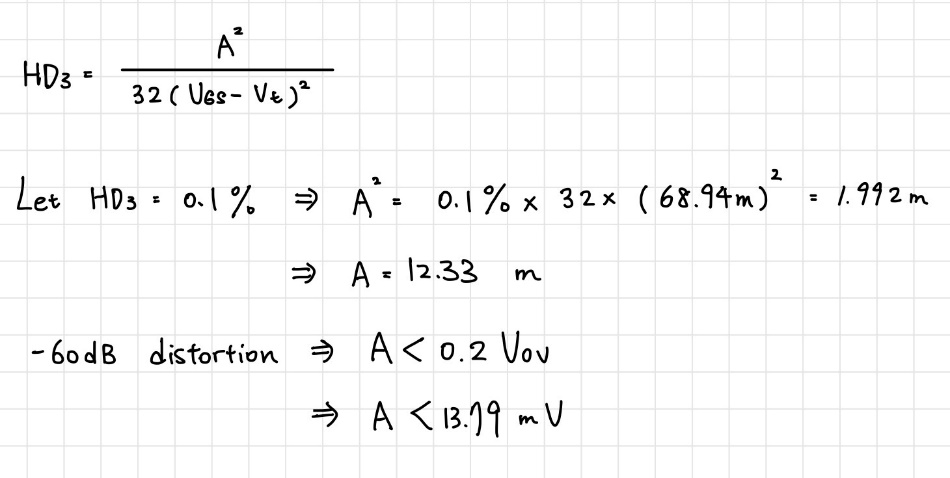


圖 15 THD result

# Compare the simulated input amplitude with the hand calculation.



# Under this amplitude please also simulate the THD performance under 100KHz and 10MHz respectively.

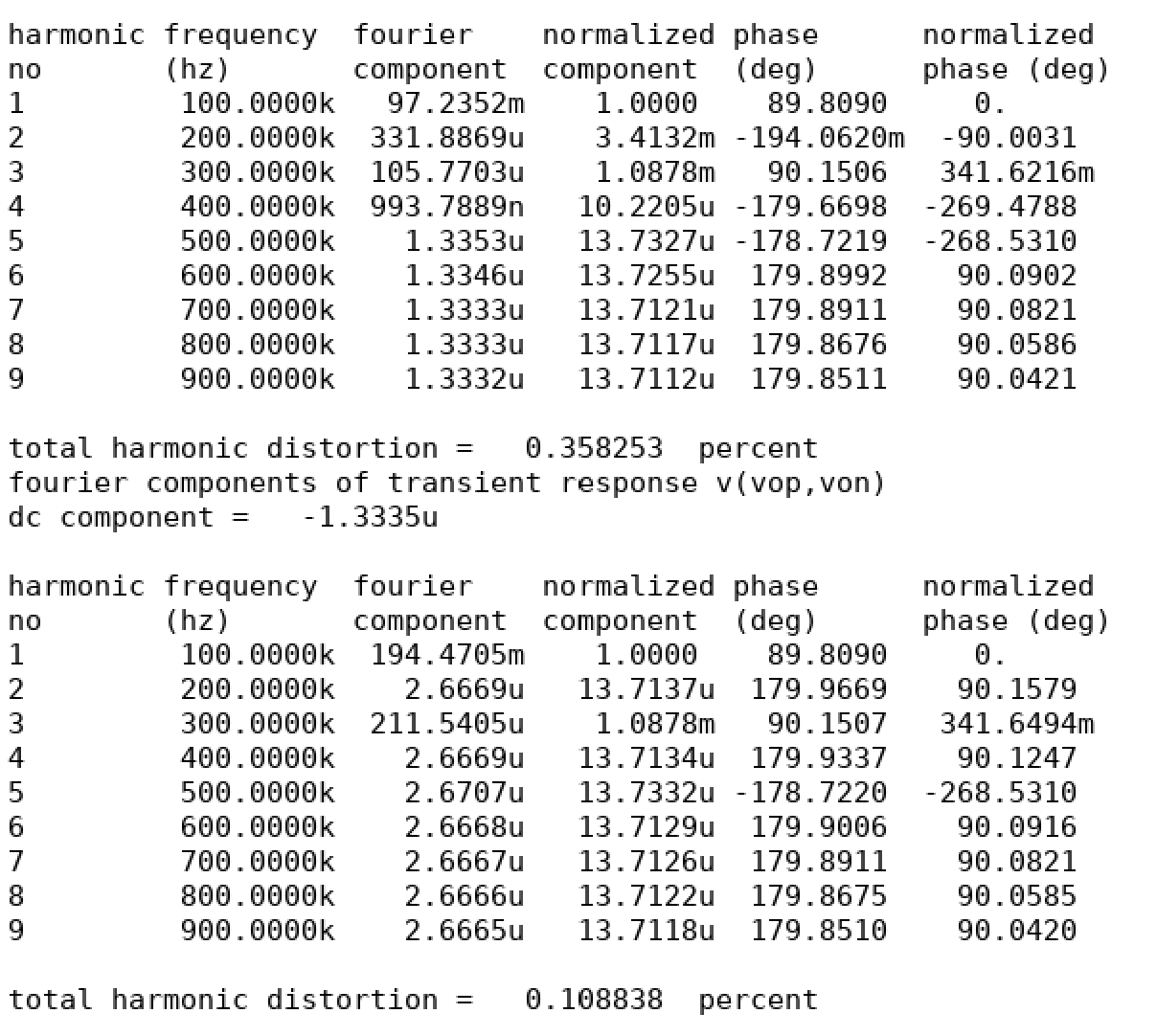


圖 16 100KHZ THD

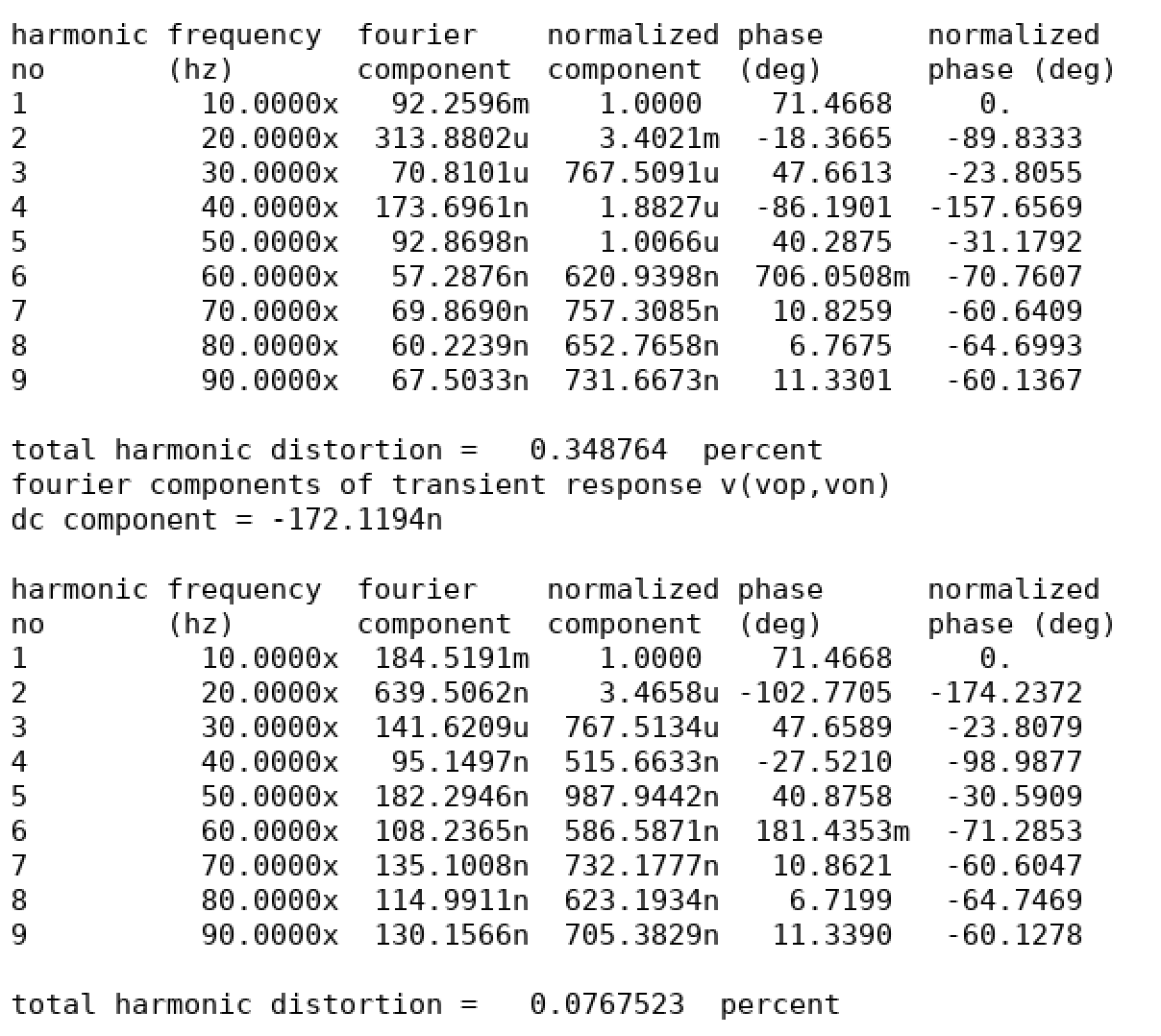


圖 17 10MHZ THD

# We will use the “bandwidth (MHz) x linear range (mV) / current (µA)” as the figure of merit (FoM). Please try to make this FoM maximal.

|  |  |  |  |
| --- | --- | --- | --- |
| Working Item | Specification | Simulation | calculation |
| Vdd | 1.5-V | | |
| Tail current | As smaill as possible(uA)(#3) | 89.16u |  |
| Differential gain | >6(V/V) | 6.003 | 6.005 |
| Input common mode | Open for design(VBS,V) | 0.65 |  |
| Tail current bias | Open for design(VBS1,V) | 0.61 |  |
| Common-mode gain | Open for design(V/V) | 1.56 | 1.69 |
| Input size Mx | Open for design(W,L),m | 0.31u/0.18u,m=10 |  |
| Differential gm | Open for design(mA,V) | 0.583(mA/V) |  |
| Load R | Open for design(Kohm) | 14.3K |  |
| Bandwidth | >30MHz(#1) | 30.2M | 30.9M |
| Linear range  OUTPUT 60dB THD@1MHZ | Single-ended input amplitude>10mV(#2) | 16.25 mV | 12.3mV |
| FoM | #1\*#2/#3 | 5.5 | 4.26 |

# Please use your design equations to explain how to achieve max FOM.

FoM要上升的話，Tail current要下降，BW要提高，Linear range要提高。同時達到gmRd=(2KVov)Rd=6及，先掌握較單一變數可操作的結果，故以(Rd//ro)<10.6K為出發點開始設計。

在設計過程，我以tail current不超過100u為原則去設計各項數值，得到的參數範圍如下:

1. ro大約落在30~40(K)，所以Rd大約需設計在14.39K以內，以免BW<30MHz。
2. 因Rd最大值約為14.4K，為使gain>6，gm必須至少0.42m，因有些製成參數無法設計(cox、electron mobility…)，optimizing gm值還需經幾組實際嘗試比較，但原則上最小值不能低於0.42m。
3. 所小W/L ratio可使THD percentage變低，也可使電流變小，而此次作業Ms的size設計大幅影響此電路的汲極電流，Is的值因此變得由甚為重要，這也是為何我在一開始就將tail current不超過100u為原則去做電路設計。
4. 閘極電壓VBS、VBS1是決定Vov大小的參數，Vov越大也可使linear range更大，但也相應的增加功耗。在linear range與tail current二選一中，我決定盡可能使linear range提高但不使tail current大於100u為前提下去做設計。(因linear range的變化值比tail current變化值，對FoM更有影響力)

接下來開始實際設計並觀察，我發現Mx的size很低程度的影響gain(因主要都是由tail current提供並決定電流)，但又同時可改善THD，多方嘗試後我認為**使所有mos size接近可得到最適當的THD與gain的平衡**(W小有助於THD但卻使增益減少)，**也搭配最大可接受的Vov值去設計直流偏壓**(VBS、VBS1)，選擇更大Vov的好處還有可使Rd不用那麼大，以利增加頻寬。