**國立清華大學**

**Analog Circuit Design**



**Homework 3**

**Feedback Amplifier**

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Operation point

# Please use .op command to print out the device parameters. And use the parameters from HSPICE to hand-calculate the results.

**表格 1 MOS size design**

|  |  |  |
| --- | --- | --- |
| **MOSFET** | **W/L** | **m** |
| **NMOS(m1)** | 35u/0.34u | 1 |
| **PMOS(m2)** | 43.4u/0.34u | 3 |

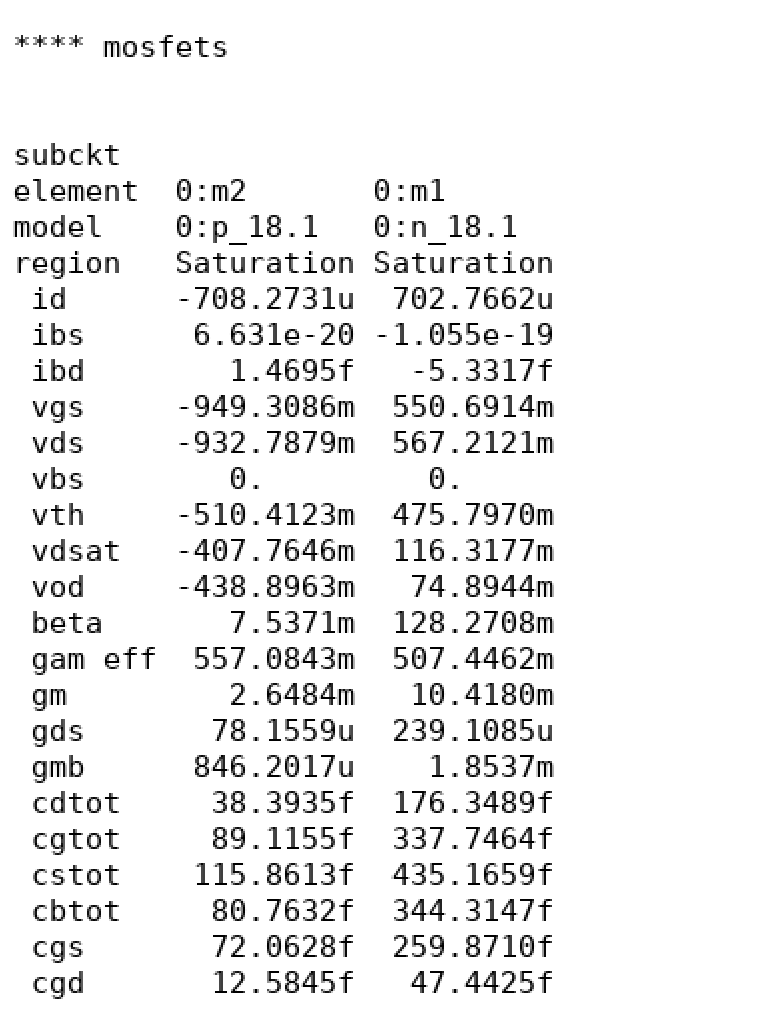


圖 1 .op result

Loop performance

# Please calculate the open-loop gain.

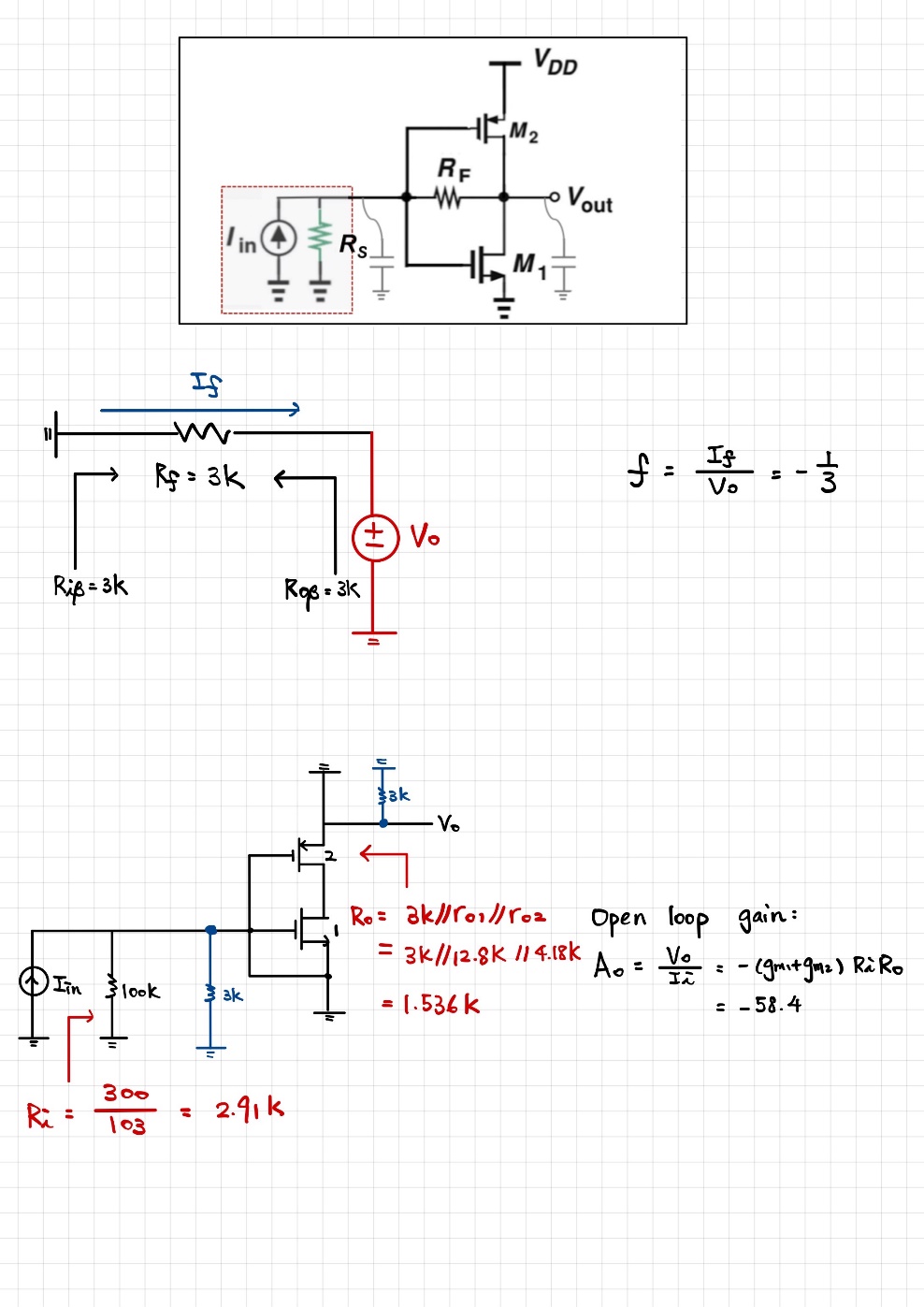


圖 2 open loop gain calculate

|  |  |  |  |
| --- | --- | --- | --- |
| **Ri** | **Rout** | **Feedback ratio** | **Open loop gain** |
| 2.91K | 1.536K | -1/3 | -58.4 |

# Please use .tf command to print out the gain, input and output impedances. And compare the simulation results with the hand calculations using the small signal parameters from (a).

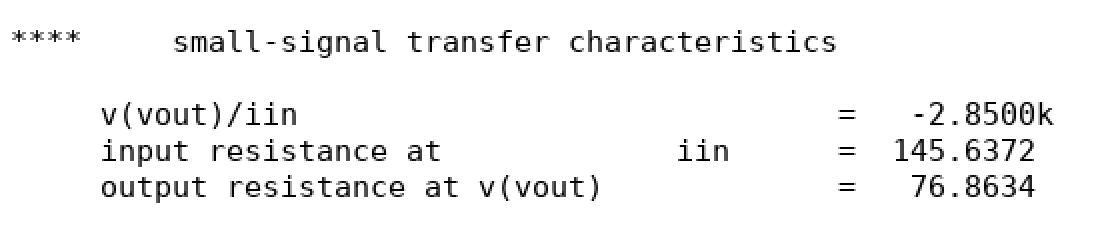


圖 3 .tf result

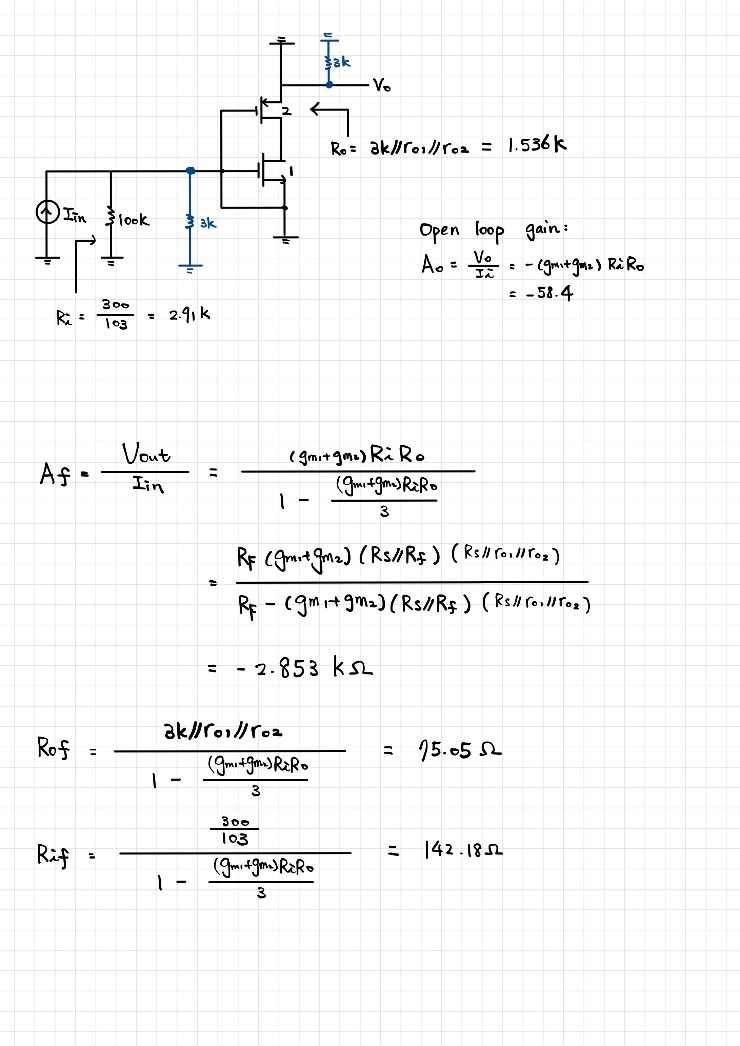


圖 4 Open loop gain

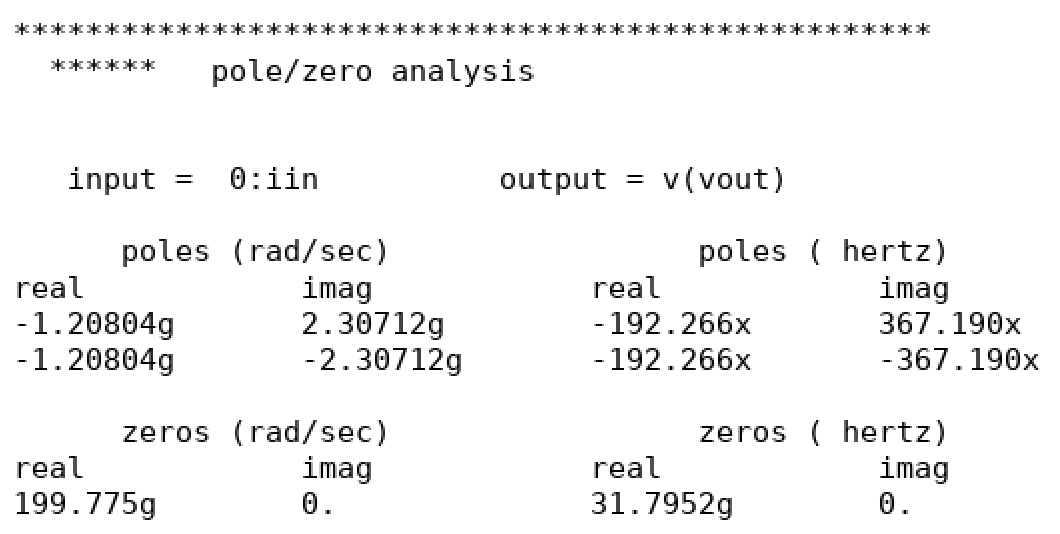
**Close loop gain誤差值:0.1%**

**Input impedance誤差值:2.3%**

**Output impedance誤差值: 2.3%**

AC SWEEP

# Plot this feedback amplifier frequency response and mark the bandwidth (DC gain -3dB point) and the poles, zeros. Please use .pz command and print out the data. And compare the simulation results with the hand calculations using the small signal parameters from (a).



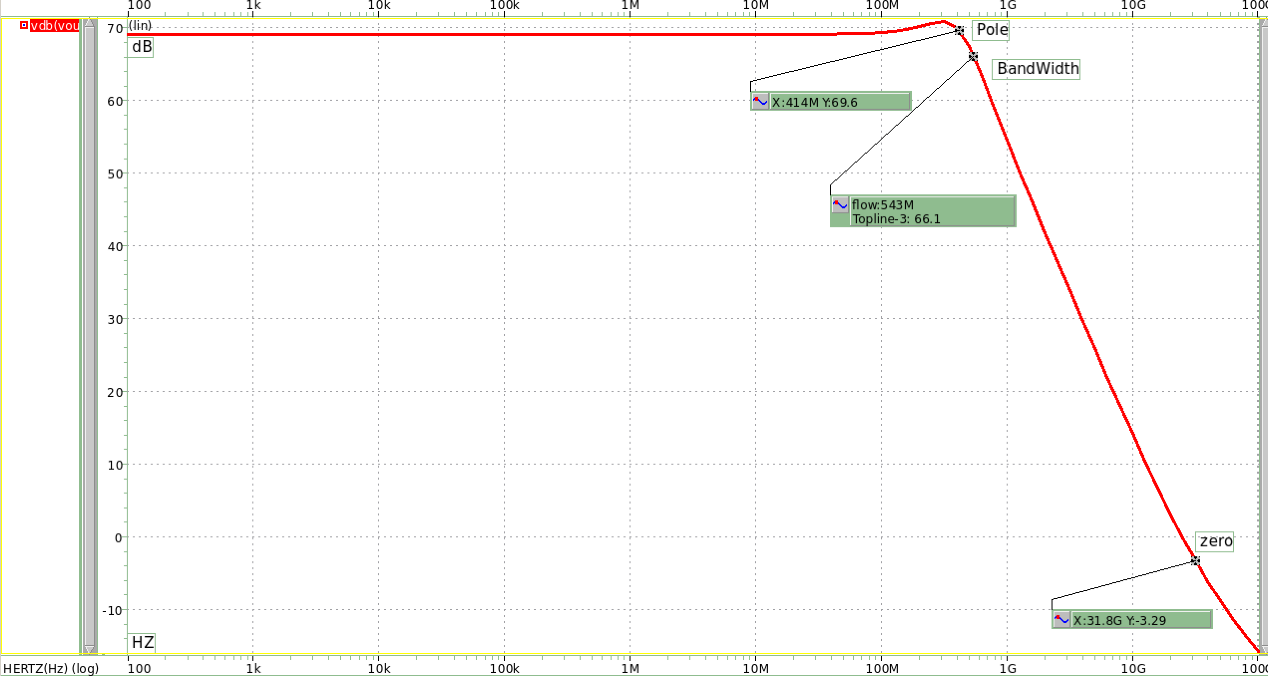


圖 5 frequency response

**表格 2 Simulation result**

|  |  |  |  |
| --- | --- | --- | --- |
| **Plot parameter** | Pole | Bandwidth | zero |
| **Frequency** | 414.4M | 543M | 31.8G |

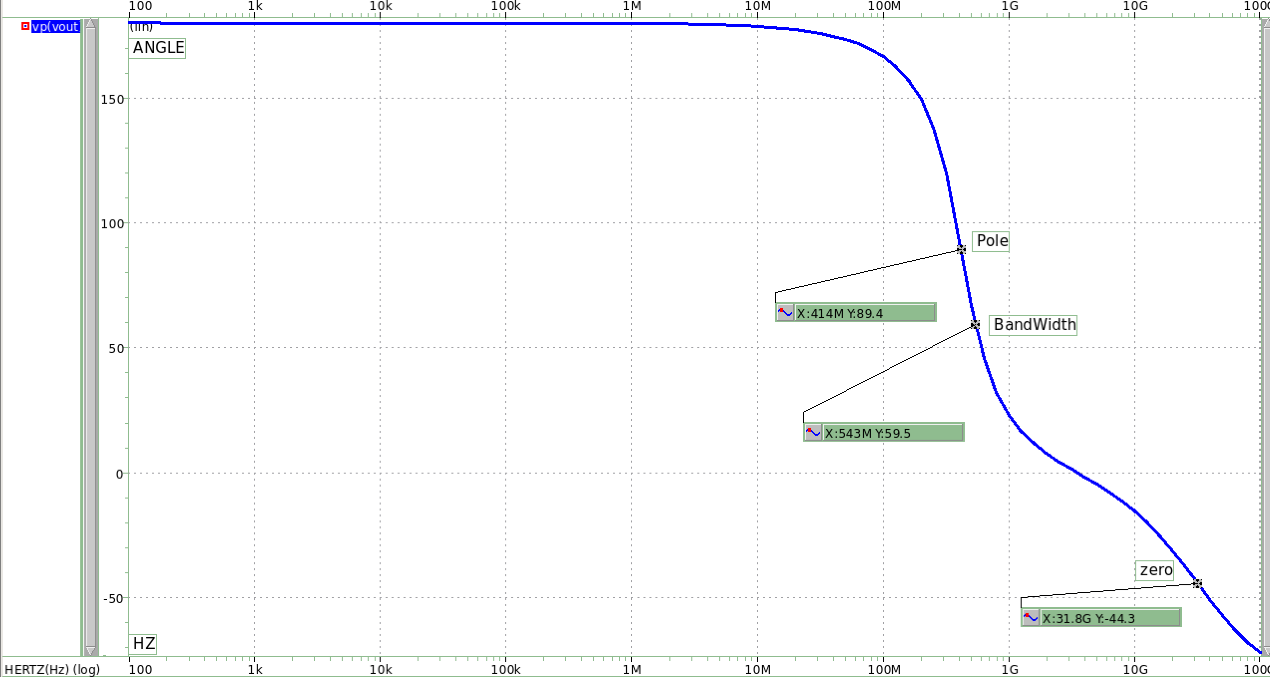
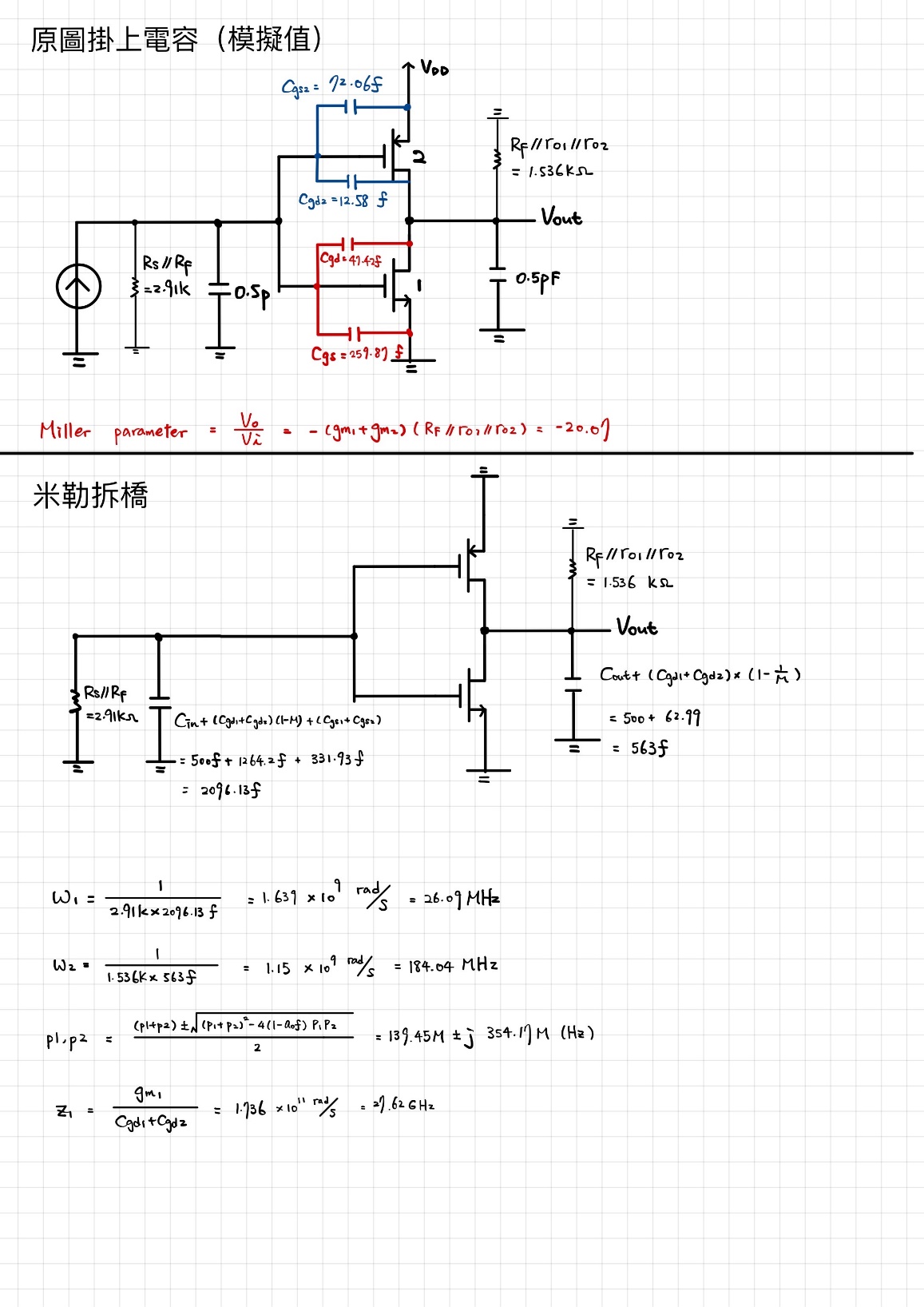


圖 6 phase response

|  |  |  |  |
| --- | --- | --- | --- |
| **Plot parameter** | Pole | Bandwidth | zero |
| **Angle** | 89.4 | 59.5 | -44.3 |



**表格 3 Hand Calculation result**

|  |  |  |  |
| --- | --- | --- | --- |
| **Plot parameter** | Pole1 | Pole1 | zero |
| **Close loop Frequency** | 372.27M | 372.27M | 27.62G |
| **Open loop Frequency** | 26.09M | 184.04M | 27.62G |

**comparison between Sim. and Cal.**

**Pole誤差值:10.17%**

**Zero誤差值:13.14%**

Discussion

# The FoM in this design is “Bandwidth (MHz) / Current (mA)”. Try to maximize this FoM.

|  |  |  |
| --- | --- | --- |
| Working Item | Simulation result | Hand calculation |
| Vdd |  |  |
| I\_GND current (mA) | 0.703m |  |
| Transimpedance gain | 2.8500K | 2.853K |
| core amp size (W/L1, W/L2) | M1:35u/0.34u  M2:43.4u/0.34u |  |
| core amp gm (gm1, gm2) | 2.6484m,10.418m |  |
| core amp ro (ro1, ro2) | 4.18K,12.8K |  |
| Bandwidth (-3dB) (MHz) | 543 |  |
| Closed-loop poles/zeros (p1, p2, z1) | -192.266+j367.19(MHz)  -192.266-j367.19(MHz)  31.7952GHz | -139.45+354.17(MHz)  -139.45-354.17 (MHz)  27.62GHz |
| Closed-loop input impedance | 145.6372 | 142.18 |
| Closed-loop output impedance | 76.8634 | 75.05 |
| FoM (MHz)/(mA) | 772.4 |  |

# Please discuss your design flow and results, especially on the loop gain and device size selection.

本次作業需符合兩原則，分別為及Bandwidth>200MHz。故需要足夠大的gm值。

而提高FoM方法為增大頻寬或降低電流，但頻寬跟電流關係為正向關係，為了提升頻寬電流必然增加;為了降低電流頻寬必然下降，經過幾次實際模擬後，**發現低電流時雖然犧牲頻寬，但低電流對FoM的提升影響更多。**故本次著重在設計符合條件下的電流，使其越小越好。

需要低電流，W/L ratio就不能太大，於是我增加MOS length，此方式比起減少Width去降低電流，對增益的影響也較小。

當 不夠大時，我嘗試增加m，使MOS並聯，發現雖然增益有提高，但頻寬降低不少，推測是因在並聯MOS時，每顆MOS的output capacitance都會對頻寬有負面影響，嘗試幾種組合後 ，m=3時普遍可以得到較好的平衡。當 不夠大時，就去調變width，也得到比調變m更好的結果(頻寬上升不驟降)。

以下針對調變W、L、m三個變數的優缺點進行討論:

1. 使W提升，對增益及頻寬都是優點，會使這兩者皆上升。但對電流來說可是非常致命的，調高0.1um左右電流便會上升約40μ，做個簡單計算:

假設現在電流是x(μA)，提高40μA帶來的影響會使FoM降低 倍，且電流(x)越大帶來的負面效應越大。但Wp和Wn總和至少需80u才可使增益大於2.85K(且此時頻寬表現頗差)，我試了三組W組合，分別為Wp=Wn; Wp>Wn; Wp<Wn，**最後得到Wn>Wp時FoM普遍較高的結果**。

1. 使L提升，對頻寬及增益的影響都不好，但都不明顯，並且能有效控制電流大小，在幾次嘗試後，**L大約落在0.35u至0.41u會是最好的範圍**。
2. 而m的部分，提高過程發現頻寬明顯下降，且電流提升，在這個情況下完全不符合直覺(頻寬與電流呈正向關係)，推測是並聯MOS時，每顆MOS的output capacitance帶來的影響，導致頻寬不升反降。m=1雖可以得到較好的頻寬表現，但使得W的調變範選擇變少，因為在設計時Wxm差不多落在100上下，若m=1，W又不可超過100μ，會少很多設計組合。