**國立清華大學**

**Analog Circuit Design**



**Homework 4**

**Two-Stage OPA**

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目錄

[(a) Operation point 4](#_Toc122221781)

[1. Please DESIGN your bias (Mb1 - Mb3) and amplifier (M1 – M5) size to make the gain at DC larger than 60dB. 4](#_Toc122221782)

[2. Print out the results from .op command. And make sure all the devices are properly biased. 4](#_Toc122221783)

[3. Use .tf command to print out the voltage gain. 5](#_Toc122221784)

[4. Verify your DC gain with hand calculation. 5](#_Toc122221785)

[(b) AC response before compensation 6](#_Toc122221786)

[1. Please simulate and plot the frequency response (magnitude and phase) of your design in (a). Mark the (i) DC gain (ii) unity gain frequency, and (iii) phase margin on figure. 6](#_Toc122221787)

[2. Use .pz to identify the poles and zeros, and mark them on bode plot. 7](#_Toc122221788)

[3. Verify the first and second dominant poles and first RHP zeros with hand calculation. 8](#_Toc122221789)

[(c) AC response after Cc compensation 9](#_Toc122221790)

[1. Please design your value of Cc and simulate the AC response in (b). (please note, your Cc must be smaller than 10pF, and the phase margin must larger than 0 in this case). 9](#_Toc122221791)

[2. Please print .pz output of the new poles (first and second dominant) and zeros (first RHP), and mark them on bode plot. 10](#_Toc122221792)

[3. Verify the compensation with hand calculation. 11](#_Toc122221793)

[(d) AC response after Cc-Rc compensation 12](#_Toc122221794)

[1. Please design your value of Rc to shift the RHP zero and simulate the AC response in (c). (please note, your unity gain frequency must be larger than 50MHz and phase margin must larger than 45 in this case). 12](#_Toc122221795)

[2. Please print .pz output of the new poles and zeros, and mark them on bode plot as (c). 13](#_Toc122221796)

[3. Verify the compensation with hand calculation. 14](#_Toc122221797)

[(e) Closed-loop transfer function 15](#_Toc122221798)

[1. Please simulation the closed-loop DC transfer curve when input from 0 to 1.5V, and plot the closed-loop gain and mark the slope. 15](#_Toc122221799)

[2. Print .tf output to discuss the gain and input/output impedance. 15](#_Toc122221800)

[3. Please calculate the closed-loop DC gain with the real op-amp gain in your design. 15](#_Toc122221801)

[(f) Closed-loop AC response 16](#_Toc122221802)

[1. Please simulation the closed-loop AC response. Draw the bode plot and mark its DC gain and -3dB frequency. 16](#_Toc122221803)

[2. Put this bode plot with open-loop response and compare the results. 17](#_Toc122221804)

[(g) Closed-loop linearity response 18](#_Toc122221805)

[1. Please simulation the closed-loop THD when input with 0.7Vpp 10kHz sinusoidal waveform. (THD has to be smaller than -60dB). 18](#_Toc122221806)

[2. Please plot the input and output waveforms. 18](#_Toc122221807)

[(h) Closed-loop step response 19](#_Toc122221808)

[1. Please plot the output waveform when input with a step- from 0.3V to 1.2V, and a step+ from 1.2V to 0.3V, with rise/fall time of 10ns. 19](#_Toc122221809)

[2. Please mark slew rate (slope between 10% - 90% of final value), and the settling time (to within 10mV error) on your step+ and step- responses. 19](#_Toc122221810)

[3. Compare slew rate simulation results with hand calculation. 19](#_Toc122221811)

[(i) Closed-loop transfer function with diff R 20](#_Toc122221812)

[1. Print .tf output to discuss the gain and input/output impedance 20](#_Toc122221813)

[2. Please discuss the difference. 20](#_Toc122221814)

[(j) Discussion 21](#_Toc122221815)

[1. Please fill the following table. and discuss your design for frequency compensation and for best FoM. 21](#_Toc122221816)

1. Operation point

## Please DESIGN your bias (Mb1 - Mb3) and amplifier (M1 – M5) size to make the gain at DC larger than 60dB.

**表格 1 MOS size**

|  |  |  |
| --- | --- | --- |
|  | **W/L(m/m)** | **m** |
| **Mb1(pmos)** | 20/0.18 | 1 |
| **Mb2(pmos)** | 10/0.18 | 1 |
| **Mb3(pmos)** | 10/0.18 | 1 |
| **M1(pmos)** | 10/0.4 | 1 |
| **M2(pmos)** | 10/0.4 | 1 |
| **M3(nmos)** | 10/0.8 | 1 |
| **M4(nmos)** | 10/0.8 | 1 |
| **M5(nmos)** | 27.5/0.4 | 1 |

## Print out the results from .op command. And make sure all the devices are properly biased.

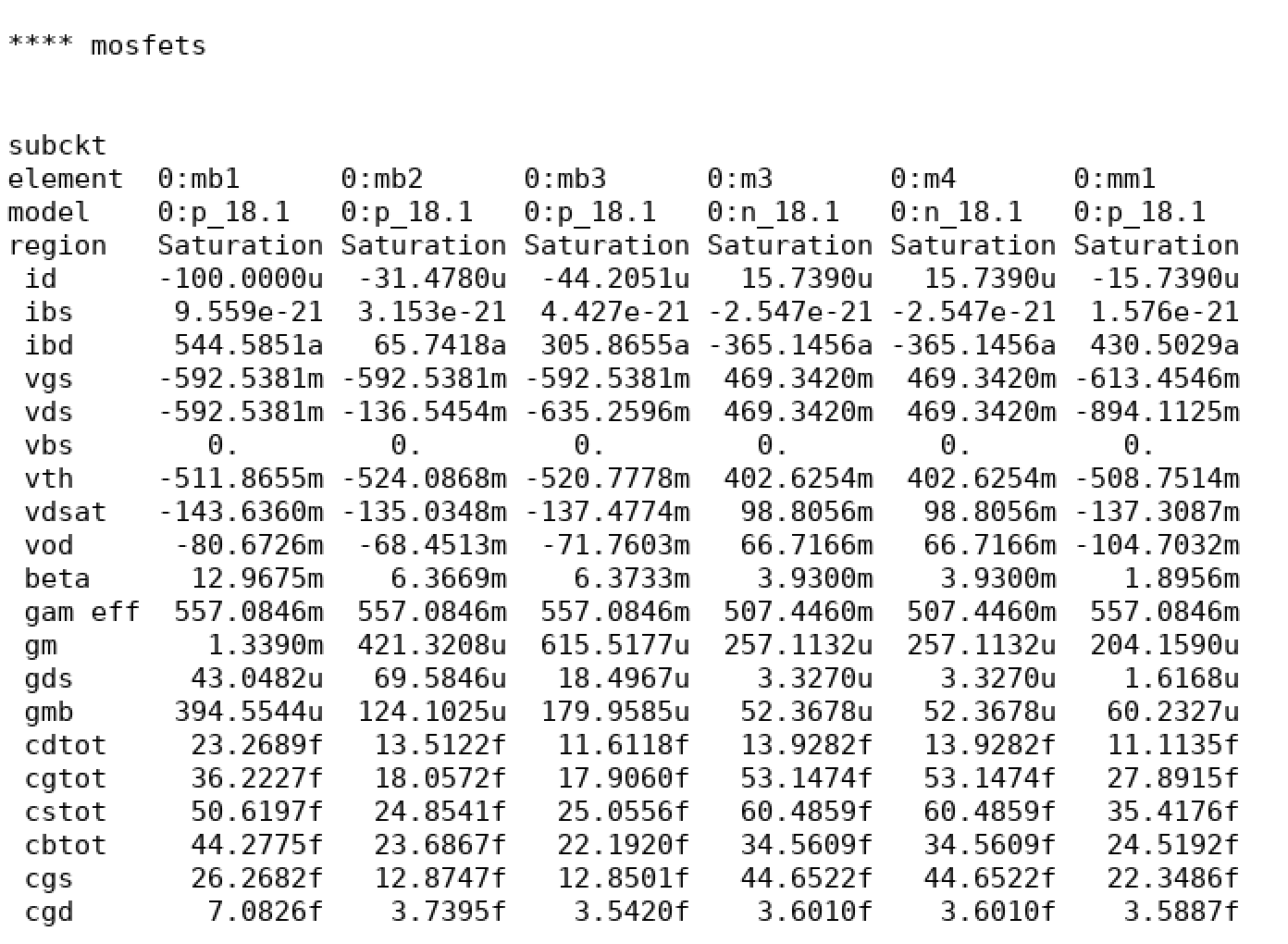
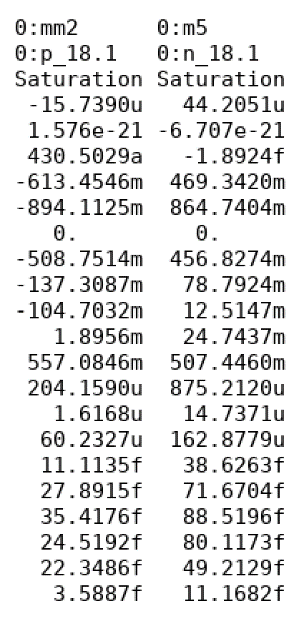


圖 1 lis file result(.op)



## Use .tf command to print out the voltage gain.

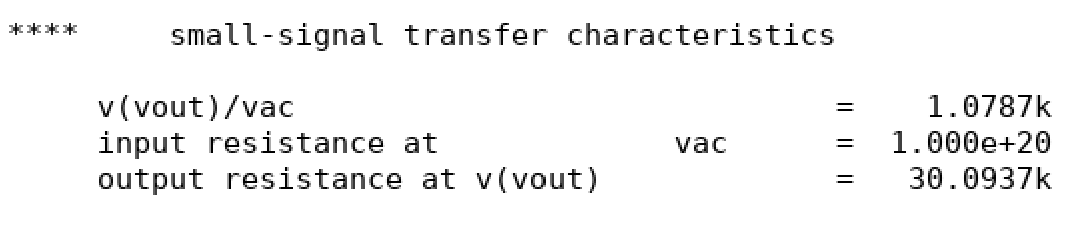
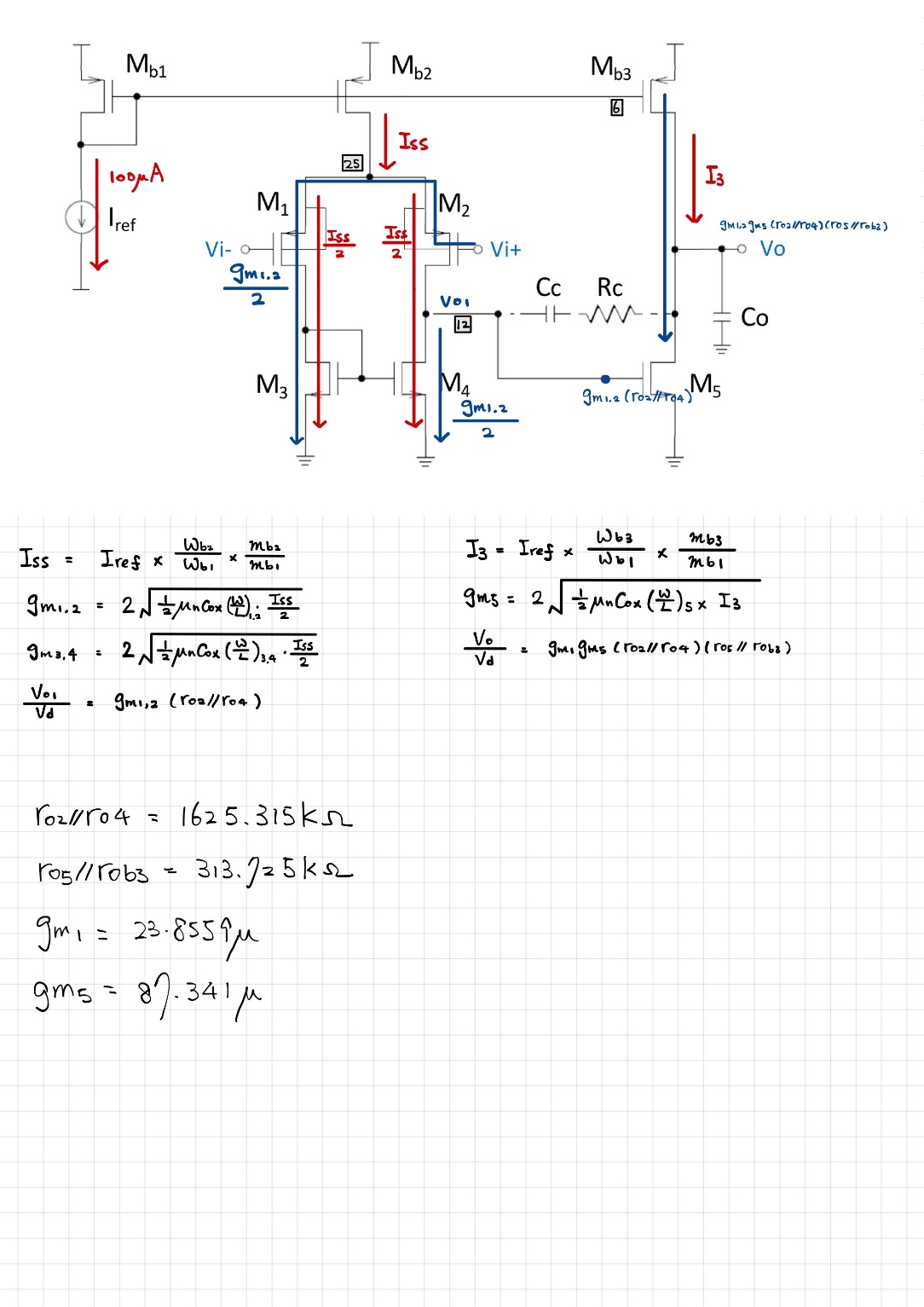


圖 2 lis file result(.tf)

## Verify your DC gain with hand calculation.



根據上頁.op result，可得:

**ro2=618.506K ; ro4=300.571K ;**

**ro5=67.856K ; rob3=54.064K**

**誤差值=**

1. AC response before compensation

# Please simulate and plot the frequency response (magnitude and phase) of your design in (a). Mark the (i) DC gain (ii) unity gain frequency, and (iii) phase margin on figure.

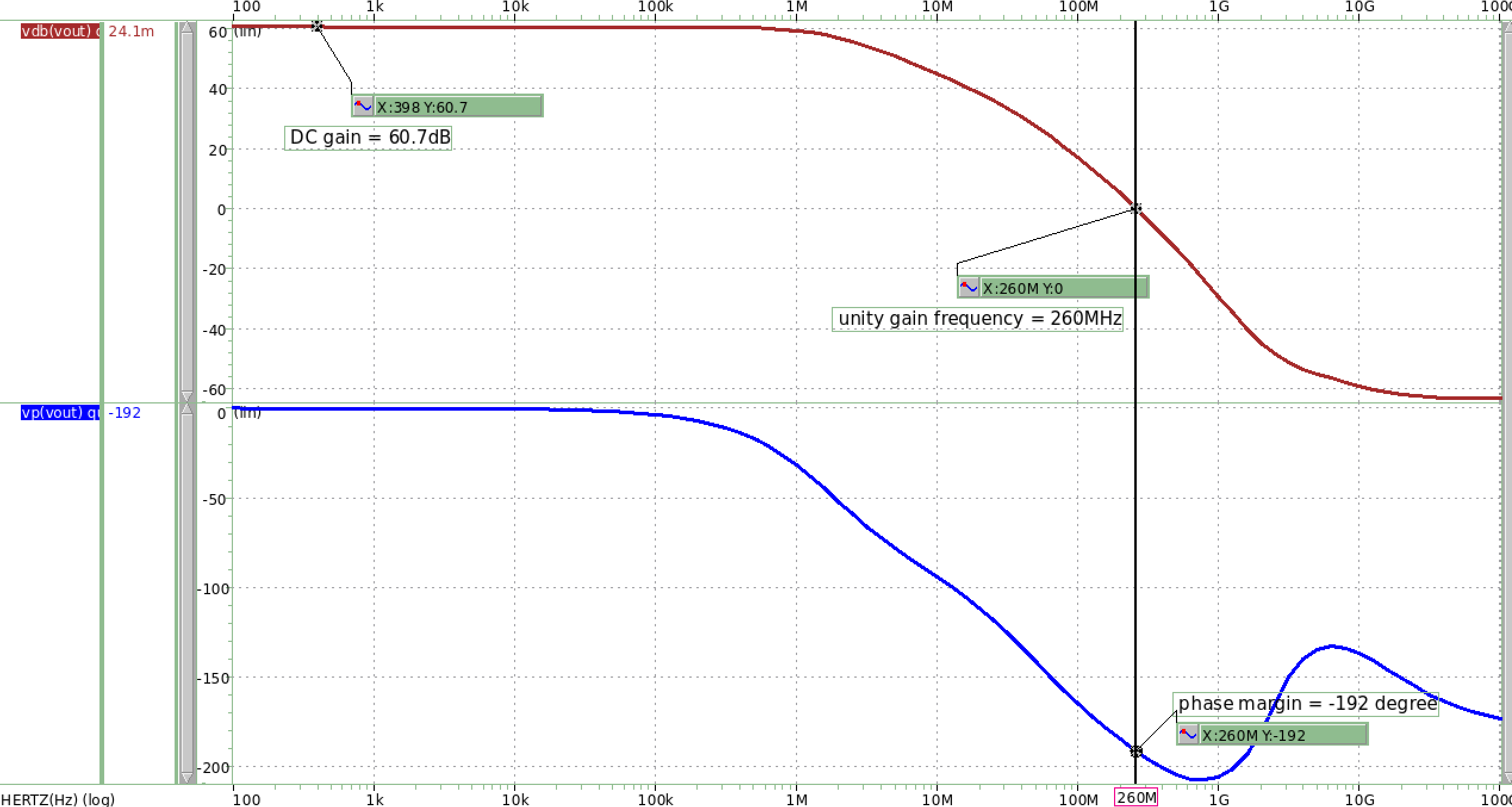
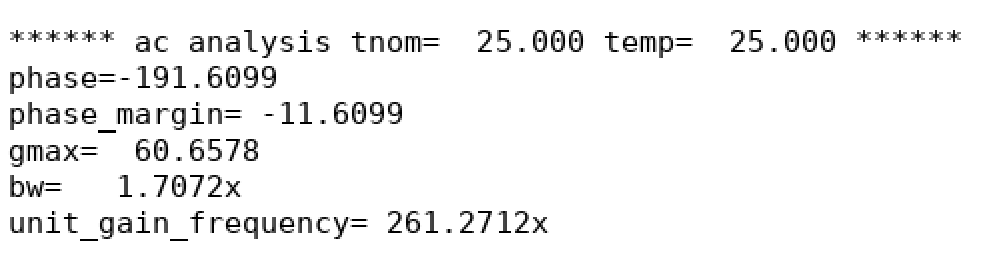


圖 3 frequency response



**DC gain=60.7dB ;**

**unity gain frequency=261.27MHz ;**

**Phase margin=-12 degree**

# Use .pz to identify the poles and zeros, and mark them on bode plot.

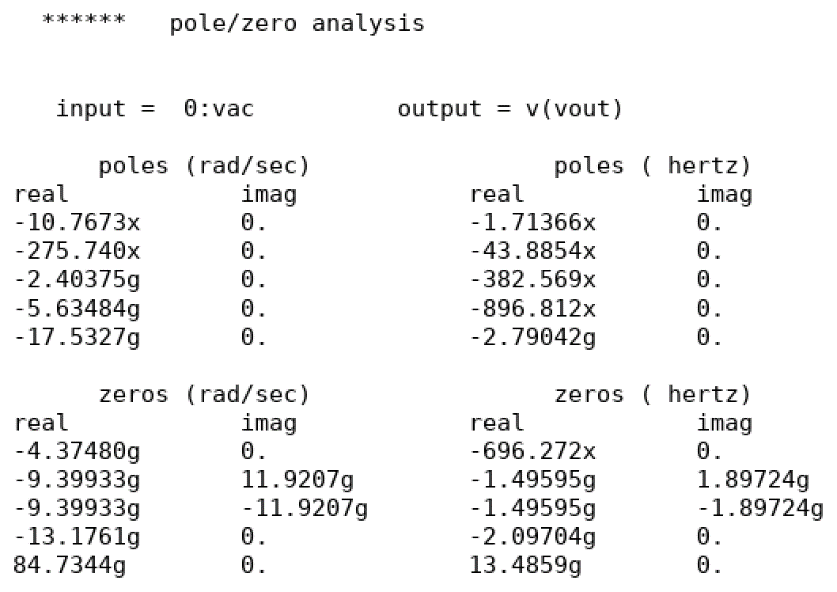


圖 4 .pz result

|  |  |  |
| --- | --- | --- |
| **First pole** | **Second pole** | **Zero** |
| 1.714MHz | 43.89MHz | 13.485GHz |



圖 5 bode plot

# Verify the first and second dominant poles and first RHP zeros with hand calculation.

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|  |  |  |  |
| --- | --- | --- | --- |
|  | **Simulation** | **Hand Calculate** | **誤差值** |
| **Pole1** | 1.7MHz | 2.2MHz | 29% |
| **Pole2** | 43.9MHz | 10.58MHz | 76% |
| **zero** | 13.49GHz | 12.47GHz | 7.5% |

1. AC response after Cc compensation

### Please design your value of Cc and simulate the AC response in (b). (please note, your Cc must be smaller than 10pF, and the phase margin must larger than 0 in this case).

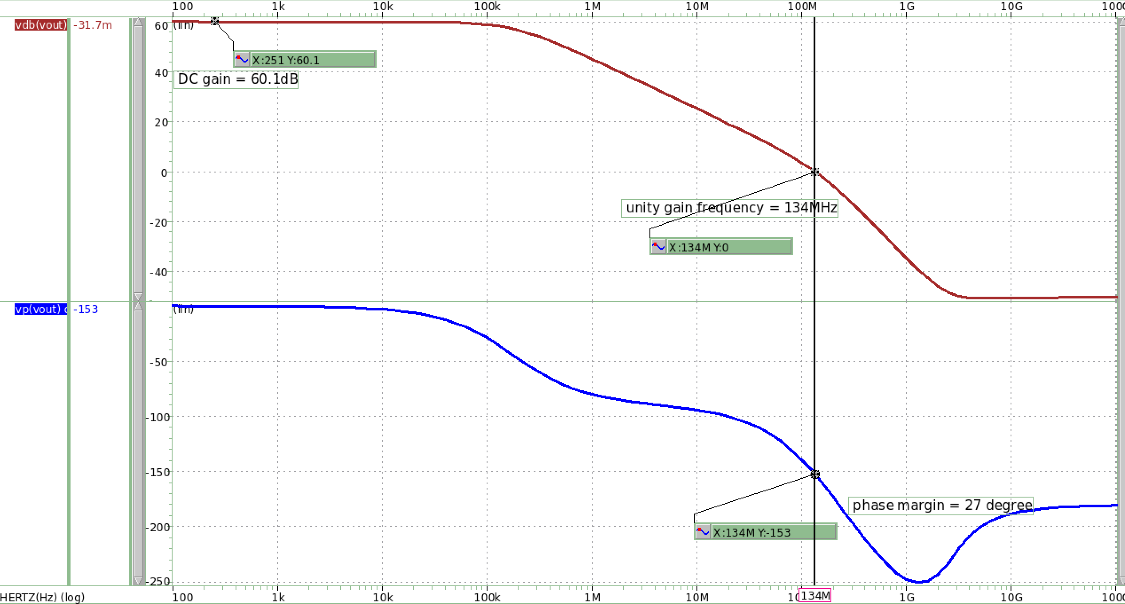
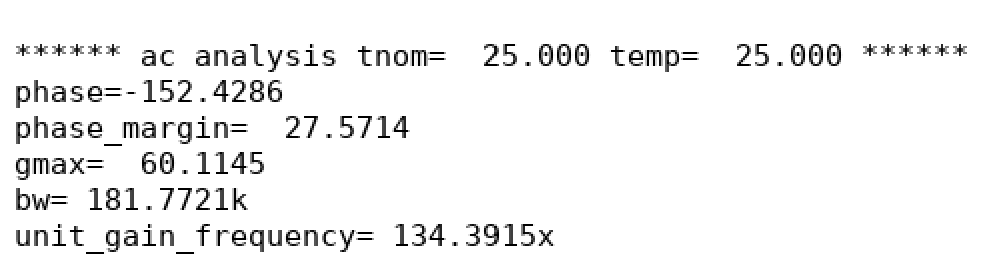
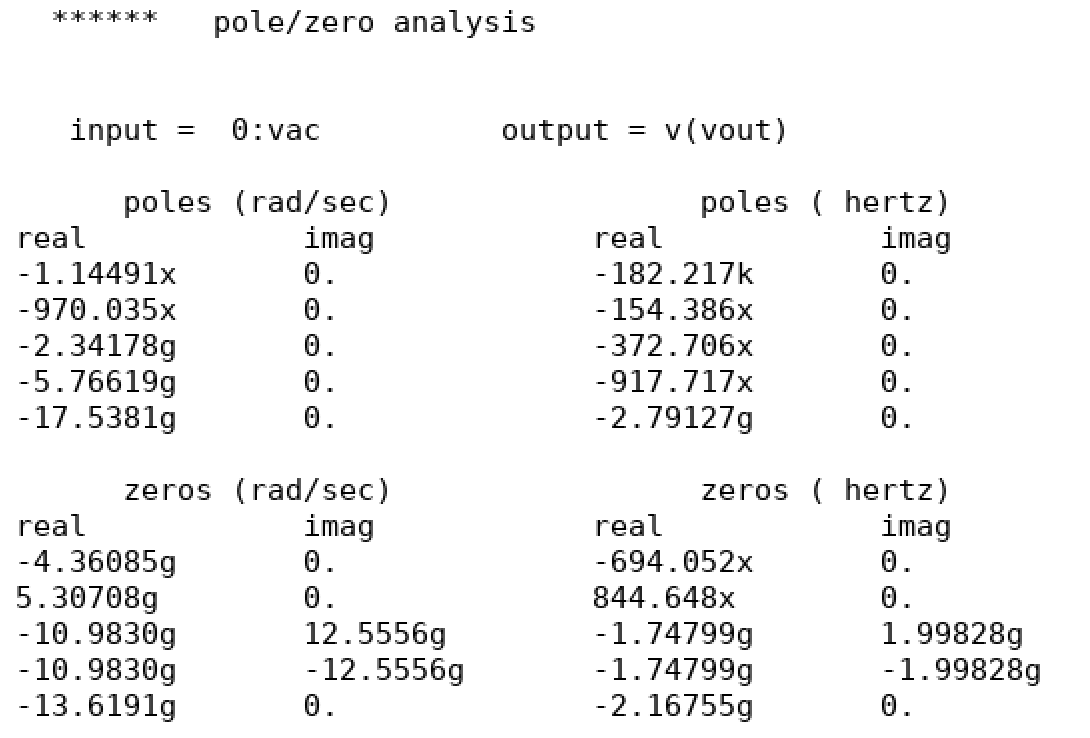


圖 6 frequency response



**Design Cc=0.15pf, phase margin=27.57∘→meet the requirement**

### Please print .pz output of the new poles (first and second dominant) and zeros (first RHP), and mark them on bode plot.

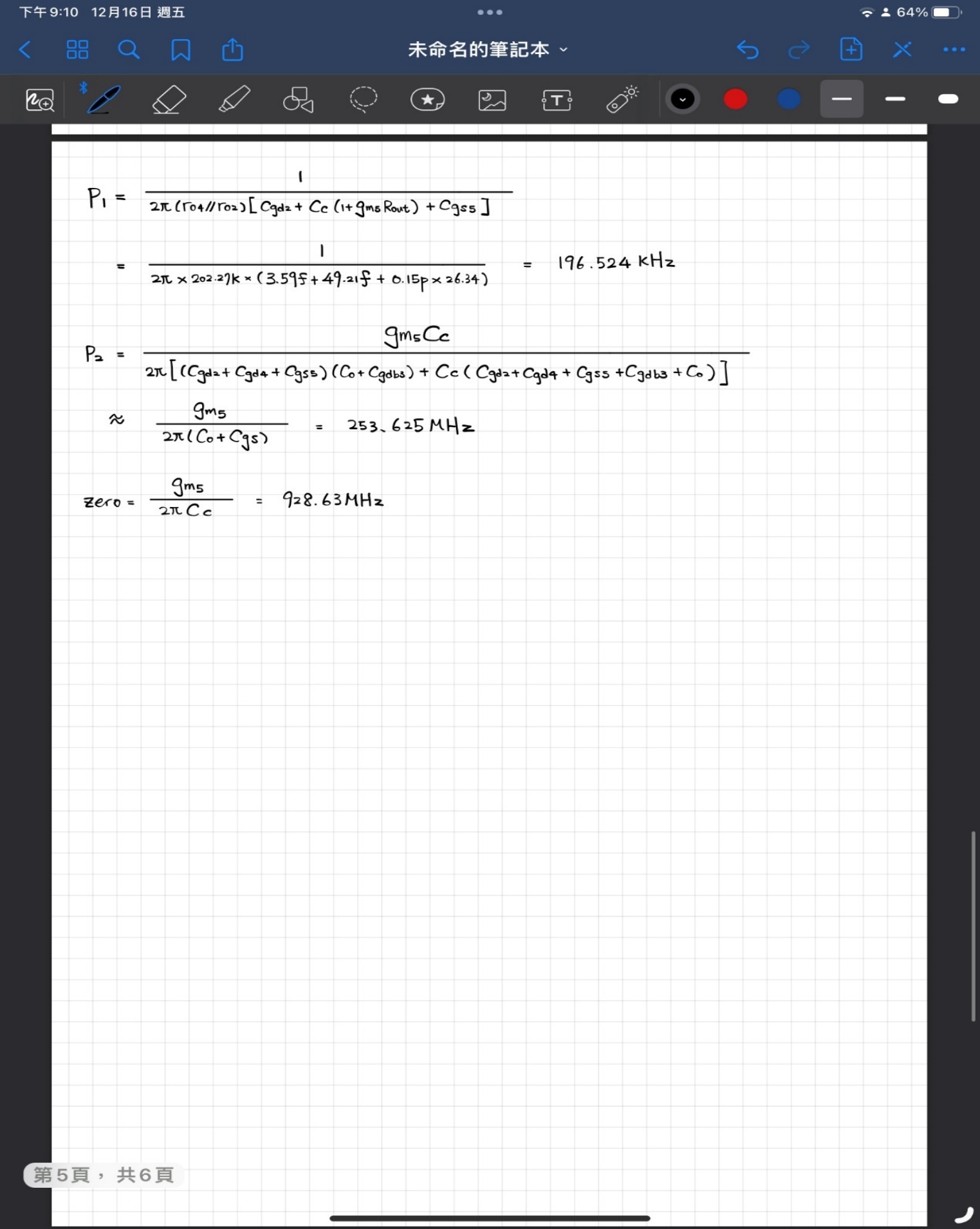


|  |  |  |
| --- | --- | --- |
| **First pole** | **Second pole** | **Zero1** |
| 182.217kHz | 154.386MHz | 844.65MHz |



圖 7 bode plot

### Verify the compensation with hand calculation.



|  |  |  |  |
| --- | --- | --- | --- |
|  | **Simulation** | **Hand Calculate** | **誤差值** |
| **Pole1** | 182.217KHz | 196.254KHz | 7.7% |
| **Pole2** | 154.386MHz | 253.625MHz | 64.3% |
| **zero** | 844.65MHz | 928.63MHz | 10% |

1. AC response after Cc-Rc compensation

#### Please design your value of Rc to shift the RHP zero and simulate the AC response in (c). (please note, your unity gain frequency must be larger than 50MHz and phase margin must larger than 45 in this case).

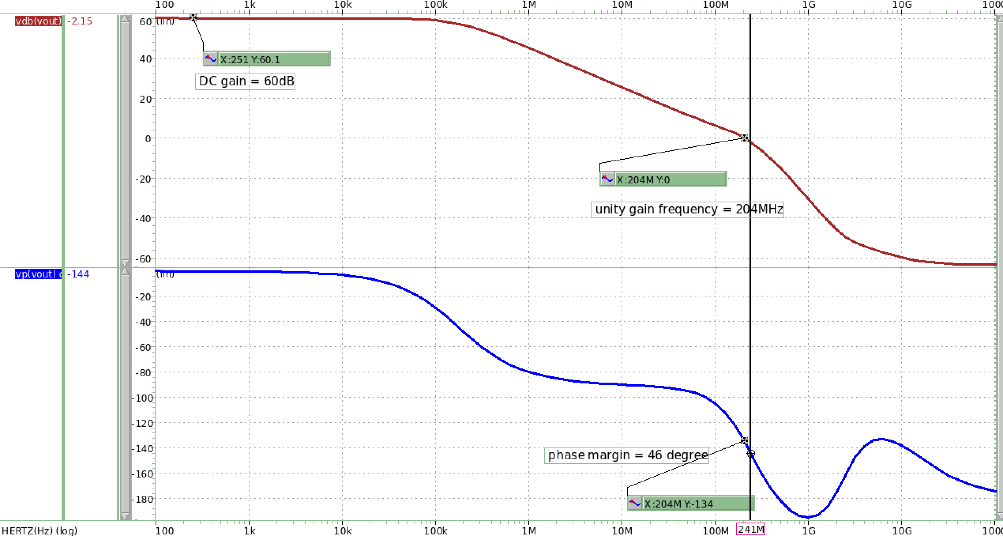
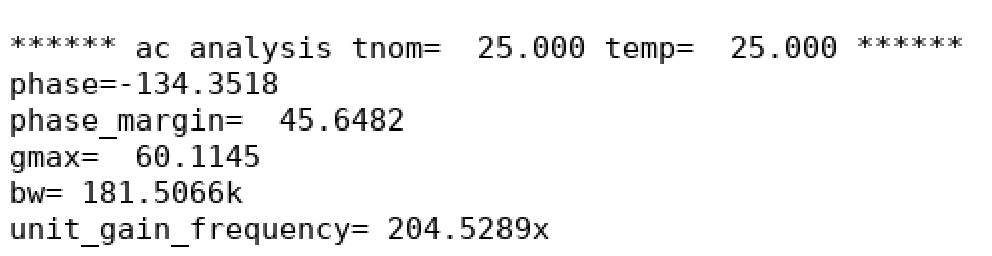


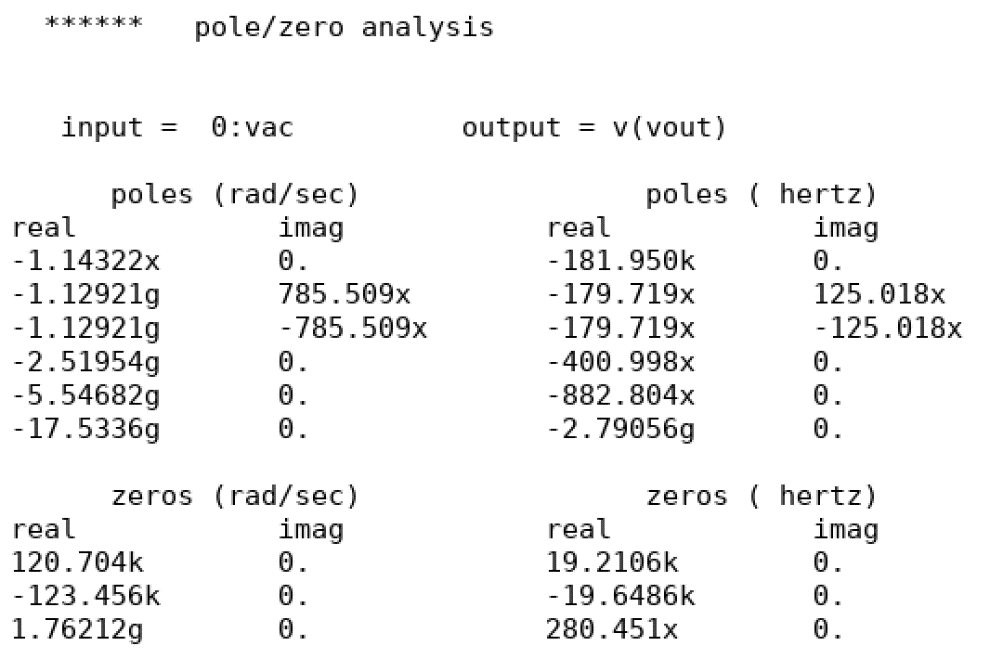
圖 8 frequency response



**Cc=0.15pf and Rc=9.5K, unit gain frequency=204.53MHz ;**

**phase margin=45.65∘→meet the requirement**

#### Please print .pz output of the new poles and zeros, and mark them on bode plot as (c).



|  |  |  |
| --- | --- | --- |
| **First pole** | **Second pole** | **Zero** |
| 181.95kHz | 401MHz | 280.45MHz |

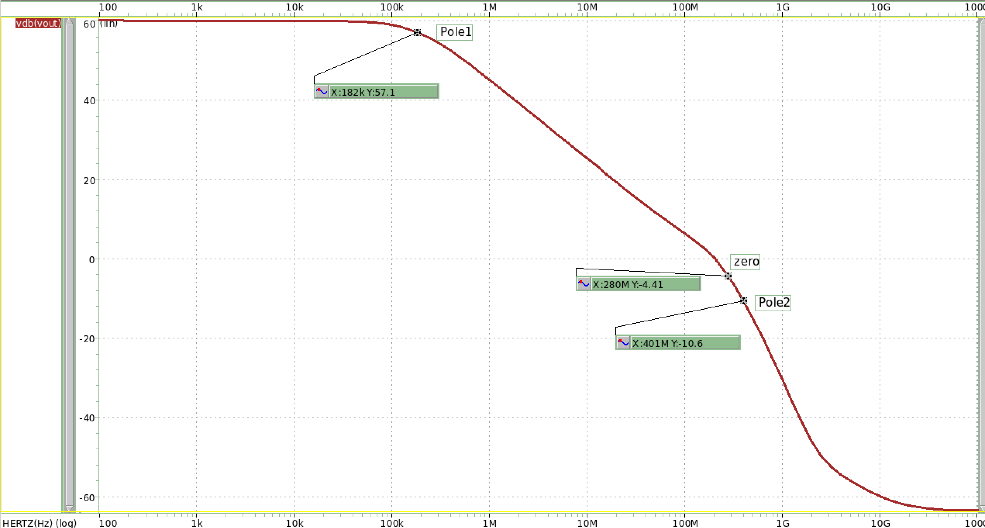
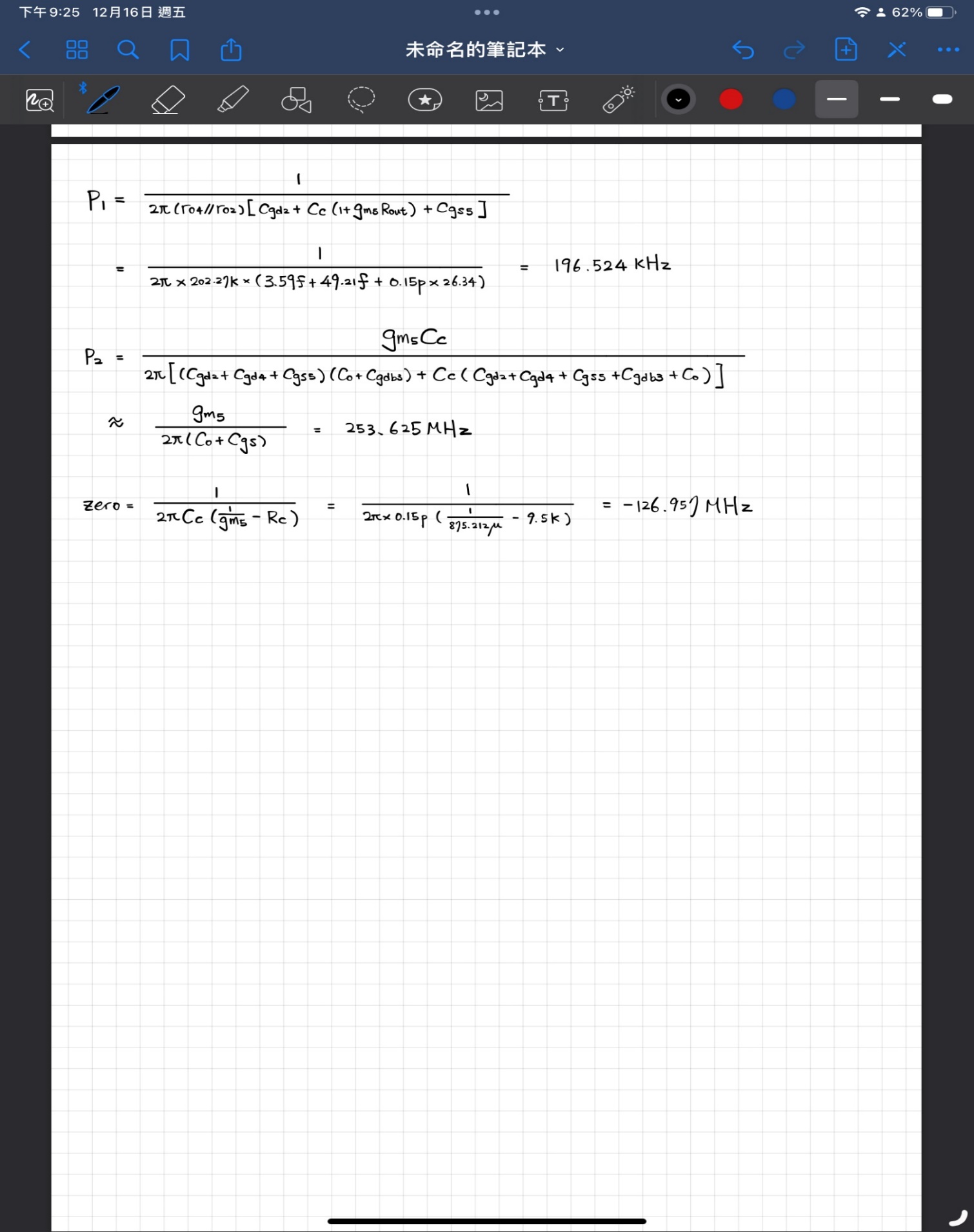


圖 9 bode plot

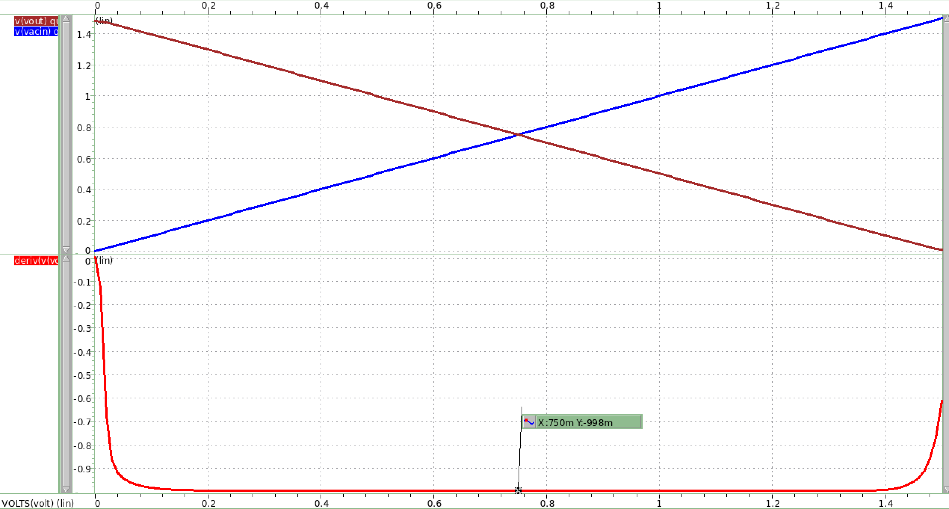
#### Verify the compensation with hand calculation.



|  |  |  |  |
| --- | --- | --- | --- |
|  | **Simulation** | **Hand Calculate** | **誤差值** |
| **Pole1** | 182.217KHz | 196.254KHz | 7.7% |
| **Pole2** | 401MHz | 253.625MHz | 36.75% |
| **zero** | 280.45MHz | 126.957MHz | 54.73% |

1. Closed-loop transfer function

##### Please simulation the closed-loop DC transfer curve when input from 0 to 1.5V, and plot the closed-loop gain and mark the slope.



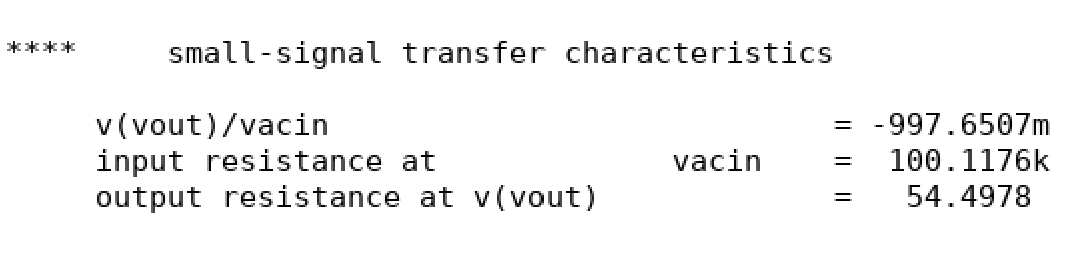
Slope = -998m

IN

OUT

圖 10 DC transfer curve

##### Print .tf output to discuss the gain and input/output impedance.



##### Please calculate the closed-loop DC gain with the real op-amp gain in your design.

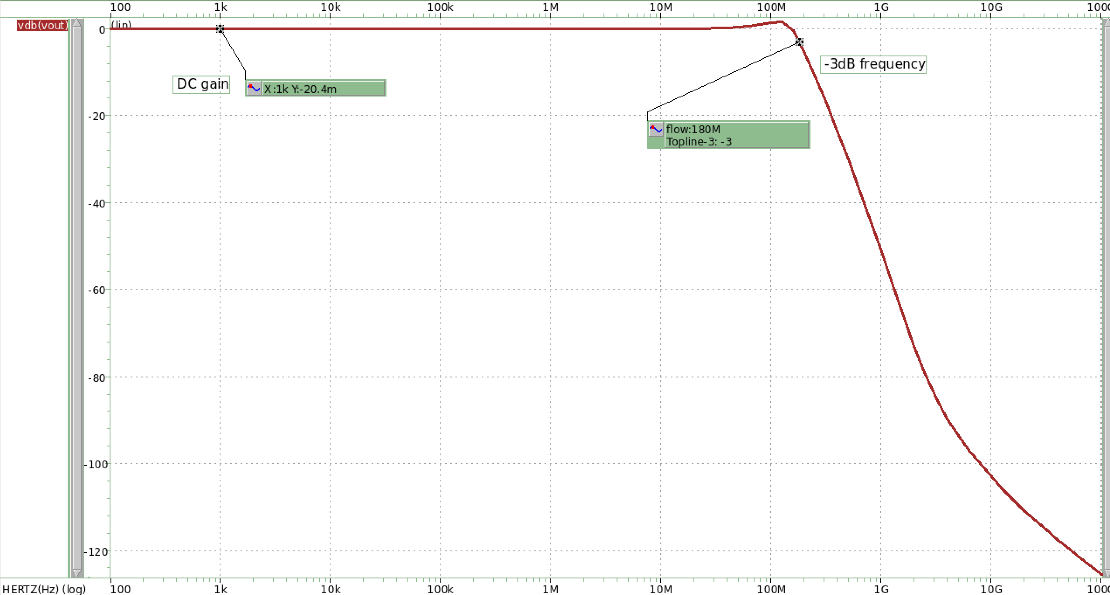
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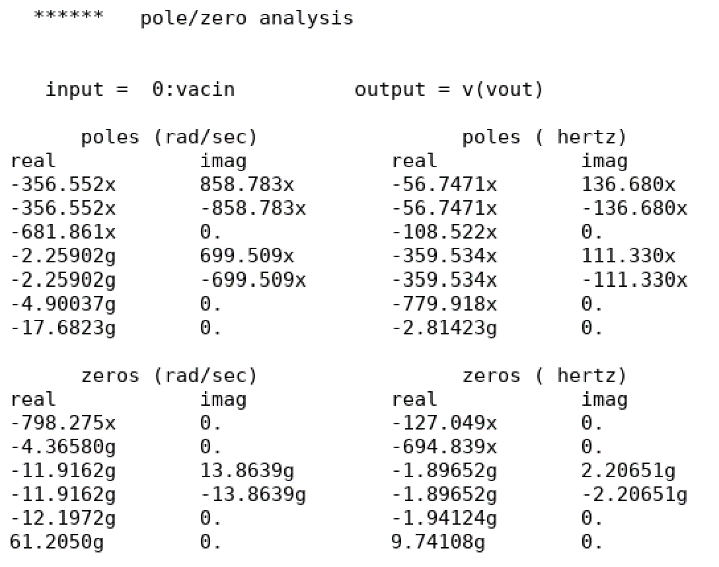
|  |  |  |
| --- | --- | --- |
| **Simulation** | **Hand Calculate** | **誤差值** |
| -0.9977 | -0.9981 | 0.05% |

1. Closed-loop AC response

###### Please simulation the closed-loop AC response. Draw the bode plot and mark its DC gain and -3dB frequency.



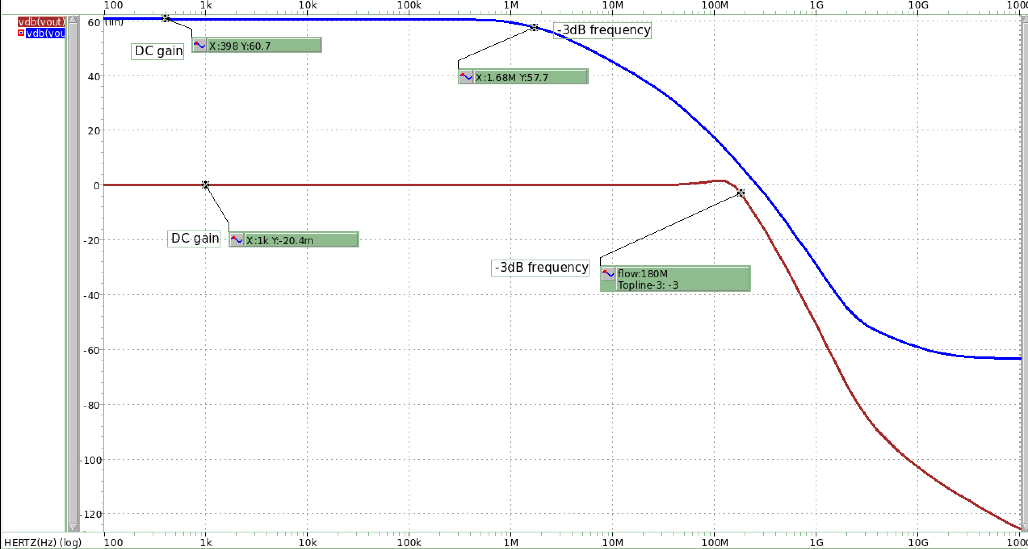
**DC gain = -20.4mdB ; -3db frequency = 180MHz**

****

|  |  |  |
| --- | --- | --- |
| **First pole** | **Second pole** | **Zero** |
| 148MHz | 376MHz | 9.7GHz |

****

###### Put this bode plot with open-loop response and compare the results.



|  |  |  |
| --- | --- | --- |
|  | **DC gain** | **-3DB frequency** |
| **Closed loop** | -20.4mdB | 180MHZ |
| **Open loop** | 60.7dB | 1.68MHz |

1. Closed-loop linearity response
2. Please simulation the closed-loop THD when input with 0.7Vpp 10kHz sinusoidal waveform. (THD has to be smaller than -60dB).

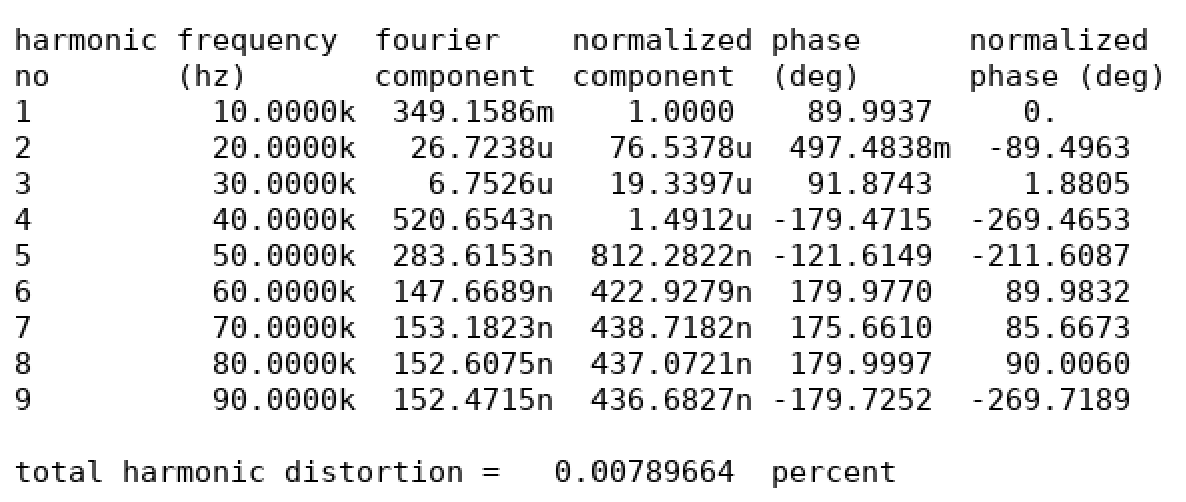
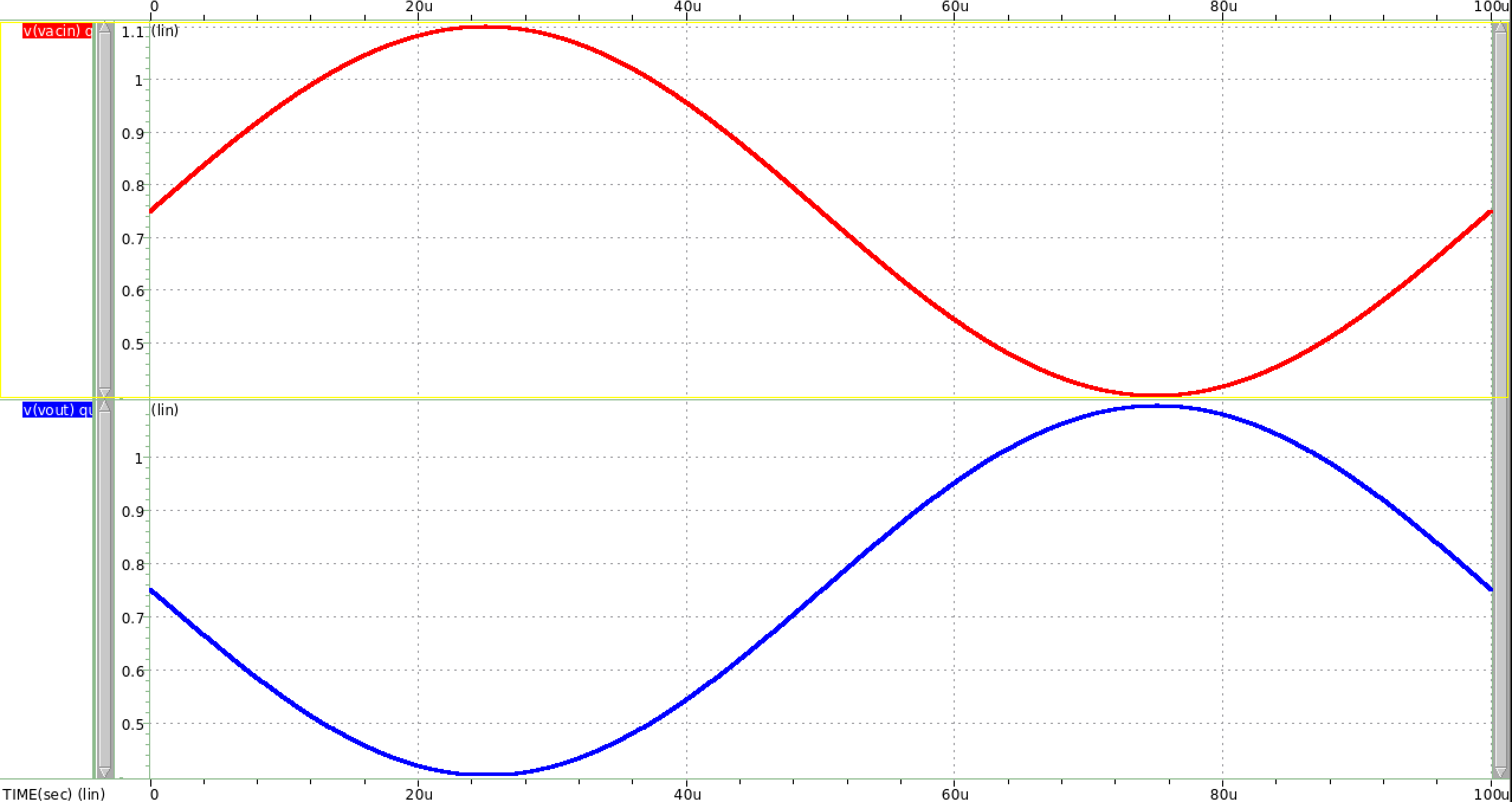


圖 11 THD result

**THD = -83.1dB**

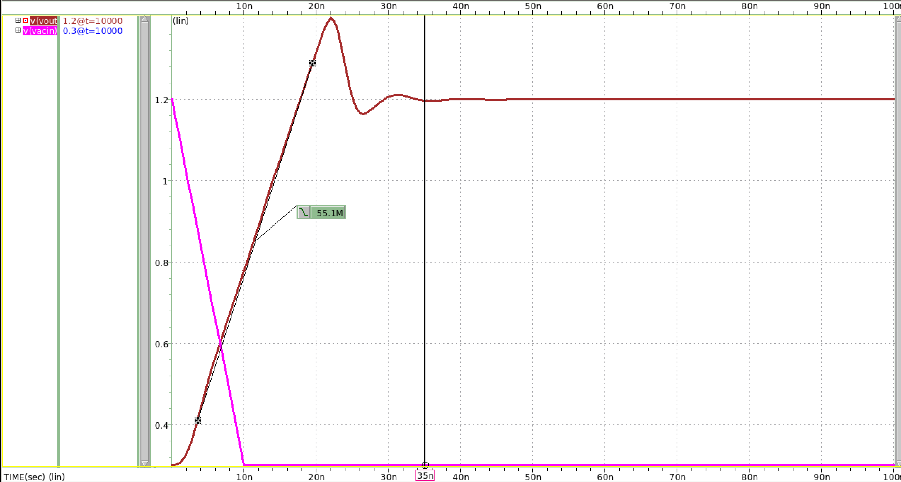
1. Please plot the input and output waveforms.



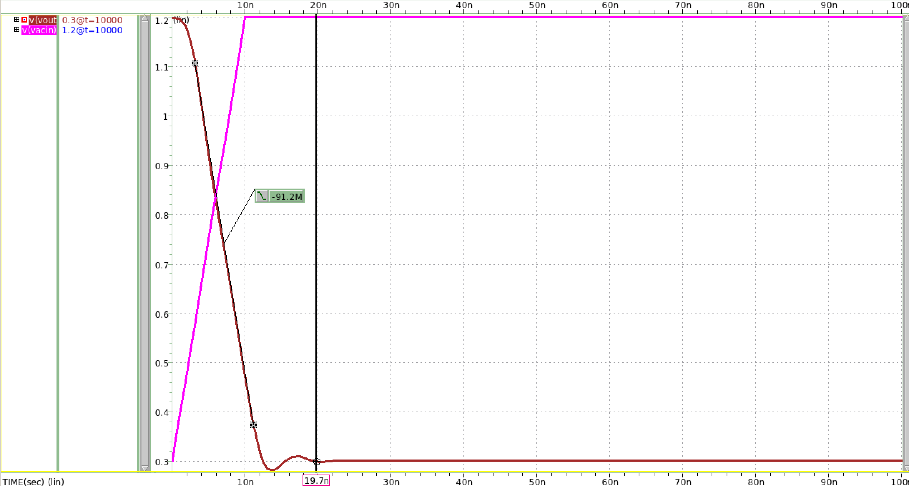
**OUTPUT**

**INPUT**

1. Closed-loop step response
2. Please plot the output waveform when input with a step- from 0.3V to 1.2V, and a step+ from 1.2V to 0.3V, with rise/fall time of 10ns.
3. Please mark slew rate (slope between 10% - 90% of final value), and the settling time (to within 10mV error) on your step+ and step- responses.



Slew Rate = 55.1M

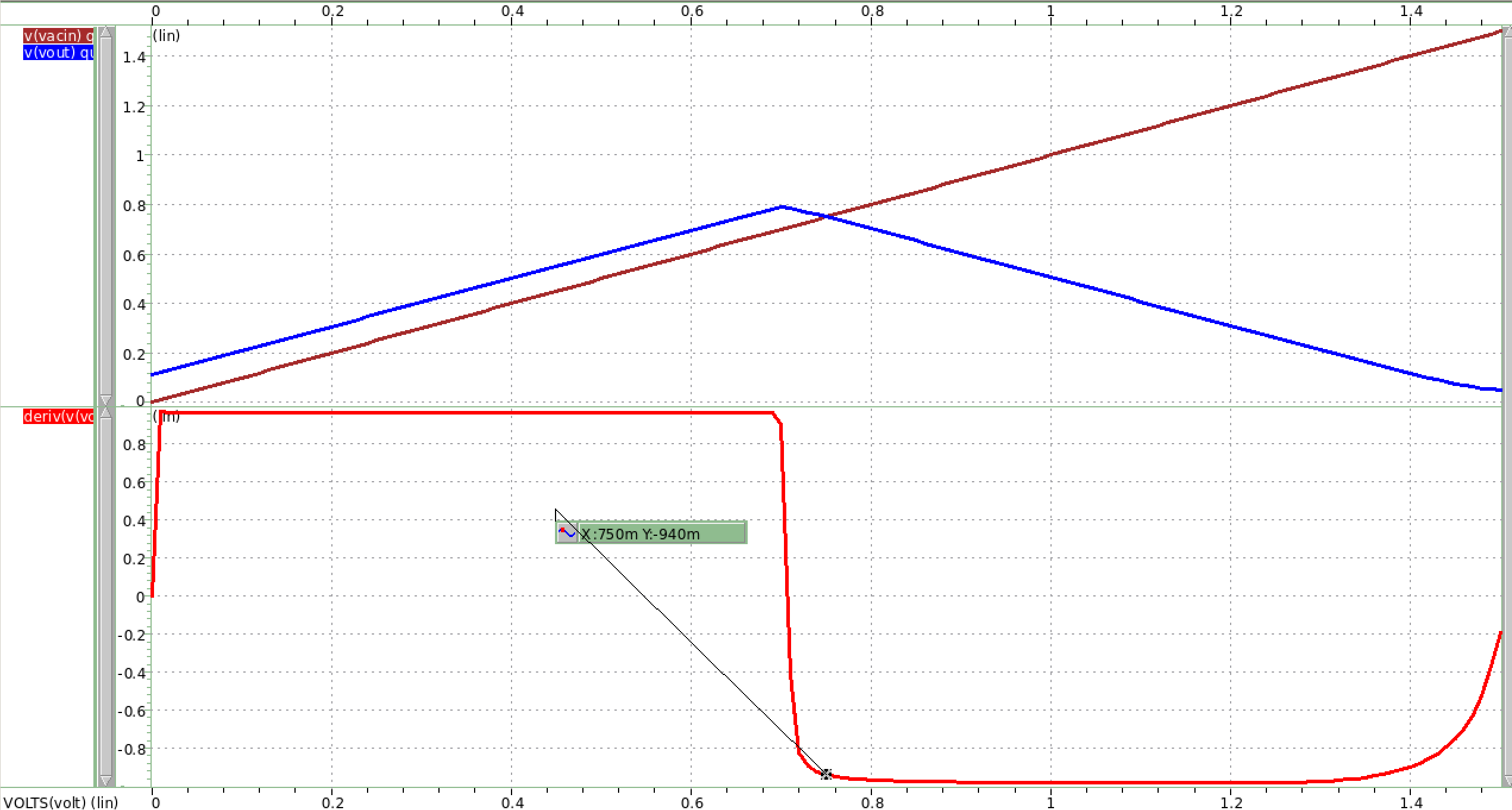


Slew Rate = -91.2M

1. Compare slew rate simulation results with hand calculation.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **Simulation** | **Hand Calculate** | **誤差值** | **settle time** |
| **SR+ ()** | 55.1M | 209.85M | 280.85% | 35ns |
| **SR- ()** | -91.2M | -62.96M | 30.96% | 19.7ns |

1. Closed-loop transfer function with diff R
2. Print .tf output to discuss the gain and input/output impedance



Slope = -940m

IN

OUT

圖 12 transfer curve

1. Please discuss the difference.

**Ri、Rf 為1k時，Vout transfer curve與Ri、Rf 為100k時不同，在Vin=0-0.75間，無法上升到VDD。**

**推測是因放大器回授增益因Ri、Rf電阻降低而降低，表現較不理想。**

**回授增益Af = Ao/1+Aoβ，而其中β=1/Rf，若Rf不夠大，將導致Af =1/β，會變成與open loop無關，直接由β決定電路回授增益。**

1. Discussion
2. Please fill the following table. and discuss your design for frequency compensation and for best FoM.

|  |  |  |
| --- | --- | --- |
| **VDD** | **1.5V** | |
| **IDD (total current exclude of Imb1) \*1** | **75.683 μA** | |
| **Imb2,Imb3** | **31.478 μA** | **44.205 μA** |
| **Rc, Cc(<10pF)** | **9.5K** | **0.15pF** |
| **Open-loop performance(after final compensation)** | | |
| **DC gain(>60dB)** | **60.1dB** | |
| **Unity gain frequency \*2** | **204.53MHz** | |
| **Phase margin** | **45.65** | |
| **Closed-loop performance(after final compensation)** | | |
| **T.H.D** | **-83.1dB** | |
| **S.R.+ \*3** | **55.1 V/μS** | |
| **S.R.- \*4** | **-91.2V/μS** | |
| **Settling time** | **35ns** | |
| **Figure of merit(after final compensation)** | | |
| **\*2/\*1** | **2.7** | |
| **\*3/\*1** | **0.73** | |
| **\*4/\*1** | **1.21** | |

**這次主要分為slew rate、unity gain frequency、IDD三者關係去調便FOM。**

**調大slew rate方法為小Cc和大電流，Cc小有助於slew rate的表現，但會使得phase margin表現變差，較容易使電路不穩定。而大電流就要看到底是slew rate成長幅度較大還是電流下降程度較多。**

**至於Rc的功能，是用於使零點頻率更大，zero =，Rc越大，便可使zero落在左半平面，phase margin會更穩定;反之若zero落在右半平面，會使電路不穩定，輸出將有可能發散。**

**實際測試幾組下來，發現此次作業的電流太小，弊大於利。固本次作業在做取捨時選擇捨棄電流，採取大電流大頻寬大slew rate的設計方向設計。**