**國立清華大學**

**Analog Circuit Design**



**Homework 5**

**Common Mode Feedback**

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Operation point for CKT B

# Please design your amplifier M1, M2, M3, M4, RF, and input common mode level to achieve differential mode DC gain of 35(V/V), common mode DC gain smaller than 0.05 (V/V), and the output common mode level of 1.0V.

|  |  |  |
| --- | --- | --- |
|  | **W/L(μm/μm)** | **m** |
| **M1** | 15/0.5 | 1 |
| **M2** | 15/0.5 | 1 |
| **M3** | 40/1.2 | 5 |
| **M4** | 40/1.2 | 5 |
| **MS** | 4.7/1 | 2 |
| **RF** | 305K | |
| **Common model level** | 0.78V | |

**電壓大小設計:**

在設計時，我先決定好VX電壓，為使MS操作在飽和區，**電壓不可小於0.52，否則MS將截止**;至於VX最大值的設計，因VX越大，MOS size 就要越小，以滿足tail current = 30μA的條件，若mos size太小將影響到其他mos可調整的彈性，故在設計VX值時，我並沒有設計太大，約落在0.53到0.6之間去做設計調整。

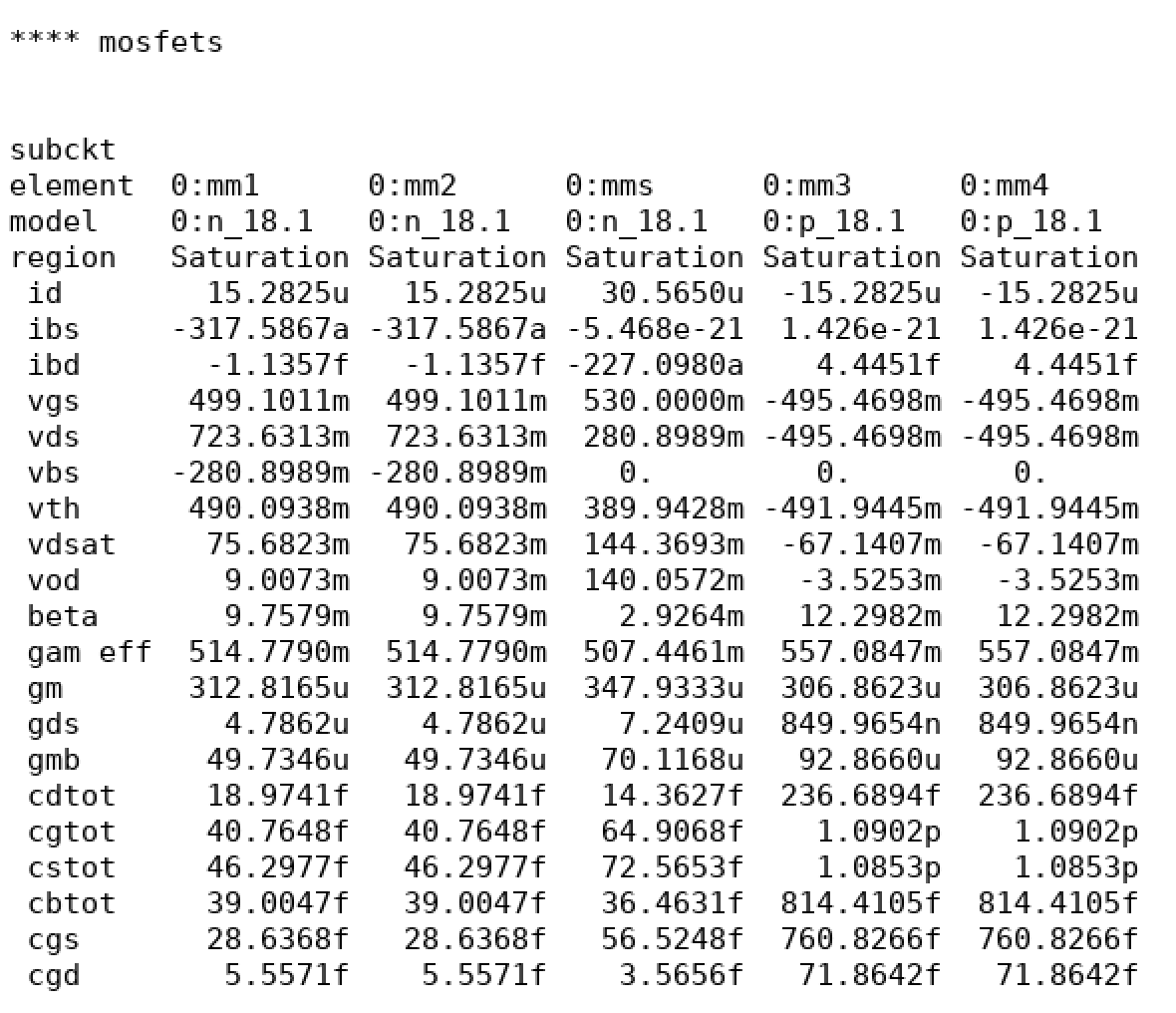
決定好VX後，接著是調整MS size 使tail current = 30μA，便可開始決定common mode level，**其值不可小於MS的drain voltage + Vt1，否則M1、M2將截止，同時也不可太大，太大的話將導致M1、M2進入線性區**。

**Gain調變:**

需同時考慮differential mode和common mode，兩個gain公式分別如下:

gm1越大，可使Ad變大，Acm變小。而ro1越小對Acm越好，但會使Ad變小，且因電流固定故調整空間不大，在設計時，先滿足使Acm<50m(V/V)，再調變RF使Ad=35(V/V)，會較有效率。

# Print out the small signal parameters using .op command.



Tail current=30μA meet the requirement

# Please use .tf command to simulate the differential and common mode gain, and print out the results.

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自動產生的描述

圖 1 differential mode gain

**Gain = 35.088(V/V)**

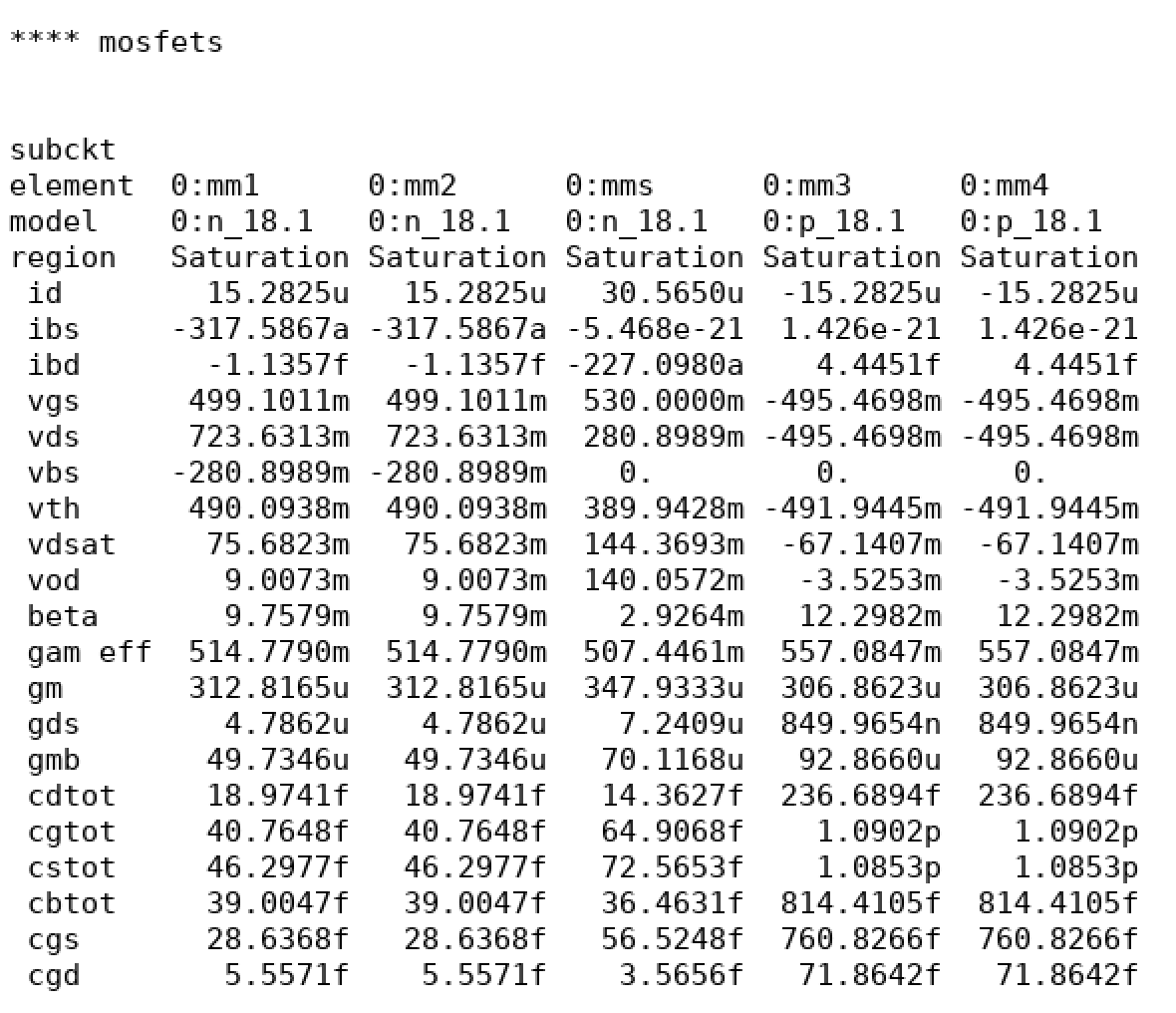
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圖 2 common mode gain

**Gain = 9.92m (V/V)**

# Please calculate the differential mode and common mode gains with the small-signal model.



**ro1 = ro2 = 208.934K**

**ro3 = ro4 = 1176.518K**

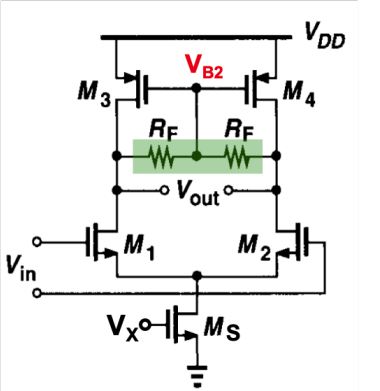
**ros = 138.104K**

**gm1 = gm2 = 312.8165μ**

**gm3 = gm4 = 306.8623μ**

**Differential gain:**

**Common gain:**

****

VA

Vo1

|  |  |  |  |
| --- | --- | --- | --- |
|  | **Simulation** | **Hand calculates** | **Error** |
| **Differential gain** | **35.0886** | **35.0893** | **0.00002%** |
| **Common gain** | **0.0099** | **0.0115** | **16.16%** |

Operation point for CKT A

# Based on the design in (a), please design the bias voltage VB1 to achieve the output common mode level of 1.0V.

**VB1 Design:**

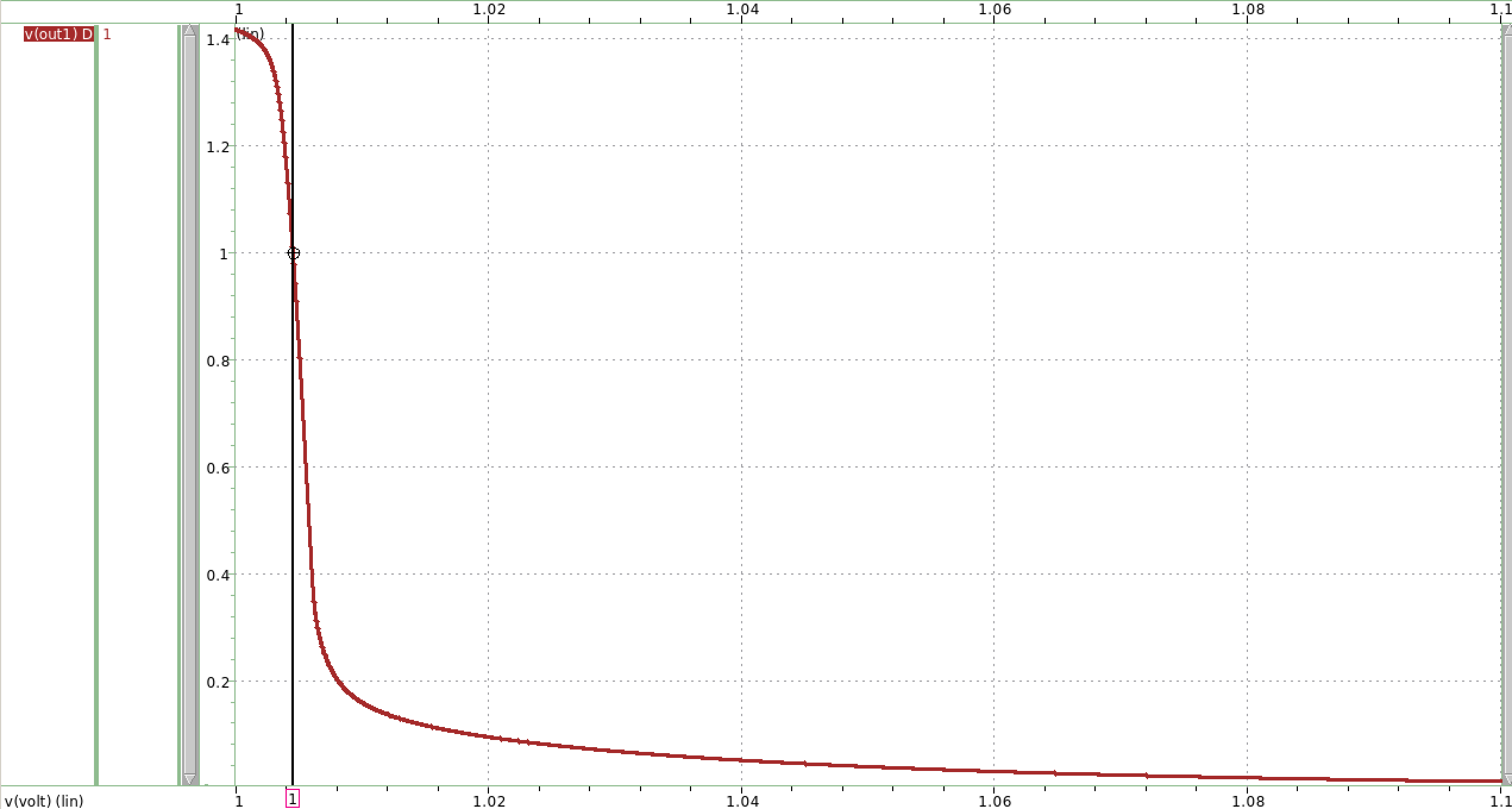
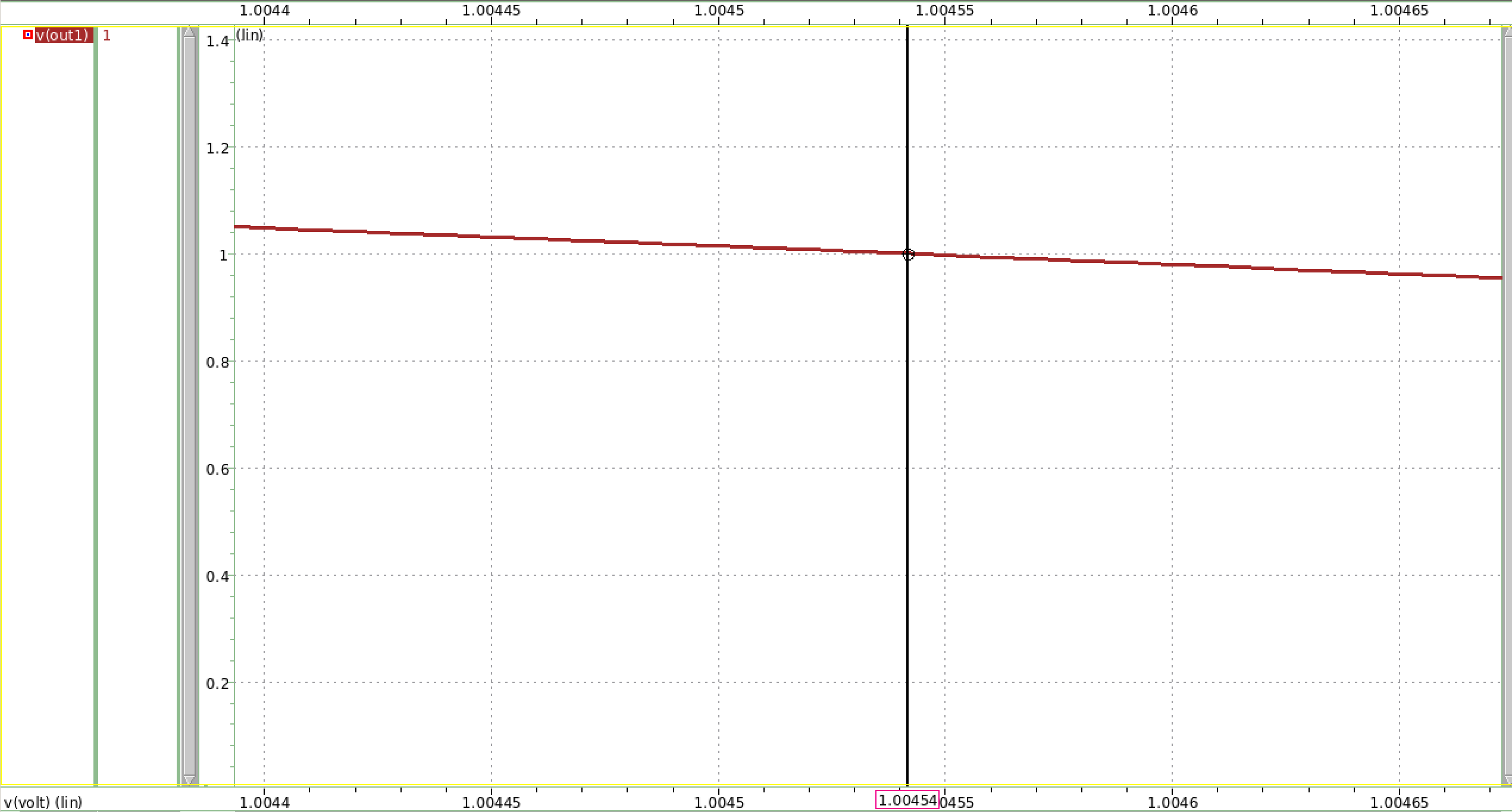


圖 3 sweeping VB1 to find the value

**利用sweep VB1變數，找出output common mode level = 1V時的VB1值。**

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**得到當VB1=1.0051，output common mode level = 1V。**

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自動產生的描述**

**模擬後，結果為output common mode level = 1V。**

# Please compare the feedback voltage VB1 with the bias voltage VB2 in (B).

**Net18 = VB1(circuit A) = 1.0045**

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**Net18 = VB2(circuit B) = 1.0045**

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自動產生的描述

Circuit B因有RF，而gate端電流為0，故兩端電壓相等，output voltage = pmos gate voltage (VB2)= 1.0045。

而Circuit A因沒有RF，output voltage 並不會等於pmos gate voltage (VB1)，但很剛好的是，上題利用dc sweep找出的VB1，恰好等於Circuit B output voltage的值，且在設計VB1過程，發現只要調變一點點，Output voltage就會改變很多。

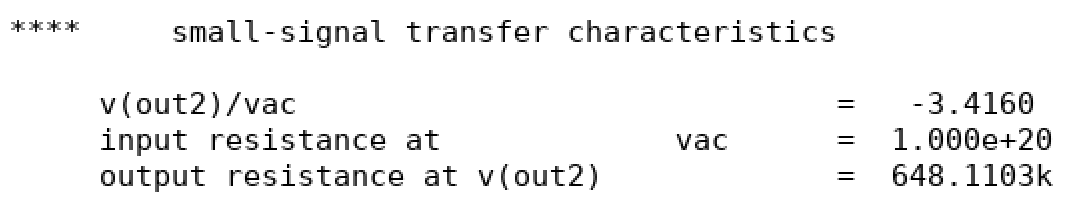
# Please use .tf command to simulate the differential and common mode gain, and print out the results.

**Differential gain:**

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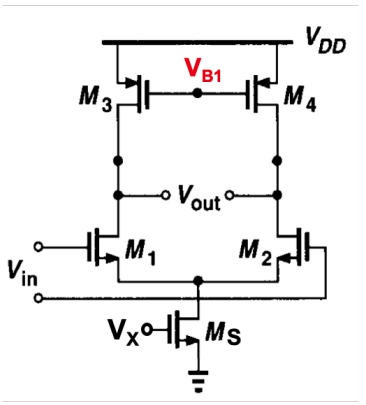
**Common gain:**



# Please calculate the differential mode and common mode gains with the small-signal model.

**Differential gain:**

**Common gain:**



|  |  |  |  |
| --- | --- | --- | --- |
|  | **Simulation** | **Hand calculates** | **Error** |
| **Differential gain** | **-55.495** | **-55.501** | **0.01%** |
| **Common gain** | **-3.416** | **-4.15** | **21.49%** |

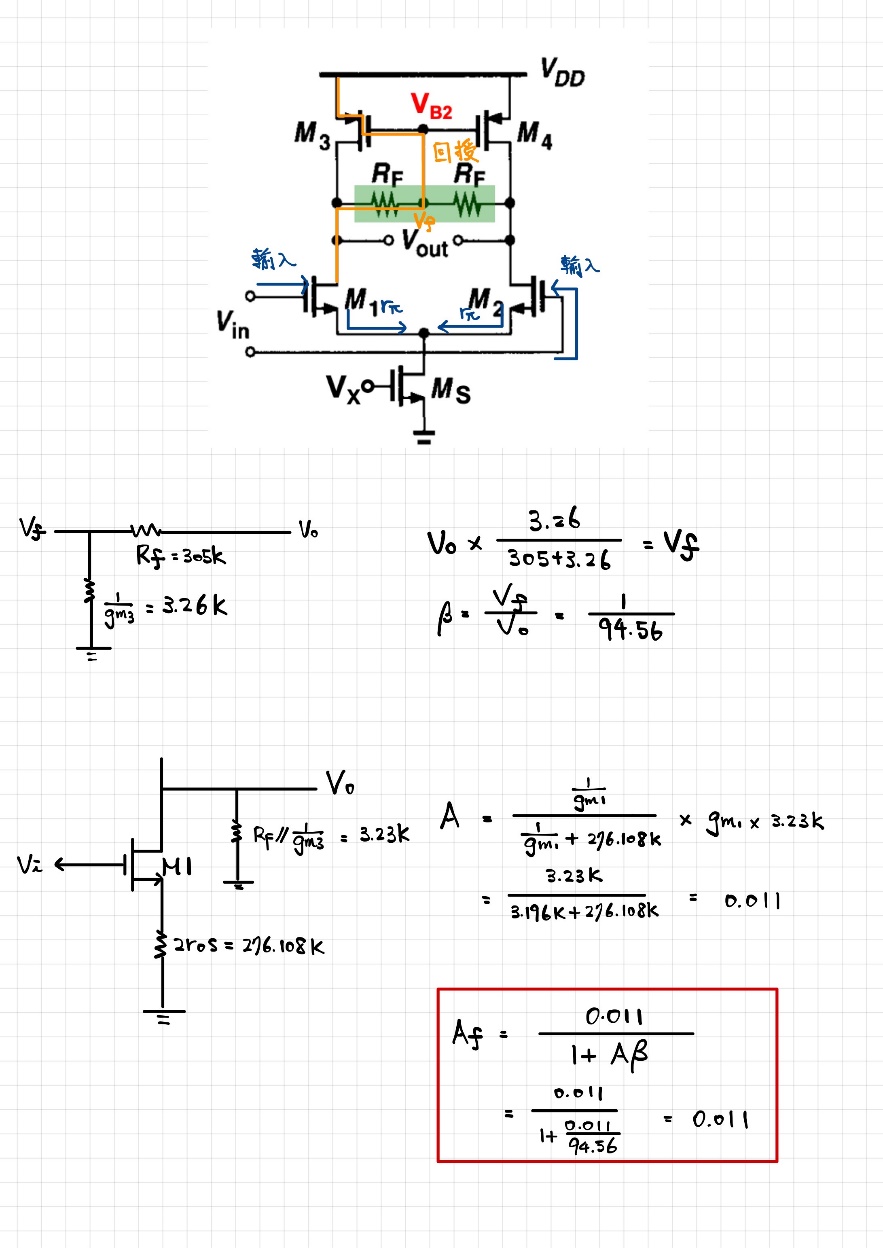
Discussion

# Please discuss the precision requirement for the bias voltage VB1.

加入VB1的目的，是為了穩定直流點。若直流工作點不穩定，將導致小訊號參數、小訊號增益等誤差很大，無法預測電路行為，故需要加入VB1穩定common output level。在設計時，通常欲加入的直流電壓會剛好等於有feedback resistance時的該點電位。

加入適當的VB1雖可使common output voltage趨近於1V，但仍無法像有feedback的電路一樣完全相等，

# Please also use the feedback concept to calculate this common mode gain.



|  |  |  |  |
| --- | --- | --- | --- |
| Working item | specification | Simulation result | Hand calculation |
| Vdd | 1.5V |  |  |
| Tail current Iss | 30μA | 30.565μ |  |
| Output common mode | 1.0V | 1.0045 |  |
| Differential voltage gain(V/V) | 35 | 35.089 |  |
| Common voltage gain (V/V) w/o CMFB |  | 3.416 | 4.15 |
| Common voltage gain (V/V) wi CMFB | <0.05 | 0.0092 | 0.0115 |
| Ms(W/LN x m) |  | 4.7μ/1μ x 2 |  |
| M1, M2(W/L x m) |  | 15μ/0.5μ x 1 |  |
| M3, M4(W/L x m) |  | 40μ/1.2μ x 5 |  |
| RF | Kohm | 305 |  |
| VB1 | V | 1.0045 |  |
| VB2 | V | 1.0045 |  |