國立清華大學

超大型積體電路設計 VLSI Design

國立清華大學

NATIONAL TSING HUA UNIVERSITY

Homework 5

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目錄

1. Please design a 4 bit binary synchronous up counter with clock frequency CLK = 200MHz, VDD = 1.8V (default) , VSS = 0V. You can use any architecture to complete the design. Try to minimize the power consumption of the counter. You can adjust the value of VDD for minimizing the power meanwhile the counter works correctly, and the maximum glitch should be less than 80ps.

(a) Please describe how you design the counter and how to reduce the glitch and power consumption of counter.

Counter Design

設計想法:

將一個一次只加 1 的電路(incrementer)與暫存器電路結合，即可實現 counter 計數器功能。概念圖如左下，其增值表如右下。

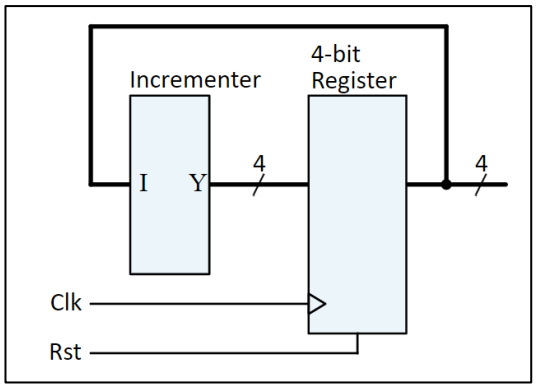


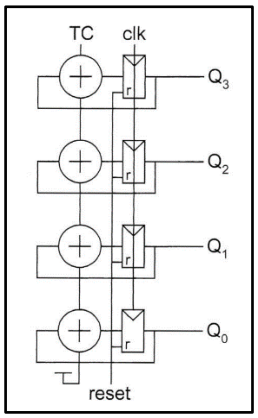
圖 1 synchronous counter

I_3	I_2	I_1	I_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	1	0	1	0
1	0	1	0	1	0	1	1
1	0	1	1	1	1	0	0
1	1	0	0	1	1	0	1
1	1	0	1	1	1	1	0
1	1	1	0	1	1	1	1
1	1	1	1	0	0	0	0

圖 2 synchronous counter truth table

實際設計電路:

參考講義上的 synchronous counter，本次作業以下圖為實際設計電路。



此電路組成，左邊為 half adder，提供 carry bit 和 sum bit，右邊則為 D Flip-Flop，提供暫存功能，每個 Flip-Flop 一次暫存 1 bit。

Schematic :

左下圖為 4 bits synchronous up counter，其中 DFF 沿用上次作業的設計，half adder 為右上圖，half adder 內部的 XOR gate 則為左下圖。

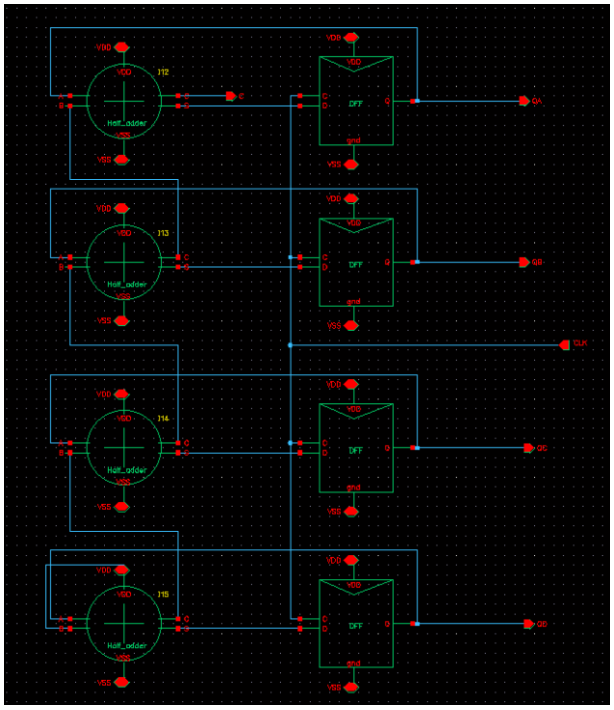


圖 3 4 bits synchronous up counter

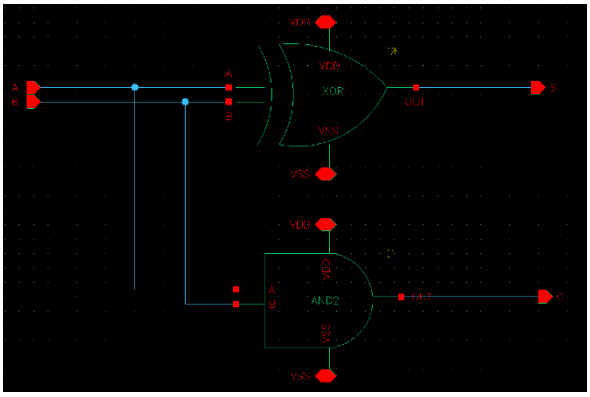


圖 4 half adder

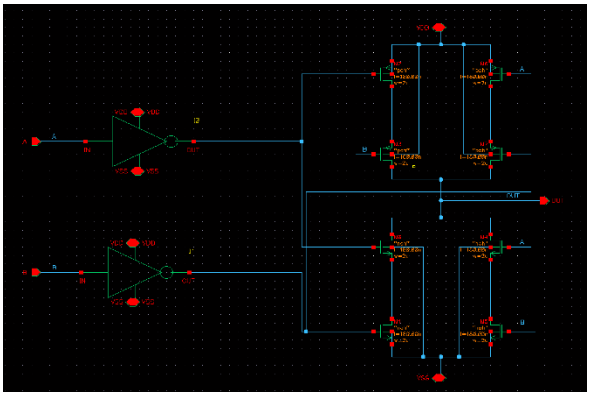


圖 5 XOR gate

設計完成後，模擬結果如下:

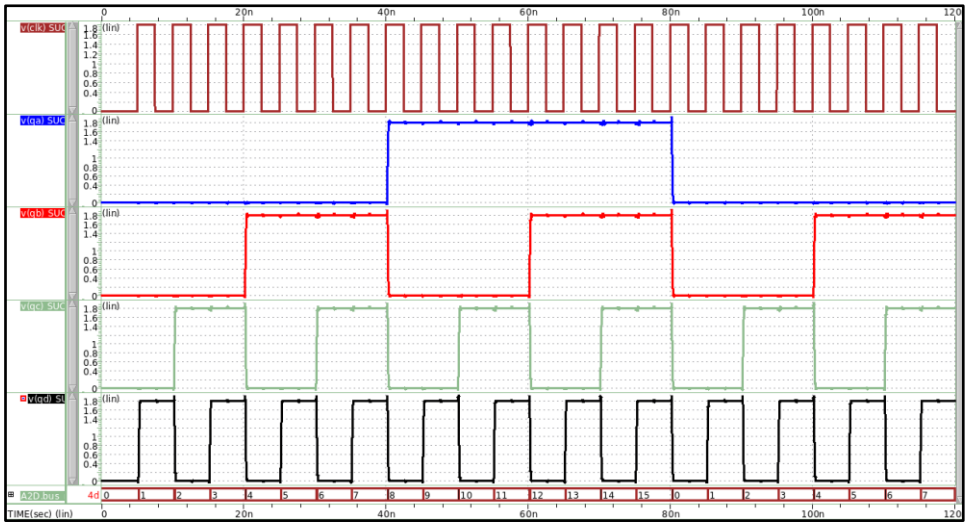


圖 6 4 bits synchronous up counter waveview

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
glitch1_2=  36.6799p  targ=  10.2968n   trig=  10.2601n
glitch3_4=  36.8311p  targ=  20.2979n   trig=  20.2611n
glitch5_6=  36.6419p  targ=  30.2975n   trig=  30.2608n
glitch7_8=  36.9010p  targ=  40.2971n   trig=  40.2602n
glitch9_10=  36.6806p  targ=  50.2969n   trig=  50.2602n
glitch11_12=  36.7982p  targ=  60.2978n   trig=  60.2610n
glitch13_14=  36.6717p  targ=  70.2969n   trig=  70.2602n
glitch15_0 = 396.3038f  targ=  80.2973n   trig=  80.2969n
pvdd=-412.4095u  from=   0.             to= 120.0000n
```

Glitch 皆發生在 odd number to even number 之間，從 truth table 可以解釋此現象，因 1 to 2(0001 →0010)、3 to 4(0011 →0100)、 5 to 6(0101 →0110)…等，皆不只一個 bit 轉態，且每個 bit 轉態時間不同，導致 glitch 現象(1 to 2 中間出現 3、3 to 4 中間出現 7…等)。

Glitch and power consumption reducing way

1. Reduce power consumption 的方法:

   降低 transistor size。將 transistor size(以 unit inverter 為例)設為 pmos width=0.6μm;nmos width=0.3μm。模擬後如下:

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
glitch1_2=  47.1119p  targ=  10.2755n   trig=  10.2284n
glitch3_4=  47.1851p  targ=  20.2757n   trig=  20.2285n
glitch5_6=  47.1297p  targ=  30.2753n   trig=  30.2282n
glitch7_8=  47.4101p  targ=  40.2759n   trig=  40.2285n
glitch9_10=  47.1724p  targ=  50.2764n   trig=  50.2293n
glitch11_12=  47.3275p  targ=  60.2757n   trig=  60.2284n
glitch13_14=  47.2000p  targ=  70.2754n   trig=  70.2282n
glitch15_0 = 357.8739f  targ=  80.2769n   trig=  80.2766n
pvdd=-127.9099u  from=   0.             to= 120.0000n
```

   Power consumption=127.9μ;

   Power consumption 從原本的 412.4095μ 降低到 127.9099μ，但 glitch 增加了，因 glitch 發生的原因是 current state 轉態時間(falling time)與 next state 轉態時間(rising time)存在 delay。

2. Glitch reduce:

   因 glitch 發生的原因是 current state 轉態時間(falling time)與 next state 轉態時間(rising time)存在 delay。故要降低 glitch time 須提高 pull down network 的能力(reduce falling time)，將 nmos width 增加即可做到。我將 XOR gate 的 nmos width=1.25μm，其餘不變，模擬結果如下:

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
glitch1_2= 128.7492f  targ=  10.3385n   trig=  10.3384n
glitch3_4= 586.5219f  targ=  20.3387n   trig=  20.3382n
glitch5_6= 147.5524f  targ=  30.3384n   trig=  30.3383n
glitch7_8= 657.6079f  targ=  40.3391n   trig=  40.3384n
glitch9_10= 324.8772f  targ=  50.3388n   trig=  50.3385n
glitch11_12= 465.6200f  targ=  60.3387n   trig=  60.3382n
glitch13_14= 188.5074f  targ=  70.3387n   trig=  70.3385n
glitch15_0= 668.1028f  targ=  80.3390n   trig=  80.3383n
pvdd=-168.6429u  from=   0.             to= 120.0000n
```

   Glitch 降至 femto 等級，雖然 power consumption 有略微上升，但仍比最一開始設計時表現還佳。

(b) Please list the glitch in each number (0 ~ 15) and find the maximum glitch.

Number to number	Glitch Value	Glitch Time
0-1	NA	0s
1-2	3	128.75fs
2-3	NA	0s
3-4	7	586.52fs
4-5	NA	0s
5-6	7	147.55fs
6-7	NA	0s
7-8	15	657.61fs
8-9	NA	0s
9-10	11	324.88fs
10-11	NA	0s
11-12	15	465.62fs
12-13	NA	0s
13-14	15	188.51fs
14-15	NA	0s
16-0	NA	668.1fs
Maximum Glitch		
668.1fs		

(c) Please measure the power of the counter.

```
pvdd=-168.6429u  from=   0.              to= 120.0000n
```

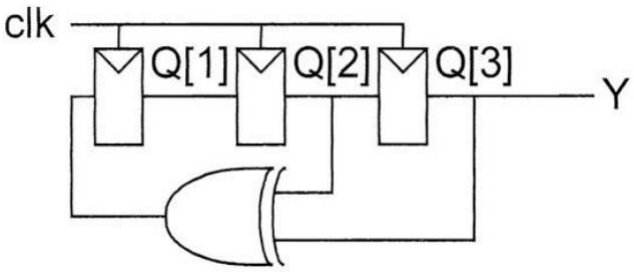
Power consumption=168.6429μW

2. Please design a 3 bit pseudo-random-bit-sequence (PRBS) generator with Linear Feedback Shift Register (LFSR) with clock frequency CLK = 200MHz, VDD = 1.8V, VSS = 0V. Try to minimize the power consumption of the PRBS generator.

(a) Please describe how you design the PRBS generator and show the pseudo-random sequence result to prove your design.

PRBS Design

參考講義上 pseudo-random sequence 的電路如下:



其 Q[1]、Q[2]、Q[3]會依照下表進行循環:

Table 10.6 LFSR sequence

Cycle	Q[1]	Q[2]	Q[3] / Y
0	1	1	1
1	0	1	1
2	0	0	1
3	1	0	0
4	0	1	0
5	1	0	1
6	1	1	0
7	1	1	1
repeats forever			

題目要求設計 3 bits 的 pseudo random bit sequence，完成此功能之電路，需要三個 Flip-Flop 提供暫存功能及一個 XOR gate，因本題為 3 bits，對應到的 characteristics polynomial 為 $1+x^2+x^3$，故設計電路時，須將第二個 Flip-Flop 的輸出與第三個 Flip-Flop 的輸出作為 XOR gate 的輸入。

實際設計電路:

沿用上次作業的 master slave based ET DFF 作為提供暫存器功能的電路，以及上題採用的 XOR gate，完成 3 bits pseudo random bit sequence 的電路設計。

Schematic :

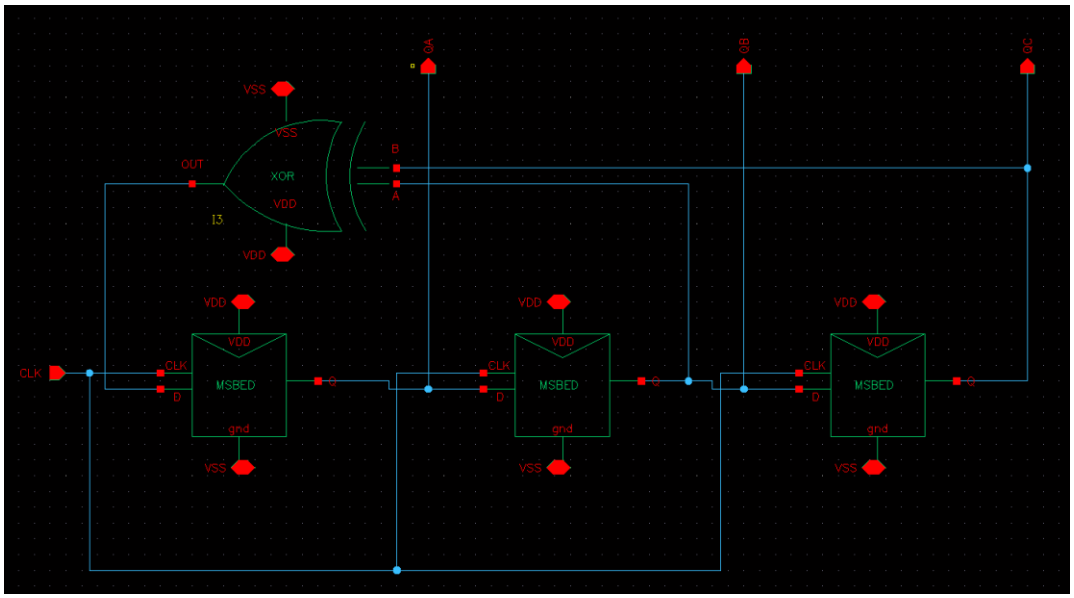


圖 7 3 bit pseudo-random-bit-sequence (PRBS) generator

模擬結果如下:

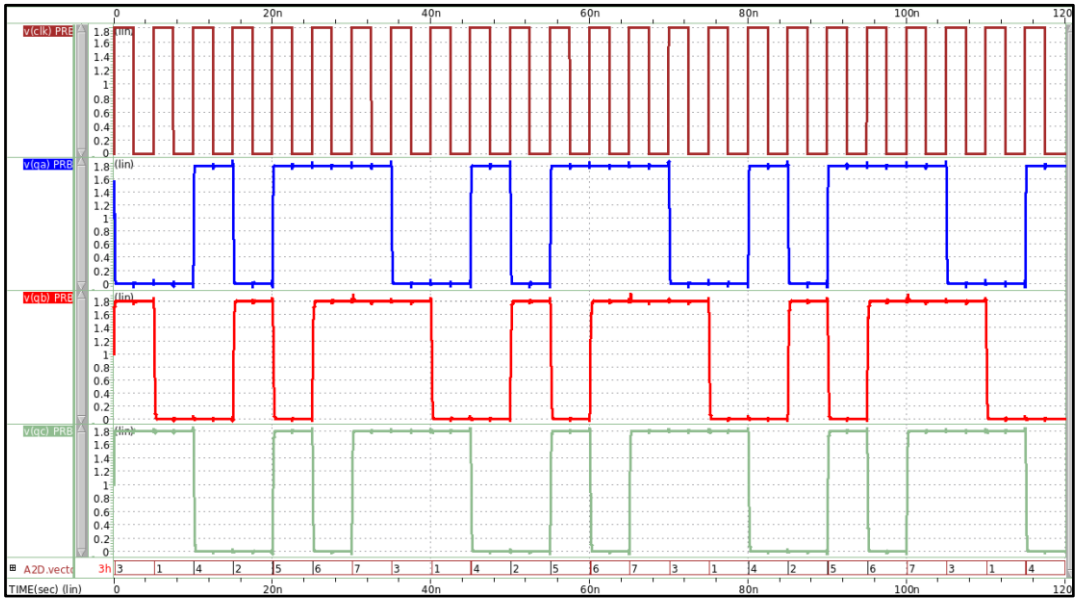


圖 8 pseudo random bit sequence waveview

The way to minimize the power

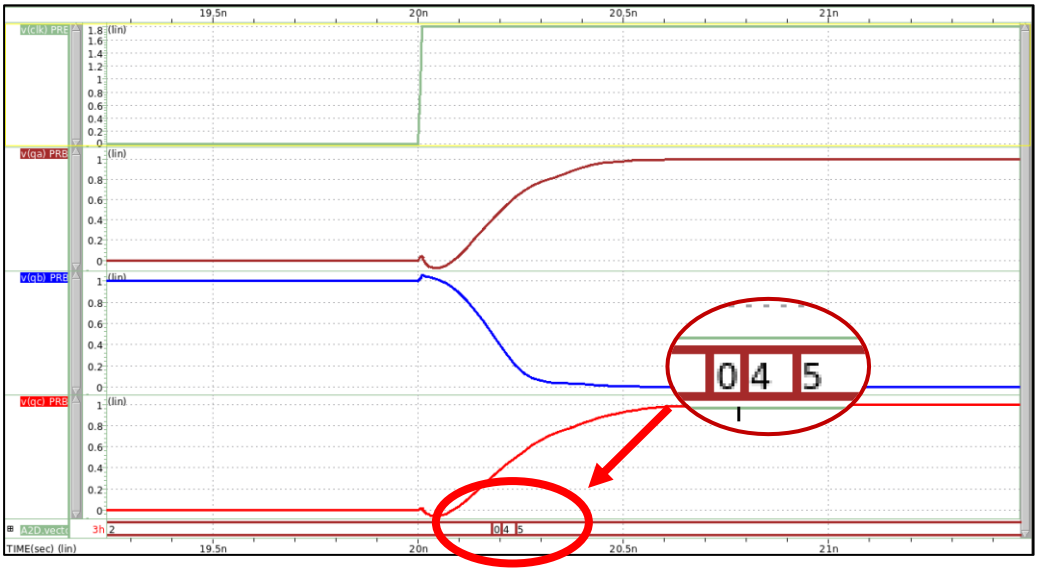
設計 3 bits 的 pseudo random bit sequence 的 mos parameter，原先採用的 mos 大小為 nmos width=1μm，pmos width=2μm 進行設計，模擬後得到的 power consumption 如下:

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
pvdd=-117.6585u  from=   0.              to= 120.0000n
```

1. 方法一:降低 VDD

   將 VDD 從 1.8V 降至 1V，模擬結果如下:

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
pvdd=  -6.9539u  from=   0.              to= 120.0000n
```



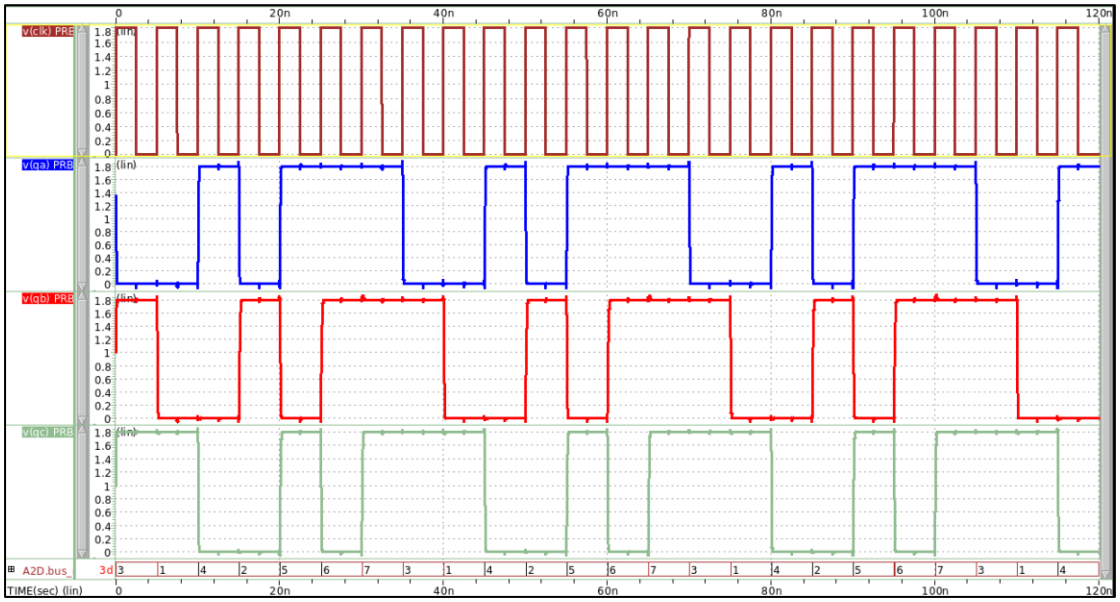
雖然 power consumption 降低到非常小，但電路的 glitch 更大，超過 80ps，固本題不採用降低 VDD 的方法去降低 power consumption。

2. 方法二: 降低 mos size

將整體 mos size 降低，nmos width=0.25μm，pmos width=0.3μm，得到的 power consumption 如下:

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
pvdd= -24.0383u  from=   0.             to= 120.0000n
```

電路功能也可正常運作:



結論:

雖然降低 VDD 會得到更好的功耗表現，但也影響電路功能，而調低 mos size 雖然沒有比直接調整 VDD 來的更有成效，但仍可明顯降低 power consumption。

(b) Please measure the power of the PRBS generator.

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
pvdd= -24.0383u  from=   0.             to= 120.0000n
```

Power consumption=24.0483μW