**國立清華大學**

**超大型積體電路設計VLSI Design**



**Homework 4**

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目錄

[1. Consider a positive-edge-triggered D flip-flop as shown in Fig. 1. Assume CLK=100MHz with tr=tf=50ps, duty cycle=50% and VDD=1.8V. Please design the logic gates that are based on unit inverter of (W/L)n= 0.6um/0.18um and (W/L)p=1.8um/0.18um.Simulate and find the setup time of this flip-flop including rising and falling input. Briefly explain what is the setup time and the way you find it. 4](#_Toc121087791)

[(a) Simulate and find the hold time of this flip-flop including rising and falling output. Briefly explain what is the hold time and the way you find it. 4](#_Toc121087792)

[(b) Simulate and find the hold time of this flip-flop including rising and falling output. Briefly explain what is the hold time and the way you find it. 4](#_Toc121087793)

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[(c) Simulate the clock to Q delay for both rising and falling input transitions. 15](#_Toc121087800)

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[2. Insert an inverter chain between 2 DFFs (shown in Fig.2) as a combinational logic to introduce a delay.( clk = 100MHz with tr = tf = 50ps, duty cycle = 50% and VDD = 1.8V). Simulate and observe the maximum and minimum delay failure condition while input = vdd and input = gnd. 21](#_Toc121087806)

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[(b) Using the DFF in Fig.3 and with the inverter size (W/L)n = 0.6um/0.2um and (W/L)p = 1.8um/0.2um, the transmission gate size (W/L)n = (W/L)p = 0.8um/0.2um. 26](#_Toc121087811)

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[(c) Use the previous results in question1 (setup time and hold time) to hand calculate the maximum and minimum delay failure condition in (a). As for (b), do the same hand calculation as (a). 38](#_Toc121087823)

[(d) Please compare and comment the results of (a) and (b) with (c). 39](#_Toc121087824)

這次報告較多頁，以下為主要大綱:

第一題:

P8-p10: DFF setup time with rising and falling input

P11-p13: DFF hold time with rising and falling input

P14: what is setup time and hold time

P15: DFF Clock to Q Delay

P16: layout、DRC、LVS

P17-P20: presim v.s.postsim

第二題:

P22-p24, p25: DFF maximum propagation delay, DFF minimum propagation delay

P26-p35:尚未insert inverter chain的 MSBED 的setup time、hold time…..

P36-p37: Master Slave Based ET DFF maximum propagation delay

P38: Master Slave Based ET DFF minimum contamination delay

P39: compare and comment 2 different DFF

# Consider a positive-edge-triggered D flip-flop as shown in Fig. 1. Assume CLK=100MHz with tr=tf=50ps, duty cycle=50% and VDD=1.8V. Please design the logic gates that are based on unit inverter of (W/L)n= 0.6um/0.18um and (W/L)p=1.8um/0.18um.Simulate and find the setup time of this flip-flop including rising and falling input. Briefly explain what is the setup time and the way you find it.

## Simulate and find the hold time of this flip-flop including rising and falling output. Briefly explain what is the hold time and the way you find it.

## Simulate and find the hold time of this flip-flop including rising and falling output. Briefly explain what is the hold time and the way you find it.

**Note: p4-p14為(a)、(b)小題內容:**

**P8為the way I find setup time.**

**P11為 the way I find hold time.**

**p14將explain what is setup time and hold time.**

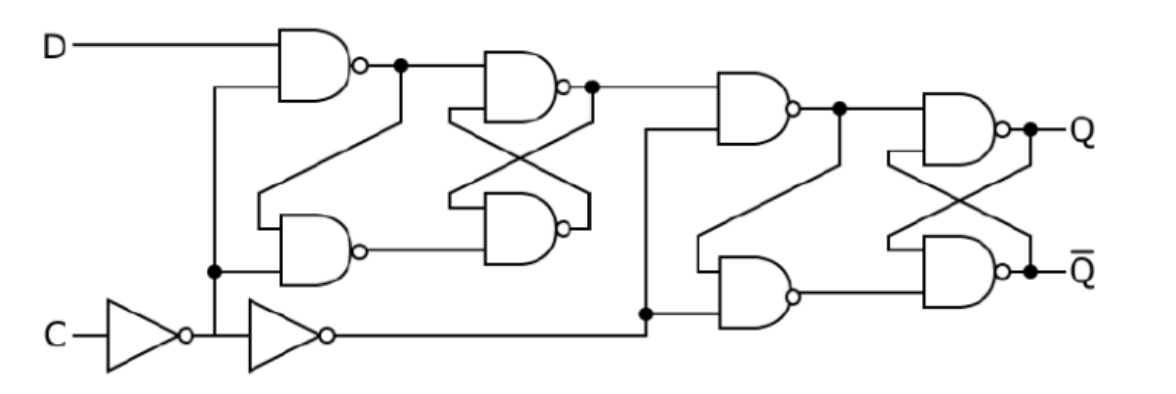


圖 1 DFF logic gate

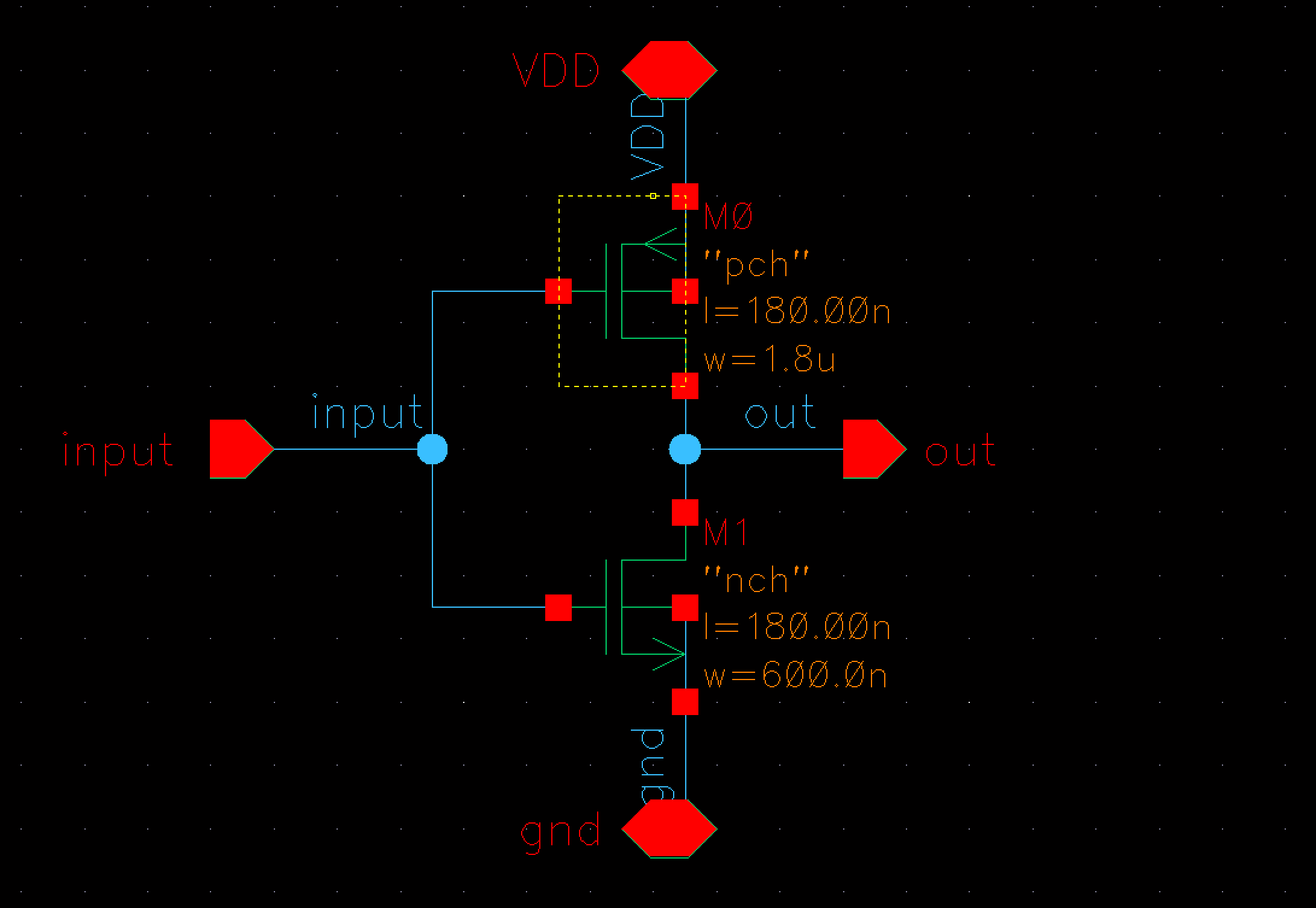


圖 2 Unit Inverter

|  |  |  |
| --- | --- | --- |
| **MOS** | **W/L** | **m** |
| PMOS | 1.8u/0.18u | 1 |
| NMOS | 0.6u/0.18u | 1 |

題目給定的unit inverter size，不需自行設計size降低propagation delay。

，稍後optimize 2 input nand delay會用到。

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圖 3 2 input NAND

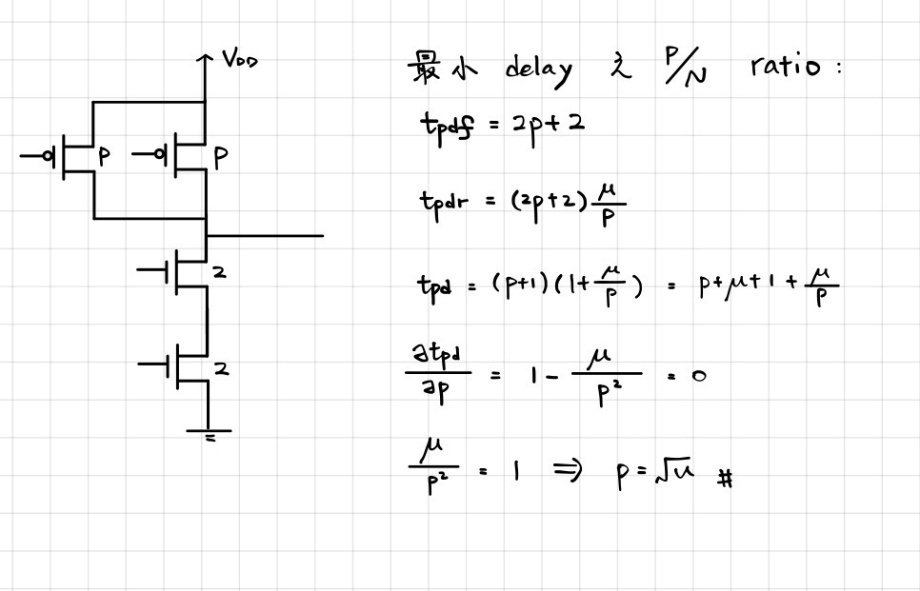


圖 4 optimizing nand delay

透過計算，得知nand在size = 時可以得到最小delay。故size設計為:

|  |  |  |
| --- | --- | --- |
| **MOS** | **W/L** | **m** |
| PMOS | 1.73u/0.18u | 1 |
| NMOS | 1.2u/0.18u | 1 |

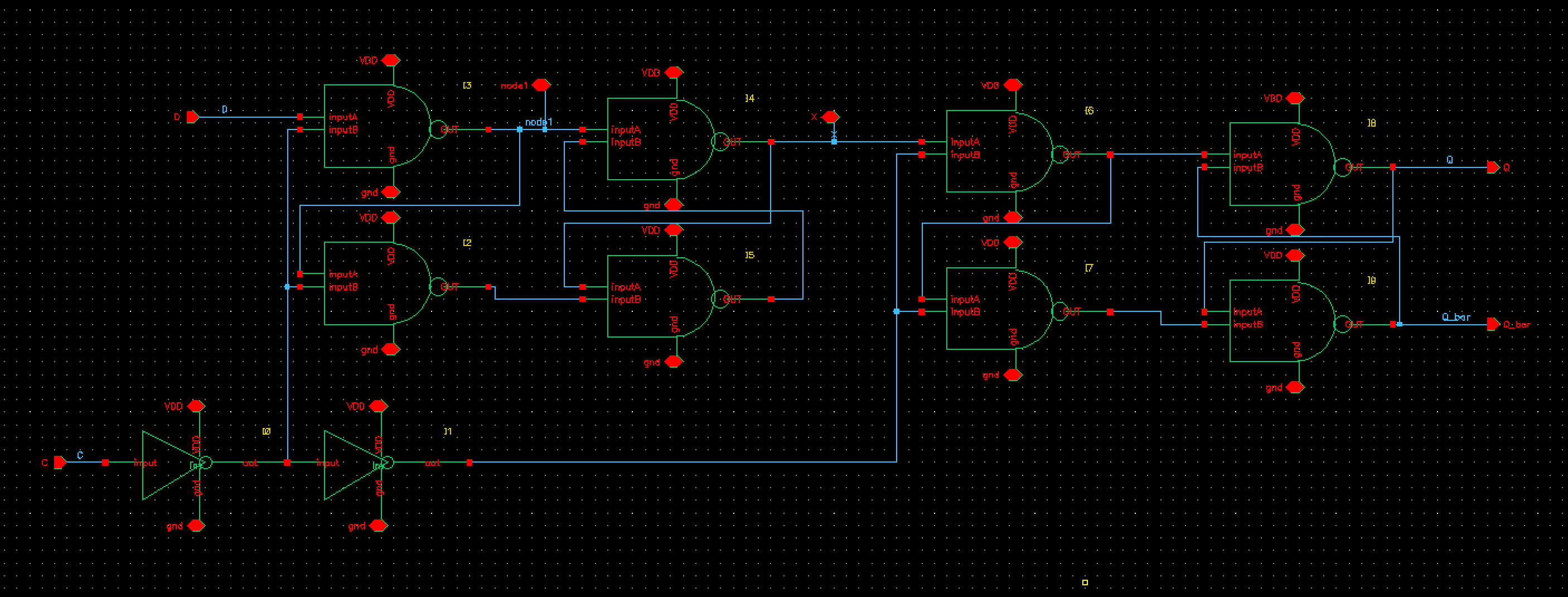


圖 5 DFF schematic

|  |  |  |
| --- | --- | --- |
| **Logic Gate** | **PMOS** | **NMOS** |
| Inverter | 1.8u/0.18u\*1 | 0.6u/0.18u\*1 |
| 2 input nand | 1.73u/0.18u\*1 | 1.2u/0.18u\*1 |

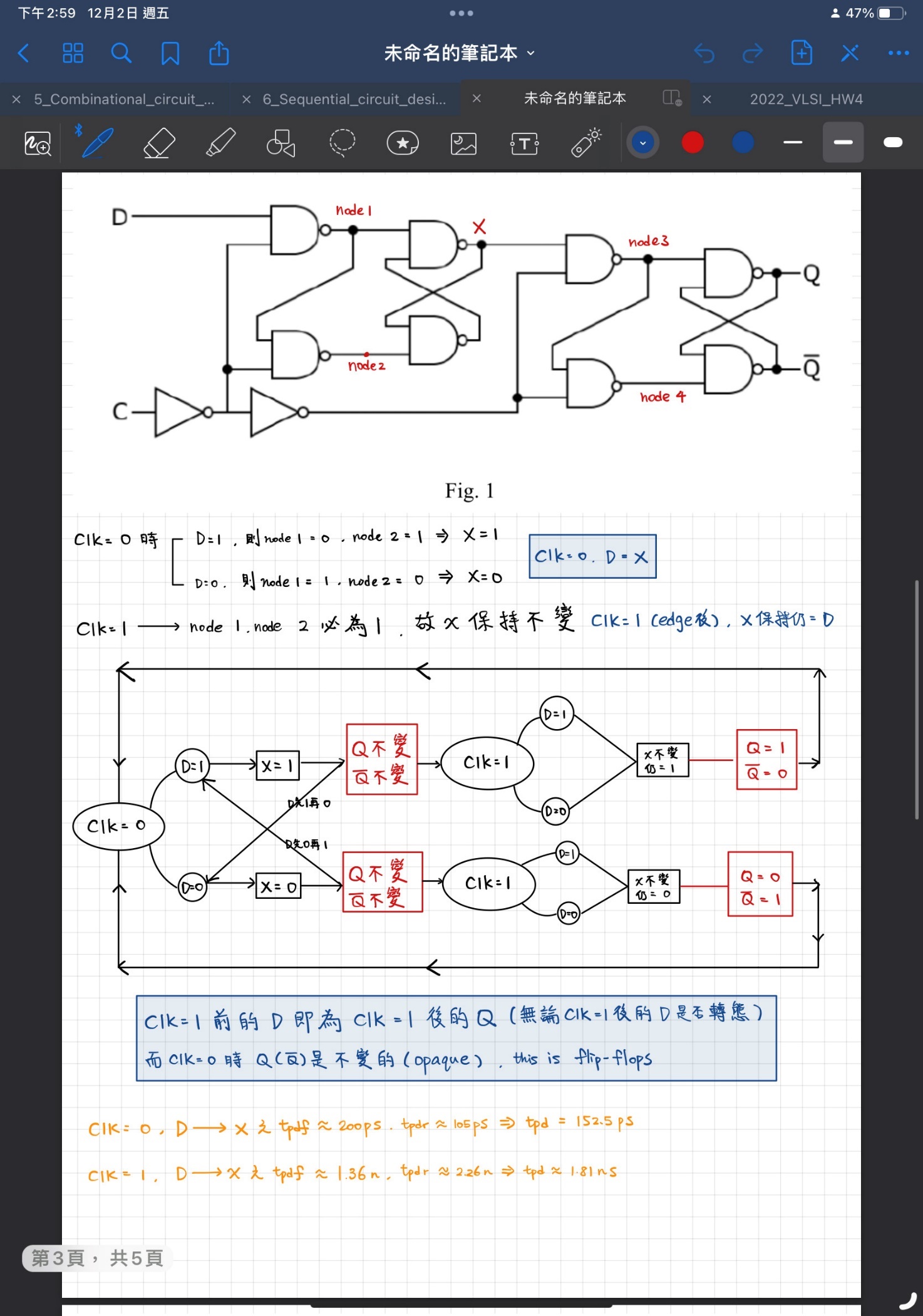


圖 6 D Flip Flop時序分析

時序分析後，D Flip Flop的電路行為:

CLK=1前的D即為CLK=1後的Q(無論CLK=1後的D是否轉態)，而CLK=0的時候Q是不變的。

得到各logic gate的size後，畫完schematic即可開始模擬電路。

The Way to Find Setup Time

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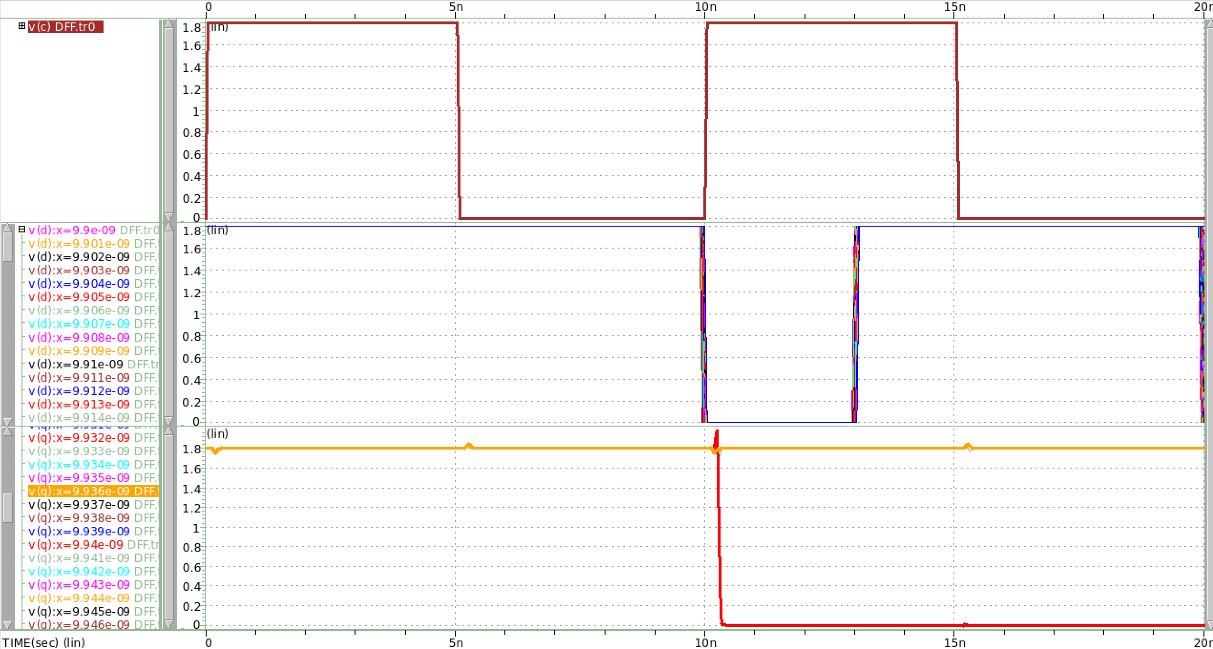
Output Q

Rising input

clock

圖 7 Setup Time finding(rising input)

透過sweep input D的delay(9.9n~10.1n)，找出輸入為rising input時output Q floating的瞬間，上圖綠色線為output Q的fail case(setup time不夠大);紅色線則為output Q 的success case。



Output Q

Falling input

clock

圖 8 Setup Time finding(falling input)

透過sweep input D的delay(9.9n~10.1n)，找出輸入為falling input時output Q floating的瞬間，上圖橘色線為output Q的fail case(setup time不夠大);紅色線則為output Q 的success case。

Setup Time Simulation (rising input)

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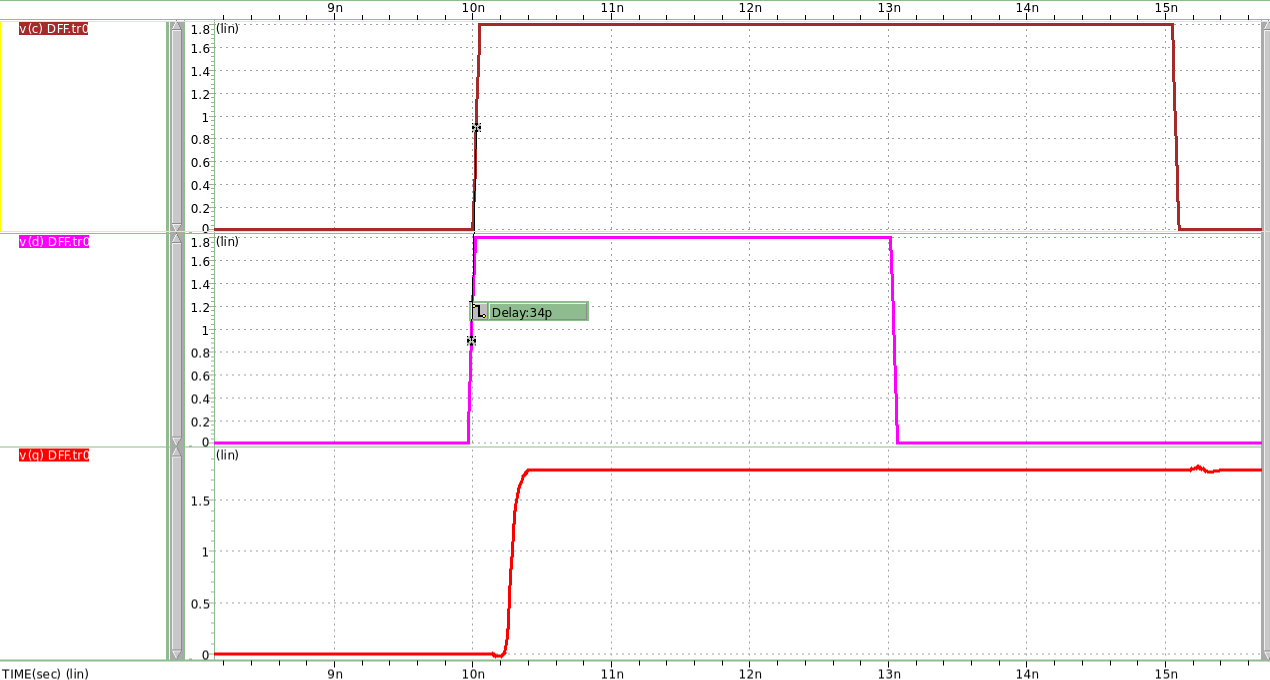
clock

Rising input

Output Q

圖 9 Setup Time failed(rising input)

當setup time為33ps時，output Q 並沒有因CLK edge而轉態為1。



Rising input

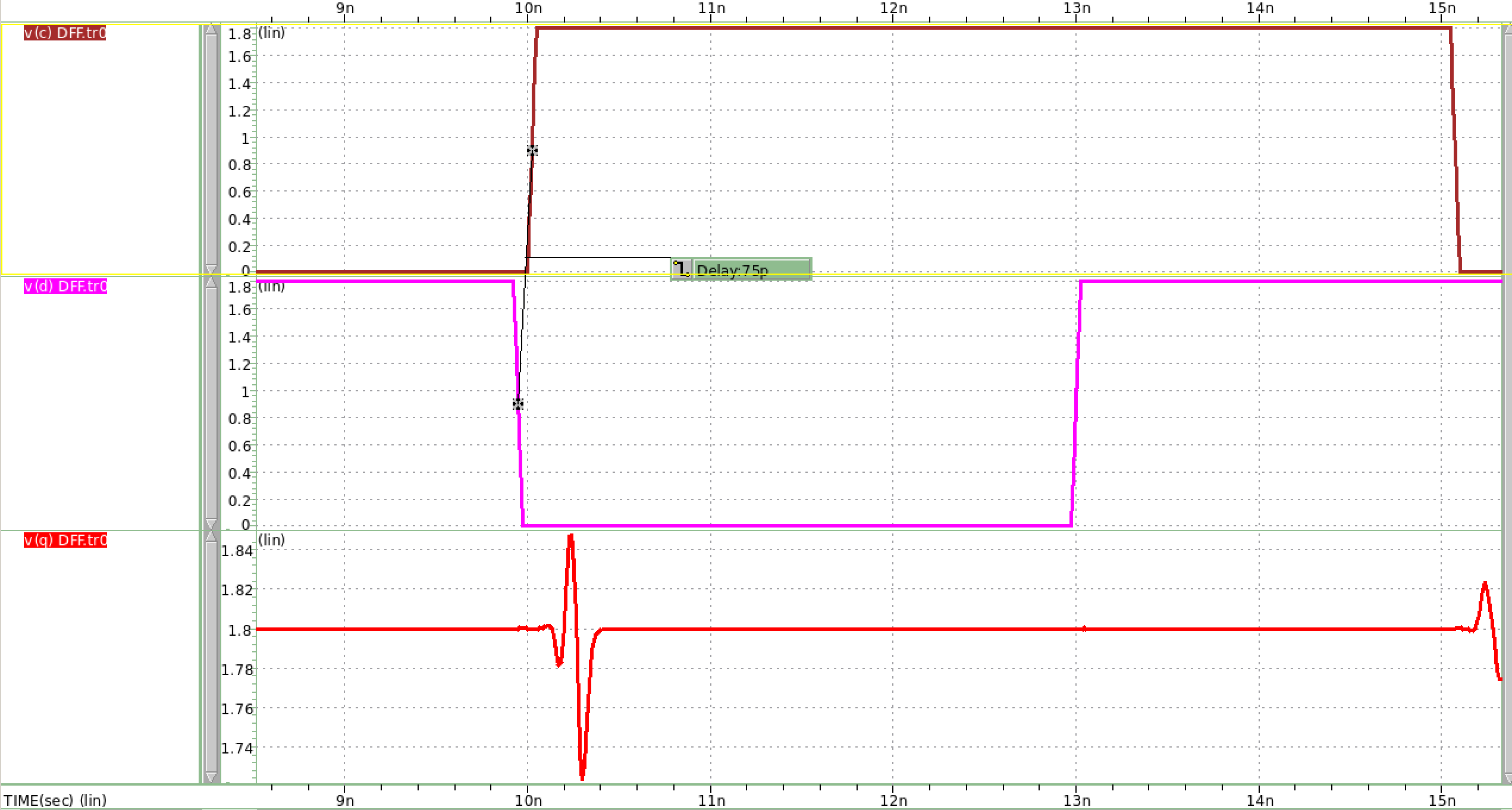
clock

Output Q

圖 10 Setup Time success(rising input)

當setup time為34ps時，output Q 因CLK edge而轉態為1。透過simulation得知input為rising input時，**minimum setup time = 34ps**。

Setup Time Simulation (falling input)



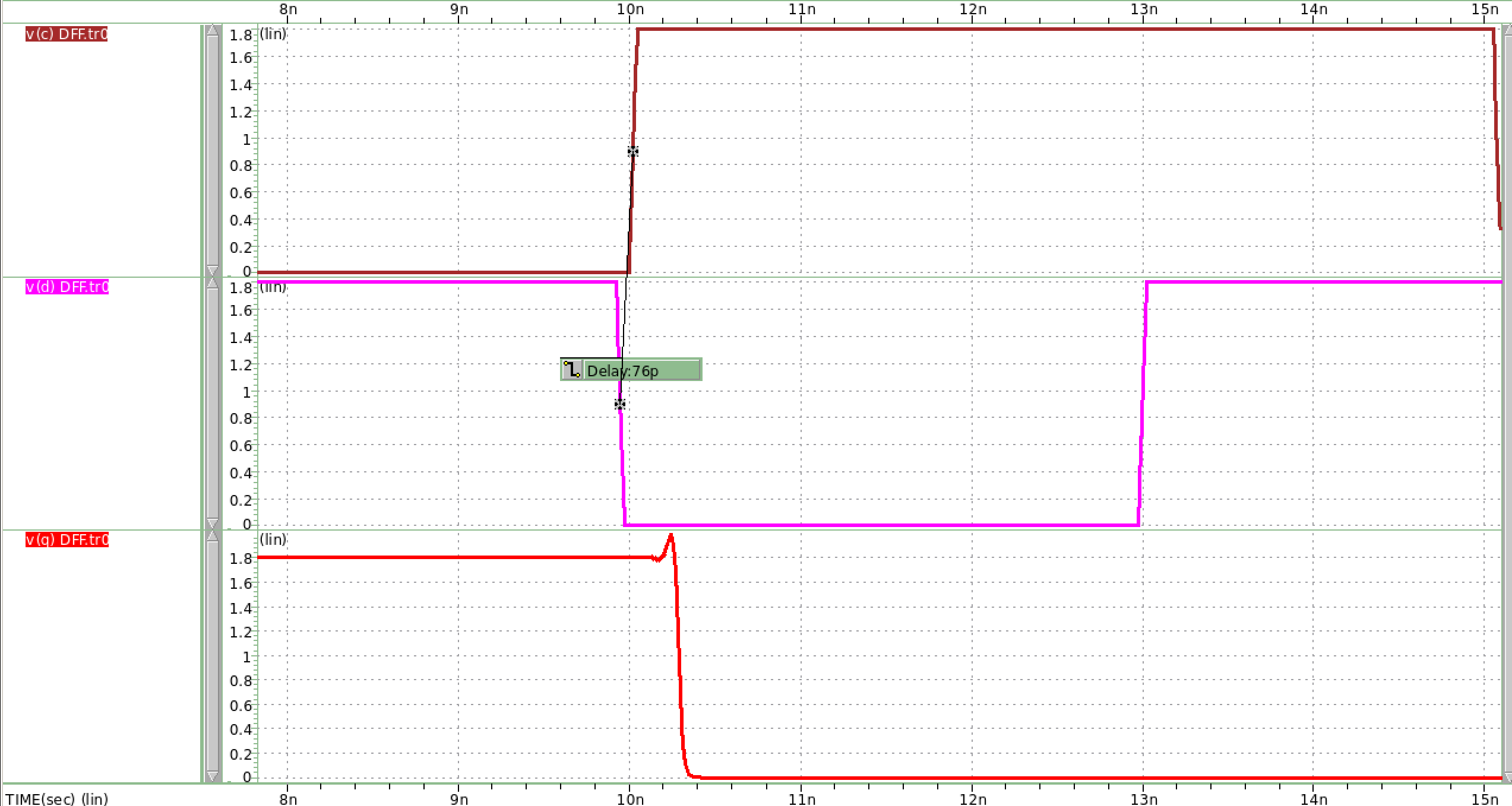
falling input

clock

Output Q

圖 11 Setup Time failed(falling input)

當setup time為75ps時，output Q 並沒有因CLK edge而轉態為0。



clock

falling input

Output Q

圖 12 Setup Time success(falling input)

當setup time為76ps時，output Q 因CLK edge而轉態為0。透過simulation得知input為falling input時，**minimum setup time = 76ps**。

The Way to Find Hold Time

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clock

Rising input

Output Q

圖 13 Hold Time finding(rising input)

將rising input delay設定在先前透過setup time simulation得知的值後(**為確保不是因setup time導致output floating**)，開始sweep input維持1的時間(50p~1000p)，找到output floating的瞬間，上圖output Q 紅色線為failed case(hold time不夠)，綠色線則為success case。

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clock

falling input

Output Q

將falling input delay設定在先前透過setup time simulation得知的值後(**為確保不是因setup time導致output floating**)，開始sweep input維持1的時間(50p~1000p)，找到output floating的瞬間，上圖output Q 紅色線為failed case(hold time不夠)，綠色線則為success case。

Hold Time Simulation (rising input)



Rising input

Output Q

clock

圖 14 Hold Time failed(rising input)

當hold time為98ps時，output Q 並沒有因CLK edge而轉態為1。



clock

Output Q

Rising input

圖 15 Hold Time success(rising input)

當hold time為99ps時，output Q因CLK edge而轉態為1。透過simulation得知input為rising input時，**minimum hold time = 99ps**。

Hold Time Simulation (falling input)



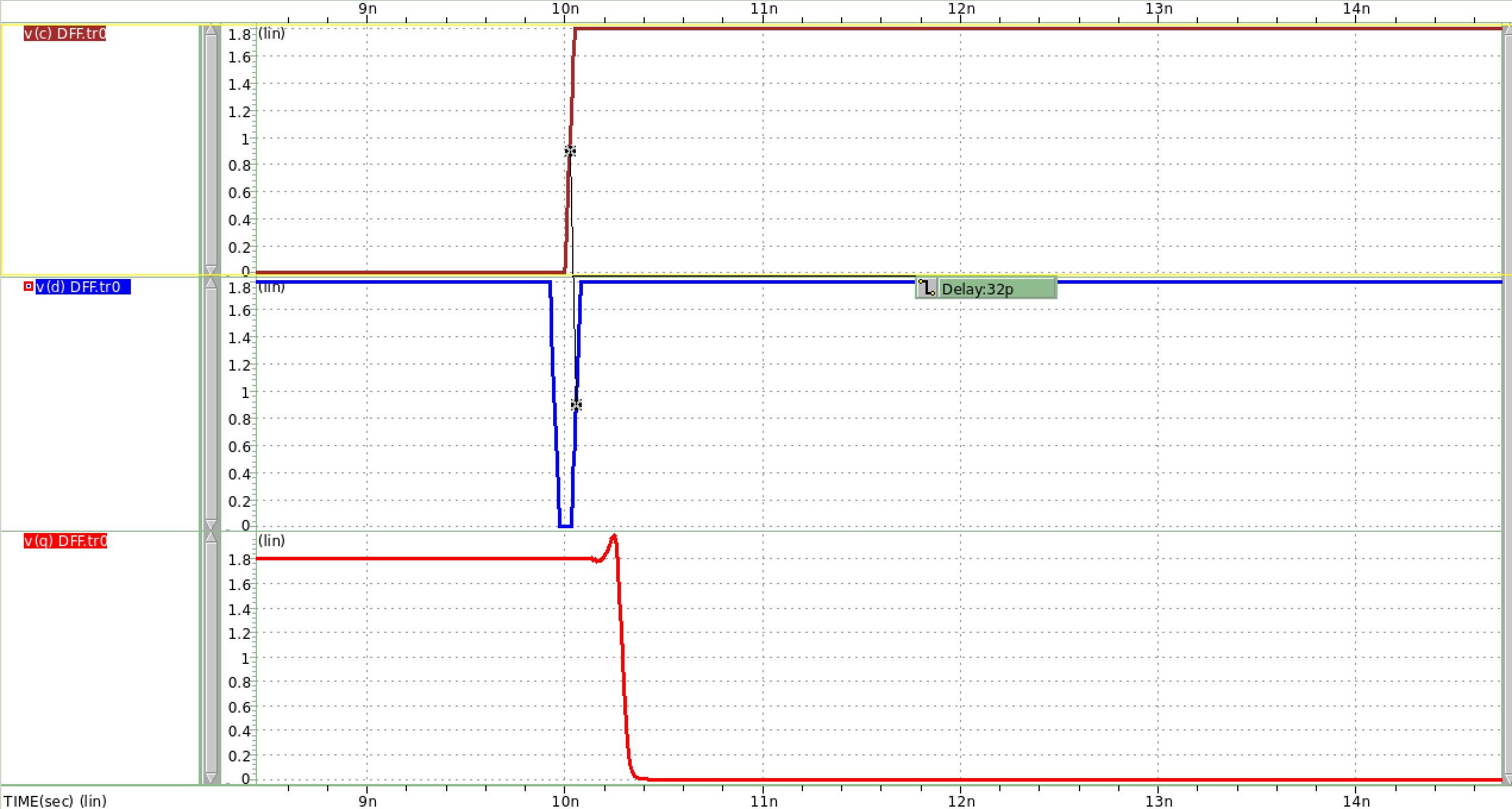
falling input

clock

Output Q

圖 16 Hold Time failed(falling input)

當hold time為31ps時，output Q 並沒有因CLK edge而轉態為0。



falling input

clock

Output Q

圖 17 Hold Time success(falling input)

當hold time為32ps時，output Q因CLK edge而轉態為0。透過simulation得知input為falling input時，**minimum hold time = 32ps。**

**將前幾頁結果整理成表格如下(success case):**

|  |  |  |
| --- | --- | --- |
|  | **Setup Time** | **Hold Time** |
| **Rising Input** | 34ps | 99ps |
| **Falling Input** | 76ps | 32ps |

**What is Setup time?**

**Setup time 即為clock edge前(本題為positive edge)，input 須維持穩定的時間(此段時間input不可再轉態)，若input在setup time時間範圍內變動，則output會floating。**

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**What is Hold time?**

**Hold time 即為clock edge後，input 須維持穩定的時間(此段時間input不可再轉態)，若input在clock edge後的hold time時間範圍內變動，則output會floating。**

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自動產生的描述**

## Simulate the clock to Q delay for both rising and falling input transitions.



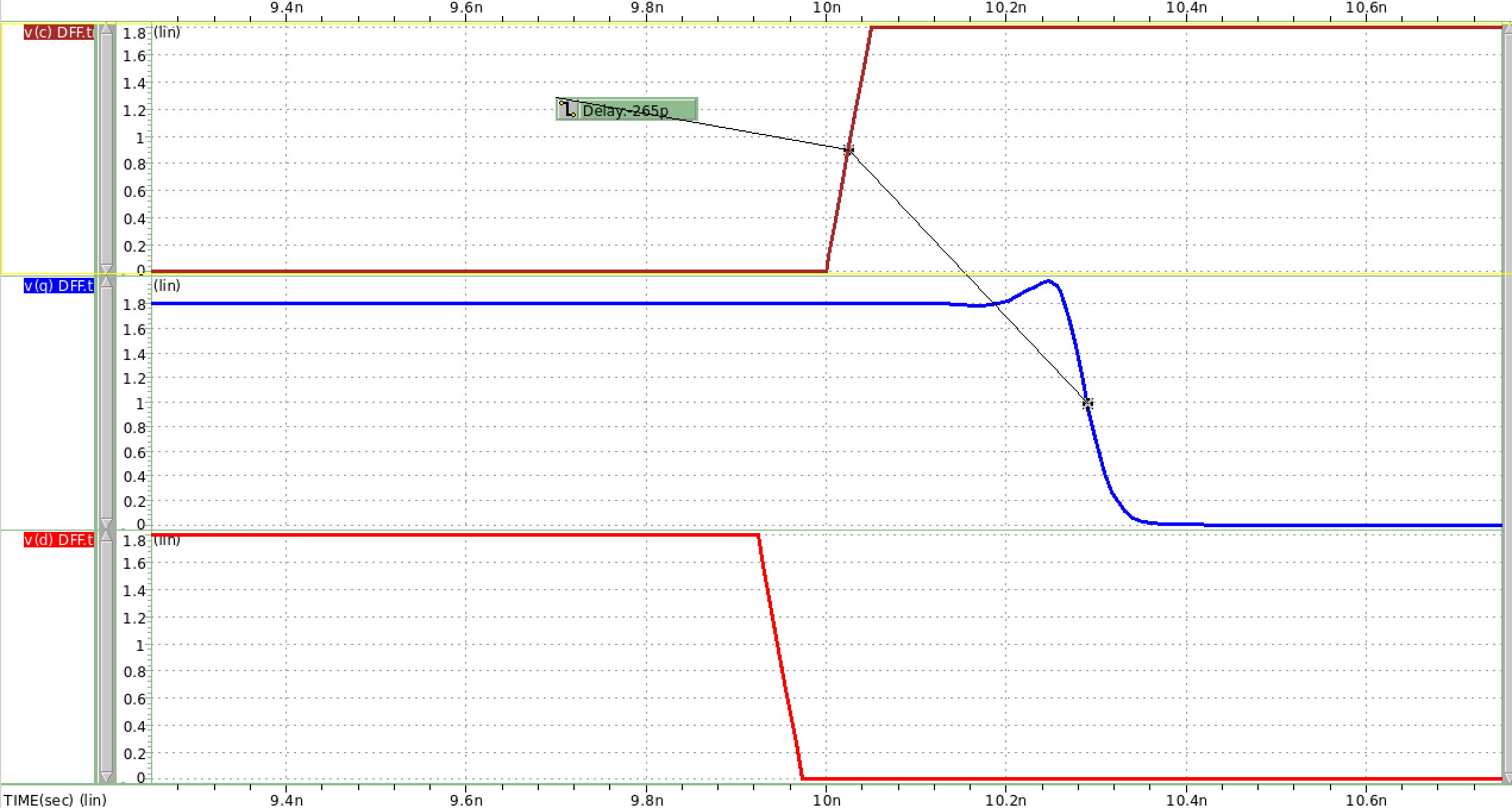
Output Q

Rising input

clock

圖 18 CLK-Q delay(rising input)

**Clock to Q delay for rising input = 258ps**



Output Q

clock

Falling input

圖 19 CLK-Q delay(falling input)

**Clock to Q delay for falling input = 265ps**

## Finish the layout, DRC, and LVS. Paste the photo of layout, DRC result and LVS result in your report.

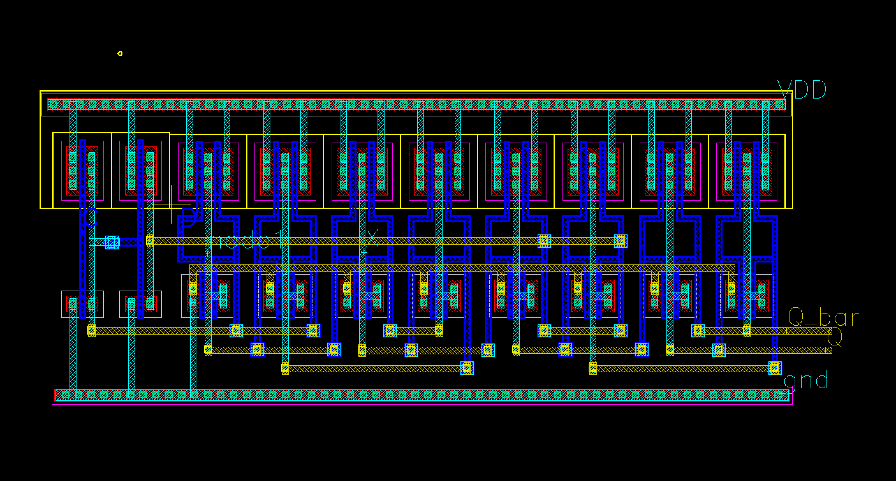


圖 20 DFF Layout

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圖 21 DRC result

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圖 22 LVS result

## Run the post-layout simulation (post-sim) and compare it with pre-layout simulation (pre-sim) in (a), (b), and (c).

Setup Time

clock

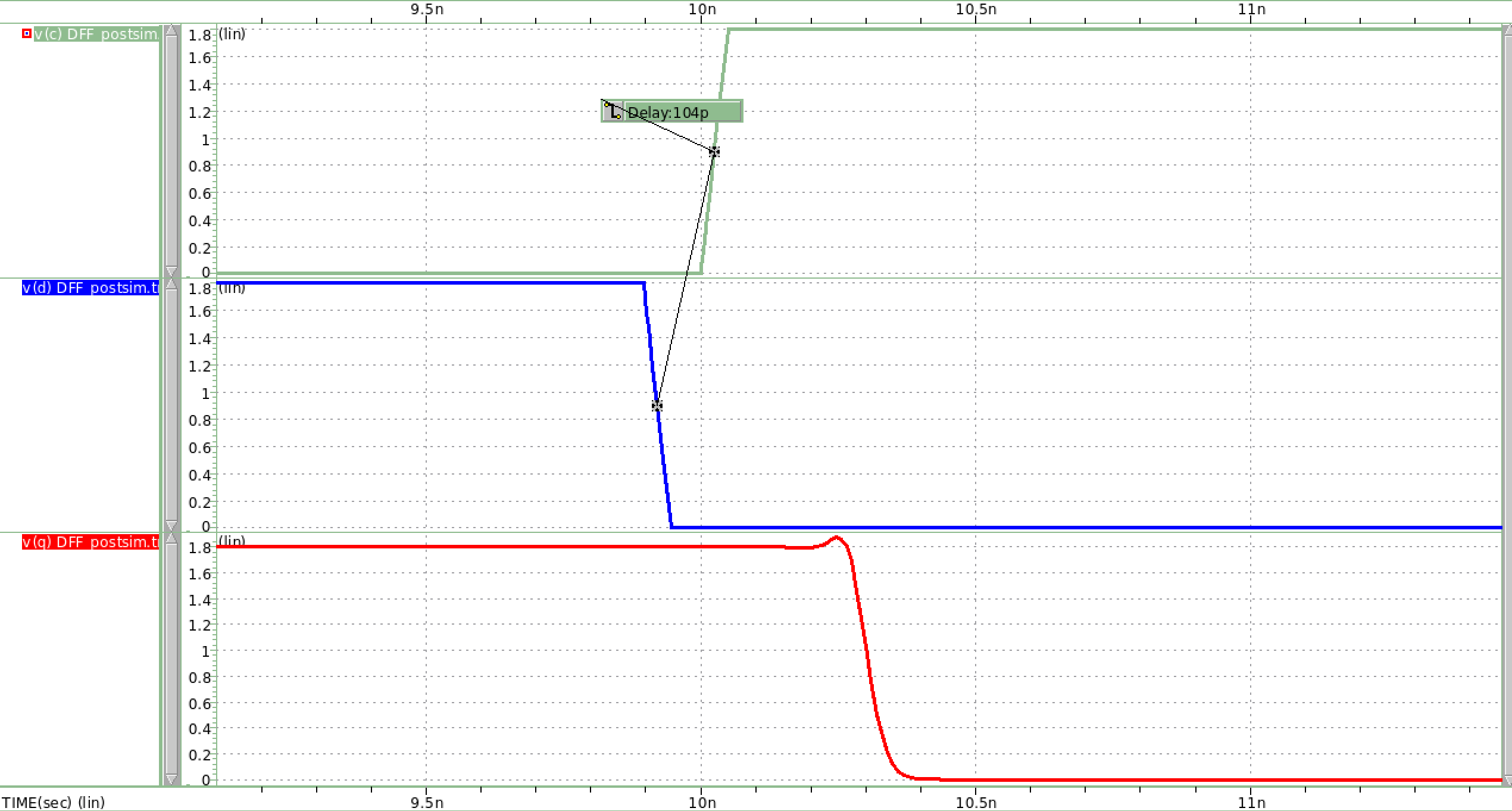
rising input

Output Q



圖 23 postsim-setup time(rising input)

**Setup time(rising input) = 49ps**



clock

falling input

Output Q

圖 24 postsim-setup time(falling input)

**Setup time(falling input) = 104ps**

Hold Time



clock

rising input

Output Q

圖 25 postsim-hold time(rising input)

**hold time(rising input) = 116ps**



falling input

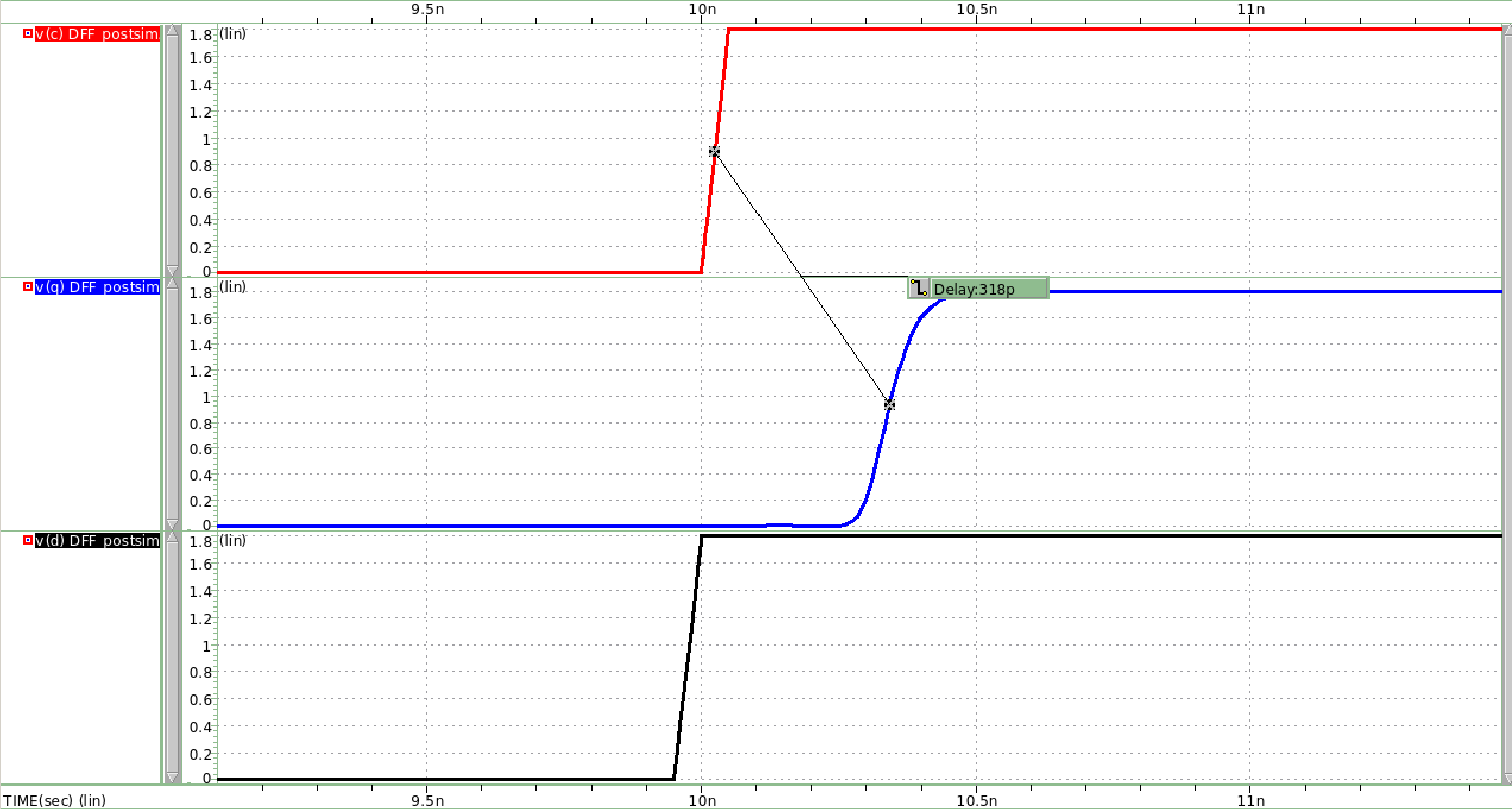
clock

Output Q

圖 26 postsim-hold time(falling input)

**hold time(falling input) = 52ps**

Clock to Q Delay



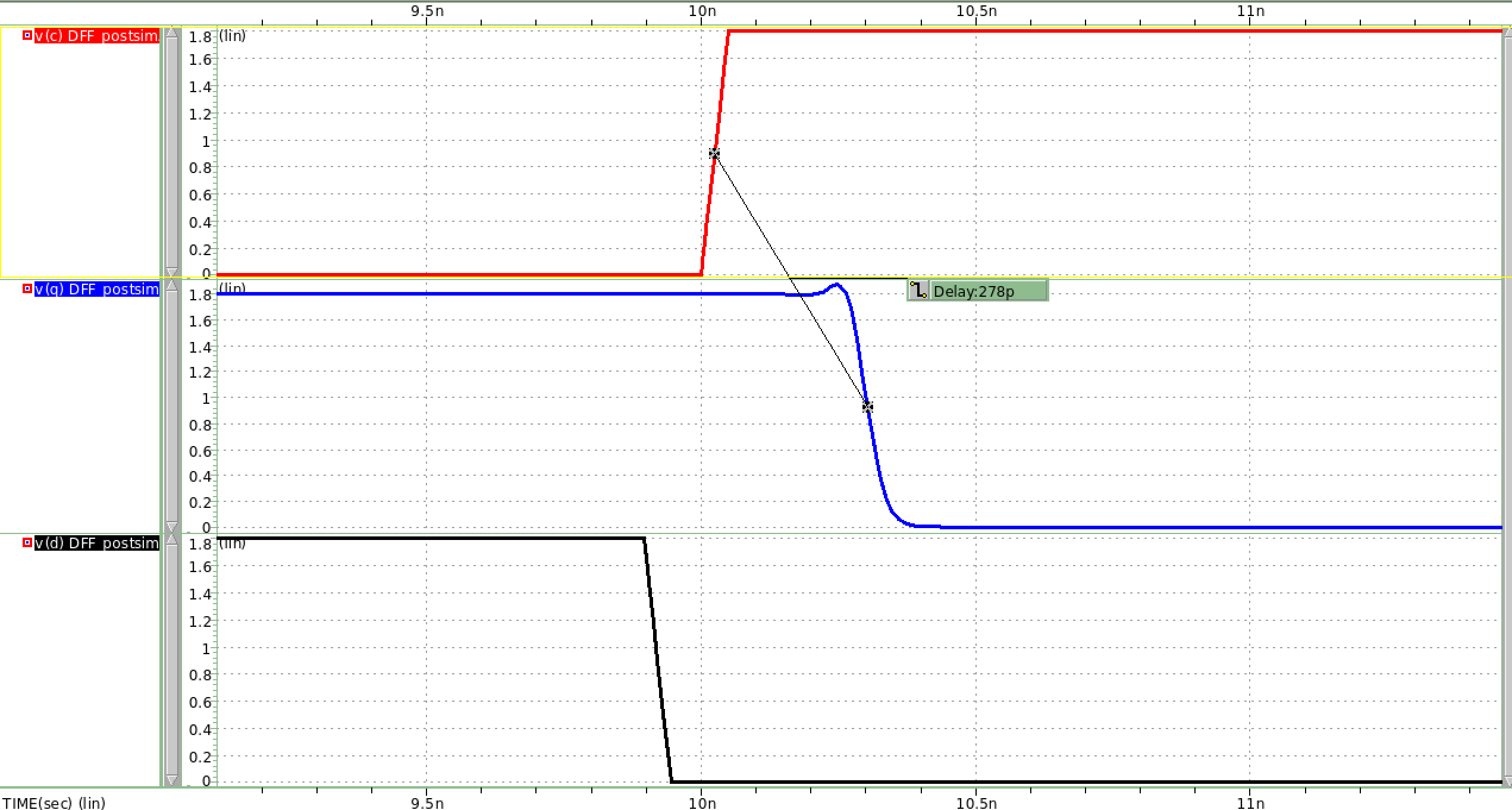
Rising input

Output Q

clock

圖 27 CLK-Q Delay(rising input)

**Clock to Q delay for rising input = 318ps**



Falling input

clock

Output Q

圖 28 CLK-Q Delay(falling input)

**Clock to Q delay for falling input = 278ps**

表格 1 DFF Simulation presim and postsim results

|  |  |  |
| --- | --- | --- |
|  | **Presim** | **Postsim** |
| **Setup Time (rising input)** | 34ps | 49ps |
| **Setup Time (falling input)** | 76ps | 104ps |
| **Hold Time (rising input)** | 99ps | 116ps |
| **Hold Time (falling input)** | 32ps | 52ps |
| **CLK-Q Delay (rising input)** | 258ps | 318ps |
| **CLK-Q Delay (falling input)** | 265ps | 278ps |

Postsim因加入寄生電容，故postsim後所需的setup time、hold time都比presim來的更多，且delay也更大。

# Insert an inverter chain between 2 DFFs (shown in Fig.2) as a combinational logic to introduce a delay.( clk = 100MHz with tr = tf = 50ps, duty cycle = 50% and VDD = 1.8V). Simulate and observe the maximum and minimum delay failure condition while input = vdd and input = gnd.

**Note: Maximum propagation delay Tpd ≦ Tc – (Tsetup + Tpcq)**

**Minimum contamination delay Tcd ≧ Thold - Tccq**

**表格 2 DFF simulation result**

|  |  |  |
| --- | --- | --- |
| **Tc = 10ns** | **Rising Input** | **Falling Input** |
| **Tsetup** | **34ps** | **76ps** |
| **Thold** | **99ps** | **32ps** |
| **CLK-Q delay** | **258ps (Tccq)** | **265ps (Tpcq)** |
| **Maximum Tpd** | **9.701ns** | |
| **Minimum Tcd** | **-159ps** | |

**由上表可得到的結論為:**

**Combinational Logic 的 propagation delay不可大於9.7ns，否則將導致第二個DFF input時setup time不夠大，最後output floating。**

**而Combinational Logic 的 contamination delay < 0ps，代表兩個DFF之間在不加入combinational logic提供delay的情況下，也可正常運作，output不會floating。**

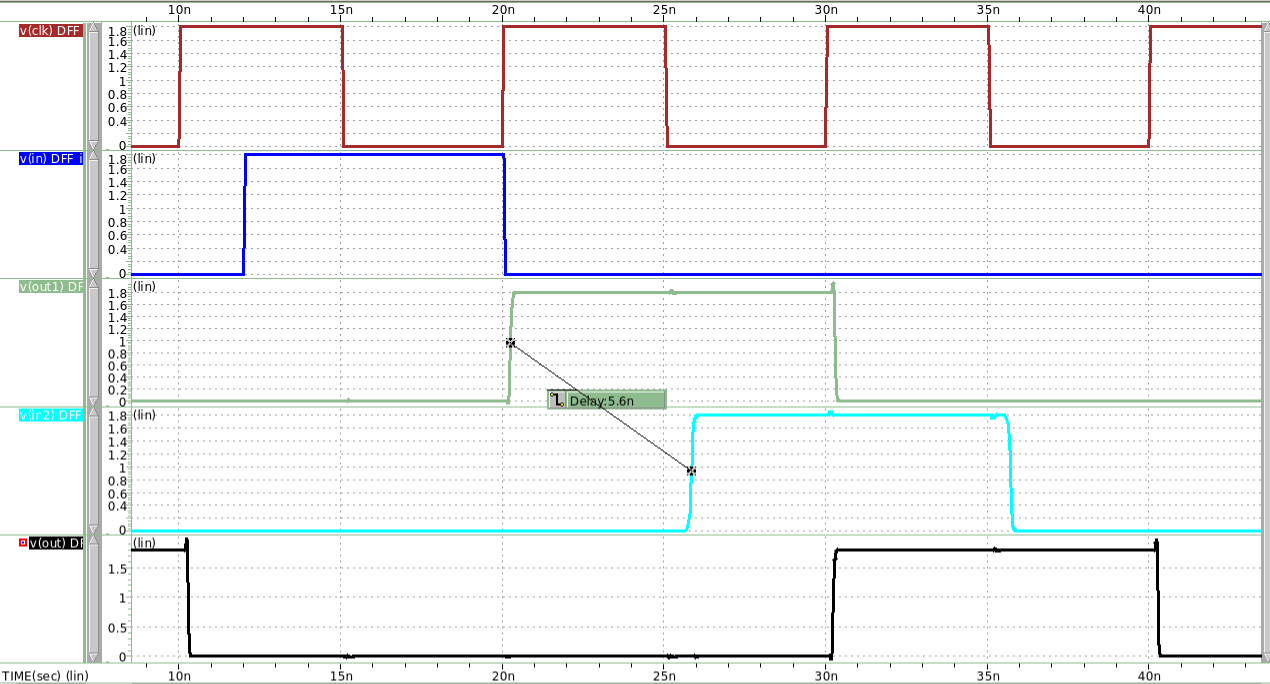
### Using the DFF you designed in previous question.

Maximum Propagation delay (INPUT=VDD)

首先，先insert an inverter chain with 4 unit inverter，前2個unit inverter我分別在output端接上電容 (1pF) 來提供propagation delay。



圖 29 DFF insert 4 stages inverter



OUT

INPUT2

OUT1

**CLK**

INPUT

圖 30 DFF insert 4 stages inverter waveview

OUT1至INPUT2的delay即為propagation delay，在DFF insert 4 stages inverter的情況下，delay為5.6ns，小於Maximum propagation delay。

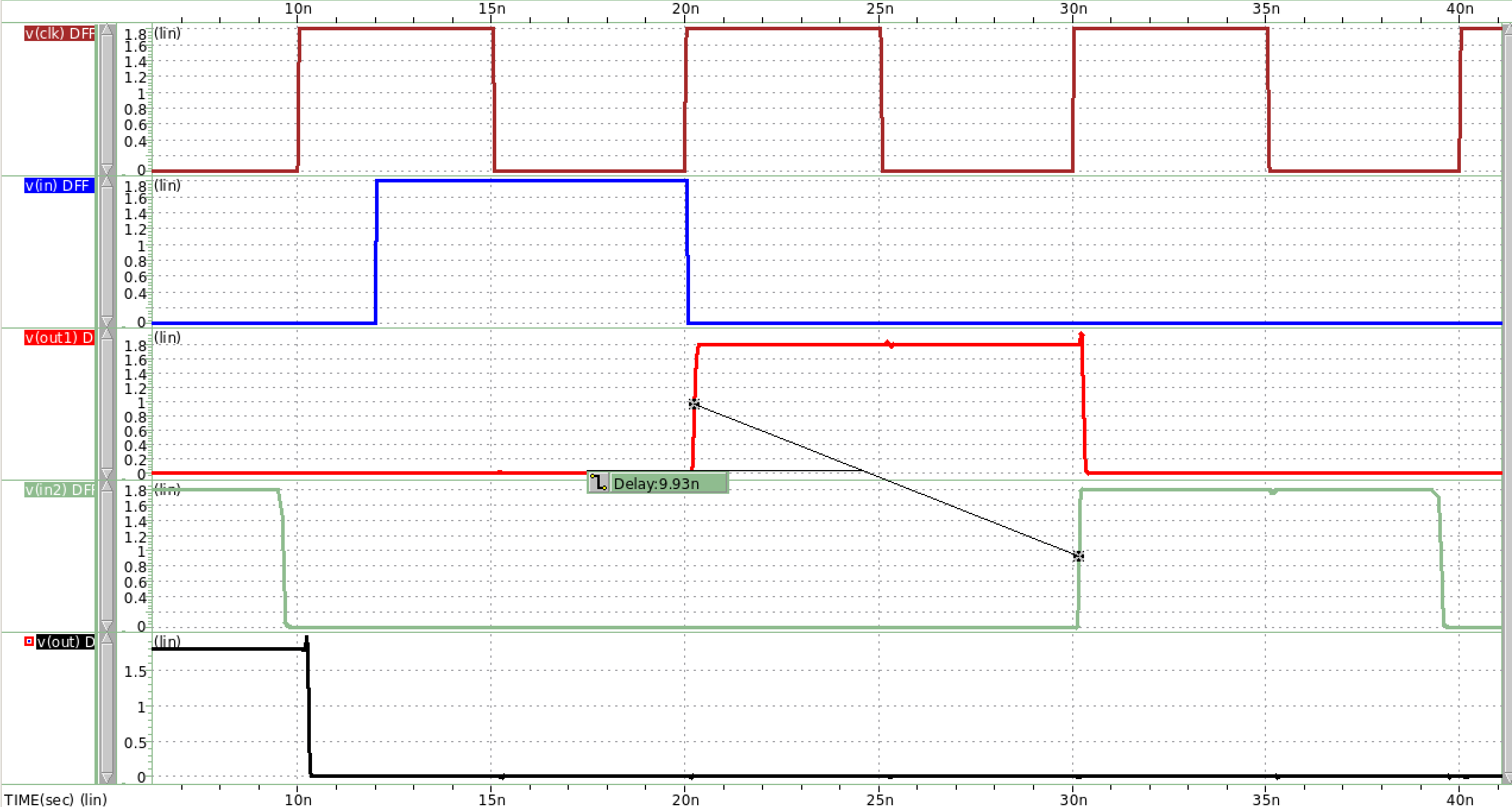
故OUT可正常輸出，電路運作正常。

接著，insert an inverter chain with 6 unit inverter，前3個unit inverter我分別在output端接上電容 (1pF) 來提供propagation delay。

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圖 31 DFF insert 6 stages inverter



INPUT2

OUT1

INPUT

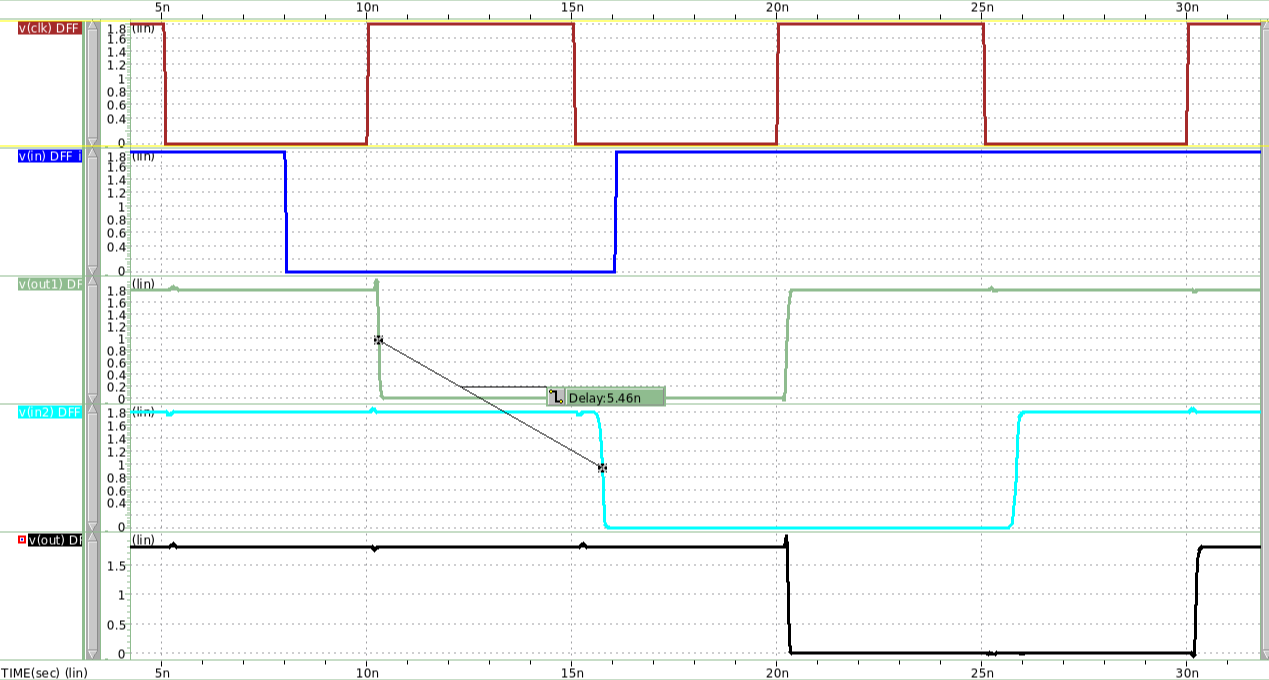
OUT

CLK

圖 32 DFF insert 6 stages inverter waveview

OUT1至INPUT2的delay在DFF insert 6 stages inverter的情況下，delay為9.93ns，大於Maximum propagation delay。電路不正常運作。

Maximum Propagation delay (INPUT=GND)



**CLK**

INPUT

OUT1

INPUT2

OUT

圖 33 DFF insert 4 stages inverter waveview

OUT1至INPUT2的delay在DFF insert 4 stages inverter的情況下，delay為5.46ns，小於Maximum propagation delay。電路正常運作。



INPUT2

OUT

OUT1

INPUT

CLK

OUT1至INPUT2的delay在DFF insert 6 stages inverter的情況下，delay為10.2ns，大於Maximum propagation delay。電路不正常運作。

Minimum Contamination Delay (INPUT=GND&=INPUT=VDD)

**Simulation結果contamination delay < 0ps，代表兩個DFF之間在不加入combinational logic提供delay的情況下，也可正常運作，output不會floating。實際設計結果如下。**

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圖 34 DFF with no combination logic

OUT

CLK

INPUT

|  |  |
| --- | --- |
| 圖 35 Rising Input | INPUT2=OUTPUT1  圖 36 Falling Input |

**實際設計模擬結果，無論是rising input還是falling input，電路接運作正常。**

**Rising input hold time=268ps;falling input hold time=229ps。接遠大於第一題所模擬的最小hold time，電路一定能運作正常。**

### Using the DFF in Fig.3 and with the inverter size (W/L)n = 0.6um/0.2um and (W/L)p = 1.8um/0.2um, the transmission gate size (W/L)n = (W/L)p = 0.8um/0.2um.

**P26-p33為單個Master Slave Based ET DFF的**

**simulation，沒有insert inverter chain。**

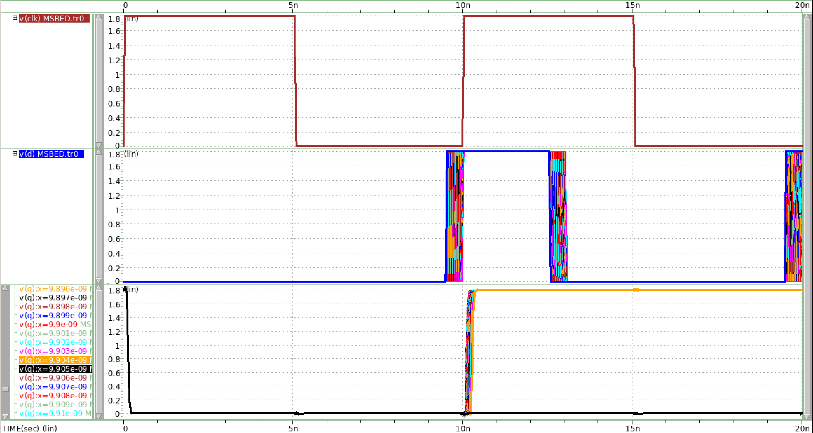
Master Slave Based ET DFF的 Setup Time and Hold Time

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圖 37 Master Slave Based ET DFF

Setup Time Finding(與p.8方法相同)

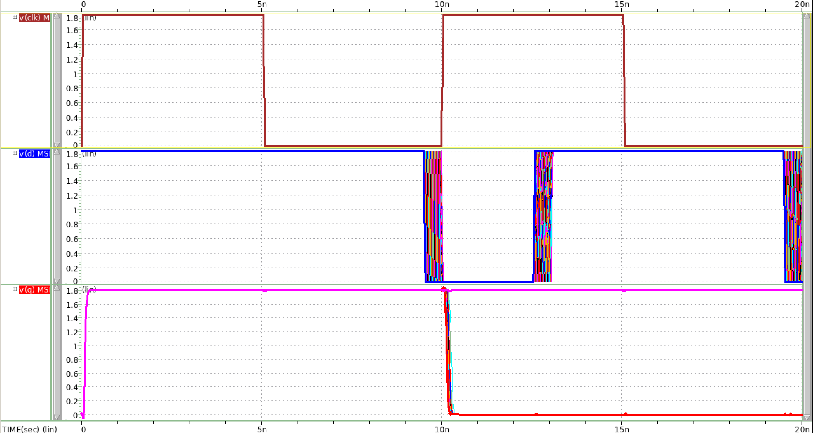


Output Q

Rising input

clock

圖 38 Setup Time finding(rising input)



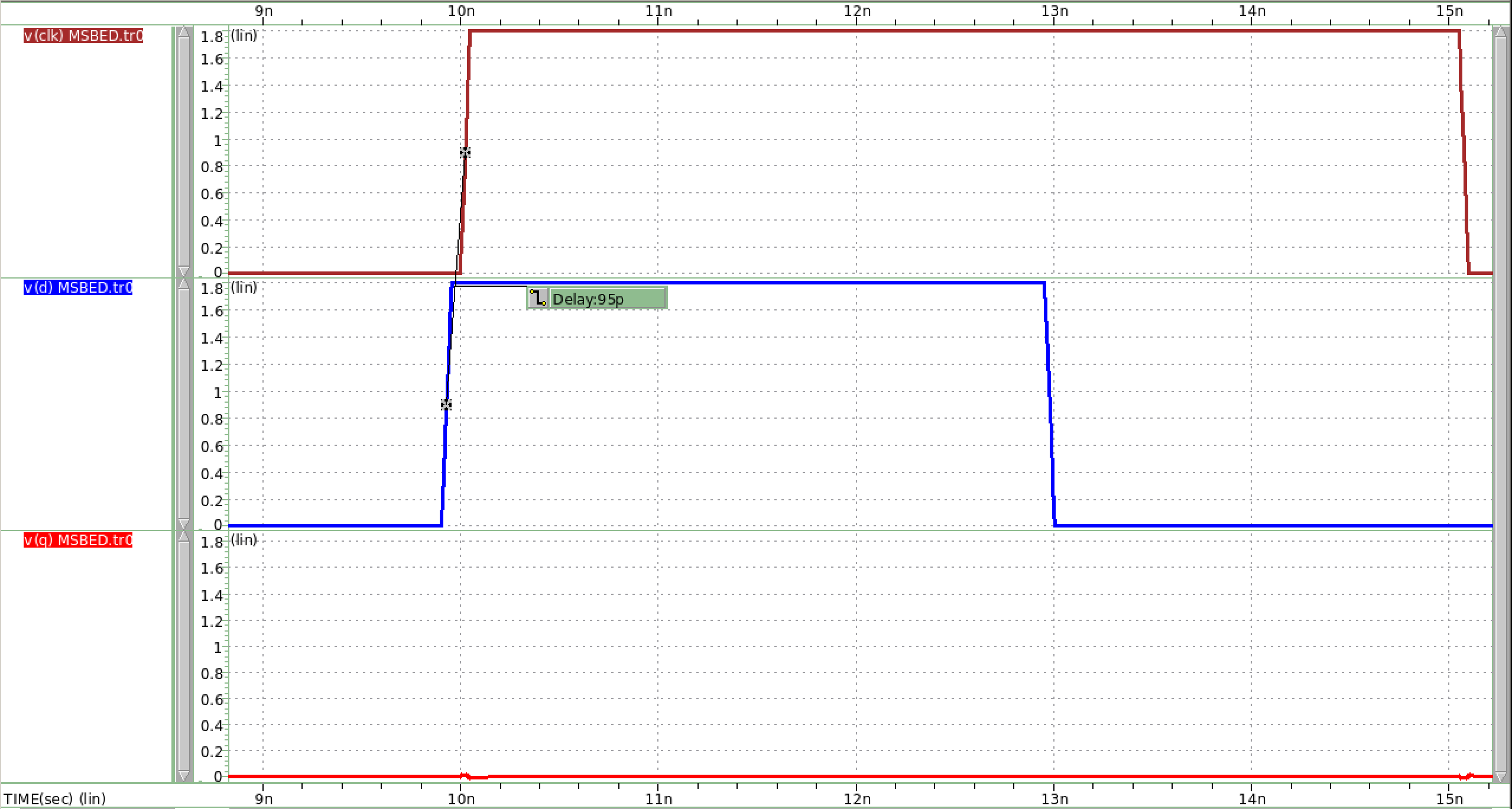
clock

Falling input

Output Q

圖 39 Setup Time finding(falling input)

Setup Time Simulation (rising input)



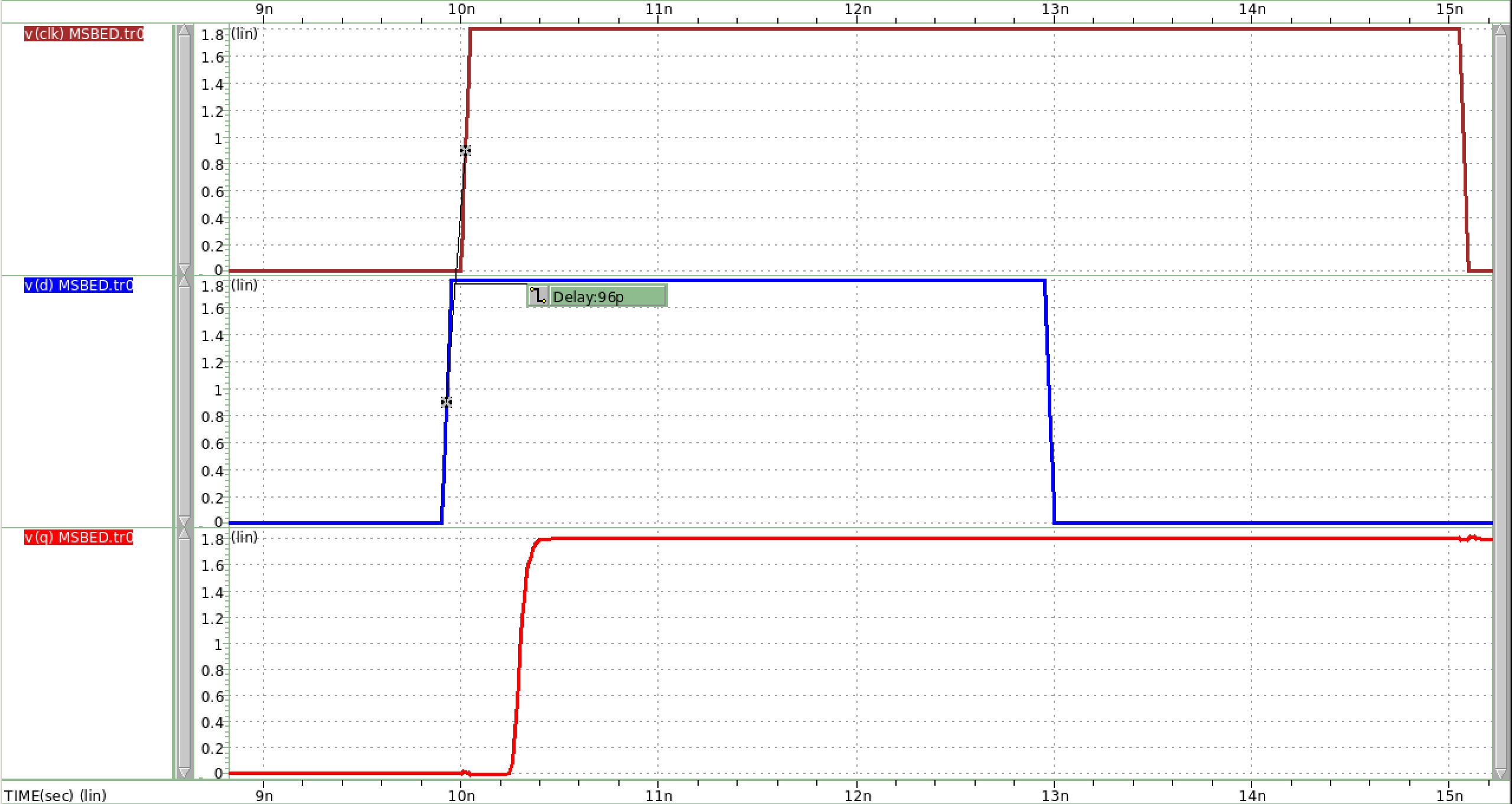
Output Q

Rising input

clock

圖 40 Setup Time failed (rising input)

**Setup Time = 95ps時，Output沒有因CLK edge而轉態為1。**



clock

Rising input

Output Q

圖 41 Setup Time success (rising input)

**Setup Time = 96ps時，Output因CLK edge而轉態為1，電路正常運作。由此可知，input為rising input時，setup time = 96ps。**

Setup Time Simulation (falling input)

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自動產生的描述

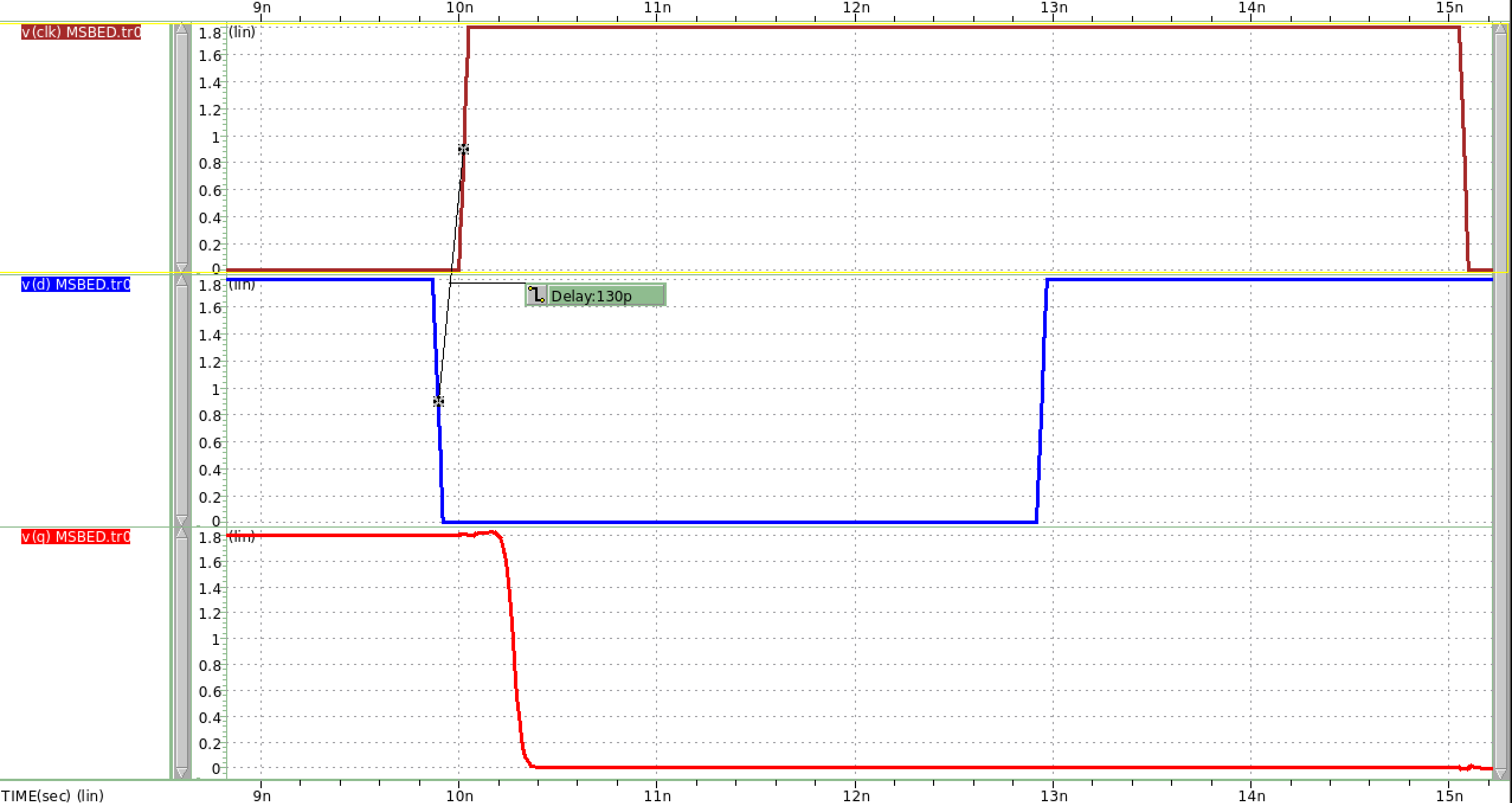
clock

Falling input

Output Q

圖 42 Setup Time failed (fallng input)

**Setup Time = 129ps時，Output沒有因CLK edge而轉態為0。**



clock

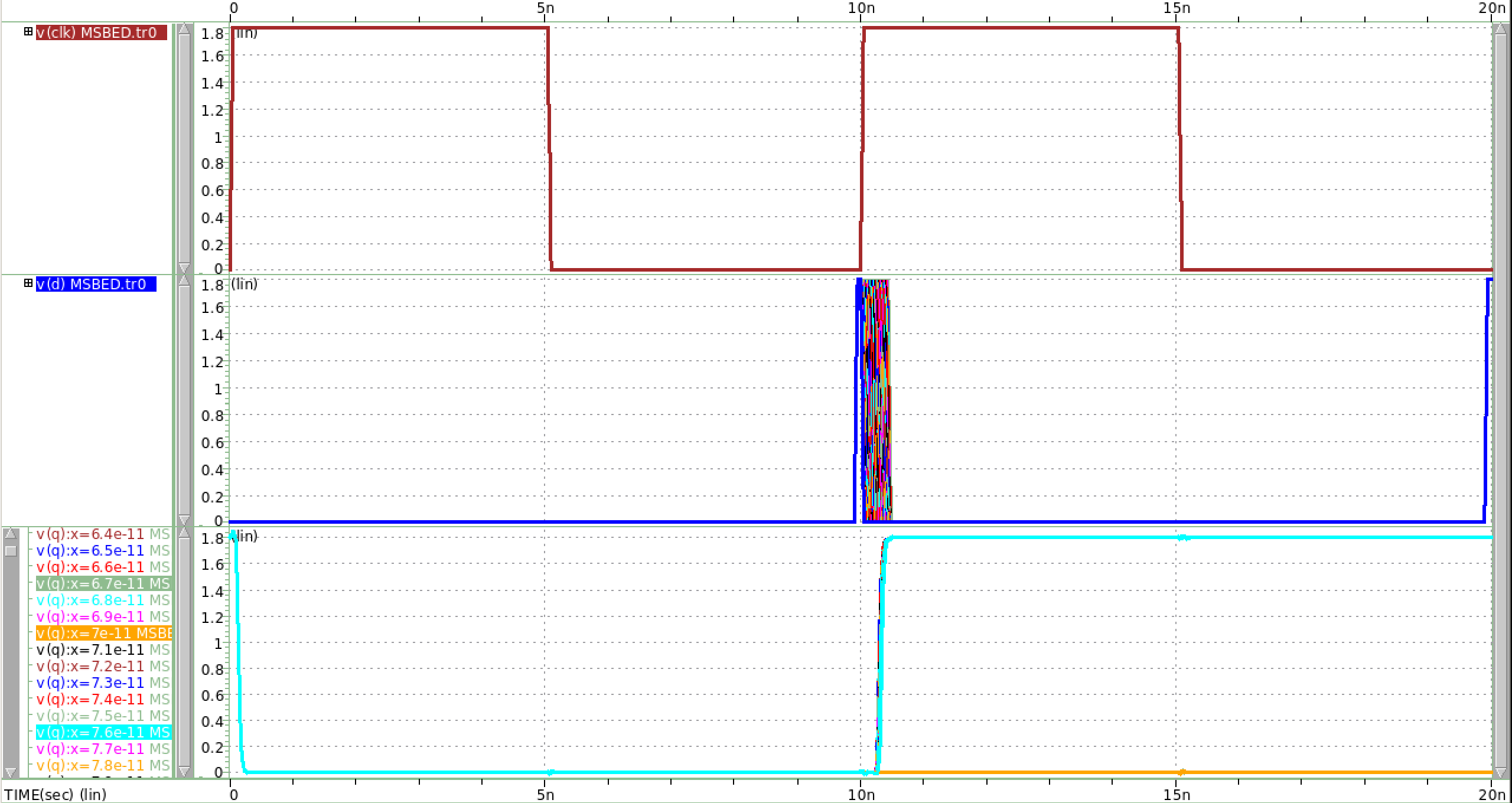
Falling input

Output Q

圖 43 Setup Time success (falling input)

**Setup Time = 130ps時，Output因CLK edge而轉態為0，電路正常運作。由此可知，input為falling input時，setup time = 130ps。**

Hold Time finding (與p.11方法相同)



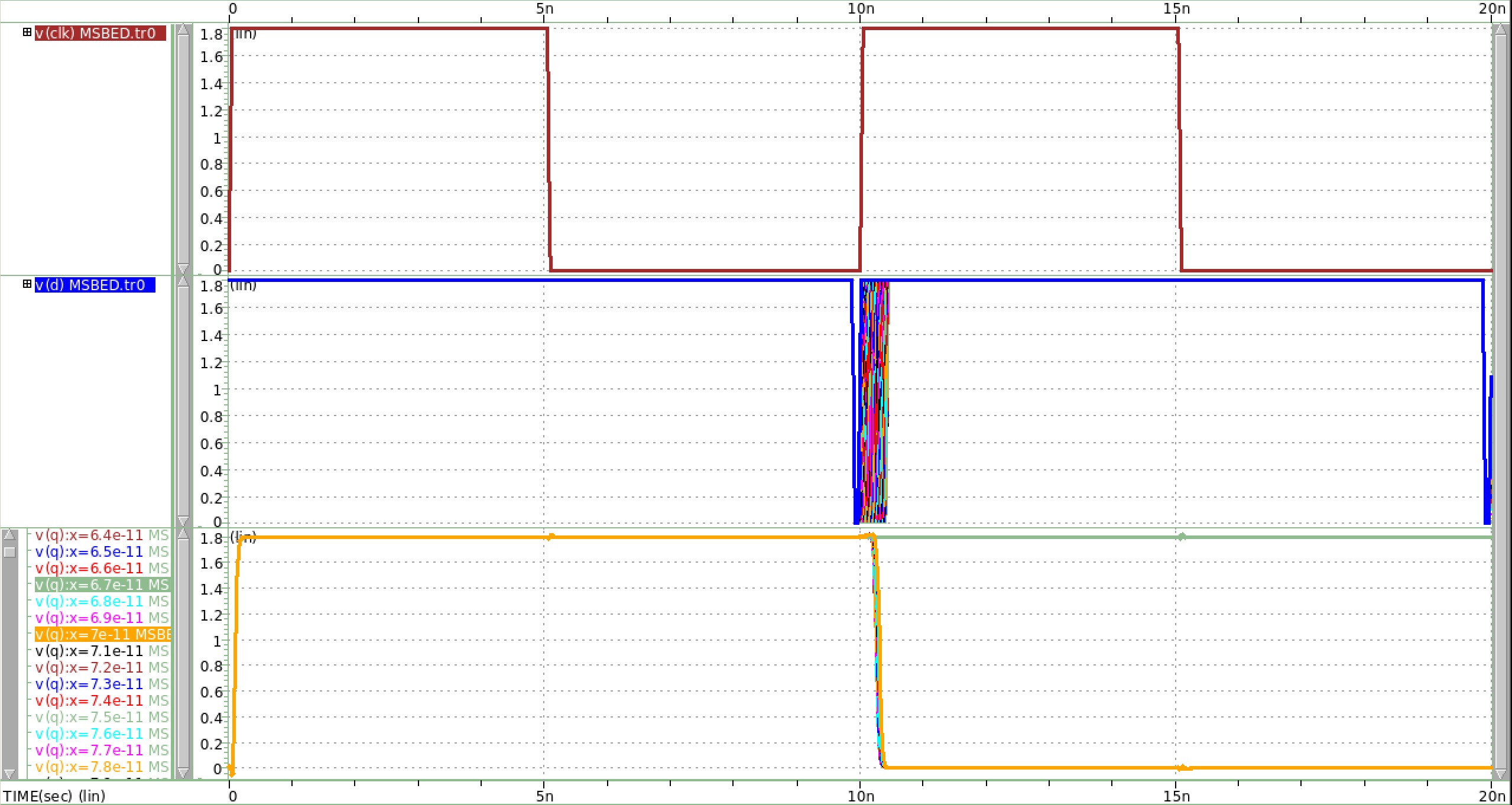
clock

Rising input

Output Q

圖 44 hold time finding(rising input)

**Output Q 淺藍色線條為failed output，橘色線條則為success output，透過兩線條交界處可得到hold time至少需要多少。**



clock

Falling input

Output Q

圖 45 hold time finding(falling input)

**Output Q 綠色線條為failed output，橘色線條則為success output，透過兩線條交界處可得到hold time至少需要多少。**

Hold Time Simulation (Rising Input)



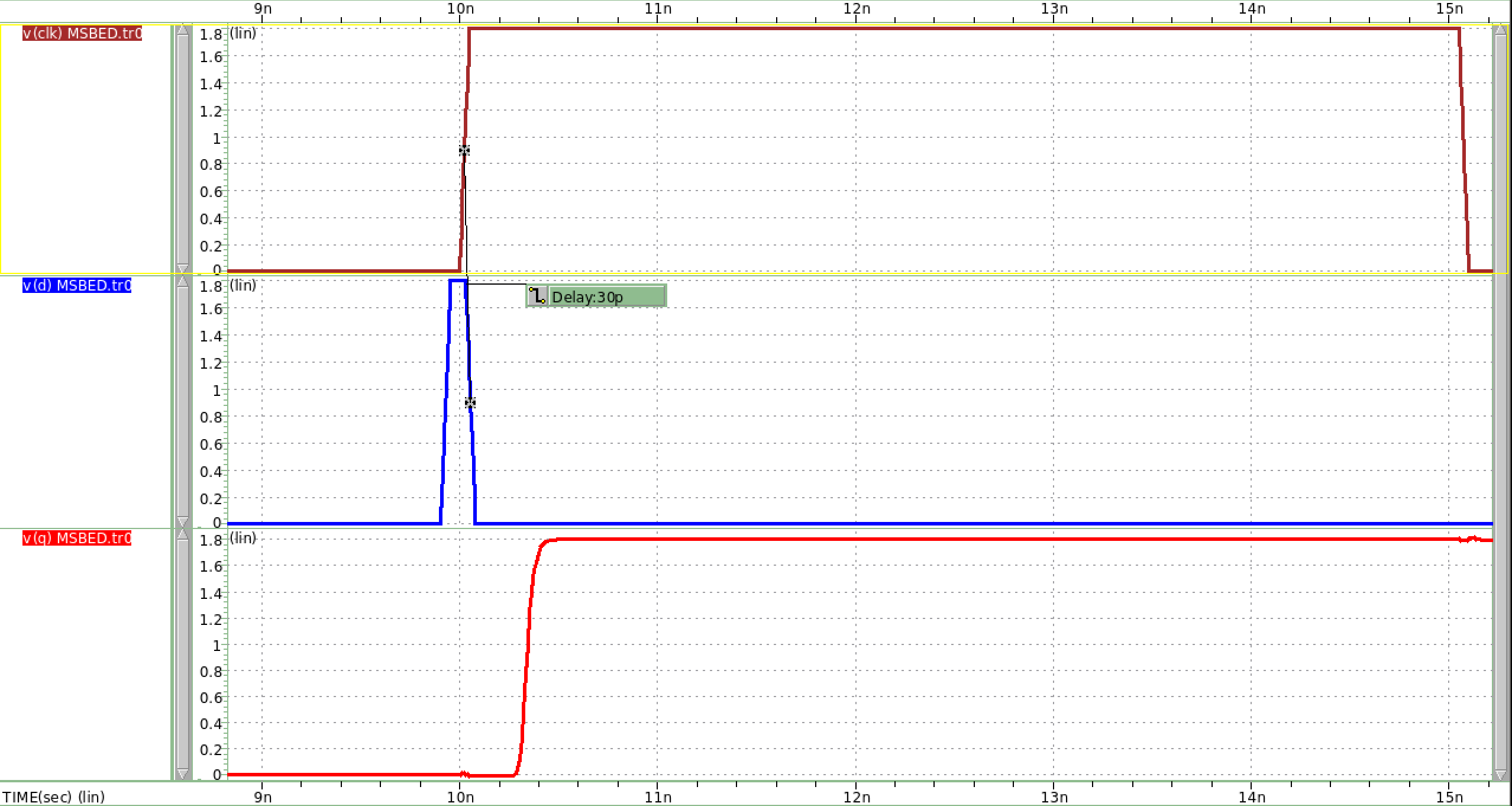
clock

Risling input

Output Q

圖 46 hold time failed (rising input)

**Hold Time = 29ps時，Output沒有因CLK edge而轉態為1。**



clock

Rising input

Output Q

圖 47 hold time success (rising input)

**Hold Time = 30ps時，Output因CLK edge而轉態為1。透過simulation可知當input為rising input時，hold time = 30ps。**

Hold Time Simulation (Falling Input)



clock

Falling input

Output Q

圖 48 hold time failed (rising input)

**Hold Time = -11ps時，Output沒有因CLK edge而轉態為1。**



clock

Falling input

Output Q

圖 49 hold time success (rising input)

**Hold Time = -10ps時，Output因CLK edge而轉態為1。透過simulation可知當input為falling input時，hold time = -10ps。**

CLK to Q Delay



圖 50 CLK to Q delay(rising input)

**Clock to Q delay for rising input = 276ps**



圖 51 CLK to Q delay(falling input)

**Clock to Q delay for rising input = 253ps**

Master Slave Based ET DFF with inverter chain

**Note: Maximum propagation delay Tpd ≦ Tc – (Tsetup + Tpcq)**

**Minimum contamination delay Tcd ≧ Thold - Tccq**

**表格 3 Master Slave Based ET DFF simulation result**

|  |  |  |
| --- | --- | --- |
| **Tc = 10ns** | **Rising Input** | **Falling Input** |
| **Tsetup** | **96ps** | **130ps** |
| **Thold** | **30ps** | **-10ps** |
| **CLK-Q delay** | **253ps (Tccq)** | **276ps (Tpcq)** |
| **Maximum Tpd** | **9.628ns** | |
| **Minimum Tcd** | **-263ps** | |

**此表格是沒有insert inverter chain的Master Slave Based ET DFF的各項simulation result。**

Maximum Propagation Delay

首先，先insert an inverter chain with 4 unit inverter，前2個unit inverter我分別在output端接上電容 (1pF) 來提供propagation delay。

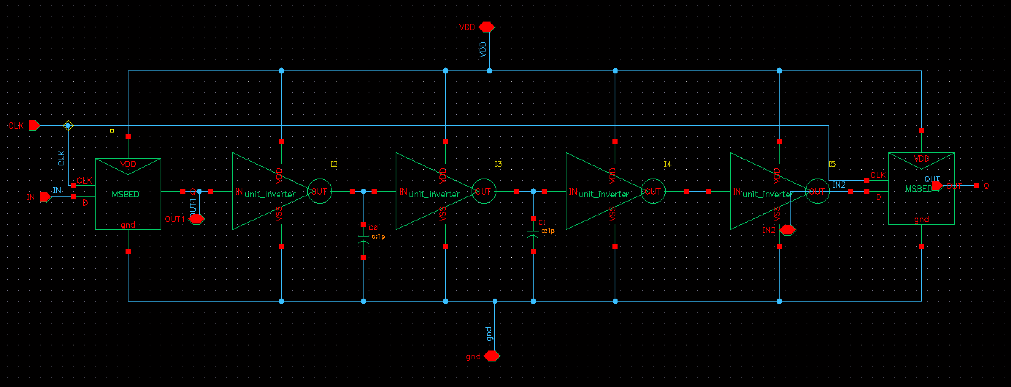


圖 52 MSBED insert 4 stage inverter

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自動產生的描述

CLK

INPUT

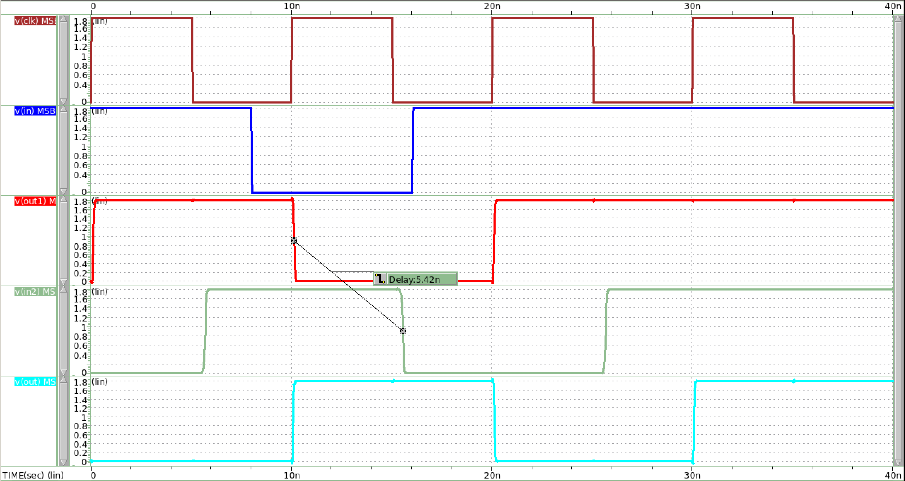
OUT1

INPUT2

OUT

圖 53 rising input

OUT1至INPUT2的delay即為propagation delay，在DFF insert 4 stages inverter的情況下，delay為5.59ns，小於Maximum propagation delay(9.628ns)。故OUT可正常輸出，電路運作正常。



CLK

INPUT

OUT1

INPUT2

OUT

圖 54 falling input

OUT1至INPUT2的delay為5.59ns，小於Maximum propagation delay(9.628ns)。故OUT可正常輸出，電路運作正常。

接著，insert an inverter chain with 6 unit inverter，前3個unit inverter我分別在output端接上電容 (1pF) 來提供propagation delay。

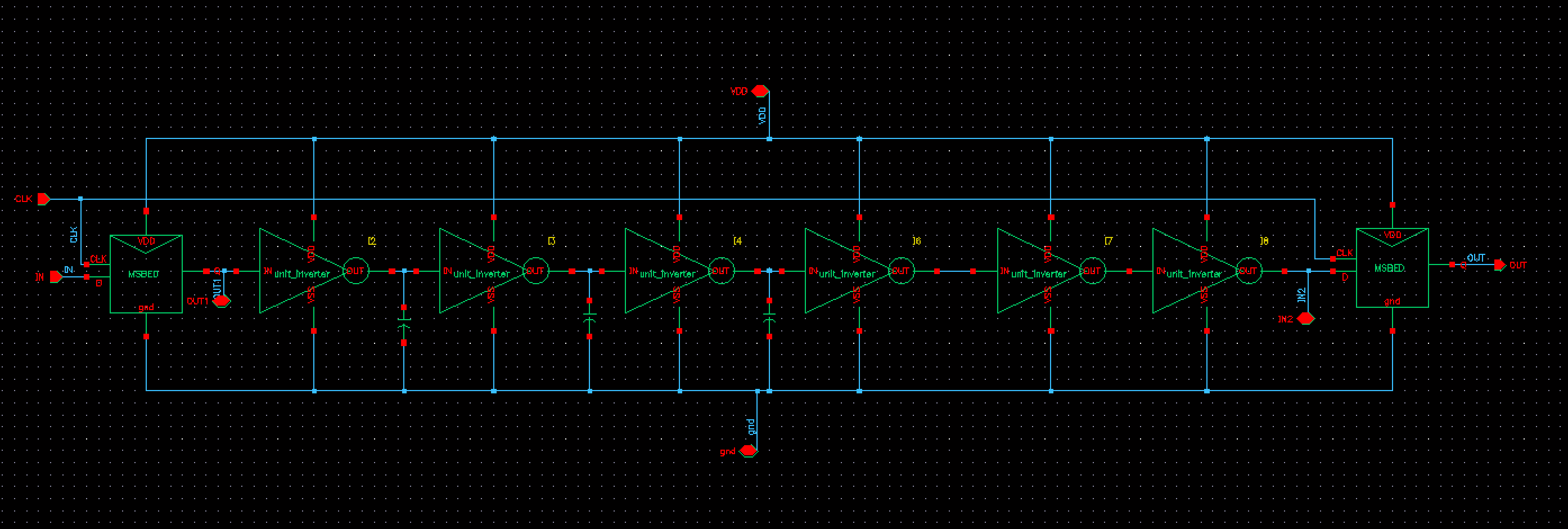
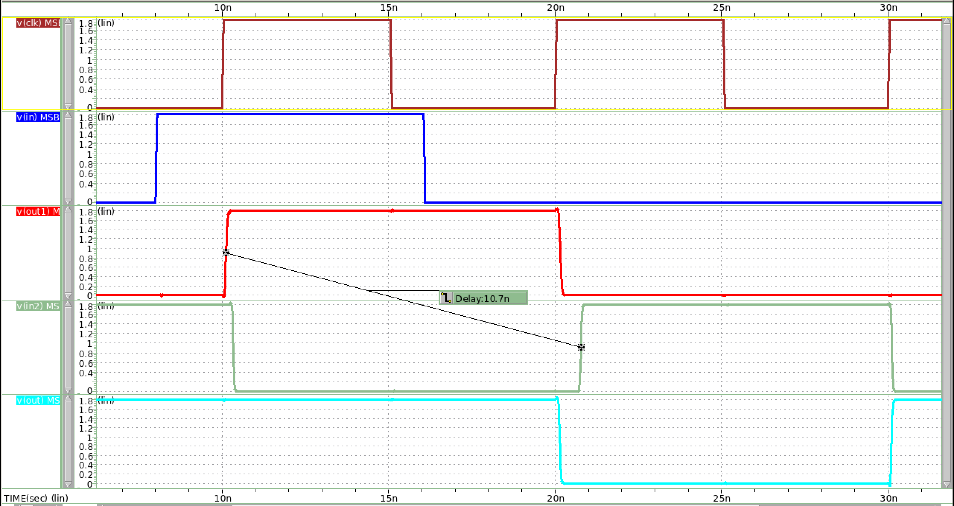


圖 55 MSBED insert 6 stage inverer



CLK

INPUT

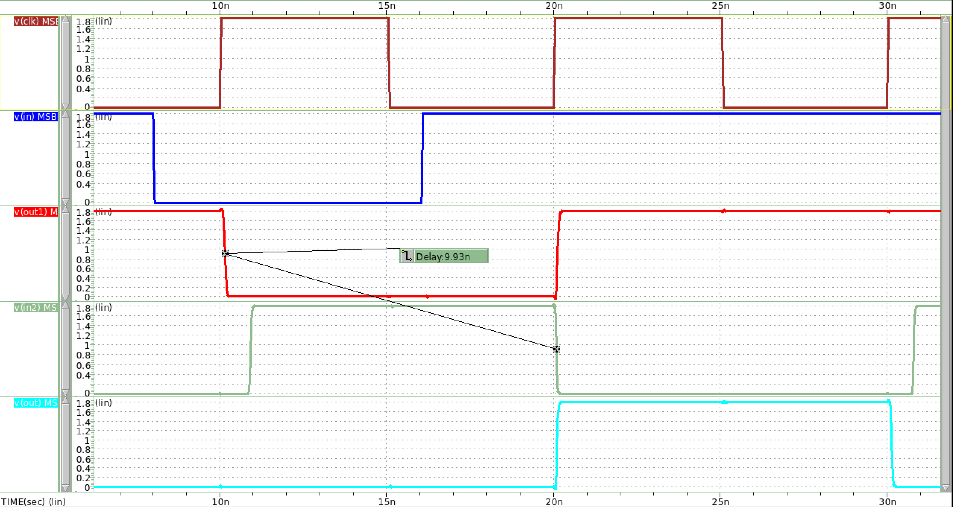
OUT1

INPUT2

OUT

圖 56 rising input

OUT1至INPUT2的delay為10.7ns，大於Maximum propagation delay(9.628ns)。因此OUT setup time不夠大，導致其無法順利在clk edge時轉態為1。



CLK

INPUT

OUT1

INPUT2

OUT

圖 57 falling input

OUT1至INPUT2的delay為9.93ns，大於Maximum propagation delay(9.628ns)。因此OUT setup time不夠大，導致其無法順利在clk edge時轉態為0。

Minimum Contamination Delay

**Simulation結果contamination delay < 0ps，代表兩個DFF之間在不加入combinational logic提供delay的情況下，也可正常運作，output不會floating。實際設計結果如下。**

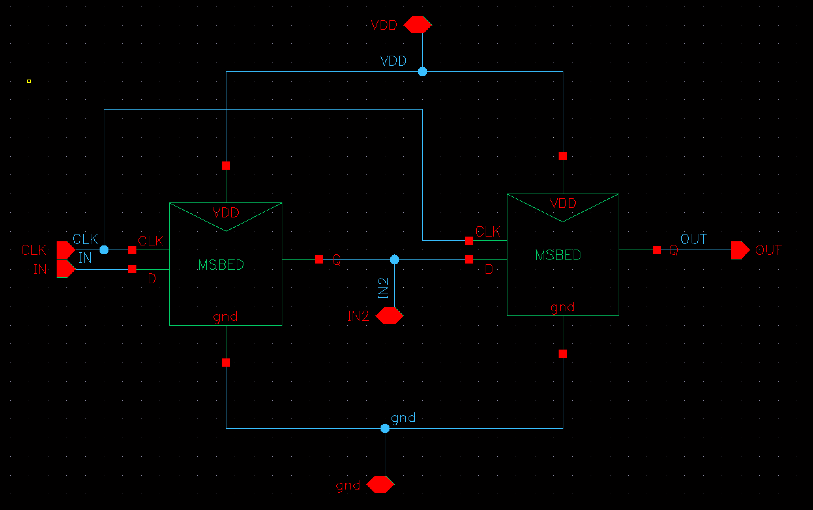


圖 58 Master Slave Based ET DFF with no inverter chain

|  |  |
| --- | --- |
| 圖 59 Rising Input | CLK  INPUT  OUT1=INPUT2  OUT  圖 60 Falling Input |

**實際設計模擬結果，無論是rising input還是falling input，電路接運作正常。**

**Rising input hold time=135ps;falling input hold time=90ps。接遠大於第一題所模擬的最小hold time，電路一定能運作正常。**

### Use the previous results in question1 (setup time and hold time) to hand calculate the maximum and minimum delay failure condition in (a). As for (b), do the same hand calculation as (a).

**Maximum propagation delay Tpd ≦ Tc – (Tsetup + Tpcq)**

**Minimum contamination delay Tcd ≧ Thold - Tccq**

**表格 4 maximum and minimum delay failure condition in (a)**

|  |  |  |
| --- | --- | --- |
| **Tc = 10ns** | **Rising Input** | **Falling Input** |
| **Tsetup** | **34ps** | **76ps** |
| **Thold** | **99ps** | **32ps** |
| **CLK-Q delay** | **258ps (Tccq)** | **265ps (Tpcq)** |
| **Maximum Tpd** | **9.701ns** | |
| **Minimum Tcd** | **-159ps** | |

**表格 5 Master Slave Based ET DFF simulation result**

|  |  |  |
| --- | --- | --- |
| **Tc = 10ns** | **Rising Input** | **Falling Input** |
| **Tsetup** | **96ps** | **130ps** |
| **Thold** | **30ps** | **-10ps** |
| **CLK-Q delay** | **253ps (Tccq)** | **276ps (Tpcq)** |
| **Maximum Tpd** | **9.628ns** | |
| **Minimum Tcd** | **-263ps** | |

### Please compare and comment the results of (a) and (b) with (c).

1. **為SR latch組成的DFF ; (b)為Master Slave Based ET DFF**

Master Slave Based ET DFF的setup time較SR latch組成的DFF長，推測是因為 Master Slave Based ET DFF經過的logic較多，故其INPUT也需更多的時間來準備。

至於hold time，Master Slave Based ET DFF的hold time較SR latch組成的DFF短，這也是因為前者logic數量較多，天生就擁有較大的propagation delay，導致Master Slave Based ET DFF input端的hold time反而不用那麼多。

根據公式:

**Maximum propagation delay Tpd ≦ Tc – (Tsetup + Tpcq)**

**Minimum contamination delay Tcd ≧ Thold - Tccq**

便可算出兩個DFF logic各自的Maximum propagation delay及Minimum contamination delay，因Master Slave Based ET DFF擁有較大的setup time及較小的hold time，使其**Maximum propagation delay較小，**若要在兩Master Slave Based ET DFF中間insert combinational logic，可以設計較小的delay logic。