2022 EE5250 VLSI Design Homework 1

Due date:2022/10/14

1. Please use the combination of CMOS to sketch the **transistor-level schematic** and **stick diagram** of the following compound gate function from those inputs A, B, C and D. (40%)

   (a) Y = A·B·C+D
   (b) Y = (A+B)·(C+D)
   (c) Y = A·C+B·C'
   (d) Y = A⊕B⊕C, ⊕ stands for XOR gate

> *<Notice>*
> *You can try to simplify the function first. Please use different color or pattern to represent different layers, and to mark or use legend to explain which color representing which layer.*
>
> *<Grading Guideline>*
> 10% for each question
> - 4% for transistor-level schematic
> - 5% for stick diagram
> - 1% for your comments.

2. Based on problem 1(a),1(b), **please finish DRC and LVS verification**. You must attach the pictures on your report which contain layout, DRC result and LVS result. (50%)

> *<Notice>*
> *$(W/L)_N$=3u/0.18u*
> *$(W/L)_P$=1u/0.18u*
> *V_{DD}=1.8V*
>
> *<Grading Guideline>*
> - 8% for layout schematic (4% for each)
> - 8% for DRC correct results (4% for each)
> - 8% for LVS correct results (4% for each)
> - 16% If meet minimum DRC rules (8% for each)
> - 10% Explain what DRC rules do you learn, please list them.
>   - ❖ Examples:
>   What's the minimum distance between metal and metal?
>   What's the minimum distance required for poly to exceed active region?

3. Draw the fabrication steps of an inverter (cross section). (10%)

➢ Please submit homework in PDF format and turn in it on eeclass system. You can finish this homework in handwriting paper and scan it into PDF format.

By CCHsieh