國立清華大學

超大型積體電路設計 VLSI Design

國立清華大學

NATIONAL TSING HUA UNIVERSITY

Homework 3

學號:111063548

姓名:蕭方凱

目錄

1. Run an inverter buffer (out = $i\bar{n}$) with output loading 75pF with VDD = 1.8V, as shown in Fig 1. (The size of the first inverter has been assigned.) (the rising time and falling time of input is 0.01ns & input frequency = 5MHz).

(a) Please find the unit inverter, calculate the g and p and use the parameter to calculate the optimum p with the simulation result and your normalization condition.

UNIT INVERTER SIZE:

Unit inverter	W/L	m
PMOS	0.6u/0.2u	3
NMOS	0.401u/0.2u	1

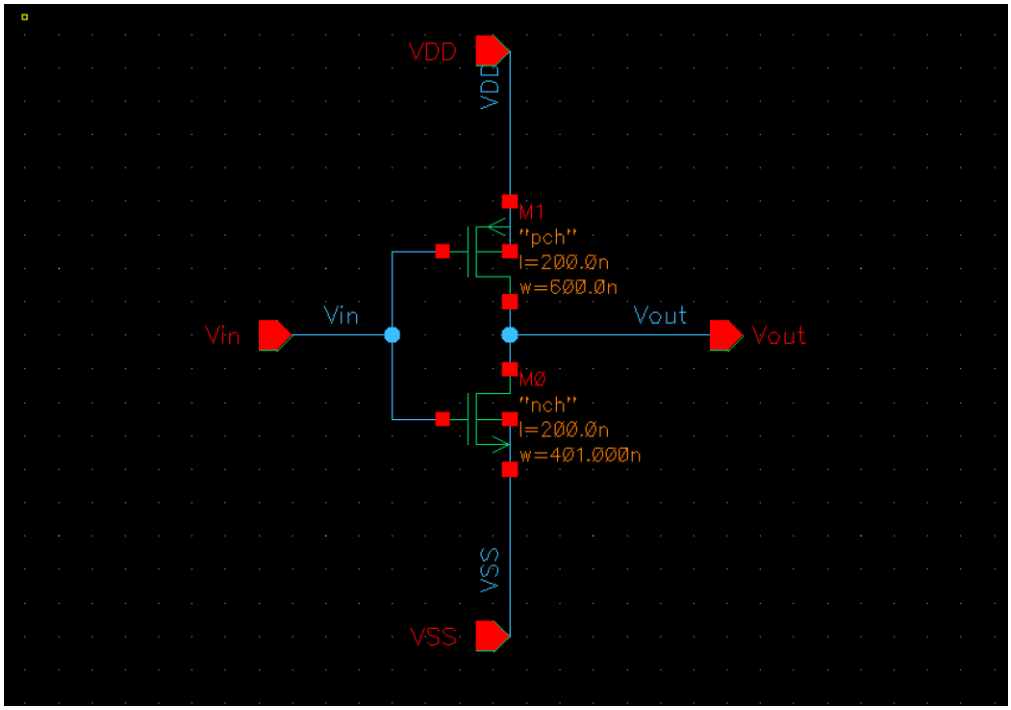


圖 1 unit inverter schematic

在選定 unit inverter size 時，有兩組 size:

1. P:828n/200n,m=3;N:600n/200n,m=1
2. P:600n/200n,m=3;N:401n/200n,m=1

但第二組得到的 g 會比較小，故 optimize delay 時選擇第二組 unit inverter 較佳

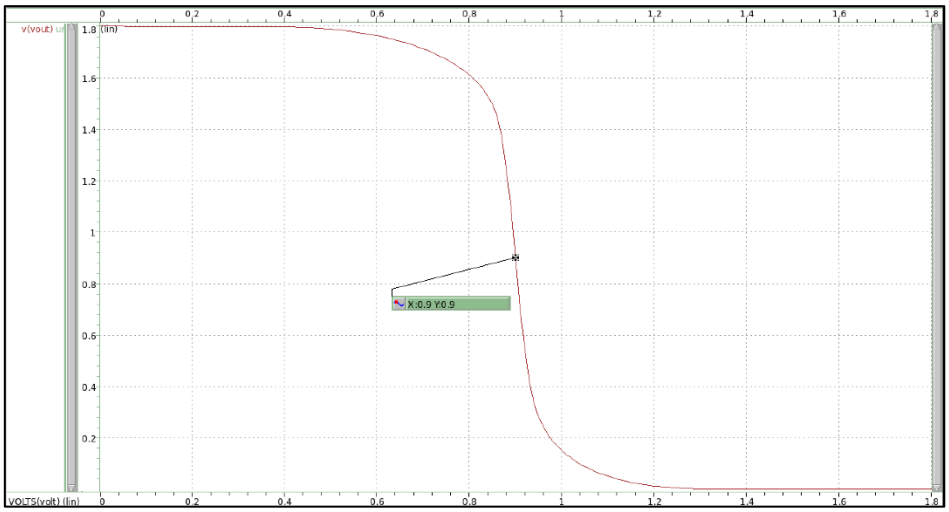


圖 2 unit unverter transfer curve(β =1)

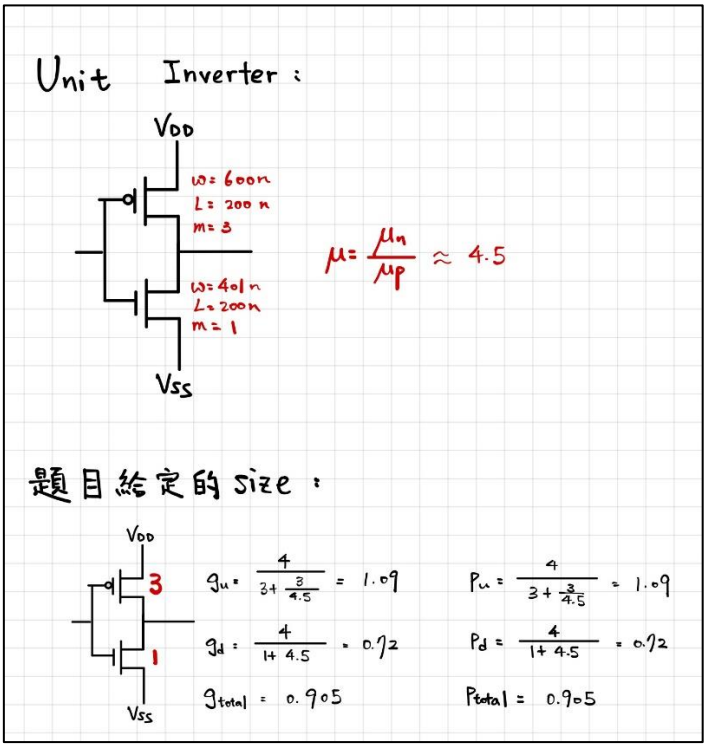
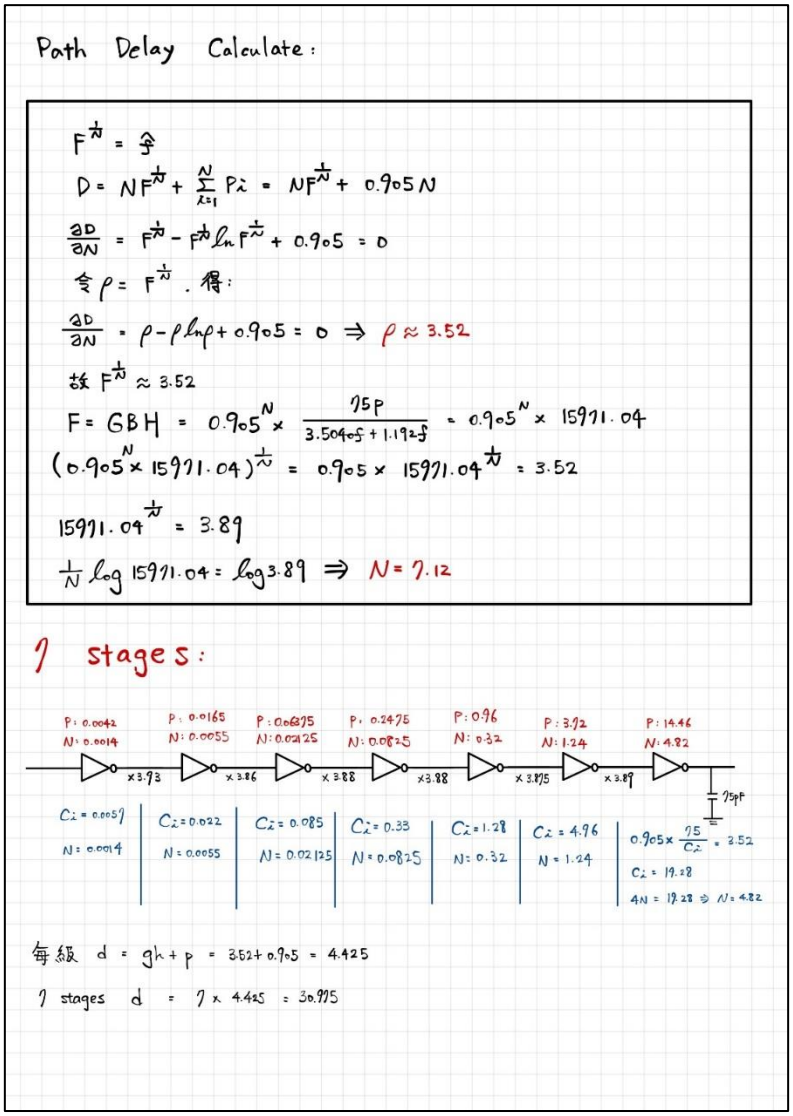


圖 3 g and p calculate

g=0.905;p=0.905

(b) Please design the size and stage of the inverter chain to reach tpdf and tpdr < 1ns



上方紅字 **P,N size** 並非真實的 size，此計算過程只為了**得到 stage 之間的 size 放大倍率**，每級間放大倍率約莫落在 3.8～3.9。而計算過程中的 **H 是題目給定的 load capacitance 與 spice 模擬出的(cgs+cgd)之比值。(Cin=Cgs+Cgd=4.696f)**

Number of stage	Parasitic delay(p)	Effort delay(f=gh)	Stage delay(d=f+p)	Path delay
7	0.905	3.52	4.425	30.975

Part1—Schematic Design

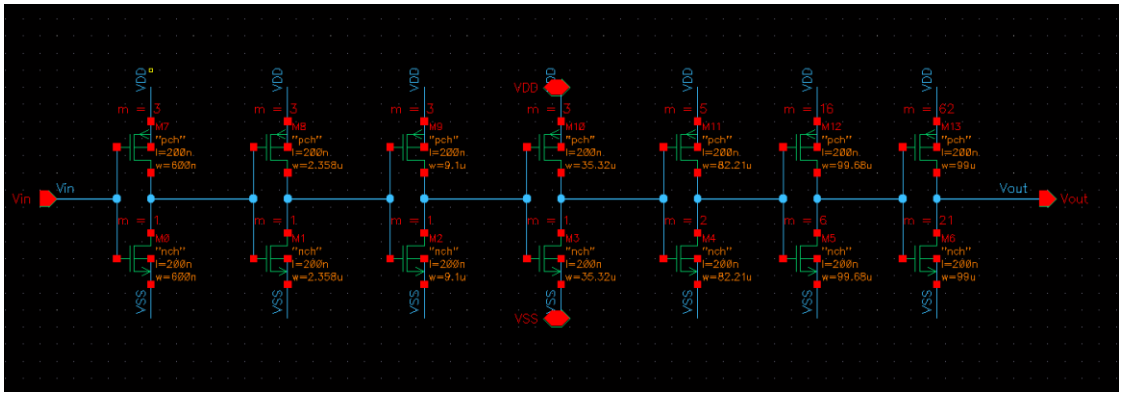


圖 4 inverter buffer schematic

表格 1 NMOS stage size

NMOS	W(L=2um)	m
First stage	0.6u	1
Second stage	2.358u	1
Third stage	9.1u	1
Fourth stage	35.32u	1
Fifth stage	82.21u	2
Sixth stage	99.68u	6
Seventh stage	99u	21

表格 2 PMOS stage size

PMOS	W(L=2um)	m
First stage	0.6u	3
Second stage	2.358u	3
Third stage	9.1u	3
Fourth stage	35.32u	3
Fifth stage	82.21u	5
Sixth stage	99.68u	16
Seventh stage	99u	62

Part2—Simulation and Waveview

數據定義:

Tpdf_0.5VDD: **input@0.5VDD** to **falling output@0.5vdd** propagation delay

Tpdr_0.5VDD: **input@0.5VDD** to **rising output@0.5vdd** propagation delay

Tpdf: **input@0.1VDD** to **falling output@0.1vdd** propagation delay

Tpdr: **input@0.9VDD** to **rising output@0.9vdd** propagation delay

```
**********************************************************************

****** transient analysis tnom=  25.000 temp=  25.000 ******
tddf_0.5vdd= 624.8854p  targ= 200.6749n   trig= 200.0500n
tpdr_0.5vdd= 630.1309p  targ= 100.7801n   trig= 100.1500n
tpdf= 740.0493p  targ= 200.7500n   trig= 200.0100n
tpdr= 759.8213p  targ= 100.8698n   trig= 100.1100n

         ***** job concluded
******
**********************************************************************
```

圖 5 propagation delay

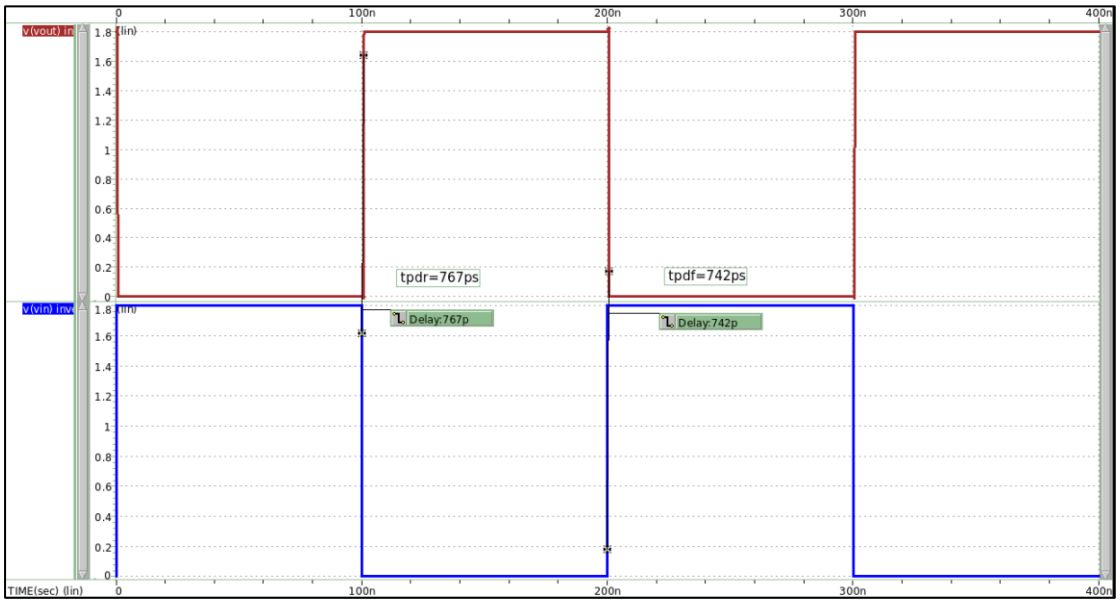


圖 6 output input waveview(.tran)

Tpdr=767ps;tpdf=742ps

Propagation delay = $\frac{tpdr+tpdf}{2}$ **= 754.5ps<0.1ns**

(c) Calculate the oscillation frequency based on the simulated parameters.

$$fosc = \frac{1}{2Nd} = \frac{1}{2x754.5p} = 662.69MHz$$

(d) Simulate the oscillation frequency

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**************************************************************************

****** transient analysis tnom=  25.000 temp=  25.000 ******
t_period=   1.1119n  targ=   1.7924n   trig= 680.5472p
frequency= 899.3827x

         ***** job concluded
******
**************************************************************************
```

圖 7 oscillation freq

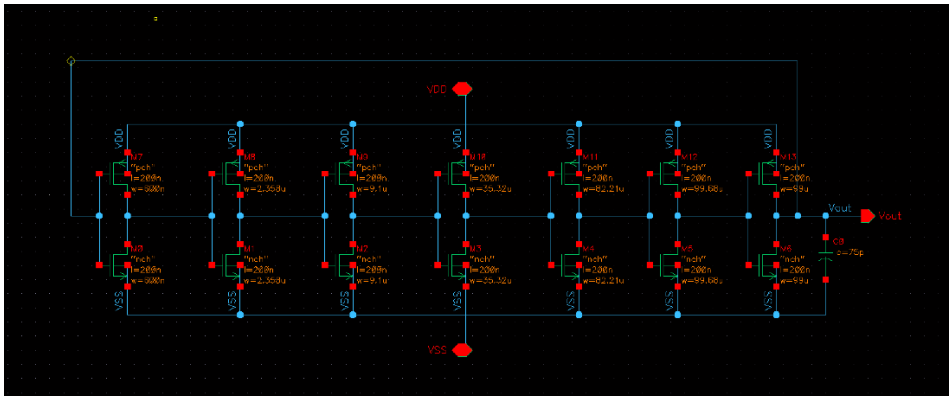


圖 8 oscillator schematic

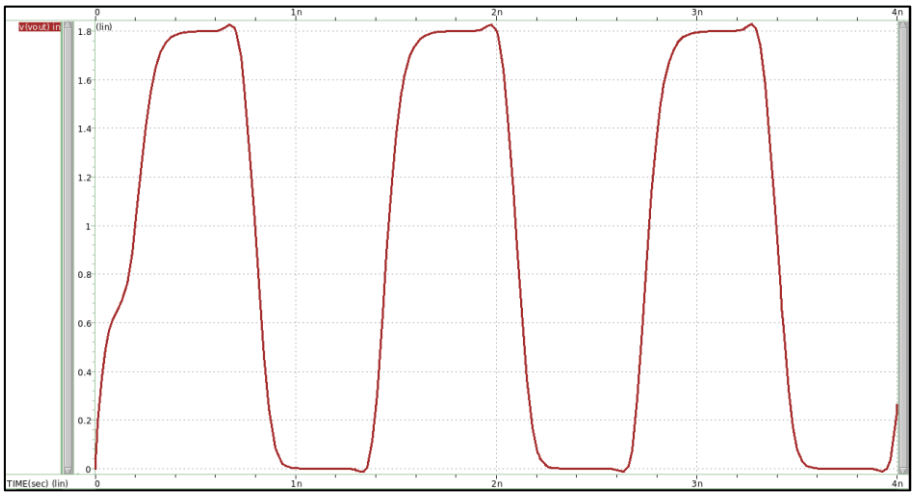


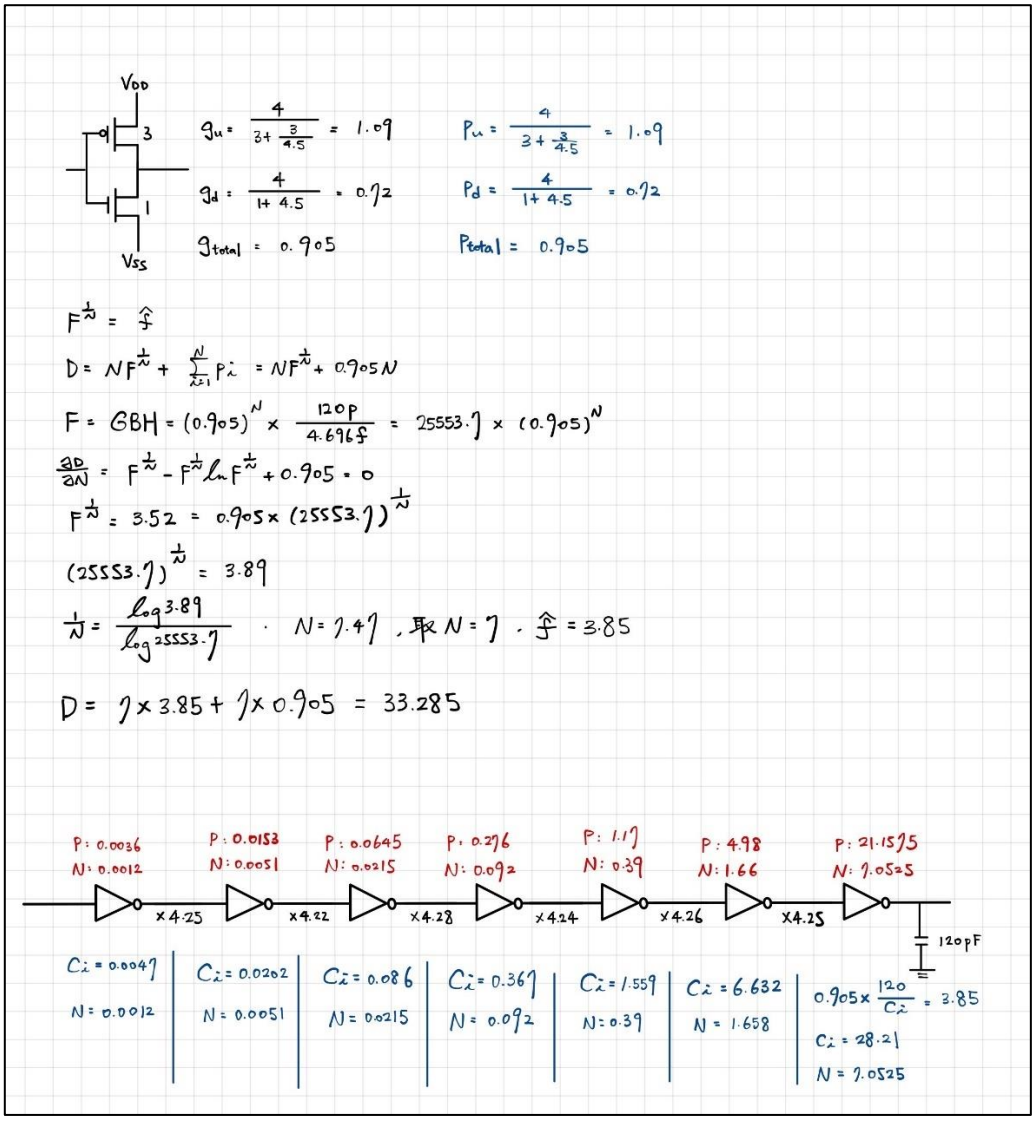
圖 9 oscillator waveview(.tran)

(e) What is the difference between (c) and (d), and comment on it.

本次作業 tpdr 和 tpdf 的定義較特別，分別定義在 rising output=0.9VDD 處和 fallinf output=0.1VDD 處，與都是 0.5VDD 處不同。

Simulation 時，分別觀察兩組定義的結果，發現定義在 0.5VDD 處的 delay 較小，**而$fosc = \frac{1}{2Nd}$ 的 d 是定義在 0.5VDD 的 propogation delay，在手算時，我是採用定義為 0.5VDD 之 propagation delay 計算**，所以 c 小題頻率會較 d 小題頻率小。

(f) Change the output loading to 120pF, fix the stage of the inverter chain, and compare the simulated oscillation frequency between the different output loading.



與(b)相同，此計算過程只為了**得到 stage 之間的 size 放大倍率**，每級間放大倍率約為 4.25。而計算過程中的 **H 是題目給定的 load capacitance 與 spice 模擬出的(cgs+cgd)之比值。(Cin=Cgs+Cgd=4.696f)**

Number of stage	Parasitic delay(p)	Effort delay(f=gh)	Stage delay(d=f+p)	Path delay(D)
7	0.905	3.85	4.755	33.285

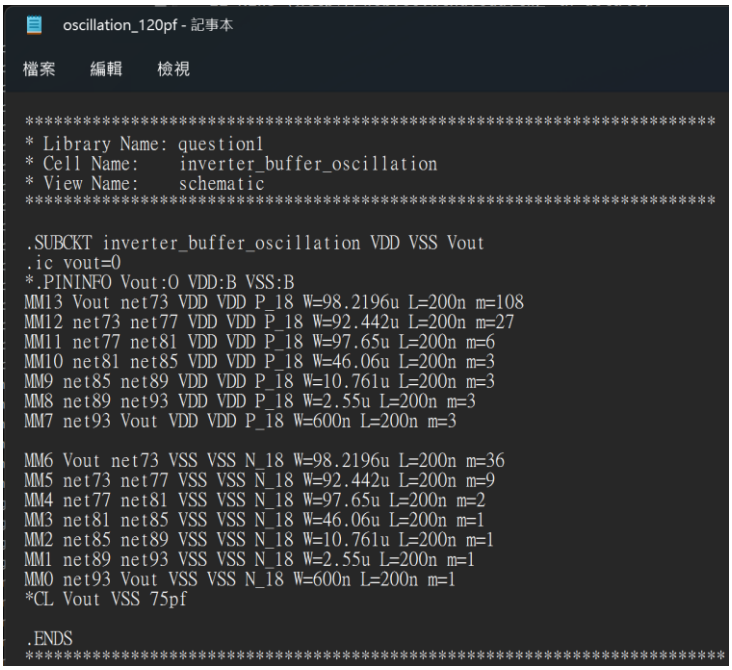


圖 10 CL=120pf oscillation sp file

表格 3 NMOS stage size

NMOS	W(L=2um)	M
First stage	0.6u	1
Second stage	2.55u	1
Third stage	10.761u	1
Fourth stage	46.06u	1
Fifth stage	97.65u	2
Sixth stage	92.442u	9
Seventh stage	98.22u	36

表格 4 PMOS stage size

PMOS	W(L=2um)	m
First stage	0.6u	3
Second stage	2.55u	3
Third stage	10.761u	3
Fourth stage	46.06u	3
Fifth stage	97.65u	6
Sixth stage	92.442u	27
Seventh stage	98.22u	108

```
**********************************************************************************

****** transient analysis tnom=  25.000 temp=  25.000 ******
t_period=   1.3827n  targ=   2.8984n   trig=   1.5157n
frequency= 723.2317x

         ***** job concluded
******
**********************************************************************************
```

圖 11 oscillation 120pf frequency

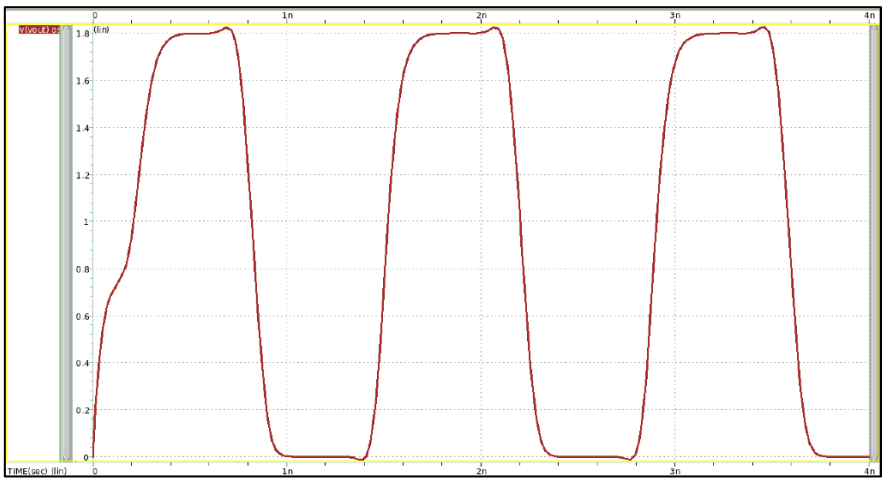


圖 12 CL=120pf oscillator waveview

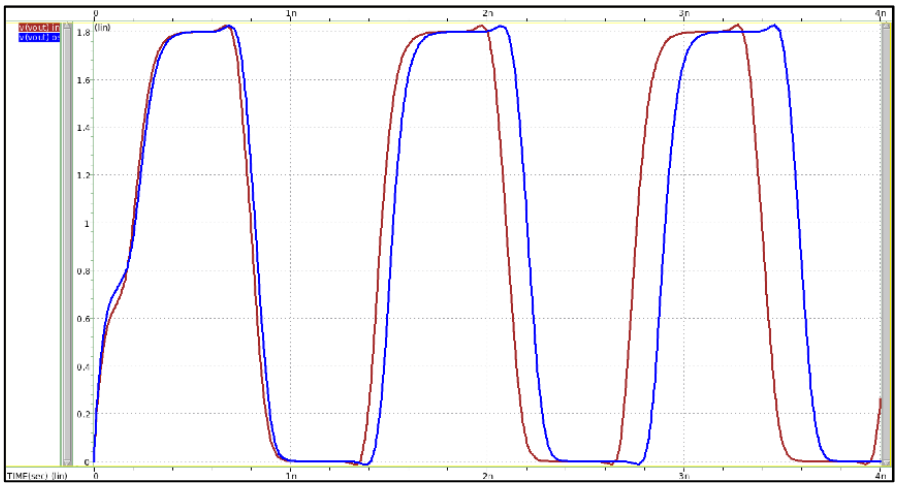


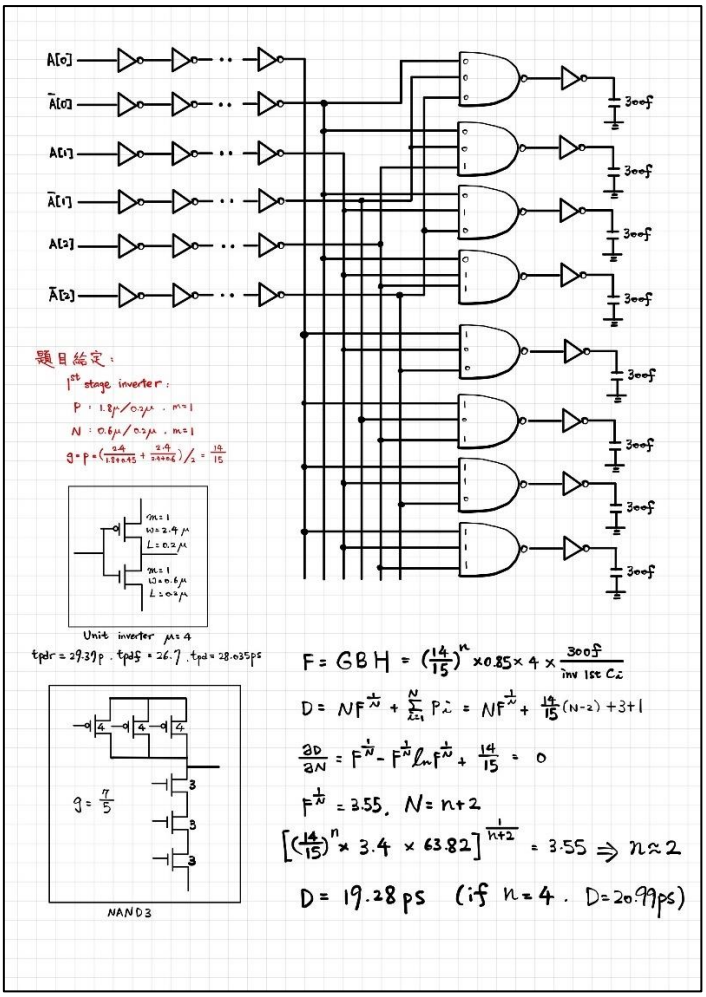
圖 13 compare between 75pf and 120pf oscillator
presim(紅) vs postsim(藍)

Bigger load capacitance cause H being larger. 因為 delay 與 H 成正比，所以 120pf 當 load capacitance 會使 propogation delay 變大。

2. Please design a 3-to-8 decoder with output loading 300fF at each output node (as shown in Fig. 2) and try to add an inverter buffer to minimize the delay from input to output of the decoder. VDD = 1.8V, and the size of the first inverter has been assigned.

(a) Describe how you design the inverter buffer and the other device size in detail.

Step1 :
hspice simulation，得到 unit inverter size 後，得到 μ 並計算題目給定 first stage inverter 的 logic effort。
Step2:
利用上一步得到之 μ，設計一個 3 input nand，並計算 logic effort。
Step3:
題目給定之 size，使整個 inverter buffer 的 Wp/Wn 比例固定為 3，故也可利用 μ 計算出 inverter buffer 的 logic effort。
Step4:
現在我們有 inverter buffer、3 input nand 的 logic effort and parasitic delay，便可計算出 Path effort，透過微分可得到最佳 number of stage to minimum the delay。
(下頁有 hand calculate 過程)



透過實際 simulation paramerter 得到 **N=2 時會有最小 delay**。

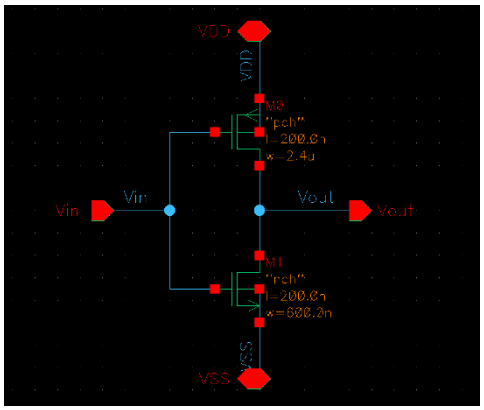


圖 14 unit inverter schematic

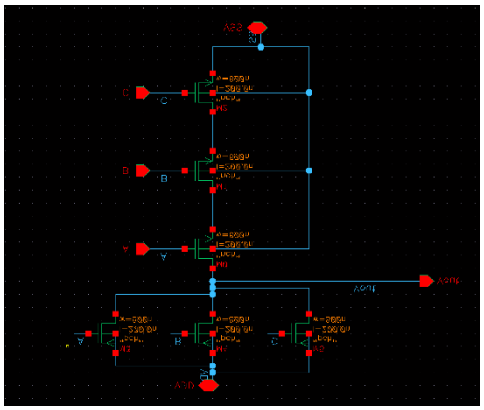


圖 15 3 input nand schematic

	Unit inverter	**3 input NAND**
(W/L)p	2.4u/0.2u	0.8u/0.2u
(W/L)n	0.6u/0.2u	0.6u/0.2u

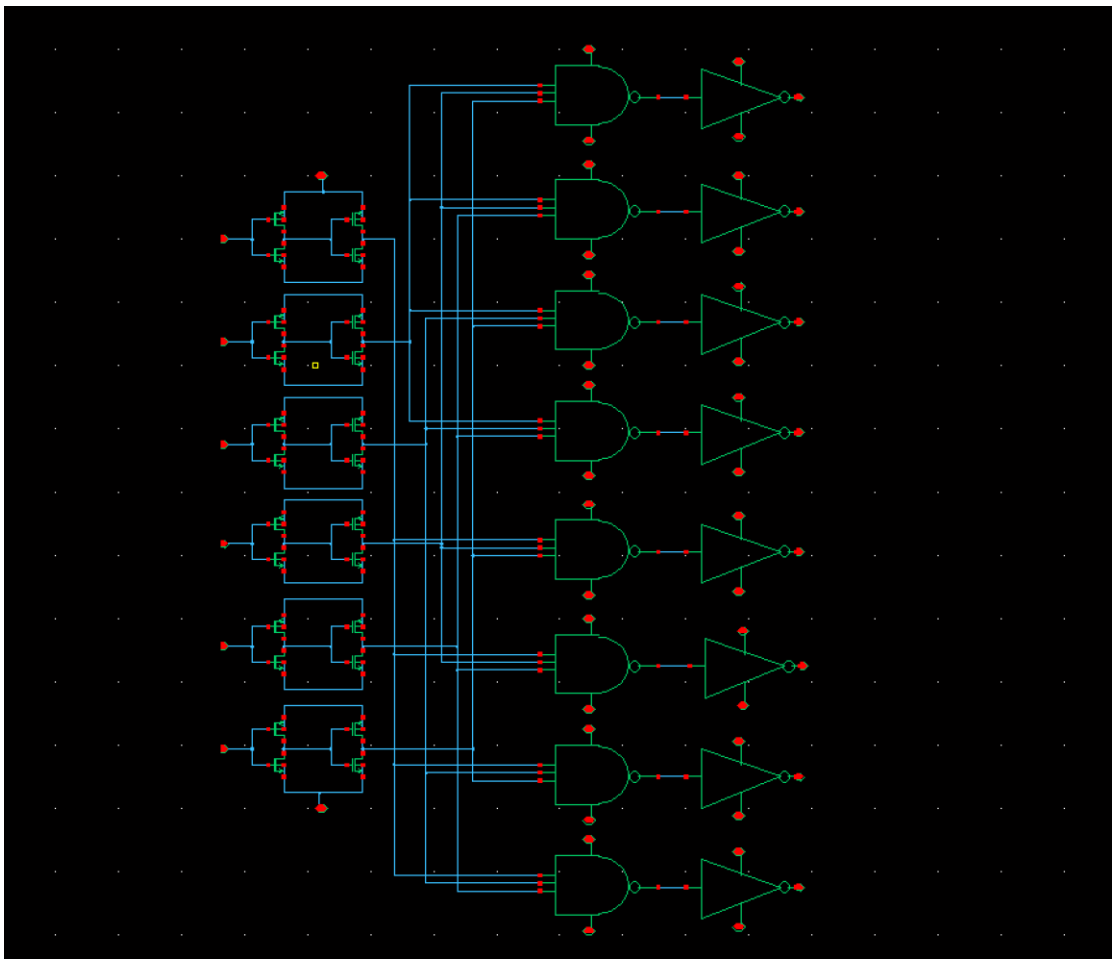


圖 16 3-8 decoder schematic

表格 5 each stage size

	1st inverter	2nd inverter	Nand3	Unit inverter
(W/L)p*m	1.8u/0.2u*1	1.8u/0.2u*4	0.8u/0.2u*1	2.4u/0.2u*1
(W/L)n*m	0.6u/0.2u*1	0.6u/0.2u*4	0.6u/0.2u*1	0.6u/0.2u*1

(b) Finish the layout(whole circuit, from “A” to “Out”), DRC, and LVS. Paste the photo of the layout, DRC result, and LVS result in your report. Please mark the length and width on the layout and calculate the area($um2$).

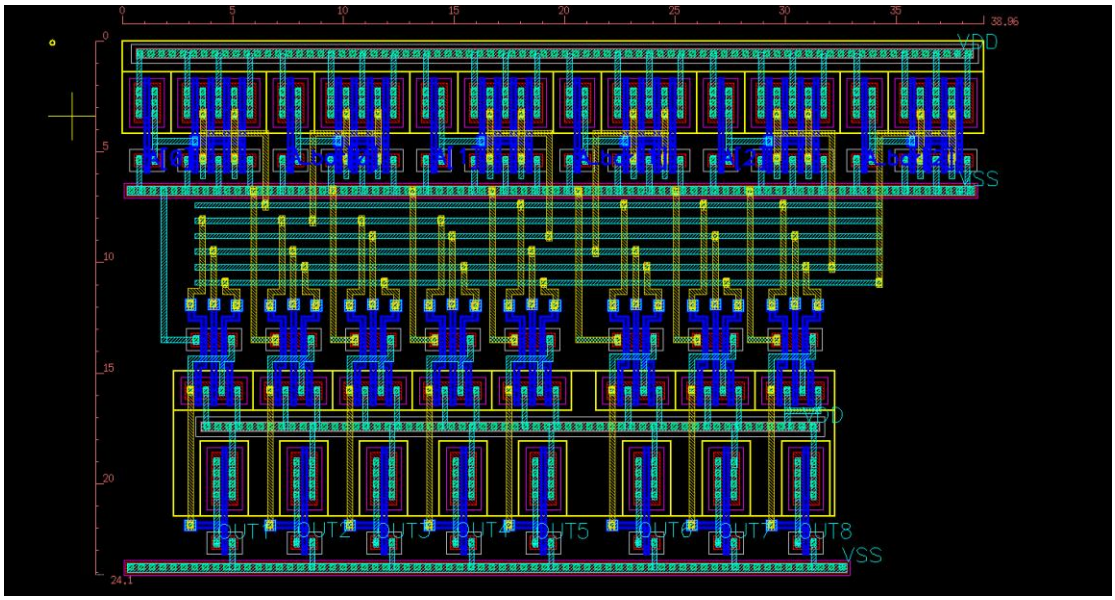


圖 17 3-8decoder layout

用 Distance 計算後，layout 面積為 39.64*24.565 = 973.7566μm^2

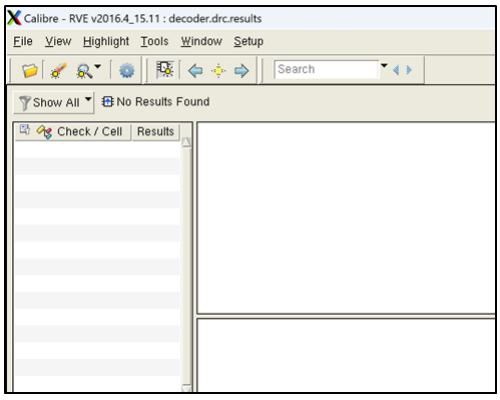


圖 18 layout DRC result

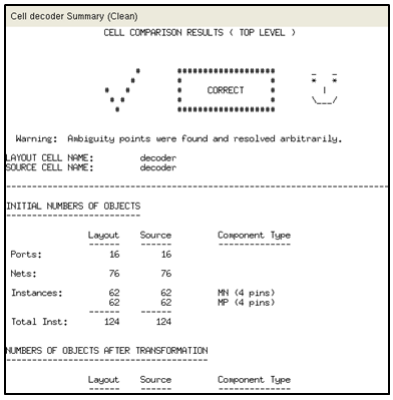


圖 19 layout LVS result

(c) Run the post-layout simulation and compare it with the pre-sim.

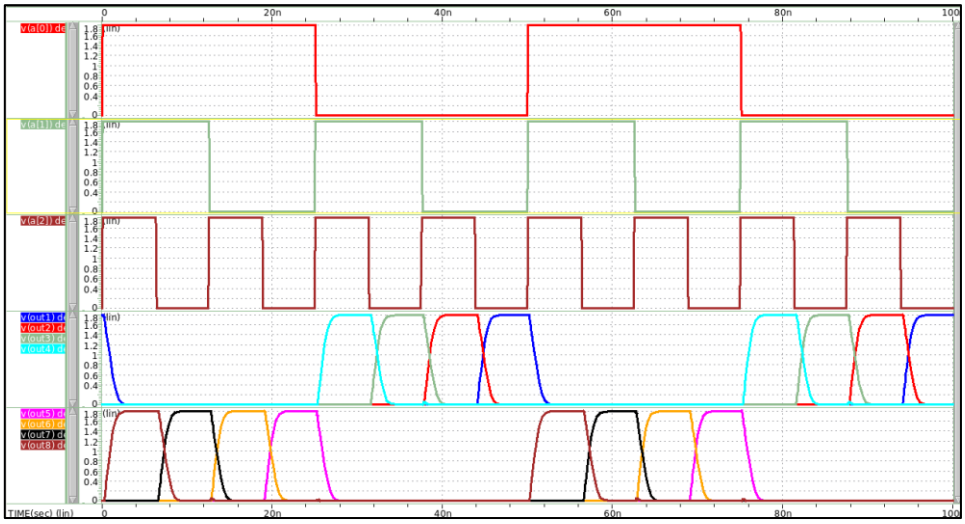


圖 20 presim waveview

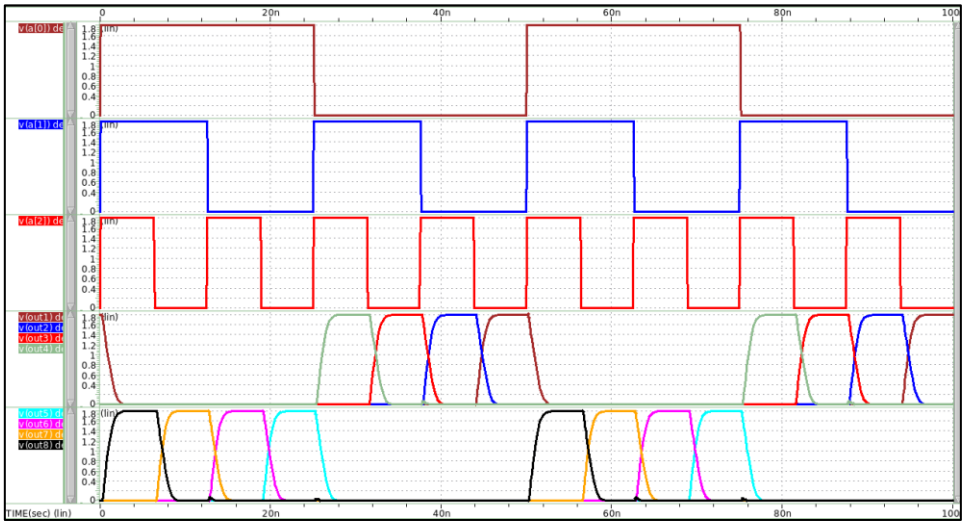


圖 21 postsim waveview

波形由上到下，分別為:

1. input A[0], is 0.01ns & input frequency = 20MHz
2. input A[1], is 0.01ns & input frequency = 40MHz
3. input A[2], is 0.01ns & input frequency = 80MHz
4. out1,out2,out3,out4(由左到右)
5. out5,out6,out7,out8,(由左到右)

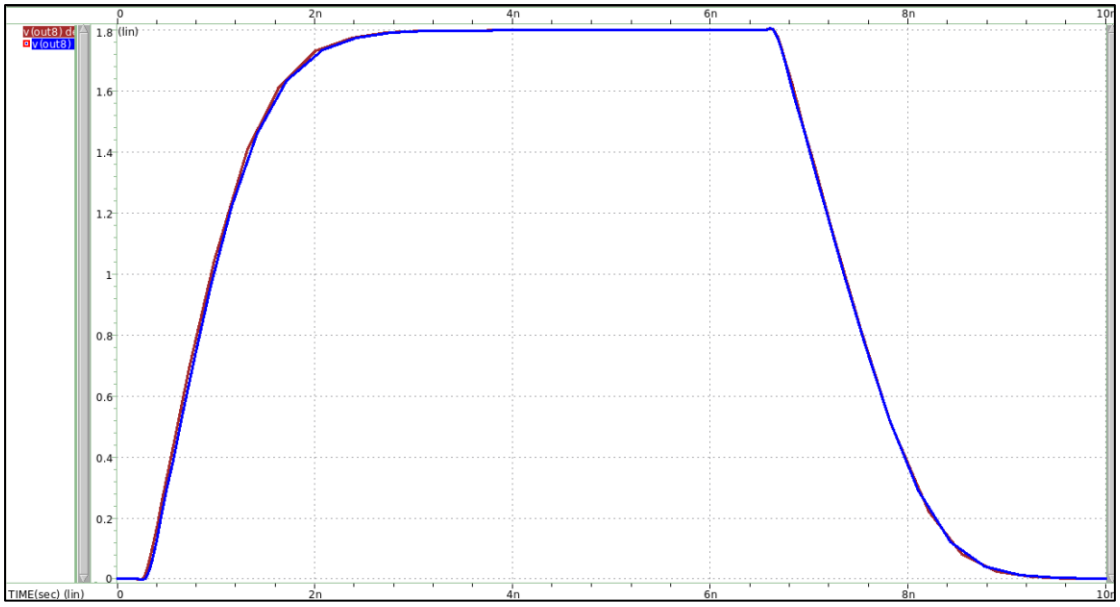


圖 22 presim(紅) vs postsim(藍)

Postsim 過後的波形(以 out8 為例)，delay 較 presim 大。推測是因為 postsim 過後，更貼近實際情況，電容更多，導致每級的 p 略微提升，進而影響整體 delay 表現。