國立清華大學

超大型積體電路設計 VLSI Design

國立清華大學

NATIONAL TSING HUA UNIVERSITY

Homework 1

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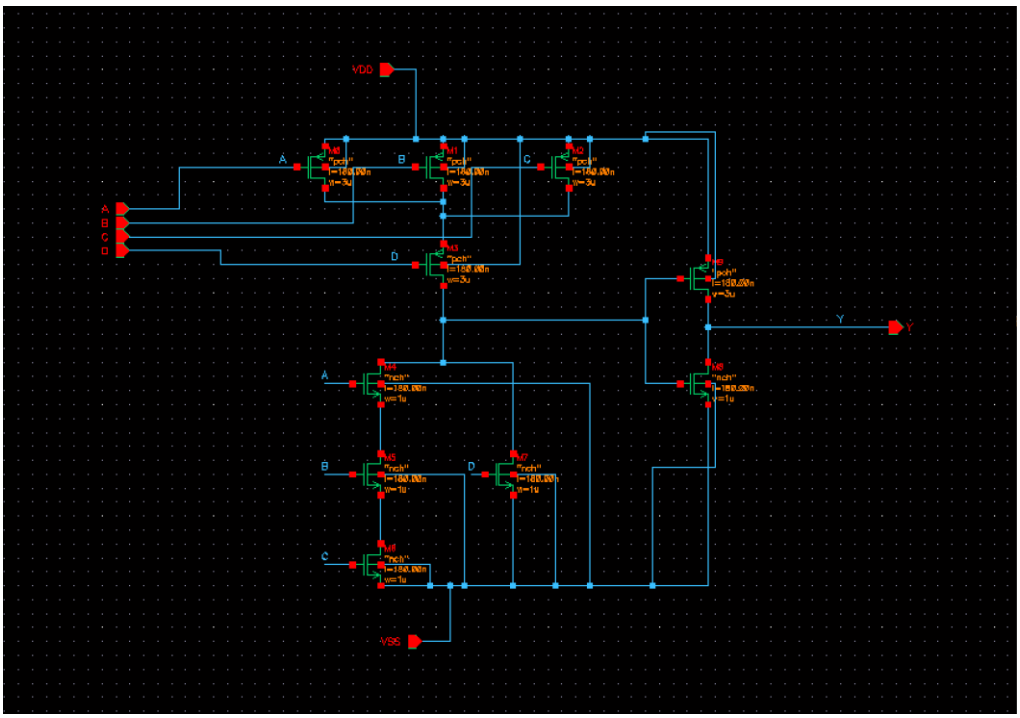
目錄

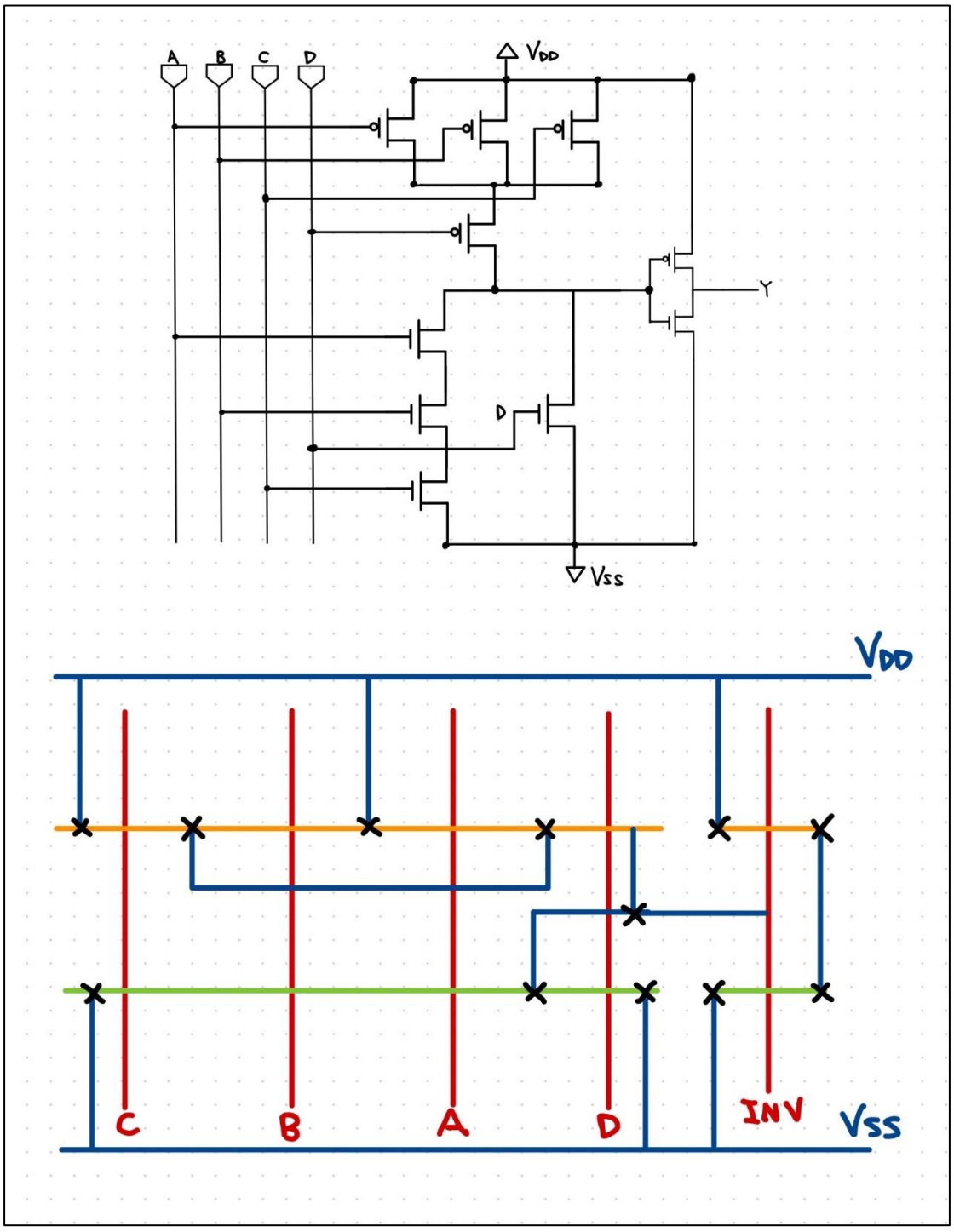
1. Please use the combination of CMOS to sketch the transistor-level schematic and stick diagram of the following compound gate function from those inputs A, B, C and D.

(a) $Y = A \cdot B \cdot C + D$

i. Schematic



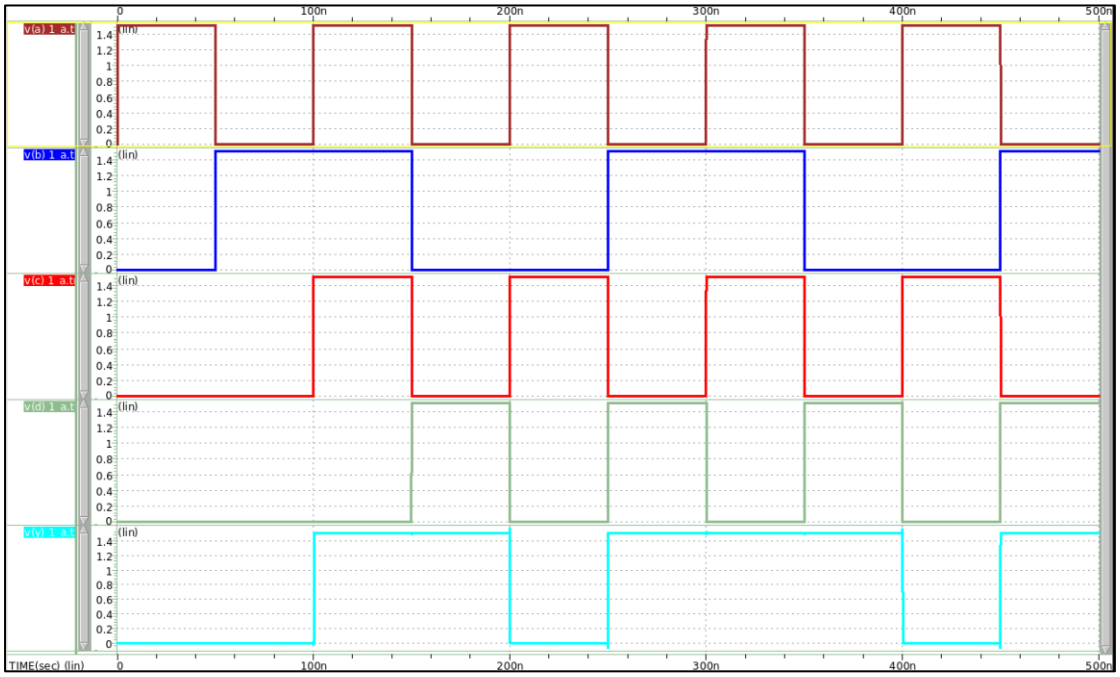
ii. Stick diagram



iii. spice code

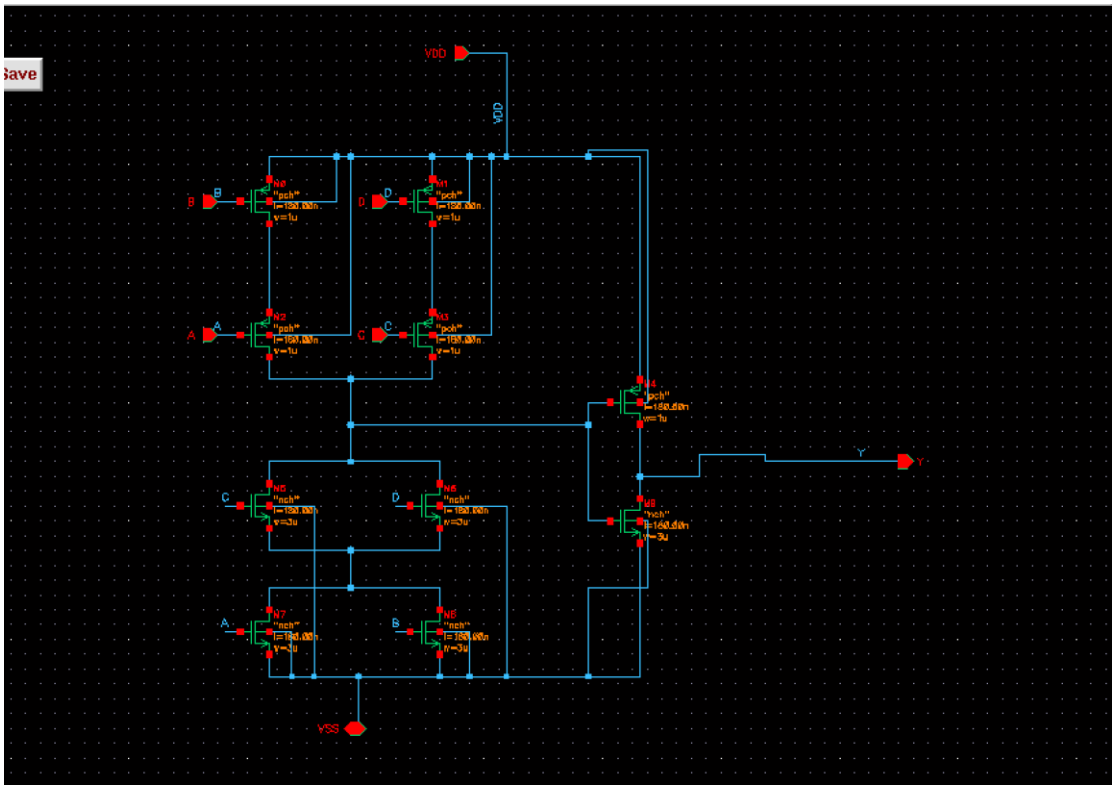
```
********************************************************************************
* Library Name: HW1
* Cell Name:    1_a
* View Name:    schematic
********************************************************************************
*ABC+D
.prot
.lib 'cic018.l' TT
.unprot
.temp 25
.option post acout=0 runlvl=6

*.SUBCKT 1_a A B C D VDD VSS Y
*.PININFO A:I B:I C:I D:I VDD:I VSS:I Y:O
MM8 Y net036 VSS VSS N_18 W=1u L=180.00n m=1
MM7 net036 D VSS VSS N_18 W=1u L=180.00n m=1
MM4 net036 A net051 VSS N_18 W=1u L=180.00n m=1
MM6 net16 C VSS VSS N_18 W=1u L=180.00n m=1
MM5 net051 B net16 VSS N_18 W=1u L=180.00n m=1
MM9 Y net036 VDD VDD P_18 W=3u L=180.00n m=1
MM3 net036 D net067 VDD P_18 W=3u L=180.00n m=1
MM2 net067 C VDD VDD P_18 W=3u L=180.00n m=1
MM0 net067 A VDD VDD P_18 W=3u L=180.00n m=1
MM1 net067 B VDD VDD P_18 W=3u L=180.00n m=1


**********source**********

VDD vdd 0 dc 1.5
VSS vss gnd dc 0

VAP A gnd PULSE 0 1.5 0 0.1n 0.1n 50n 100n
VBP B gnd PULSE 0 1.5 50n 0.1n 0.1n 100n 200n
VCP C gnd PULSE 0 1.5 100n 0.1n 0.1n 50n 100n
VDP D gnd PULSE 0 1.5 150n 0.1n 0.1n 50n 100n


**********analysis**********
.op
.tran 0.1ns 500n
*.tf v(vout) va
.probe v(vout)

.AC DEC 100 1K 1G


.end
```

iv. waveview result

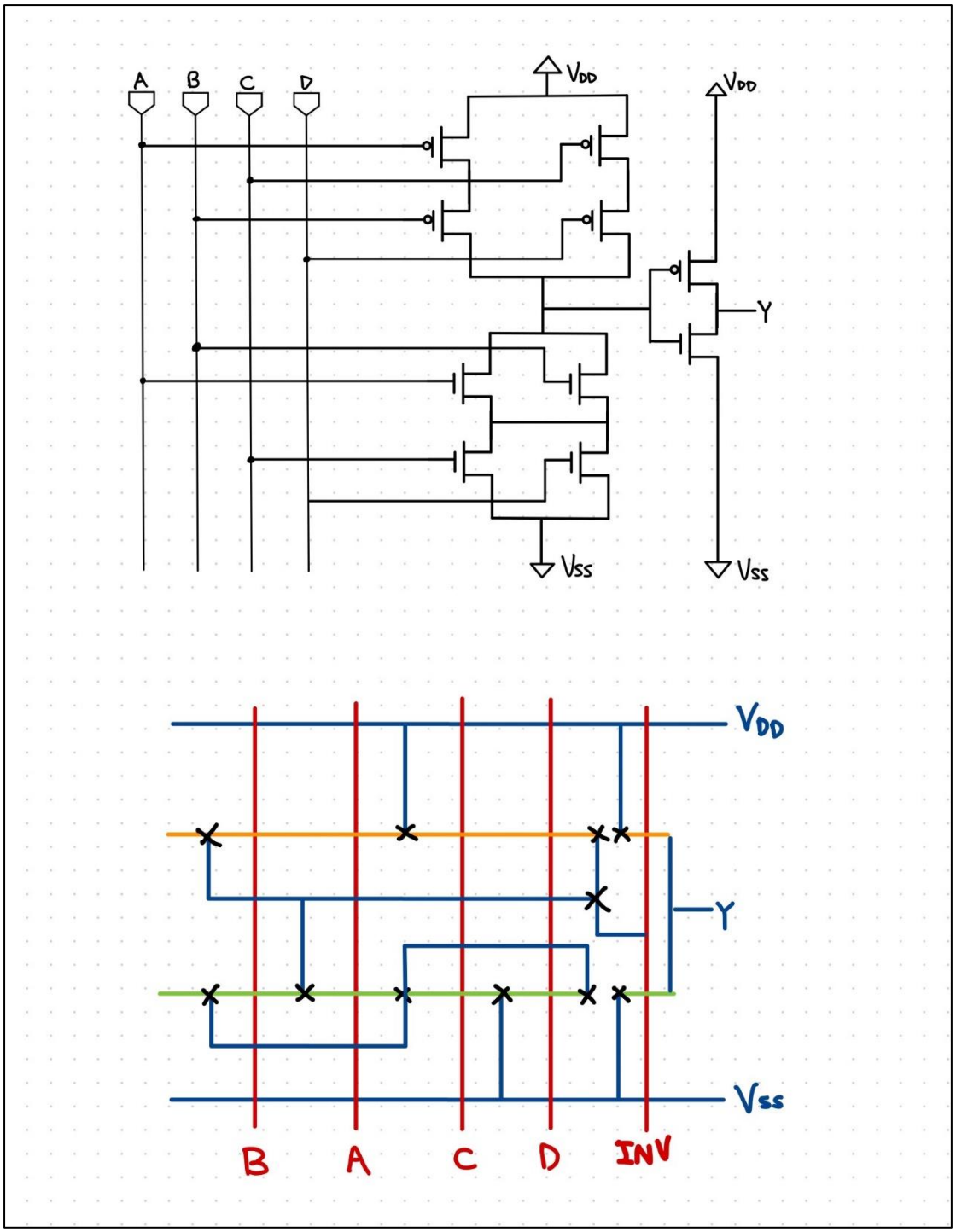


(b) Y = (A+B)·(C+D)

i. Schematic



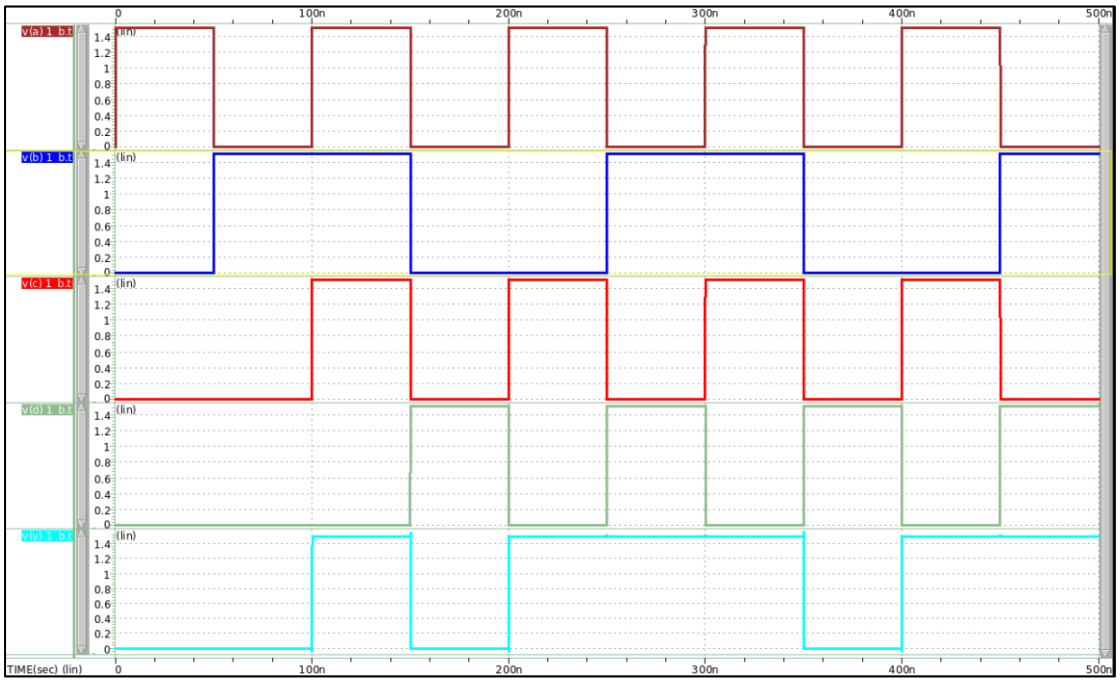
ii. Stick diagram



iii. Spice code

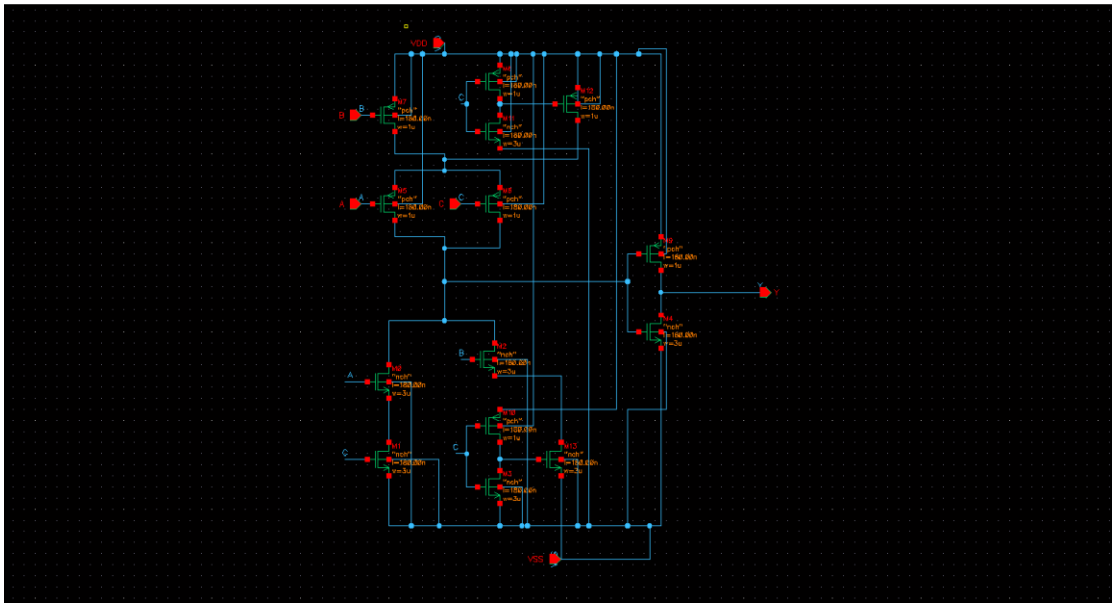
```
********************************************************************************
* Library Name: HW1
* Cell Name:    1_b
* View Name:    schematic
********************************************************************************
.prot
.lib 'cic018.l' TT
.unprot
.temp 25
.option post acout=0 runlvl=6

*.SUBCKT 1_b A B C D VDD VSS Y
*.PININFO A:I B:I C:I D:I VDD:I Y:O VSS:B
MM9 Y net52 VSS VSS N_18 W=1u L=180.00n m=1
MM8 net44 B VSS VSS N_18 W=1u L=180.00n m=1
MM7 net44 A VSS VSS N_18 W=1u L=180.00n m=1
MM6 net52 D net44 VSS N_18 W=1u L=180.00n m=1
MM5 net52 C net44 VSS N_18 W=1u L=180.00n m=1
MM4 Y net52 VDD VDD P_18 W=3u L=180.00n m=1
MM3 net52 C net61 VDD P_18 W=3u L=180.00n m=1
MM2 net52 A net65 VDD P_18 W=3u L=180.00n m=1
MM1 net61 D VDD VDD P_18 W=3u L=180.00n m=1
MM0 net65 B VDD VDD P_18 W=3u L=180.00n m=1

**********source**********

VDD vdd 0 dc 1.5
VSS vss gnd dc 0

VAP A gnd PULSE 0 1.5 0 0.1n 0.1n 50n 100n
VBP B gnd PULSE 0 1.5 50n 0.1n 0.1n 100n 200n
VCP C gnd PULSE 0 1.5 100n 0.1n 0.1n 50n 100n
VDP D gnd PULSE 0 1.5 150n 0.1n 0.1n 50n 100n


**********analysis**********
.op
.tran 0.1ns 500n
*.tf v(vout) va
.probe v(vout)

.AC DEC 100 1K 1G


.end
```

iv. Waveview result

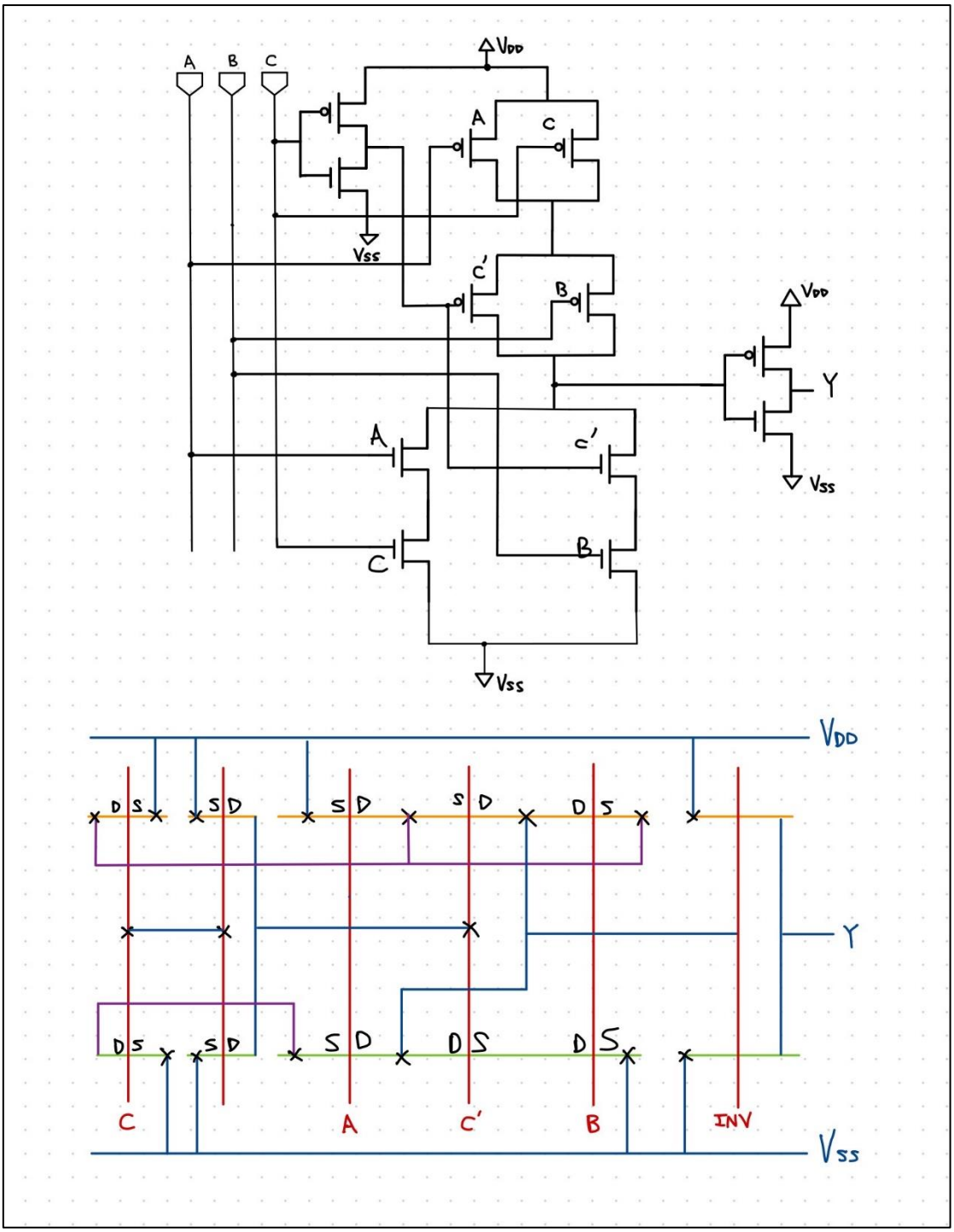


(c) $Y = A \cdot C + B \cdot C'$

i. Schematic



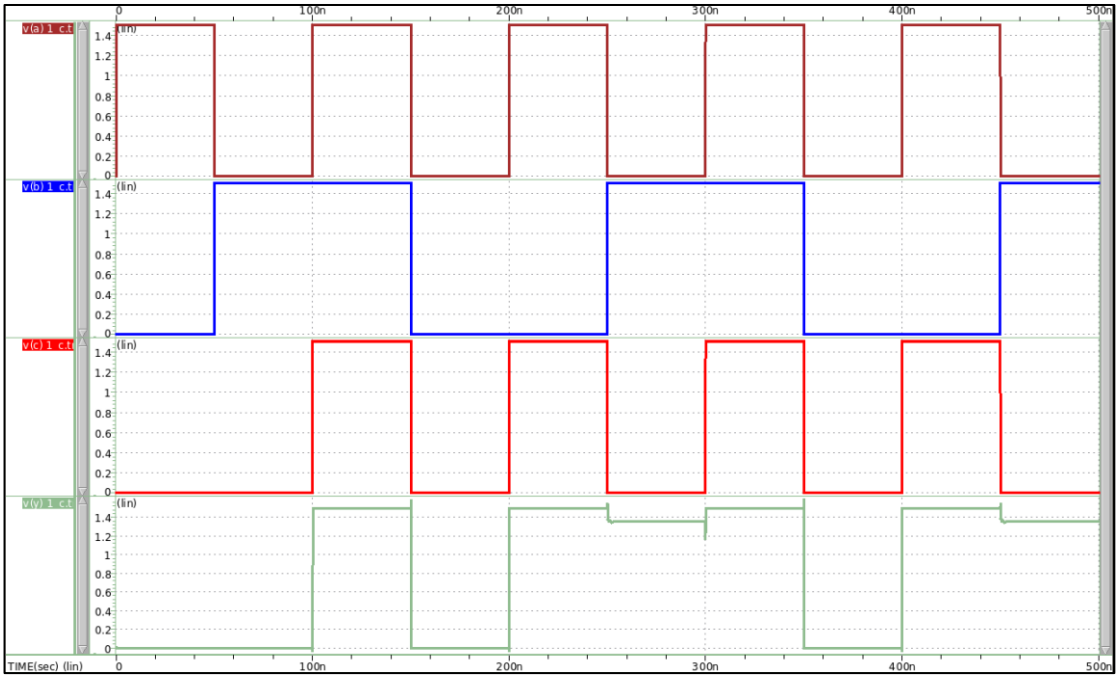
ii. Stick diagram



iii. Spice code

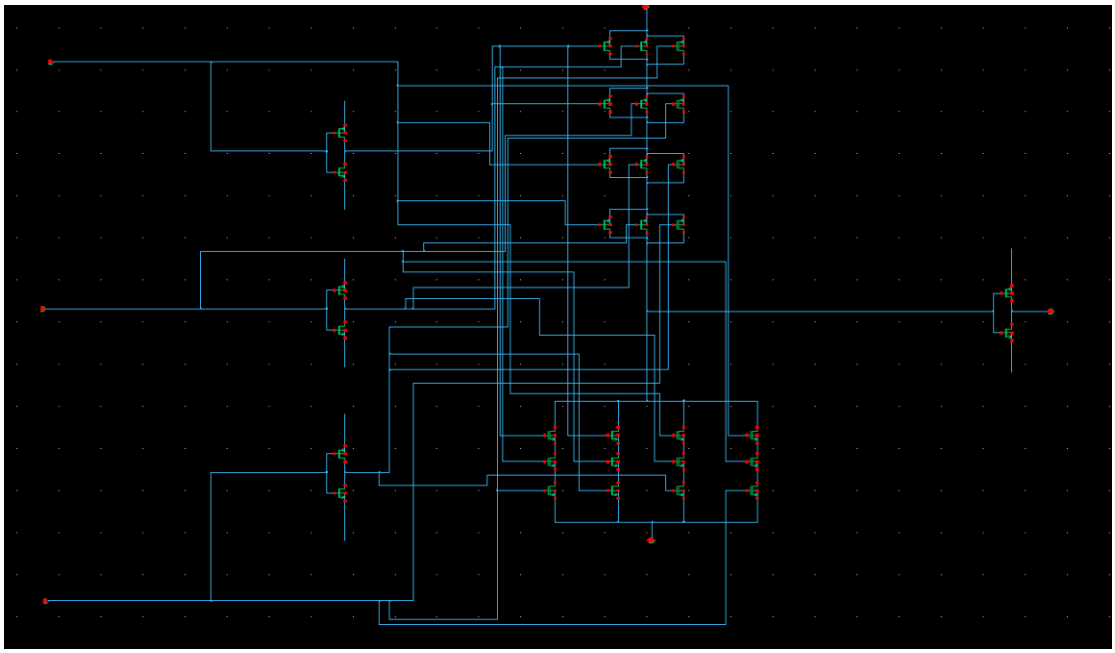
```
********************************************************************************
* Library Name: HW1
* Cell Name:    1_c
* View Name:    schematic
********************************************************************************
.prot
.lib 'cic018.l' TT
.unprot
.temp 25
.option post acout=0 runlvl=6

*.SUBCKT 1_c A B C VDD VSS Y
*.PININFO A:I B:I C:I VDD:I VSS:I Y:O
MM12 net20 net29 VDD VDD P_18 W=3u L=180.00n m=1
MM10 net5 C net8 VDD P_18 W=3u L=180.00n m=1
MM9 Y net11 VDD VDD P_18 W=3u L=180.00n m=1
MM8 net29 C VDD VDD P_18 W=3u L=180.00n m=1
MM7 net20 B VDD VDD P_18 W=3u L=180.00n m=1
MM6 net11 C net20 VDD P_18 W=3u L=180.00n m=1
MM5 net11 A net20 VDD P_18 W=3u L=180.00n m=1
MM13 net48 net5 VSS VSS N_18 W=1u L=180.00n m=1
MM11 net29 C VSS VSS N_18 W=1u L=180.00n m=1
MM4 Y net11 VSS VSS N_18 W=1u L=180.00n m=1
MM3 net5 C VSS VSS N_18 W=1u L=180.00n m=1
MM2 net11 B net48 VSS N_18 W=1u L=180.00n m=1
MM1 net33 C VSS VSS N_18 W=1u L=180.00n m=1
MM0 net11 A net33 VSS N_18 W=1u L=180.00n m=1

**********source**********

VDD vdd 0 dc 1.5
VSS vss gnd dc 0

VAP A gnd PULSE 0 1.5 0 0.1n 0.1n 50n 100n
VBP B gnd PULSE 0 1.5 50n 0.1n 0.1n 100n 200n
VCP C gnd PULSE 0 1.5 100n 0.1n 0.1n 50n 100n


**********analysis**********
.op
.tran 0.1ns 500n
*.tf v(vout) va
.probe v(vout)
.AC DEC 100 1K 1G
.end
```

iv. Waveview result

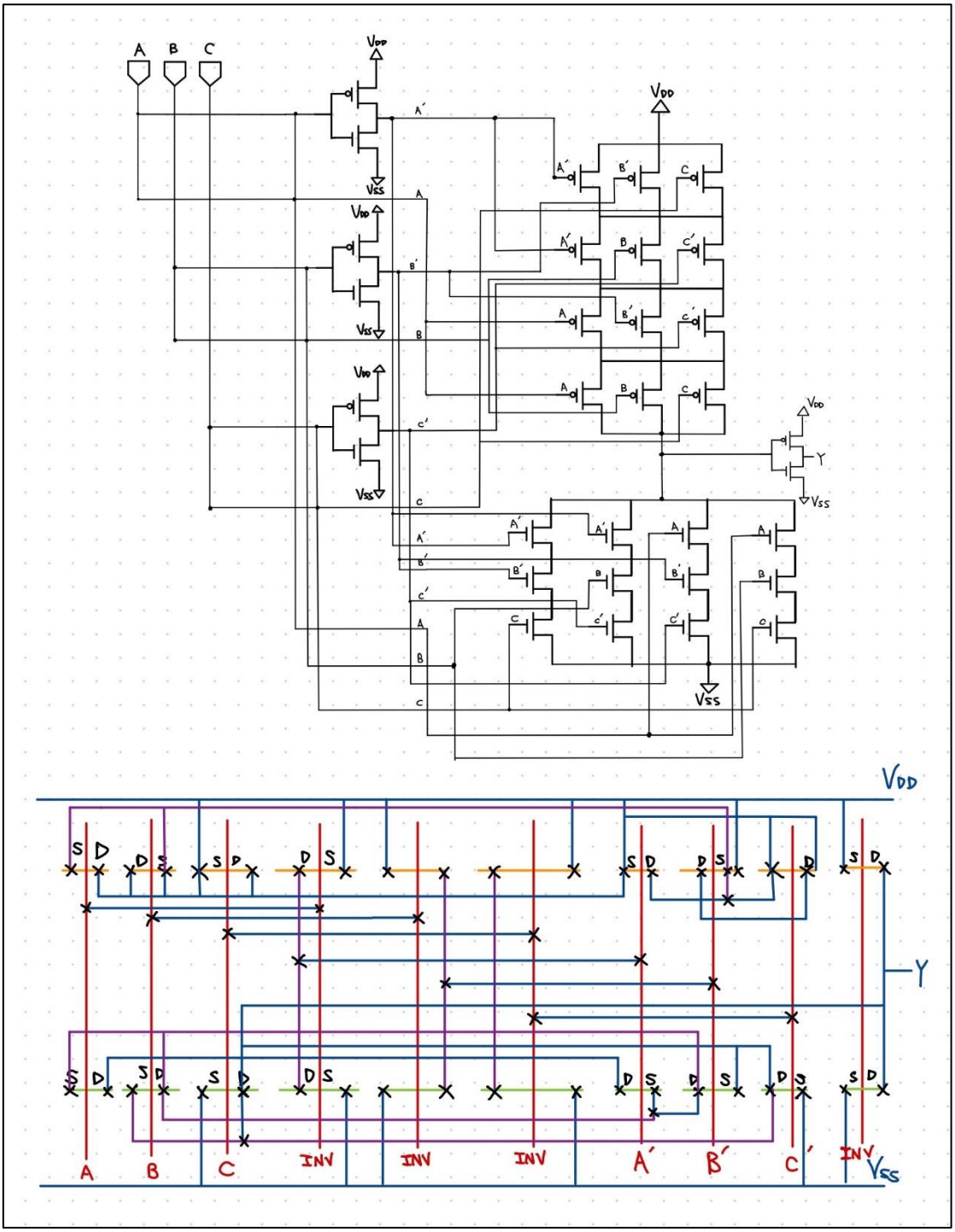


(d) $Y = A \oplus B \oplus C$, $\oplus$ stands for XOR gate

i. Schematics



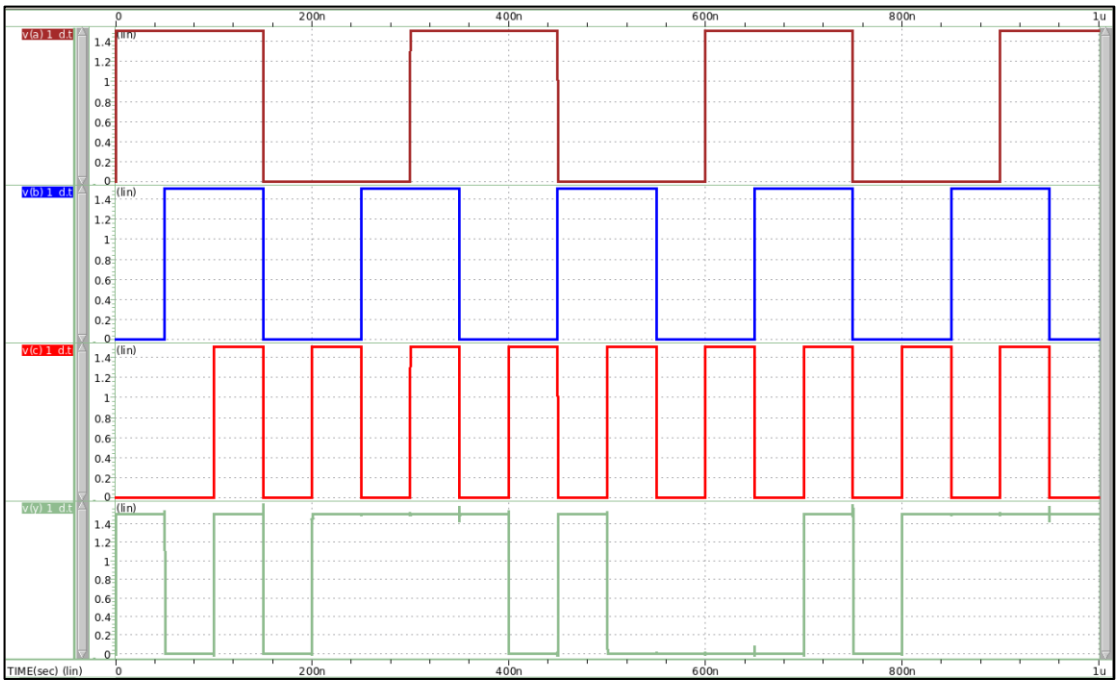
ii. Stick diagram



iii. Spice code

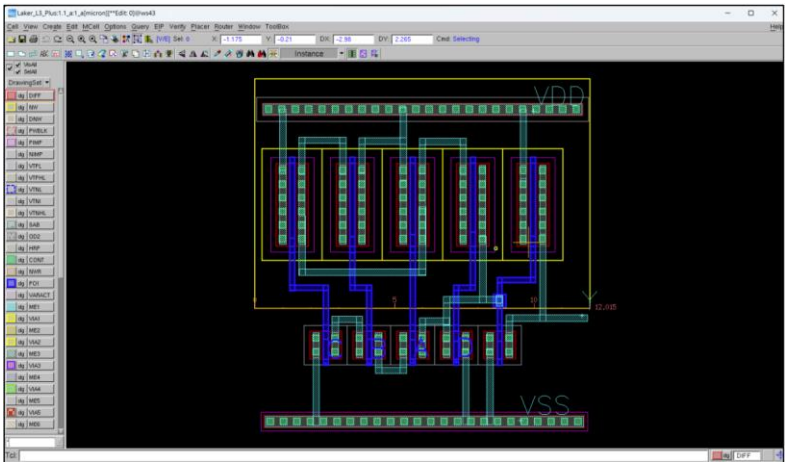
```
*.SUBCKT 1_d A B C VDD VSS Y
*.PININFO A:I B:I C:I Y:O VDD:B VSS:B
MM25 net0170 A net11 net11 N_18 W=1u L=180.00n m=1
MM24 net11 B net15 net15 N_18 W=1u L=180.00n m=1
MM23 net15 C VSS VSS N_18 W=1u L=180.00n m=1
MM22 net19 C_bar VSS VSS N_18 W=1u L=180.00n m=1
MM21 net23 B_bar net19 net19 N_18 W=1u L=180.00n m=1
MM20 net0170 A net23 net23 N_18 W=1u L=180.00n m=1
MM19 net0170 A_bar net35 net35 N_18 W=1u L=180.00n m=1
MM18 net35 B net39 net39 N_18 W=1u L=180.00n m=1
MM17 net39 C_bar VSS VSS N_18 W=1u L=180.00n m=1
MM31 Y net0170 VSS VSS N_18 W=1u L=180.00n m=1
MM7 net43 C VSS VSS N_18 W=1u L=180.00n m=1
MM6 net47 B_bar net43 net43 N_18 W=1u L=180.00n m=1
MM5 net0170 A_bar net47 net47 N_18 W=1u L=180.00n m=1
MM29 C_bar C VSS VSS N_18 W=1u L=180.00n m=1
MM26 A_bar A VSS VSS N_18 W=1u L=180.00n m=1
MM1 B_bar B VSS VSS N_18 W=1u L=180.00n m=1
MM32 Y net0170 VDD VDD P_18 W=3u L=180.00n m=1
MM16 net0170 A net68 net68 P_18 W=3u L=180.00n m=1
MM15 net0170 B net68 net68 P_18 W=3u L=180.00n m=1
MM14 net0170 C net68 net68 P_18 W=3u L=180.00n m=1
MM13 net68 C_bar net88 net88 P_18 W=3u L=180.00n m=1
MM12 net68 B_bar net88 net88 P_18 W=3u L=180.00n m=1
MM11 net68 A net88 net88 P_18 W=1u L=180.00n m=1
MM10 net88 A_bar net92 net92 P_18 W=3u L=180.00n m=1
MM9 net88 B net92 net92 P_18 W=3u L=180.00n m=1
MM8 net88 C_bar net92 net92 P_18 W=3u L=180.00n m=1
MM4 net92 C VDD VDD P_18 W=3u L=180.00n m=1
MM3 net92 B_bar VDD VDD P_18 W=3u L=180.00n m=1
MM2 net92 A_bar VDD VDD P_18 W=3u L=180.00n m=1
MM27 A_bar A VDD VDD P_18 W=3u L=180.00n m=1
MM30 C_bar C VDD VDD P_18 W=3u L=180.00n m=1
MM0 B_bar B VDD VDD P_18 W=3u L=180.00n m=1

**********source**********

VDD vdd 0 dc 1.5
VSS vss gnd dc 0

VAP A gnd PULSE 0 1.5 0 0.1n 0.1n 150n 300n
VBP B gnd PULSE 0 1.5 50n 0.1n 0.1n 100n 200n
VCP C gnd PULSE 0 1.5 100n 0.1n 0.1n 50n 100n


**********analysis**********
.op
.tran 0.1ns 1000n
```

iv. Waveview result

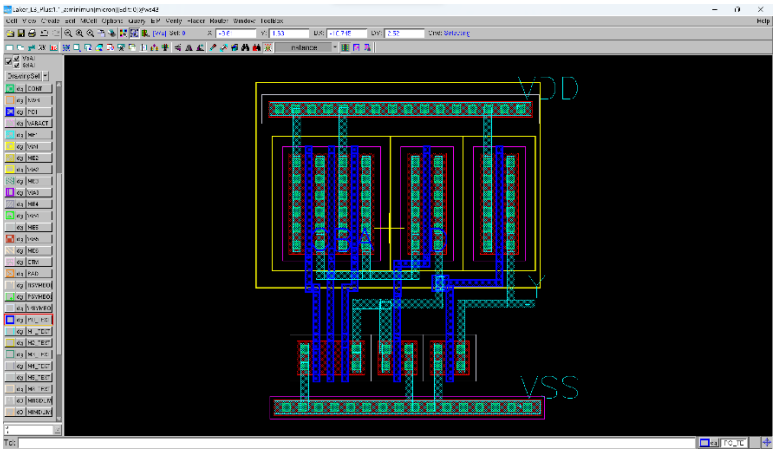


Comments

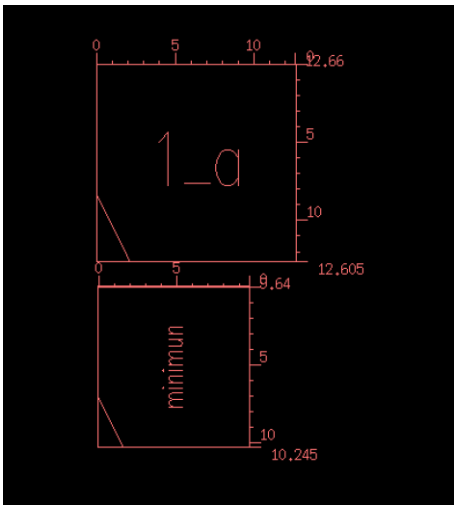
本次作業我在畫 layout 時嘗試兩種畫法，雖然這是基礎觀念但仍然獲得很直接的感受。下圖以第一題 a 小題為例。



將每個 mos 分開(面積較大)



串並 mos(面積較小)

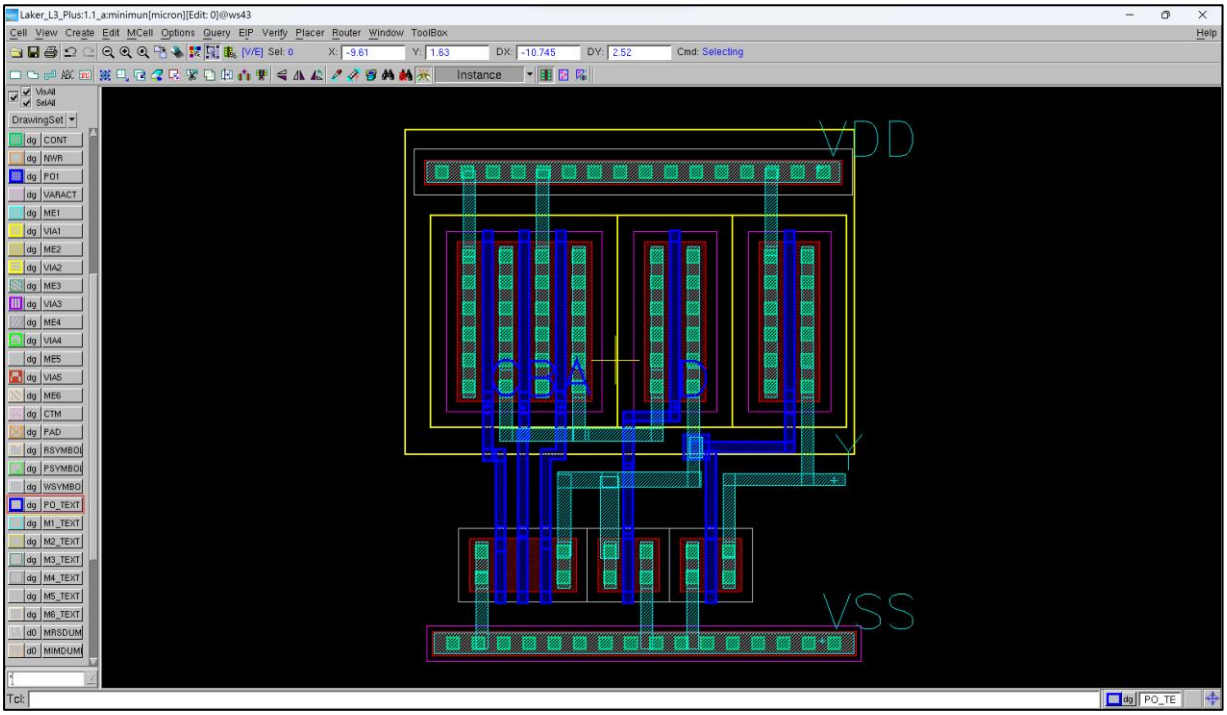


兩者使用面積差了約 39%

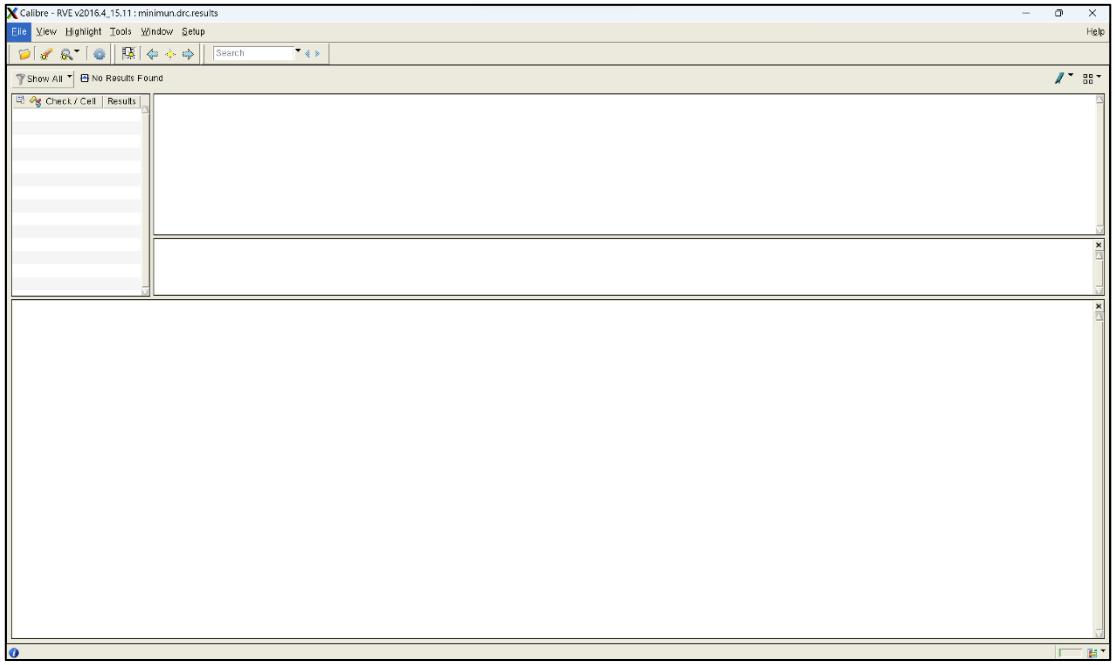
2. Based on problem 1(a),1(b), please finish DRC and LVS verification. You must attach the pictures on your report which contain layout, DRC result and LVS result.

(a) $Y = A \cdot B \cdot C + D$

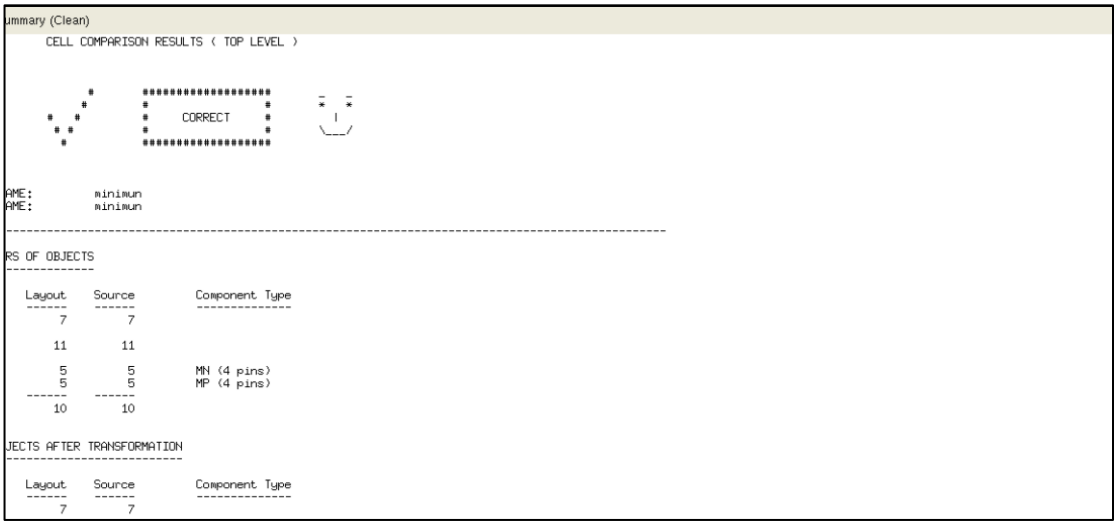
i. Layout



ii. DRC result

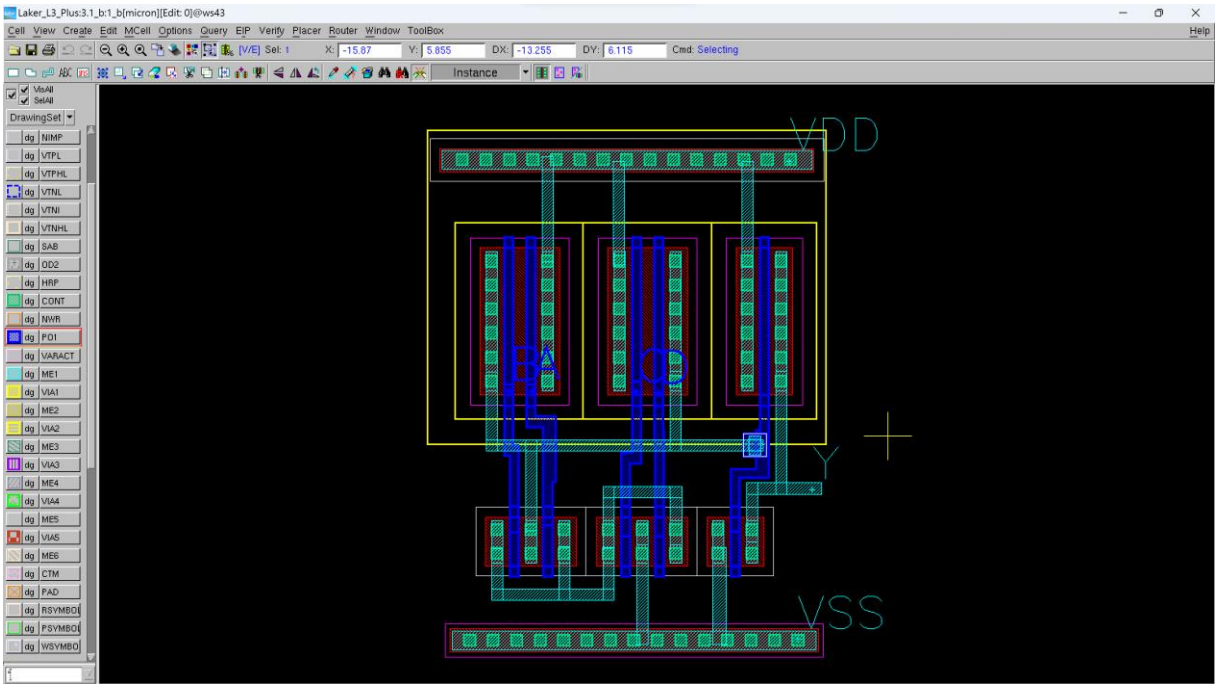


iii. LVS result

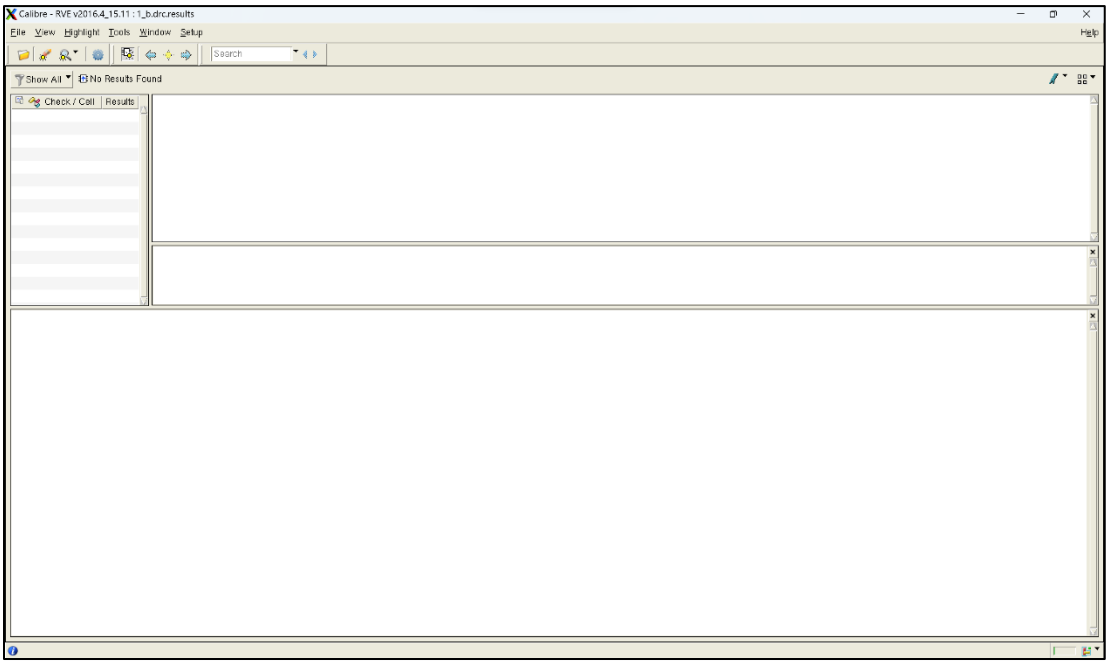


(b) Y = (A+B)·(C+D)

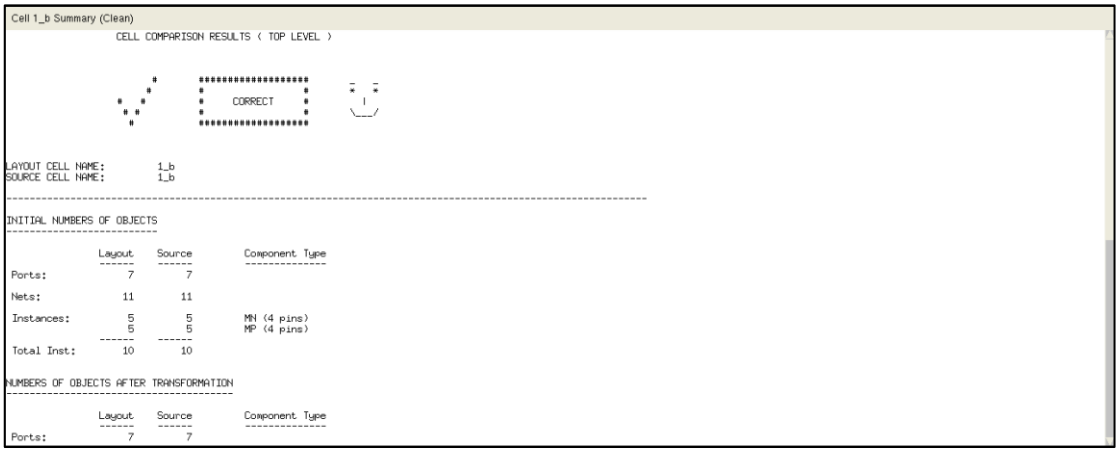
i. Layout



ii. DRC result



iii. LVS result



(c) Explain what DRC rules do you learn, please list them.

1. Minimum width of Metal line is 0.23um when transistor channel length is 0.18um.
2. If the same layer cross each other, it makes a contact.
3. If the different layer just cross, it doesn't make contact but if contact has to be made, we should mark it.
4. Minimum area of contact should be 0.23u x 0.23u when transistor channel length is 0.18um.
5. We should draw N-WELL contact to enclose PMOS and VDD(positive source).
6. Minimum distance between different layers is 0.25u.
7. Minimum NWELL overlap N+ diffusion is 0.25um
8. Minimum space between two Poly regions on field area is 0.25um.
9. Gate at 90 degree angle is not allowed.(merge them to solve)
10. Minimum PO1 width for 1.8V NMOS or PMOS or interconnect is 0.18um
11. Minimum space between two NPlus regions is 0.45um
12. Minimum space between ME1 regions is 0.24um where MET1 width < 10um

3. Draw the fabrication steps of an inverter (cross section).