2022 EE5250 VLSI Design Homework 2

Due date:2022/10/30

**Set temperature = 25 degree for each corner during simulation.*

1. Run the HSPICE simulation to answer the following question, use $V_{DD} = 1.5V$.

   (a) Please design five **INVERTER** gates (one for each corner) with $(\mathrm{W/L})_n = 1\mu\mathrm{m}/0.2\mu\mathrm{m}$ while $(\mathrm{W/L})_p$ is your design. Run the transfer curve (like Fig.1), the transition point should be $V_{OUT} = 0.5V_{DD}$ @ $V_{in} = 0.5\ V_{DD}$ in 5 process corners (TT, SS, FF, SF, FS). Please comment on the differences. (10%)

   (b) Using the transfer curve you simulated in (a), calculate the value of $V_{IL}, V_{IH}, V_{OL}, V_{OH}$ and NM_H and NM_L in 5 process corners (TT, SS, FF, SF, FS). Please comment on the differences. (10%)

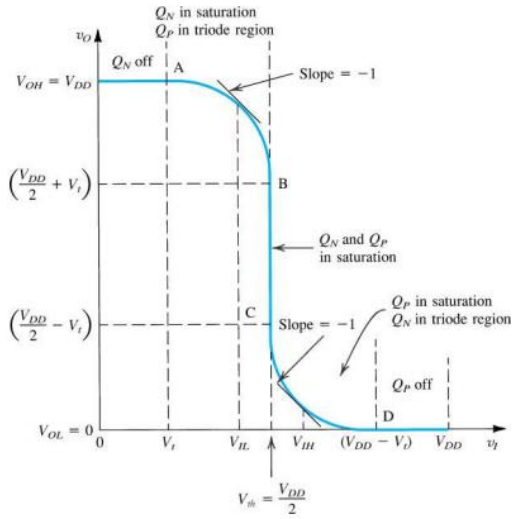

Fig. 1

   (c) Using the **INVERTER** designed in (a) with $V_{DD} = 1.5V$. Input signal = 0V-1.5V @2MHz with rising time / falling time = 0.1ns and loading capacitor $C_{load} = 800fF$ at output.

Table. 1

INVERTER					
Input	CLK @2MHz				
Corner	TT	SS	FF	SF	FS
t_{pHL}					
t_{pLH}					
t_r					
t_f					

Run HSPICE transient simulation at 5 corners and finding following values. Please comment on the differences. (10%)

t_{pHL} (from input to falling output crossing $0.5V_{DD}$)

t_{pLH} (from input to rising output crossing $0.5V_{DD}$)

t_r (from output crossing $0.2V_{DD}$to $0.8V_{DD}$)

t_f (from output crossing $0.8V_{DD}$to $0.2V_{DD}$)

2. Run the HSPICE simulation to answer the following question, use $V_{DD} = 1.5V$.

   (a) Please design five **2-input NAND** gates (one for each corner) with $(W/L)_n = 3\mu m/0.2\mu m$ while $(W/L)_p$ is your design. (BOTH PMOS sizes should be same.) **Connect the two input together** to run the transfer curve (like Fig.1), the transition point should be $V_{OUT} = 0.5V_{DD}$ @ $V_{in} = 0.5\ V_{DD}$ in 5 process corners. (TT, SS, FF, SF, FS). (10%)

   (b) Using the transfer curve you simulated in (a), calculate the value of $V_{IL}, V_{IH}, V_{OL}, V_{OH}$ and NM_H and NM_L in 5 process corners. (TT, SS, FF, SF, FS) (10%)

   (c) What are the differences in $(W/L)_p/(W/L)_n$ between Q1(a) and Q2(a)? Please comment on the difference. (10%)

   (d) Using the **2-input NAND** designed in (a) with $V_{DD} = 1.5V$. Input signal (A or B) = 0V-1.5V@2MHz with rising time / falling time = 0.1ns and loading capacitor $C_{load} = 800fF$ at output.

Table. 2

NAND2	Case1					Case2				
Input A	CLK @2MHz					1.5V				
Input B	1.5V					CLK @2MHz				
Corner	TT	SS	FF	SF	FS	TT	SS	FF	SF	FS
t_{pHL}										
t_{pLH}										
t_r										
t_f										

Change one input from 0V to 1.5V at a time and fix another one (See Table. 2).Run HSPICE transient simulation at 5 corners and finding following values. Please comment on the differences between Case1 and Case2 for each corner. (10%)

t_{pHL} (from input to falling output crossing $0.5V_{DD}$)

t_{pLH} (from input to rising output crossing $0.5V_{DD}$)

t_r (from output crossing $0.2V_{DD}$to $0.8V_{DD}$)

t_f (from output crossing $0.8V_{DD}$to $0.2V_{DD}$)

3. Complete the layout and post-sim of Inverter in Q1 @ TT corner and 2-input NAND in Q2 @ TT corner.

   (a) Finish DRC and LVS verification. Paste the pictures of layout, DRC result and LVS result in your report. (15%)

   (b) Run the post-layout simulation (post-sim) for Q1(c) and Q2(d) compare them with pre-layout simulation (pre-sim). Please comment on the differences. (15%)

➢ Please submit homework in PDF format and turn in it on eeclass system. You can finish this homework in handwriting paper and scan it into PDF format.

By CCHsieh