2022 EE5250 VLSI Design Homework 4

Due date: 2022/12/12

* *The following should be included in your report: (a) picture of schematic & layout and clearly mark the name and unit of the x-axis and y-axis (b) picture of waveform with cursor values (c) your comment*

1. Consider a positive-edge-triggered D flip-flop as shown in Fig. 1. Assume C**LK=100MHz with tr=tf=50ps, duty cycle=50% and VDD=1.8V**.
Please design the logic gates that are based on unit inverter of **(W/L)n= 0.6um/0.18um and (W/L)p=1.8um/0.18um**. (50%)

(a) Simulate and find the setup time of this flip-flop including rising and falling input. Briefly explain what is the setup time and the way you find it. (7%)

(b) Simulate and find the hold time of this flip-flop including rising and falling output. Briefly explain what is the hold time and the way you find it. (7%)

(c) Simulate the clock to Q delay for both rising and falling input transitions. (7%)

(d) Finish the layout, DRC, and LVS. Paste the photo of layout, DRC result and LVS result in your report. (8%)

(e) Run the post-layout simulation (post-sim) and compare it with pre-layout simulation (pre-sim) in (a), (b), and (c). (21%)

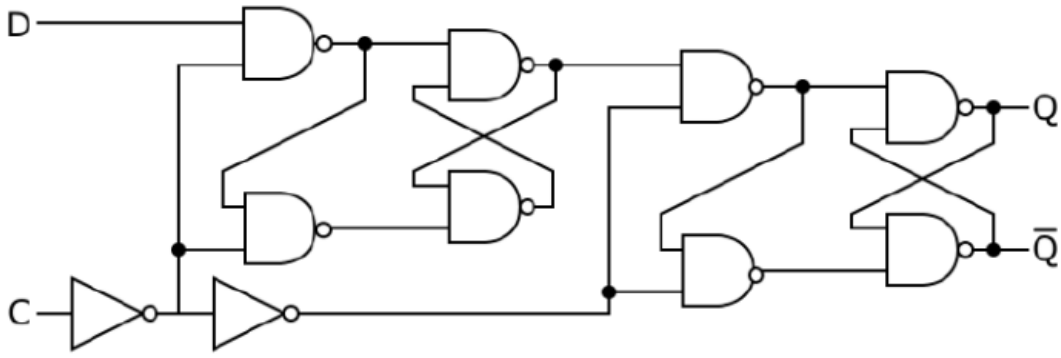

Fig. 1

By CCHsieh

2. Insert an inverter chain between 2 DFFs (shown in Fig.2) as a combinational logic to introduce a delay. (50%)

clk = 100MHz with tr = tf = 50ps, duty cycle = 50% and VDD = 1.8V

Simulate and observe the maximum and minimum delay failure condition while input = vdd and input = gnd.

(a) Using the DFF you designed in previous question (15%)

(b) Using the DFF in Fig.3 and with the inverter size (W/L)n = 0.6um/0.2um and (W/L)p = 1.8um/0.2um, the transmission gate size (W/L)n = (W/L)p = 0.8um/0.2um. (15%)

(c) Use the previous results in question1 (setup time and hold time) to hand calculate the maximum and minimum delay failure condition in (a). As for (b), do the same hand calculation as (a). (10%)

(d) Please compare and comment the results of (a) and (b) with (c). (10%)

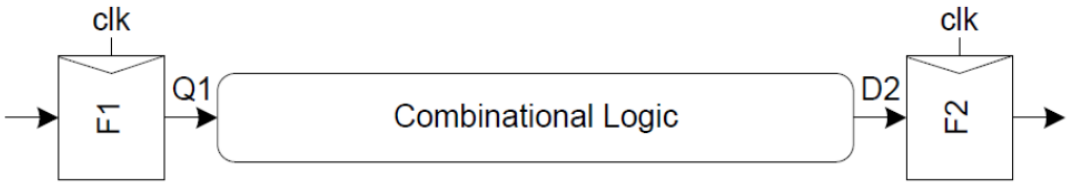

Fig. 2

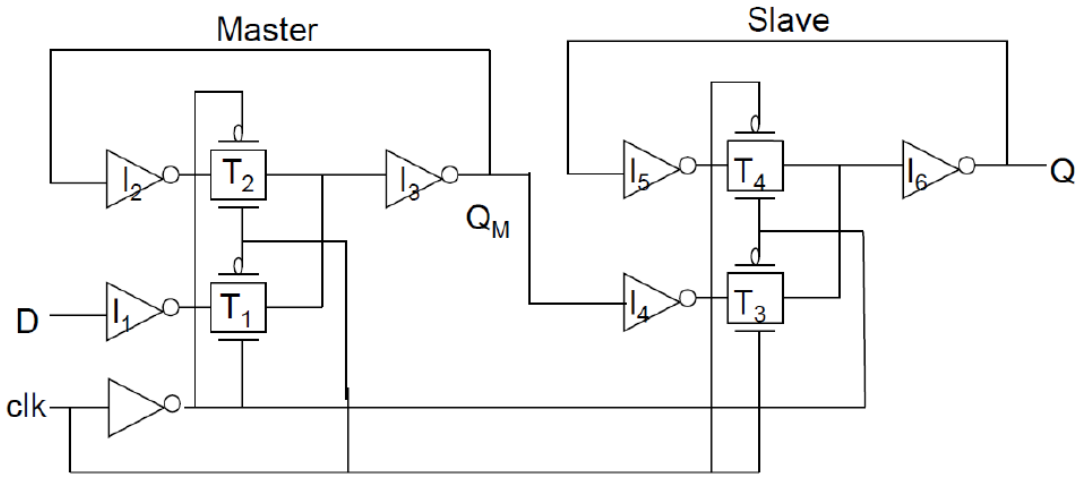

Fig. 3 Mater Slave Based ET DFF

By CCHsieh