2022 EE5250 VLSI Design Homework 5

Due date:2022/12/29

* *Total score : 90*
Bonus : +0 ~ +5

1. Please design a 4 bit binary synchronous up counter with clock frequency CLK = 200MHz, $V_{DD} = 1.8V$ (default) , $V_{SS} = 0V$. You can use any architecture to complete the design. **Try to minimize the power consumption of the counter**. You can adjust the value of V_{DD} for minimizing the power meanwhile the counter works correctly, and the maximum glitch should be less than 80ps.

   (a) Please describe how you design the counter and how to reduce the glitch and power consumption of counter. (40%)
   (b) Please list the glitch in each number (0 ~ 15) and find the maximum glitch. (20%)
   (c) Please measure the power of the counter. (5%)

<***Notice***>

- The rising time and falling time of clock is **10ps**
- The time step in transient simulation should be ≦ **1ps**
- You can use the following code to measure the power, the time duration is a complete period.

  *.measure tran PVDD AVG PAR('(V(Vdd)*I(Vdd))') from=___ to=___*
- You can use the **'A to D' function** in WaveView to convert the binary code to decimal value and check whether your function works.
  i. select the waveform (B[0]~B[3]), click 'A to D'
  ii. set the 'Center Logic Threshold' to $0.5V_{DD}$, click 'OK' , there will be several waveforms at the bottom of the WaveView
  iii. 'Group' these waveforms and sort the signal order in Bus Configuration
  iv. Right click the group waveforms 'Radix', select 'Decimal'.
- Remember that when you change the value of V_{DD}, you should change the 'Center Logic Threshold' to $0.5V_{DD}$.

2. Please design a 3 bit pseudo-random-bit-sequence (PRBS) generator with Linear Feedback Shift Register (LFSR) with clock frequency CLK = 200MHz, $V_{DD} = 1.8V$, $V_{SS} = 0V$. **Try to minimize the power consumption of the PRBS generator**.

   (a) Please describe how you design the PRBS generator and show the pseudo-random-sequence result to prove your design. (20%)
   (b) Please measure the power of the PRBS generator. (5%)

<***Notice***>

- The rising time and falling time of clock is **10ps**
- The time step in transient simulation should be ≦ **1ps**
- You can use the following code to measure the power, the time duration is a complete period.

  *.measure tran PVDD AVG PAR('(V(Vdd)*I(Vdd))') from=___ to=___*

∗ The following should be included in your report:
(a) picture of schematic and clearly mark the name and unit of the x-axis and y-axis
(b) picture of waveform with cursor values
(c) your comment

By CCHsieh