國立清華大學

超大型積體電路設計 VLSI Design

國立清華大學

NATIONAL TSING HUA UNIVERSITY

Homework 2

學號:111063548

姓名:蕭方凱

目錄

1. Run the HSPICE simulation to answer the following question, use VDD = 1.5V.

(a) Please design five INVERTER gates (one for each corner) with (W/L)n = 1μm/0.2μm while (W/L)p is your design. Run the transfer curve (like Fig.1), the transition point should be $VOUT$ = 0.5VDD @ Vin = 0.5 VDD in 5 process corners (TT, SS, FF, SF, FS). Please comment on the differences.

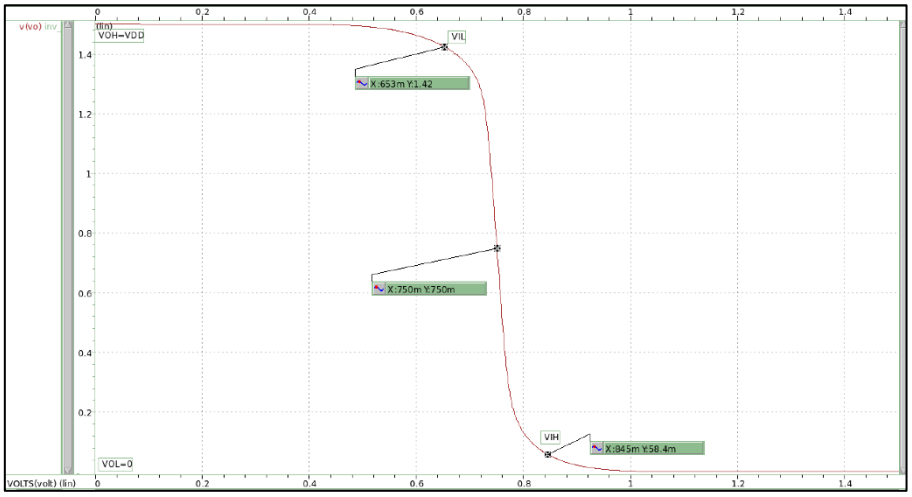


圖 1 TT Corner

W=4.15u,L=0.2u

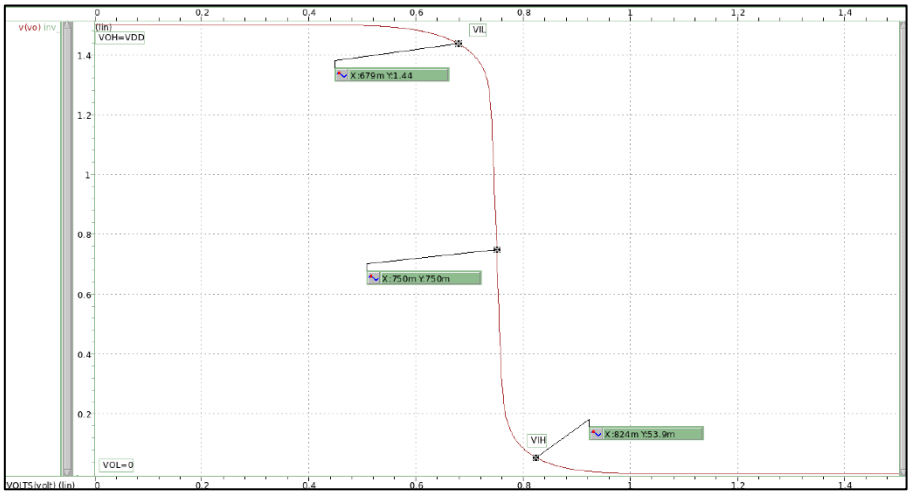


圖 2 SS corner

W=3.65u,L=0.2u

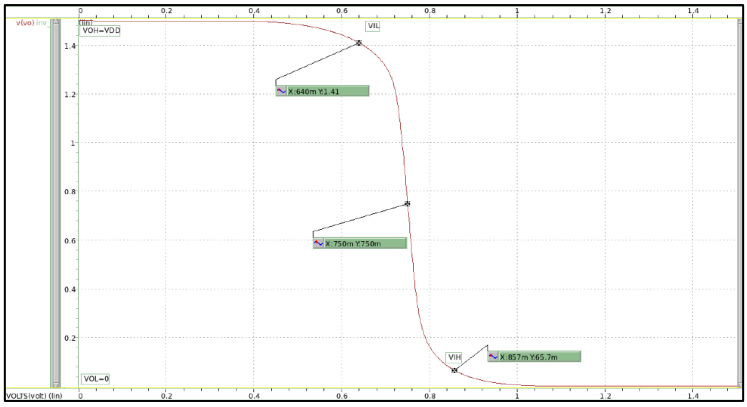


圖 3 FF Corner

W=4.11u,L=0.2u

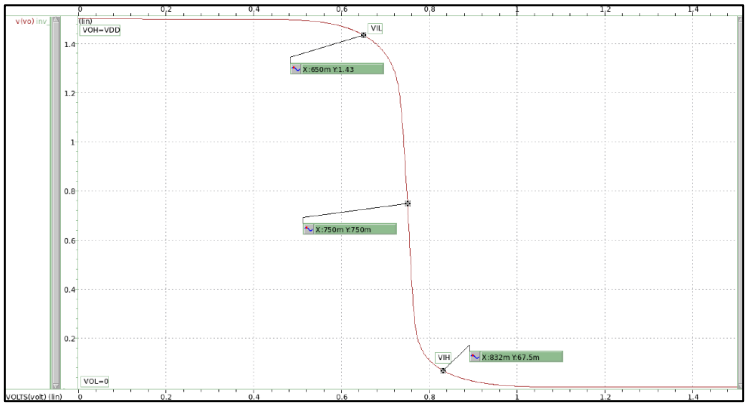


圖 4 SF Corner

W=0.914u,L=0.2u

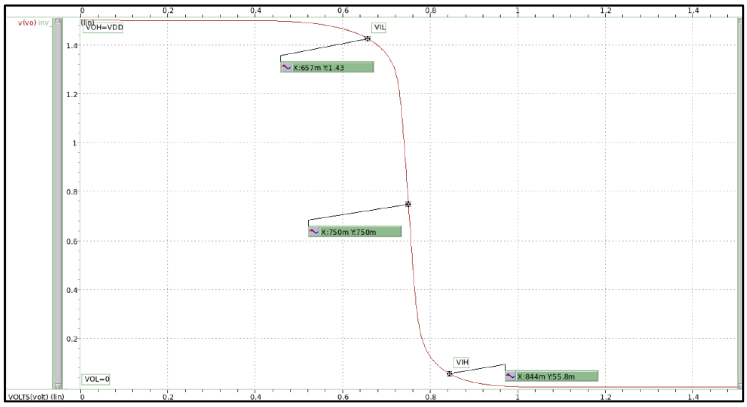


圖 5 FS Corner

W=4.16u,L=0.2u

Comment:

上面五張圖依序為 TT、SS、FF、SF、FS，從圖形上可看出每個圖形的變化趨勢都有細微的差別。

TT ： 圖形對稱，VIL 和 VIH 處的二次曲線變化速度接近。

SS ： 圖形對稱，VIL 和 VIH 處的二次曲線變化速度接近。但變化速度都比 TT corner 快，故中間 sat 處直線較為陡峭。

FF ： 圖形對稱，VIL 和 VIH 處的二次曲線變化速度接近。但變化速度比 TT corner 慢，故中間 sat 處直線較為平坦。

SF ： 圖形較不對稱，在 VIL 處的曲線變化速度較 VIH 處大。

FS ： 圖形較不對稱，在 VIL 處的曲線變化速度較 VIH 處小。

斜線較為陡峭之 corner，雖可以更快速切換高低狀態，但若要調到 $VOUT = 0.5VDD$ @ $Vin = 0.5\ VDD$，較為困難，斜率與敏感度呈正相關。而斜率較為平坦之 corner 則相反，各有優缺。TT 為最平衡的 corner。

(b) Using the transfer curve you simulated in (a), calculate the value of VIL,VIH, VOL,VOH and NMH and NML in 5 process corners (TT, SS, FF, SF, FS). Please comment on the differences.

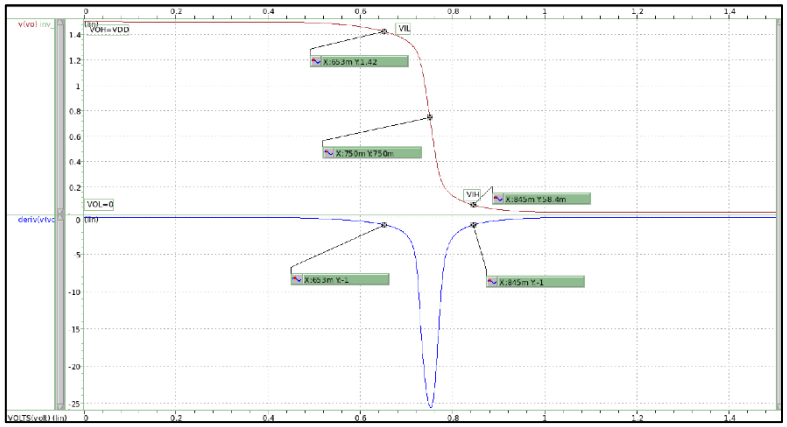


圖 6 TT Corner

VIL=653mv;VIH=845mv;VOL=0V;VOH=1.5V

NMH=VOH-VIH=655mv;NML=VIL-VOL=653mv

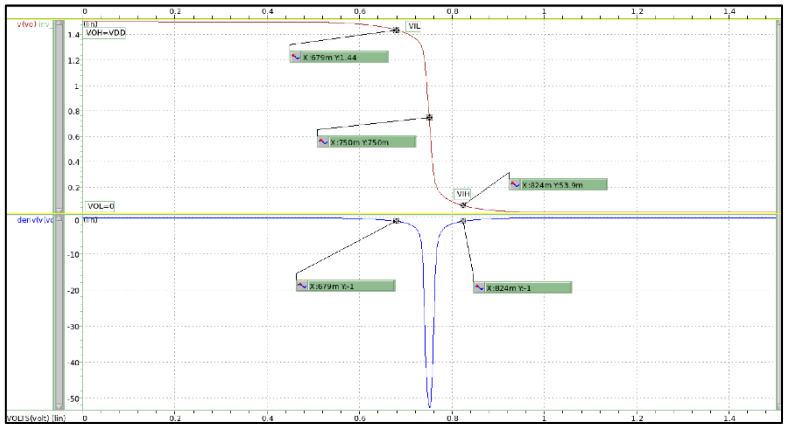


圖 7 SS Corner

VIL=679mv;VIH=824mv;VOL=0V;VOH=1.5V

NMH=VOH-VIH=676mv;NML=VIL-VOL=679mv

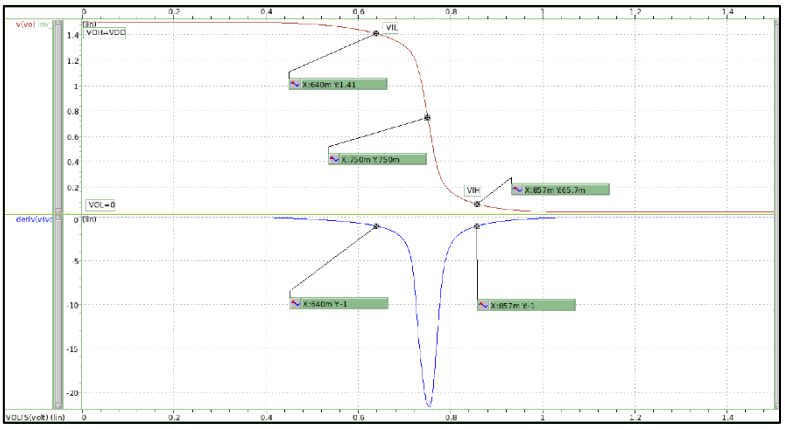


圖 8 FF Corner

VIL=640mv;VIH=857mv;VOL=0V;VOH=1.5V

NMH=VOH-VIH=643mv;NML=VIL-VOL=640mv

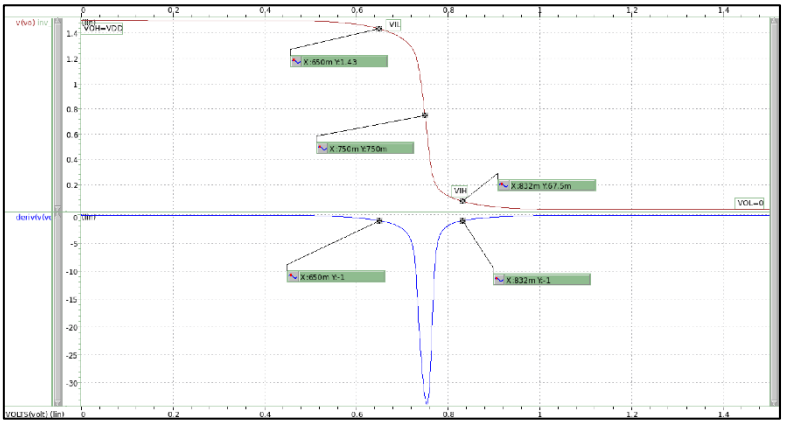


圖 9 SF Corner

VIL=650mv;VIH=832mv;VOL=0V;VOH=1.5V

NMH=VOH-VIH=668mv;NML=VIL-VOL=650mv

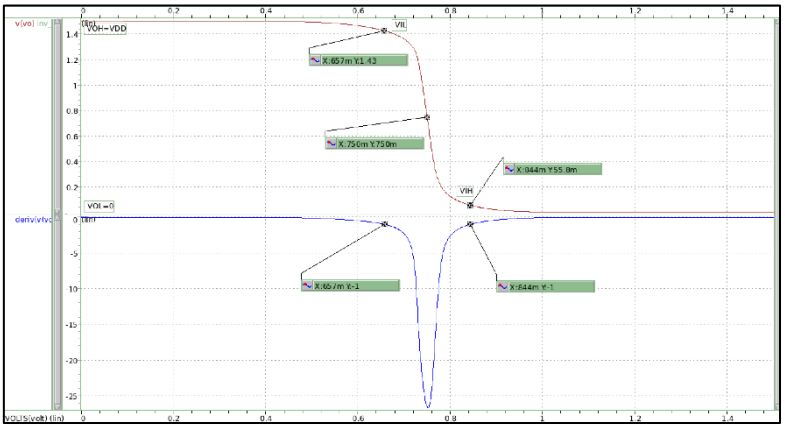


圖 10 FS Corner

VIL=657mv;VIH=844mv;VOL=0V;VOH=1.5V

NMH=VOH-VIH=656mv;NML=VIL-VOL=657mv

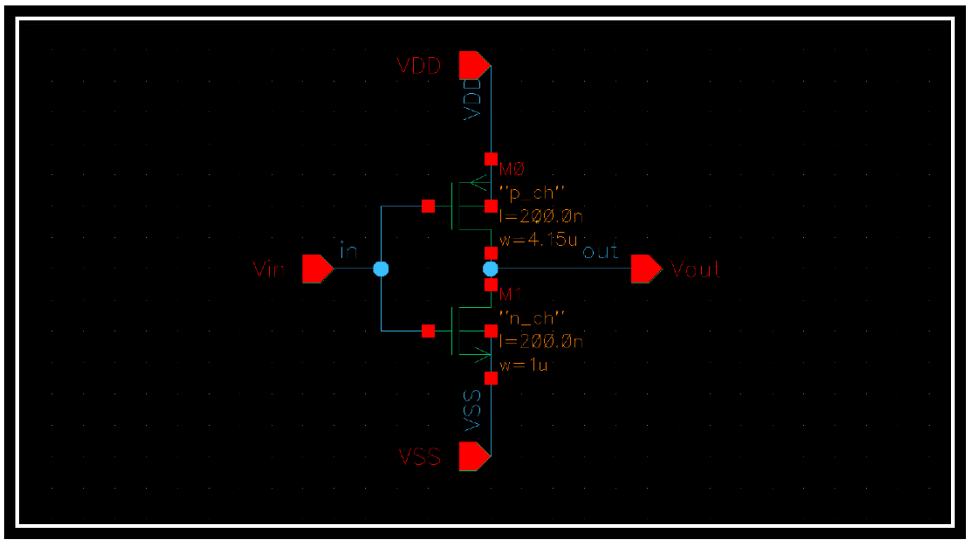


圖 11 Inverter schematic

Comment:

因 S 代表飽和電流小、閥值大；F 代表飽和電流大、閥值小。

可從上面 5 張圖觀察出相較 TT corner，SS corner 擁有更好的 Noise Margin，VIL 更大、VIH 更小，換句話說 SS Corner 可以擁有更多輸入電壓的選擇，input voltage forbidden zone 也更小。

而 FF Corner 則相反，forbidden zone 較 TT 大，故在選擇輸入訊號時條件更為嚴苛，但相對擁有更大的飽和電流。

SF Corner 的情況也符合理論，其 VIL 及 VIH 都比 TT corner 小，造成其 NML 比較差但 NMH 比較好;而 FS corner 的 VIL 要比 TT corner 來的大，波形結果也是符合的。

(c) Using the INVERTER designed in (a) with VDD = 1.5V. Input signal = 0V-1.5V @2MHz with rising time / falling time = 0.1ns and loading capacitor $Cload$ = 800fF at output.

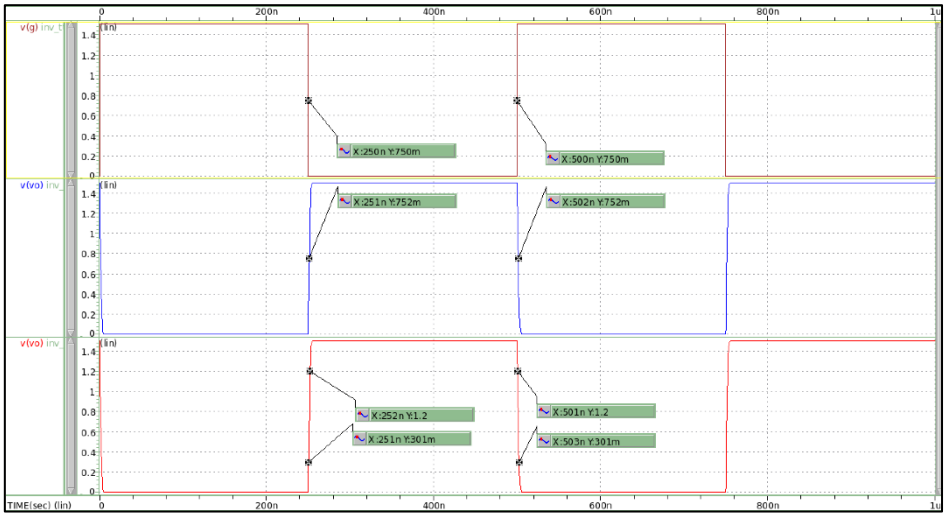


圖 12 TT Corner .tran simulation

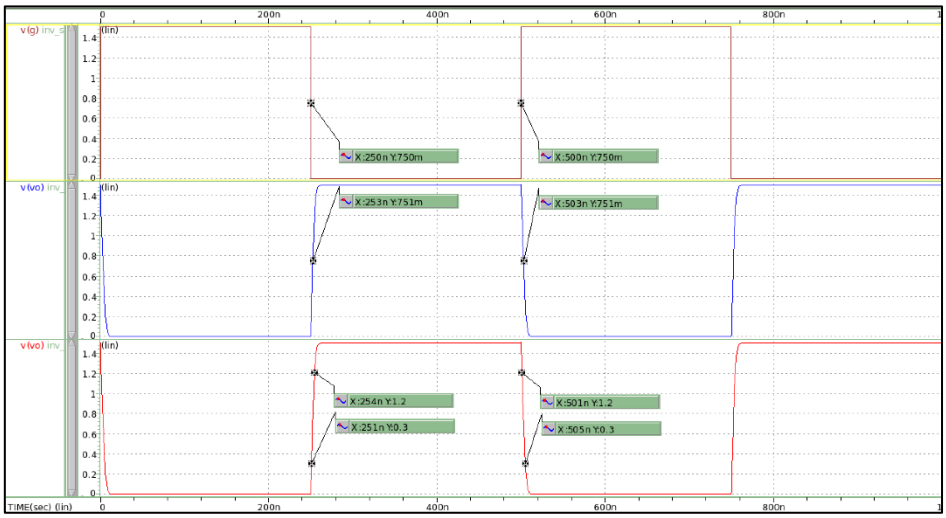


圖 13 SS Corner .tran simulation

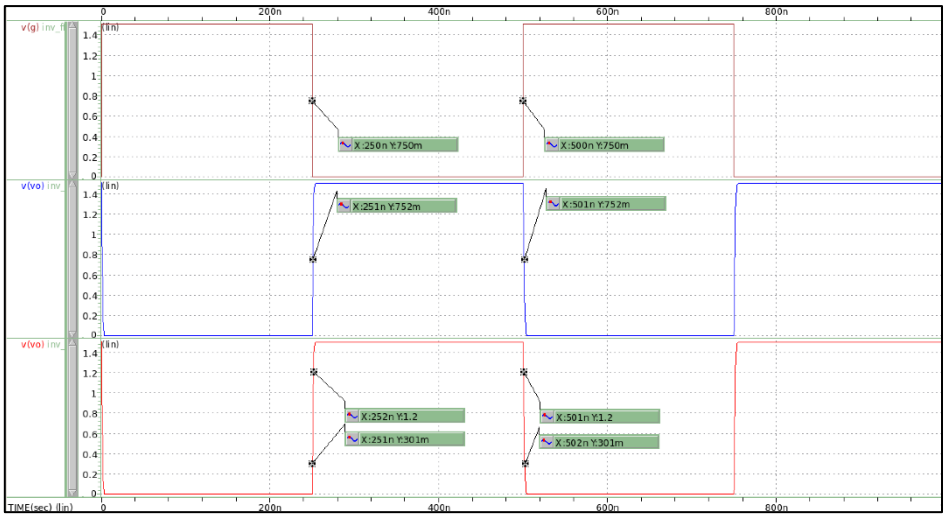


圖 14 FF Corner .tran simulation

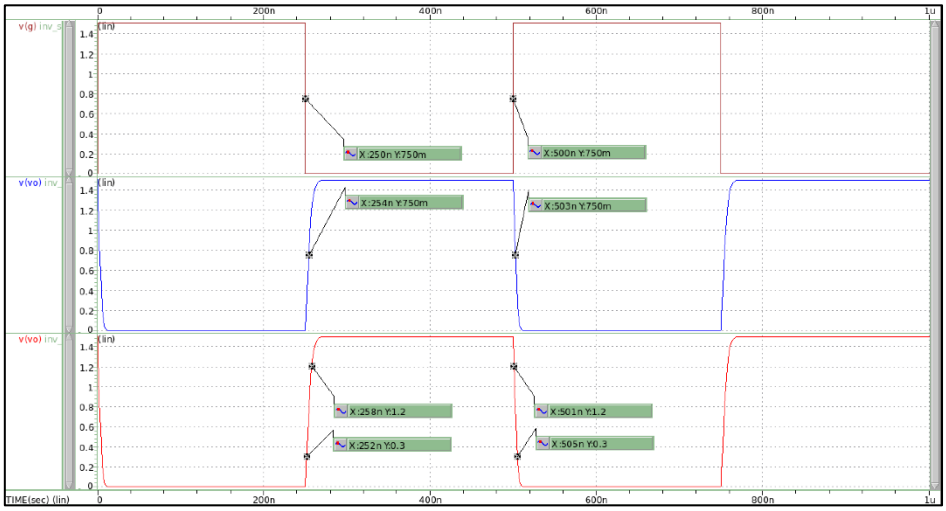


圖 15 SF Corner .tran simulation

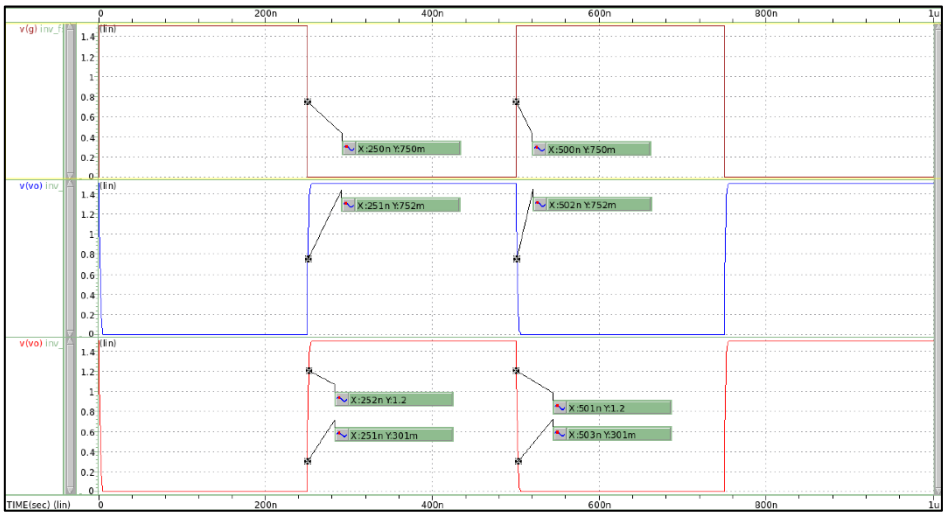


圖 16 FS Corner .tran simulation

INVERTER					
Input	CLK@2MHZ				
Corner	TT	SS	FF	SF	FS
t_{PHL}	2ns	3ns	1ns	3ns	2ns
t_{PLH}	1ns	3ns	1ns	4ns	1ns
t_r	1ns	3ns	1ns	6ns	1ns
t_f	2ns	4ns	1ns	4ns	2ns

Comment:

在分析 TT Corner 和 SS Corner 結果時，因本題 nMOS size 為題目給定，我推測是因 pMOS 的 Width 設計稍大，導致 pull-up 電流較大，使得 rising time 比 falling time 小。

而 SF Corner 理應是 slow NMOS, fast PMOS, 若兩個 MOS symmetric，結果應該為 rising time<falling time，但實際結果卻相反，推測是在設計 PMOS size 時，設計較小導致其 pull-up 電流不夠強。

在 t_{PHL} 和 t_{PLH} 部分可看到 FF Corner 的 delay 是最小的。這與理想符合，而 FS 和 SF Corner 都沒有比 TT Corner 延遲表現出色。

2. Run the HSPICE simulation to answer the following question, use VDD = 1.5V.

(a) Please design five 2-input NAND gates (one for each corner) with (W/L)n = 3µm/0.2µm while (W/L)p is your design. (BOTH PMOS sizes should be same.) Connect the two input together to run the transfer curve (like Fig.1), the transition point should be $VOUT$ = 0.5VDD @ Vin = 0.5 VDD in 5 process corners. (TT, SS, FF, SF, FS).

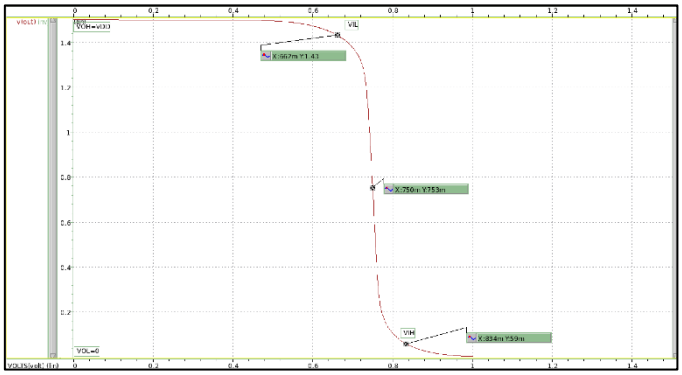


圖 17 TT Corner

W=2.86u,L=0.2u

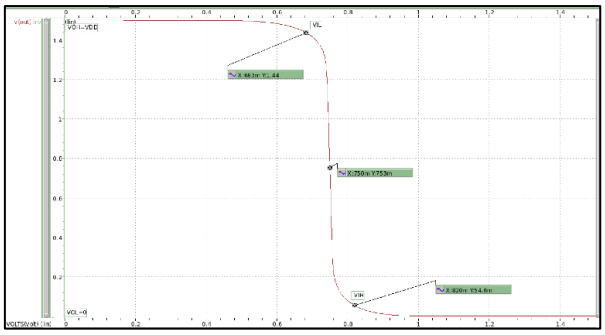


圖 18 SS Corner

W=2.99u,L=0.2u

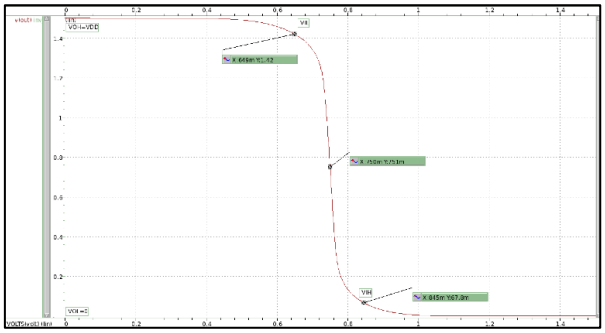


圖 19 FF Corner

W=2.79u,L=0.2u

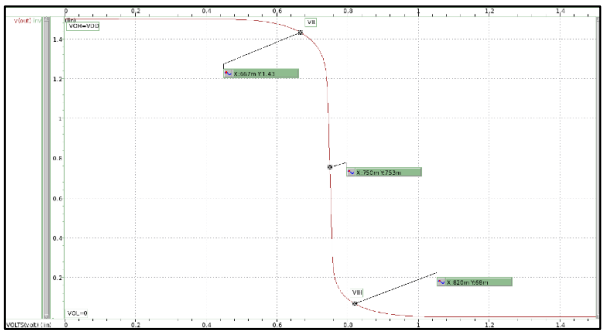


圖 20 SF Corner

W=0.7u,L=0.2u

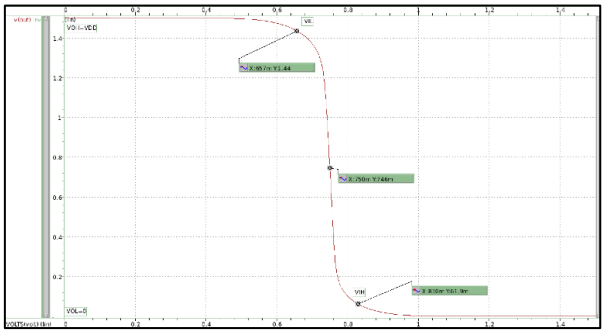


圖 21 FS Corner

W=2.95u,L=0.2u

(b) Using the transfer curve you simulated in (a), calculate the value of VIL,VIH, VOL,VOH and NMH and NML in 5 process corners. (TT, SS, FF, SF, FS).

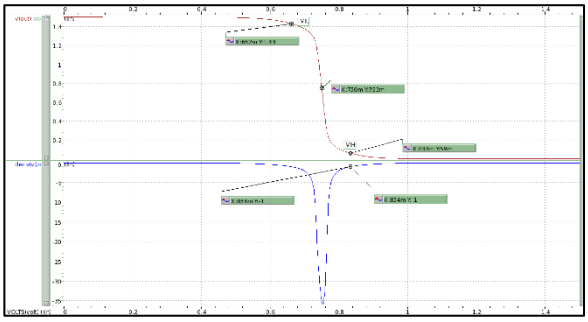


圖 22 TT Corner

圖 23 SS Corner

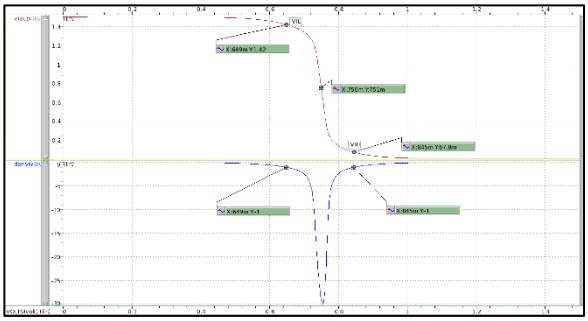


圖 24 FF Corner

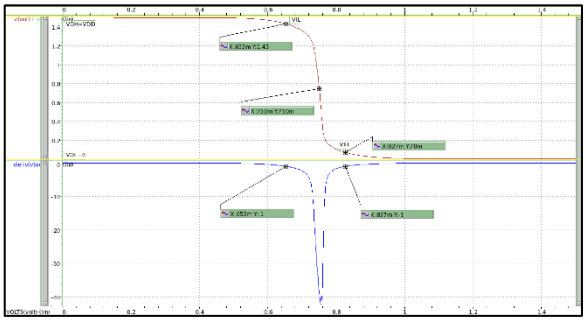


圖 25 SF Corner

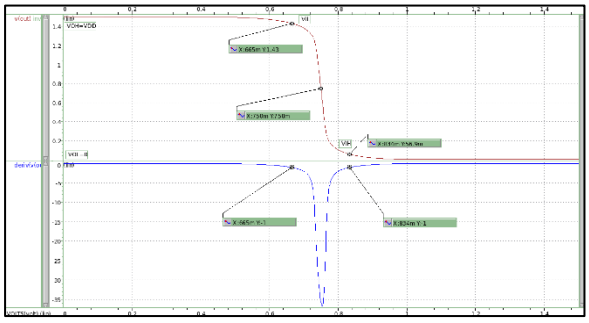
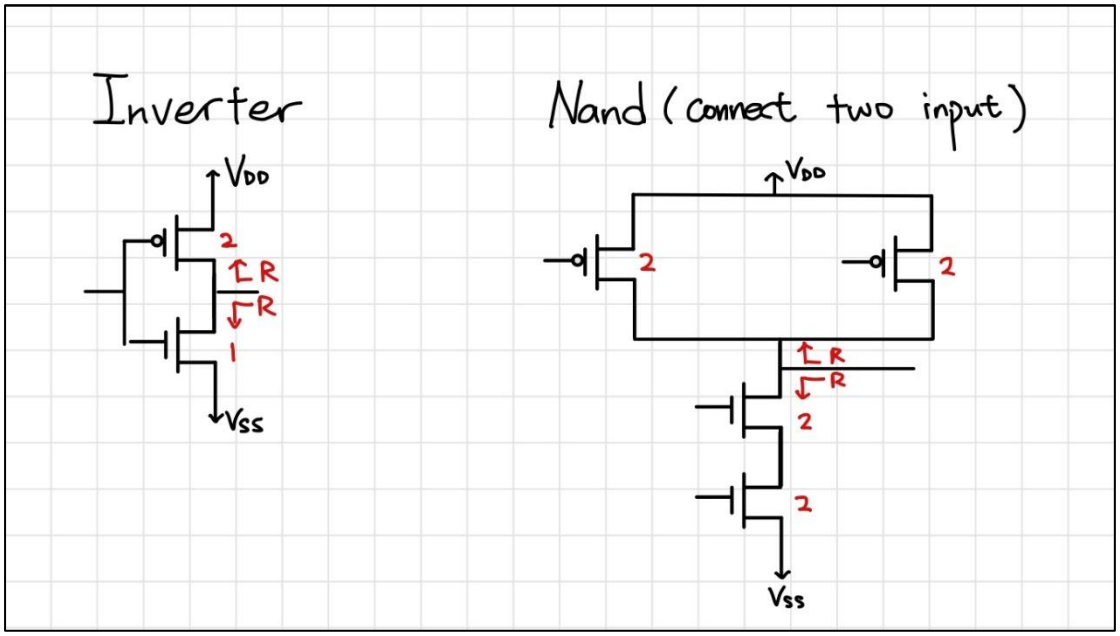


圖 26 FS Corner

(c) What are the differences in (W/L)p/(W/L)n between Q1(a) and Q2(a)? Please comment on the difference.



為使 pull-up network and pull-down network symmetric, 在設計 inverter 電路時的 MOS size 與 2 input NAND 會不同，從上圖大概計算一下 path effort，得:

Inverter:F=GH=1

2 input NAND:F=GH=(4/3)*2=8/3

故理論上 2 input NAND delay 會更嚴重。

(d) Using the 2-input NAND designed in (a) with VDD = 1.5V. Input signal (A or B) = 0V-1.5V@2MHz with rising time / falling time = 0.1ns and loading capacitor $Cload$ = 800fF at output.

CASE1(A:0-1.5@2MHZ,B:1.5)

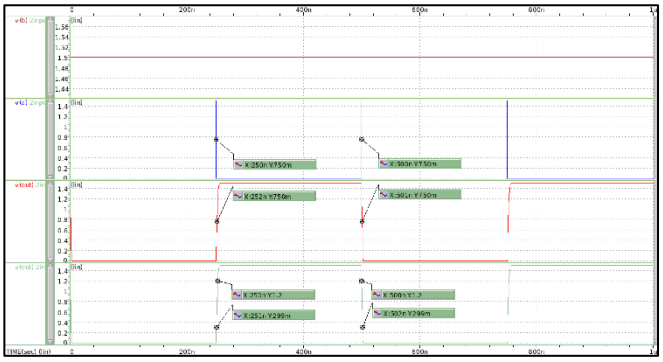


圖 27 TT Corner

CASE2(A:1.5,B:0-1.5@2MHZ)

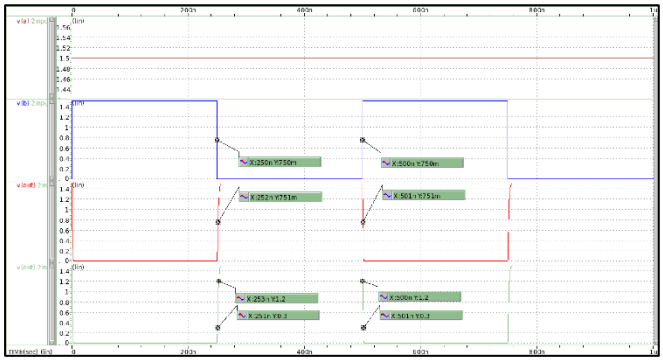


圖 28 TT Corner

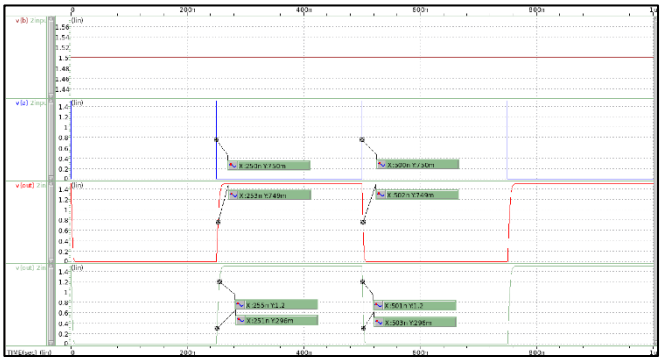


圖 29 SS Corner

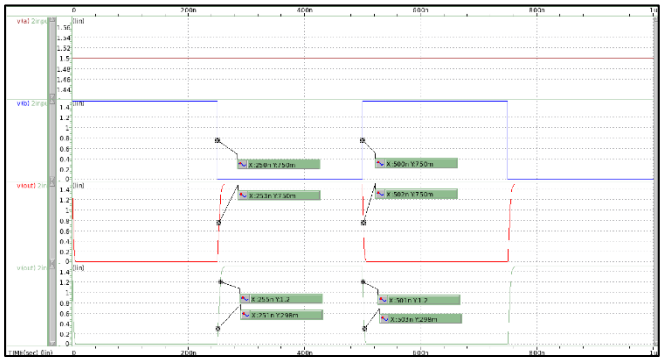


圖 30 SS Corner

CASE1(A:0-1.5@2MHZ,B:1.5)

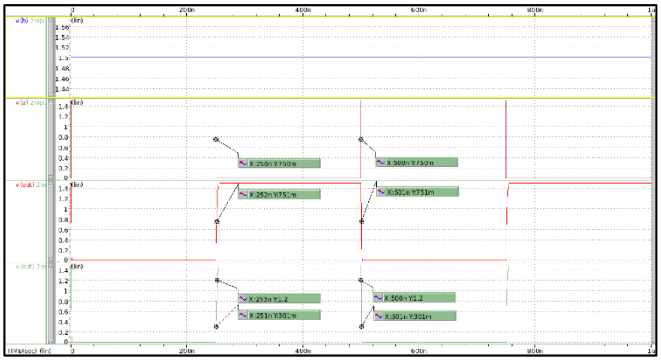


圖 31 FF Corner

CASE2(A:1.5,B:0-1.5@2MHZ)

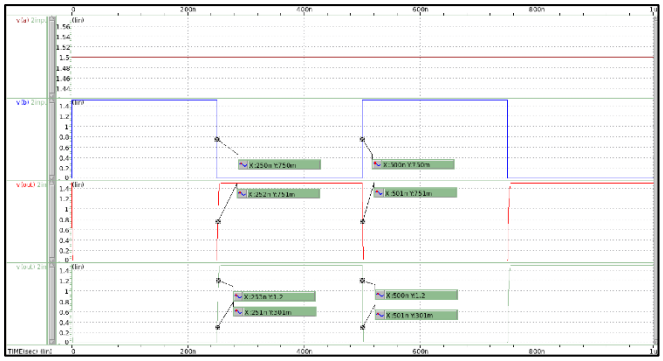


圖 32 FF Corner

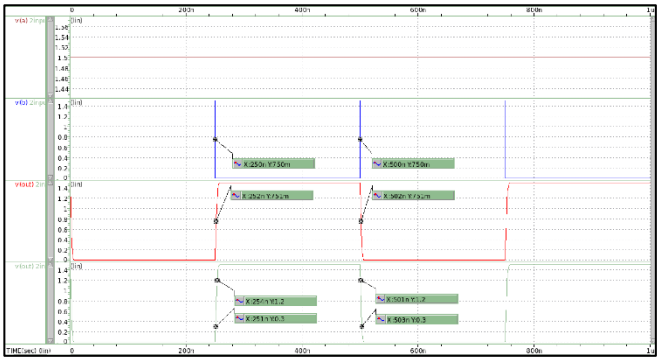


圖 33 SF Corner

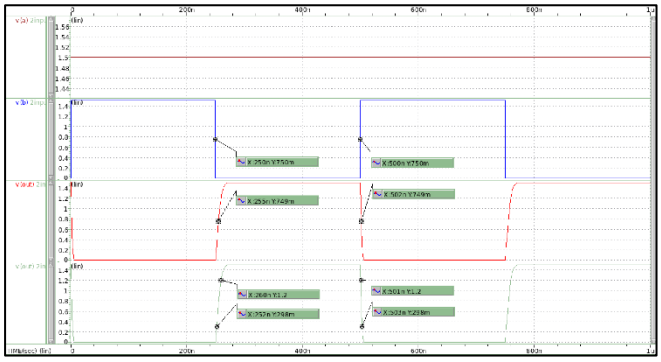


圖 34 SF Corner

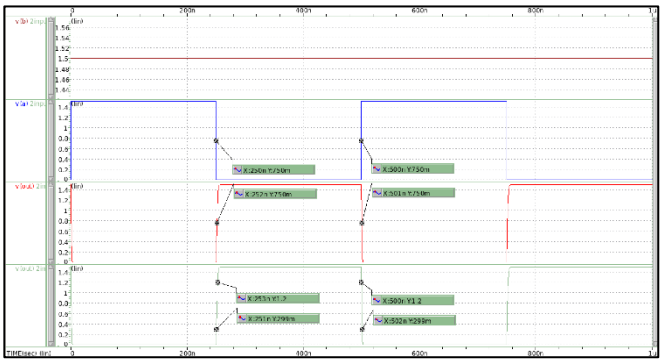


圖 35 FS Corner

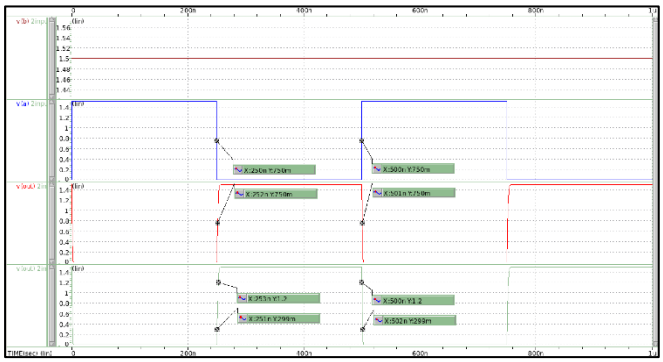


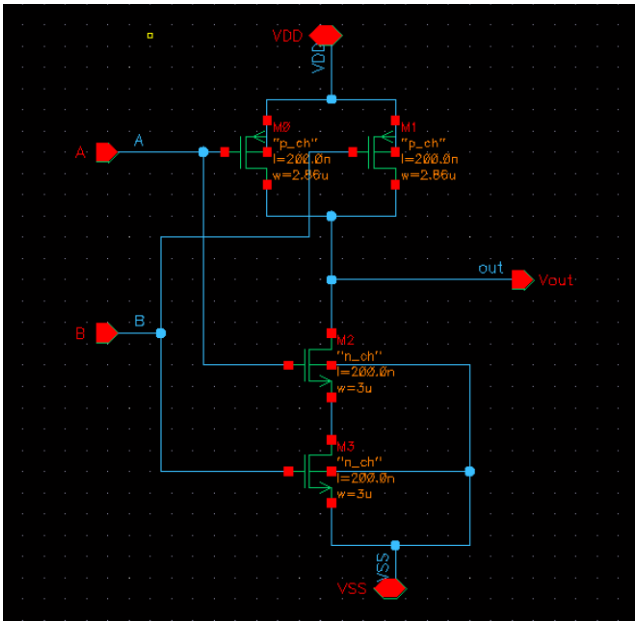
圖 36 FS Corner

NAND2	Case1					Case2				
Input A	CLK@2MHZ					1.5V				
Input B	1.5V					CLK@2MHZ				
Corner	TT	SS	FF	SF	FS	TT	SS	FF	SF	FS
t_{PHL}	1ns	2ns	1ns	2ns	1ns	1ns	2ns	1ns	2ns	1ns
t_{PLH}	2ns	3ns	2ns	2ns	2ns	2ns	3ns	2ns	5ns	2ns
Tr	2ns	4ns	2ns	3ns	2ns	2ns	4ns	2ns	8ns	2ns
Tf	2ns	2ns	1ns	2ns	2ns	1ns	2ns	1ns	2ns	2ns

Comment:

表格數據最大差異是 SF Corner，Case 2 的 rising time 較長，推測是因為在畫 transient schematic 時，INPUT B 因是時脈訊號，INPUT A 是直流訊號(不存在延遲)而 INPUT B 是畫在下方的 NMOS，距離輸出較遠，導致延遲較明顯。

好比有一台 A 車與 B 車要同時到達終點，而 B 較 A 慢，那當然是讓 B 靠近終點一點再一起出發會比較容易使得兩車同時抵達終點，而不是 A 車先抵達後還要等 B 車。



INPUT B 在下方時，若為時脈訊號，將造成延遲

3. Complete the layout and post-sim of Inverter in Q1 @ TT corner and 2-input NAND in Q2 @ TT corner.

(a) Finish DRC and LVS verification. Paste the pictures of layout, DRC result and LVS result in your report.

INVERTER:

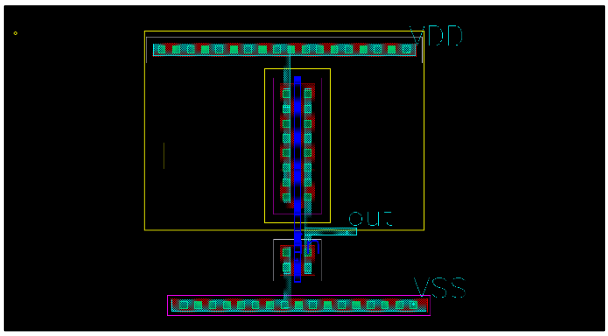


圖 37 Layout

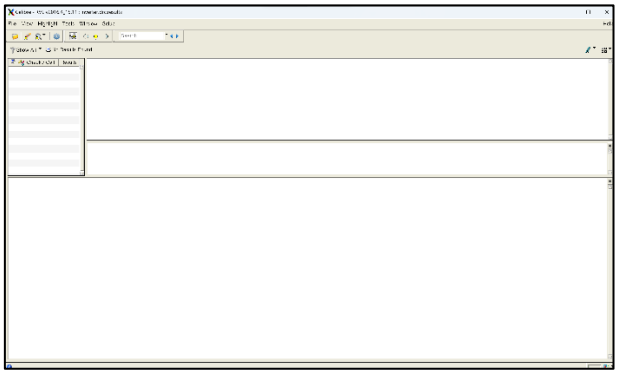


圖 38 DRC result

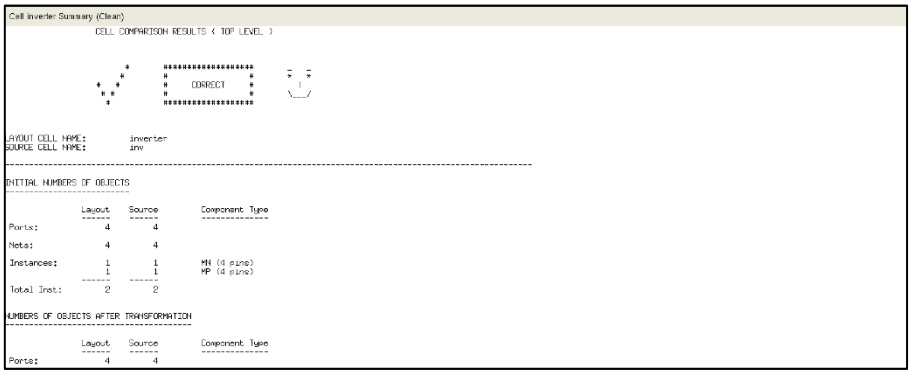


圖 39 LVS result

2 INPUT NAND:

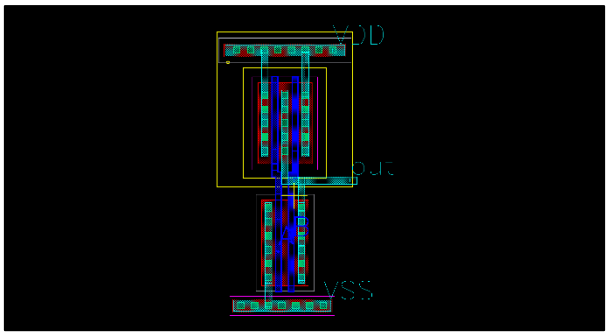


圖 40 Layout

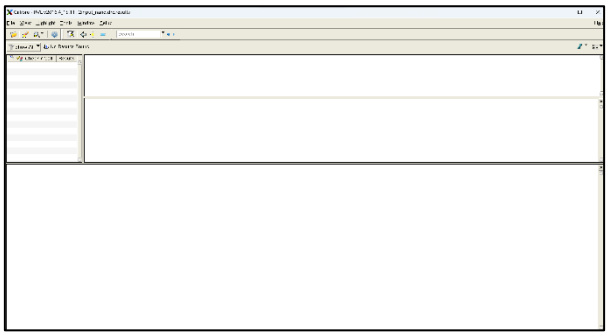


圖 41 DRC result

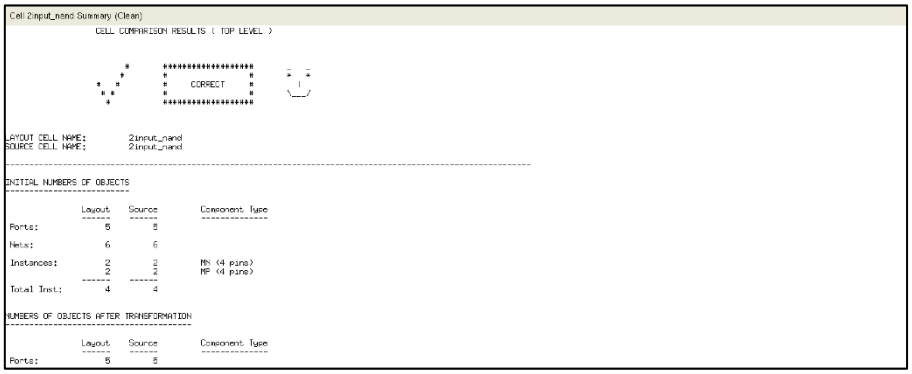
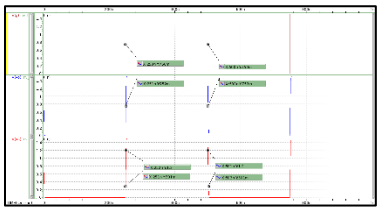
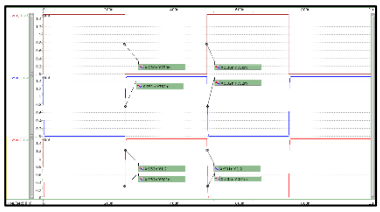
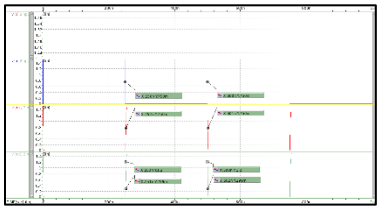
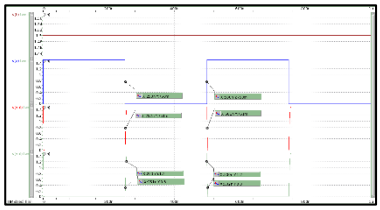
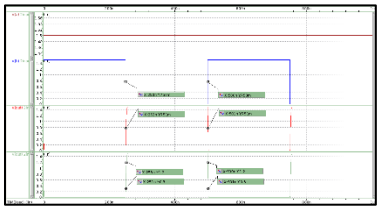
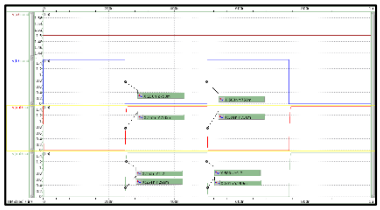


圖 42 LVS result

(b) Run the post-layout simulation (post-sim) for Q1(c) and Q2(d) compare them with pre-layout simulation (pre-sim). Please comment on the differences.

	Presim	Postsim
INVERTER		
2-INPUT NAND(CASE1)		
2-INPUT NAND(CASE2)		

COMMENT:

上圖對比可發現 POSTSIM 的輸出波型相較 PRESIM 往左移，推測是因 POSTSIM 加入了寄生參數，與實際工作情況更為貼近，但不論是 inverter 還是 2 -input NAND，波形都與 PRESIM 時沒太大差異，仍是具有反向器功能的電路設計。