國立清華大學 電機工程學系

111 學年度第二學期

EE-6250 超大型積體電路測試 VLSI Testing

Homework #2 (佔學期總成績 10 分)

(可兩人一組) Due Date：23:59pm, May 15 (Monday), 2023, (逾時不收)

Submission to https://eeclass.nthu.edu.tw/ 作業區

1. (100%) Consider the **design of a testable circuit** for computing a sequential divider.
   (a) (20%) Write the **RTL code** in Verilog or VHDL that takes in two 8-bit positive integers, A[7:0] and B[7:0], and produces its quotient Q[7:0] and remainder R[7:0].
   (b) (20%) **Verify the correctness of your RTL code** by a testbench. You should try it out by at least 3 pairs of input numbers.
   (c) (20%) **Use a synthesis script to convert your RTL code into a gate-level netlist**. Report the final **gate count**, the **maximum operating speed** (in MHz) and the **estimated power dissipation** in (mW) using *Design Compiler*.
   (d) (20%) **Add the scan chain** into your gate-level netlist obtained by part(c), report the resulting gate count, the maximum operating speed (in MHz) of your circuit. Compare to the non-scan version, and report the **area overhead percentage** and **performance penalty** due to scan chain insertion.
   (e) (20%) Run **ATPG** using a commercial tool available and report the **fault coverage**.

Note: 繳交資料: Combine all of the following items into a single PDF file for submission to our 【清華大學-數位學習平台】(https://eeclass.nthu.edu.tw/). On top of the combined PDF file there should be a cover page with your 系所，中英文姓名，學號等資訊.

- In addition to the answers to the above questions, you should include your (1) Verilog Code, (2) testbench, (3) simulation waveforms, (4) synthesized netlist, and (5) scan-inserted netlist.
- 各個組員的負責項目，或是**實作**貢獻方式的一段簡述。(若**無實際實作貢獻**之組員將零分計算。)