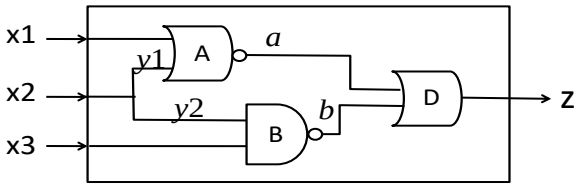
國立清華大學 電機工程學系
111 學年度第二學期
EE-6250 超大型積體電路測試 VLSI Testing
Homework #1 (佔學期總成績 10 分)
(每人一組) Due Date：23:59pm, March 20 (Monday), 2023, **(逾時不收)**
Submission to https://eeclass.nthu.edu.tw/ 作業區

1. Consider the testing of a gate-level circuit as shown below. The primary input signals are {x1, x2, x3} and the primary output signal is {z}. The output signals of logic gates {A, B} are denoted as {*a*, *b*}, and the branches of primary input signal x2 is called y1 and y2, respectively.



   (a) (50%) Write a software program (using C, C++, or any other programing language) that can **exhaustively simulate the logic behavior of the given circuit** under each of the 2^3 = 8 input vectors). Note that this can be done by executing the following Boolean equations in sequence in your program:

   ***a* = ~(x1 or x2);**
   ***b* = ~(x2 and x3);**
   z = (*a* or *b*);

   List the results as a truth table for output signal *z*. (Note this truth table contains 8 entries, one for each input combination).

   (b) (50%) Enhance your program so that it can perform **exhaustive fault simulation for bridging faults, {*AND-bridging* between *a* and *b*} and {*OR-bridging* between *y*1 and *x*3}**. Note that you need to report the total number of possible test patterns for each of the above two bridging faults. (Hint: perform fault injection, run exhaustive simulation on the faulty circuit, and then compare the results with those of the fault-free circuit. The fault injection can be done **manually** by changing the compiled code.)

Note: 繳交資料: (1) Combine your answers to the above questions (a)-(b) into a single PDF file. (2) Append to the above combined file your source code of your C or C++ program. (3) Attach a cover page with your 系所，中英文姓名，學號等資訊 before submitting your all-in-one file to our【清華大學-數位學習平台】(https://eeclass.nthu.edu.tw/).