國立清華大學 電機工程學系

111 學年度第二學期

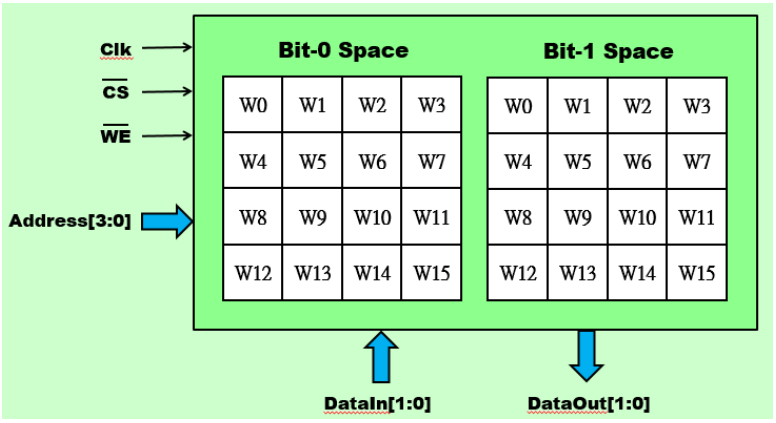
**EE-6250 超大型積體電路測試 VLSI Testing**

**Homework #3 (佔學期總成績 10 分)**

(可兩人一組) Due Date：23:59pm, June 5 (Monday), 2023, (逾時不收)

Submission to https://eeclass.nthu.edu.tw/ 作業區

1. Learn how to implement a Built-In Self-Test Circuit for a synchronous SRAM with 16 words, namely {W0 to W15}, with each word having only 2-bit data, arranged in a 4 row by 4 column configuration as shown below. Assume a clock rate of 100MHz.




(a) Write the **Verilog model for this SRAM** and verify it with a simple testbench to show the functional correctness. Show the simulation waveforms produced.

(b) Write a **synthesizable Verilog code** to realize the **Built-In Self-Test (BIST) function** for this SRAM block. Include the checkerboard test and the march test as discussed in class in your test algorithm. Replace the testbench in (a) with this BIST circuit and conduct the Verilog simulation again. Show the simulation waveforms produced.

(c) **Synthesize** your BIST circuit using Design Compiler. Report the critical path delay of your BIST circuit.

(d) Perform **gate-level simulation** including your BIST circuit and the Verilog model for the SRAM block under test. Assume a clock rate of 100MHz. Does you BIST circuit report a test result of "pass"? If not, discuss why.

(e) Increase the clock rate gradually (i.e., from 100MHz to some higher rates) and check if at some point the test result becomes erroneous (i.e., turning from "pass" to "fail"). Discuss if you can derive the **maximum operating speed** of your BIST circuit in this experiment.

(f) Try to **inject a stuck-at-1 fault to bit #2 of the SRAM word #5**, and report the test result of your BIST at 100MHz.

**Note: 繳交資料:** Submit the following documents (combined into a PDF file) to our【清華大學-數位學習平台】(https://eeclass.nthu.edu.tw/).

- **A cover page containing 所有組員之系所，中英文姓名，學號等資訊**
- **Your results in response to questions (a)-(f). Note that you should include in this report your Verilog codes, simulation waveforms, test results, maximum operating speed, and faulty simulation waveforms and test results.**