**國立清華大學**

**超大型積體電路設計VLSI Design**



**Homework 1**

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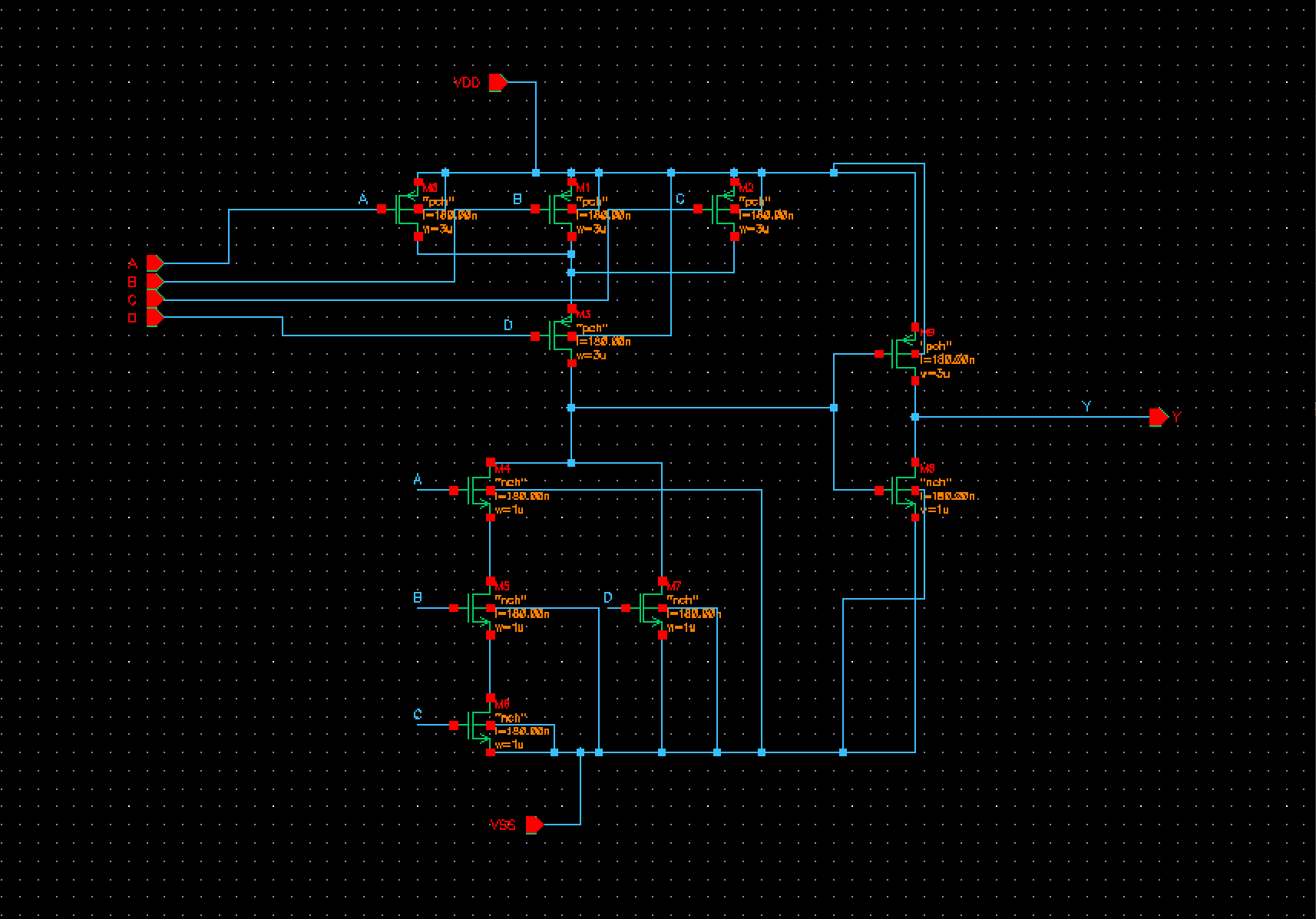
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# Please use the combination of CMOS to sketch the transistor-level schematic and stick diagram of the following compound gate function from those inputs A, B, C and D.

## Y = A·B·C+D

### Schematic



### Stick diagram

### spice code

一張含有 文字 的圖片

自動產生的描述

### waveview result

## Y = (A+B)·(C+D)

#### Schematic

一張含有 文字, 光 的圖片

自動產生的描述

#### Stick diagram

#### Spice code

一張含有 文字 的圖片

自動產生的描述

#### Waveview result

## Y = A·C+B·C’

##### Schematic

一張含有 光, 黑暗 的圖片

自動產生的描述

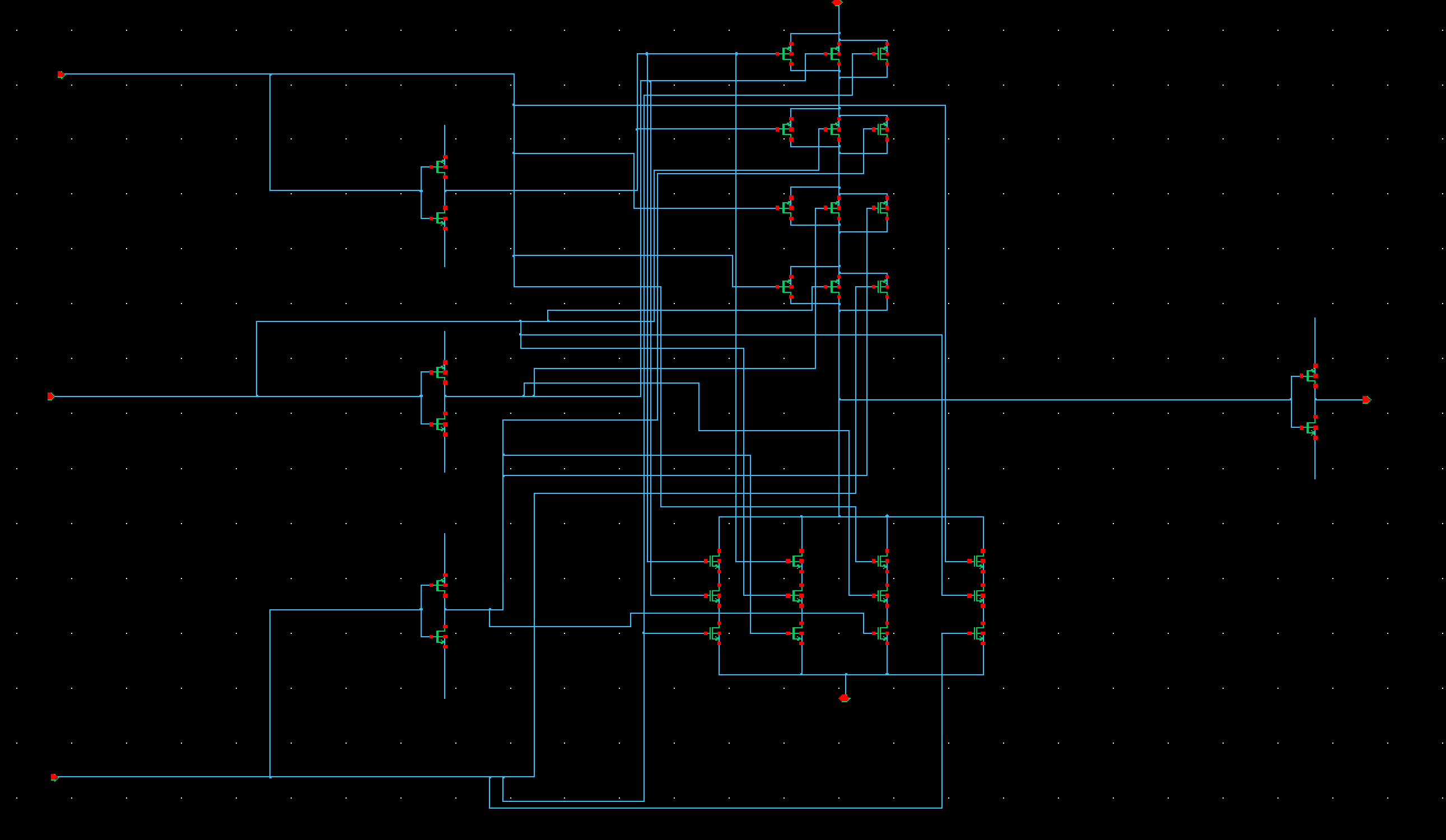
##### Stick diagram

##### 一張含有 文字 的圖片 自動產生的描述Spice code

##### Waveview result

## Y = A⊕B⊕C, ⊕ stands for XOR gate

###### Schematics



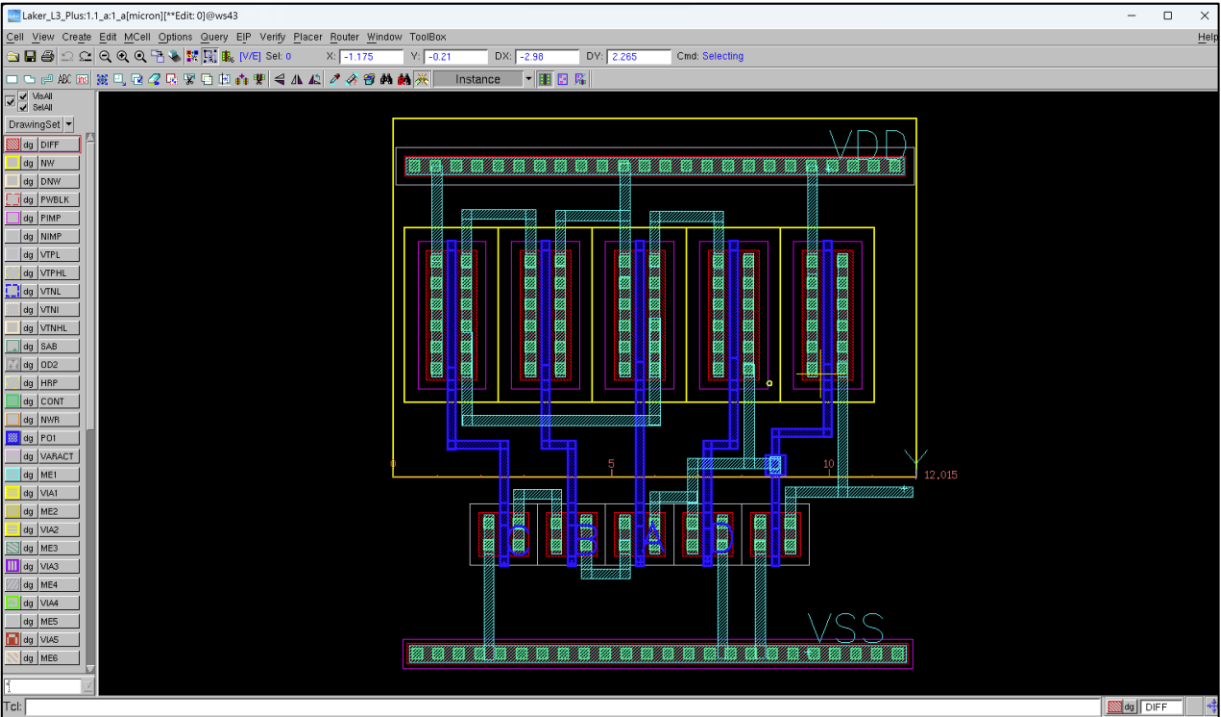
###### Stick diagram

###### 一張含有 文字 的圖片 自動產生的描述Spice code

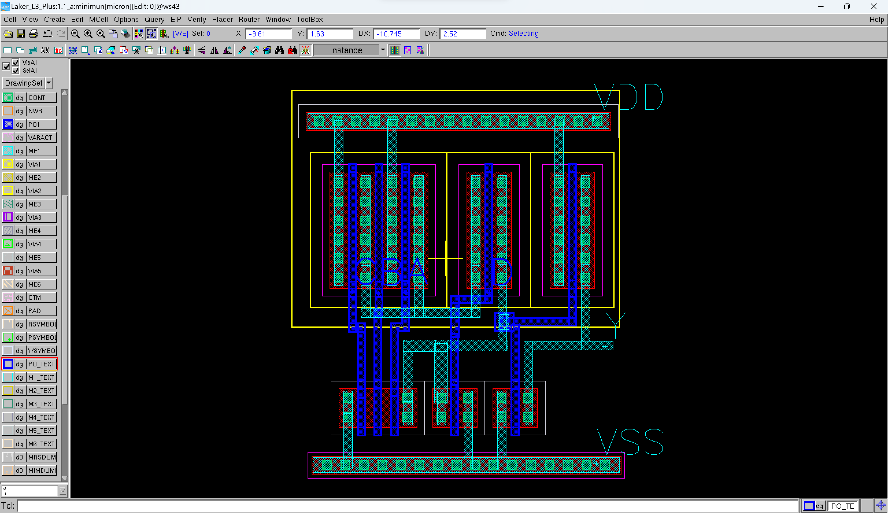
###### Waveview result

**Comments**

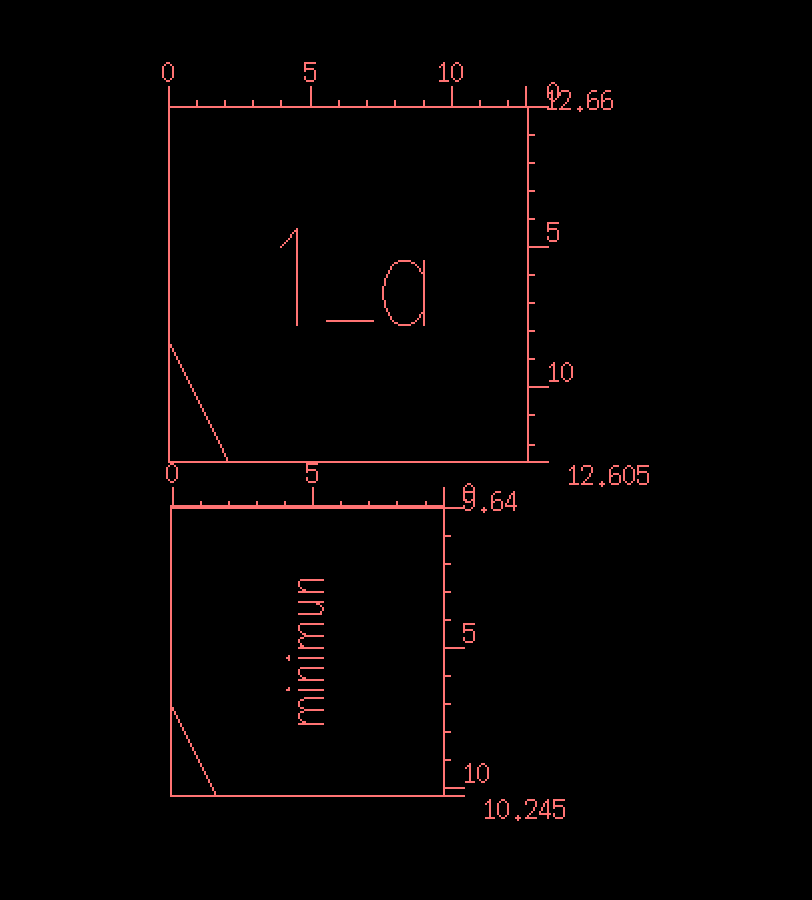
本次作業我在畫layout時嘗試兩種畫法，雖然這是基礎觀念但仍然獲得很直接的感受。下圖以第一題a小題為例。



將每個mos分開(面積較大)



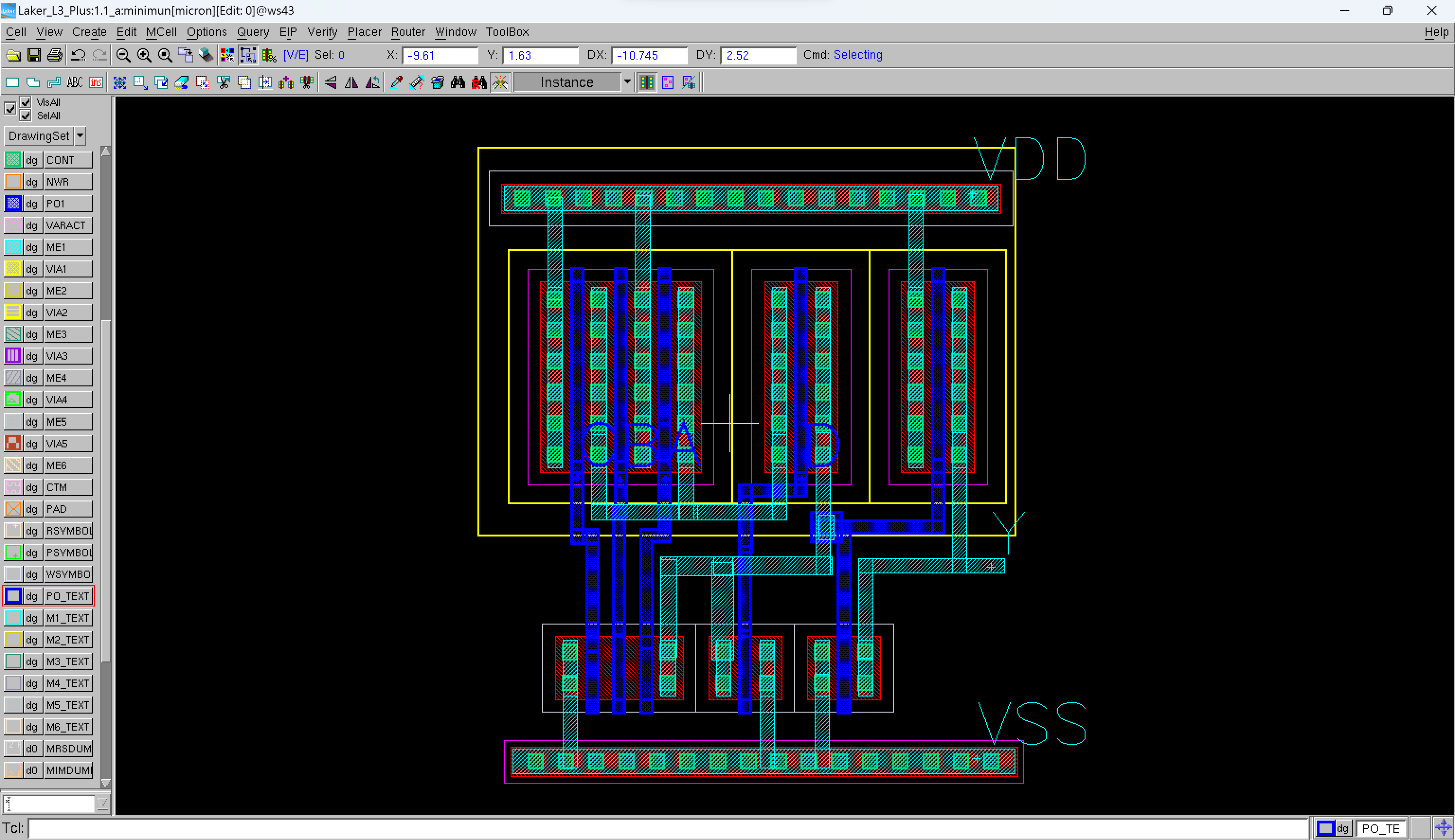
串並mos(面積較小)

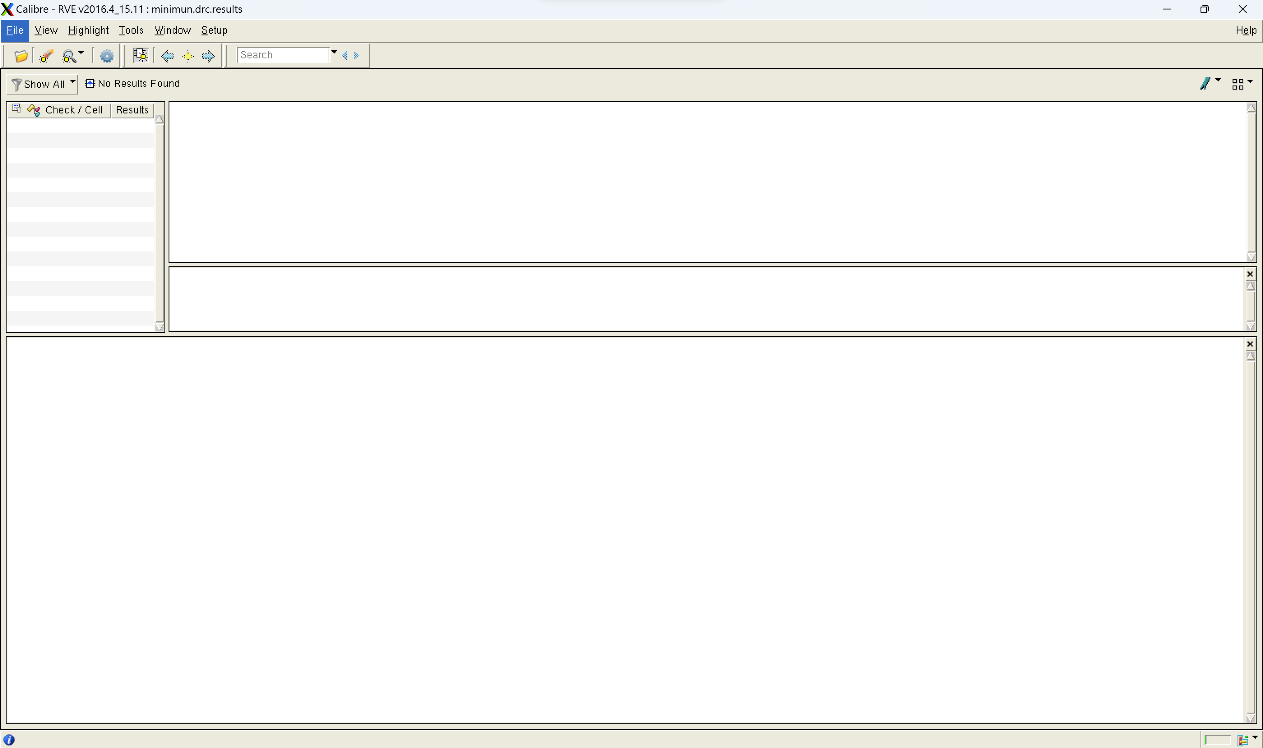


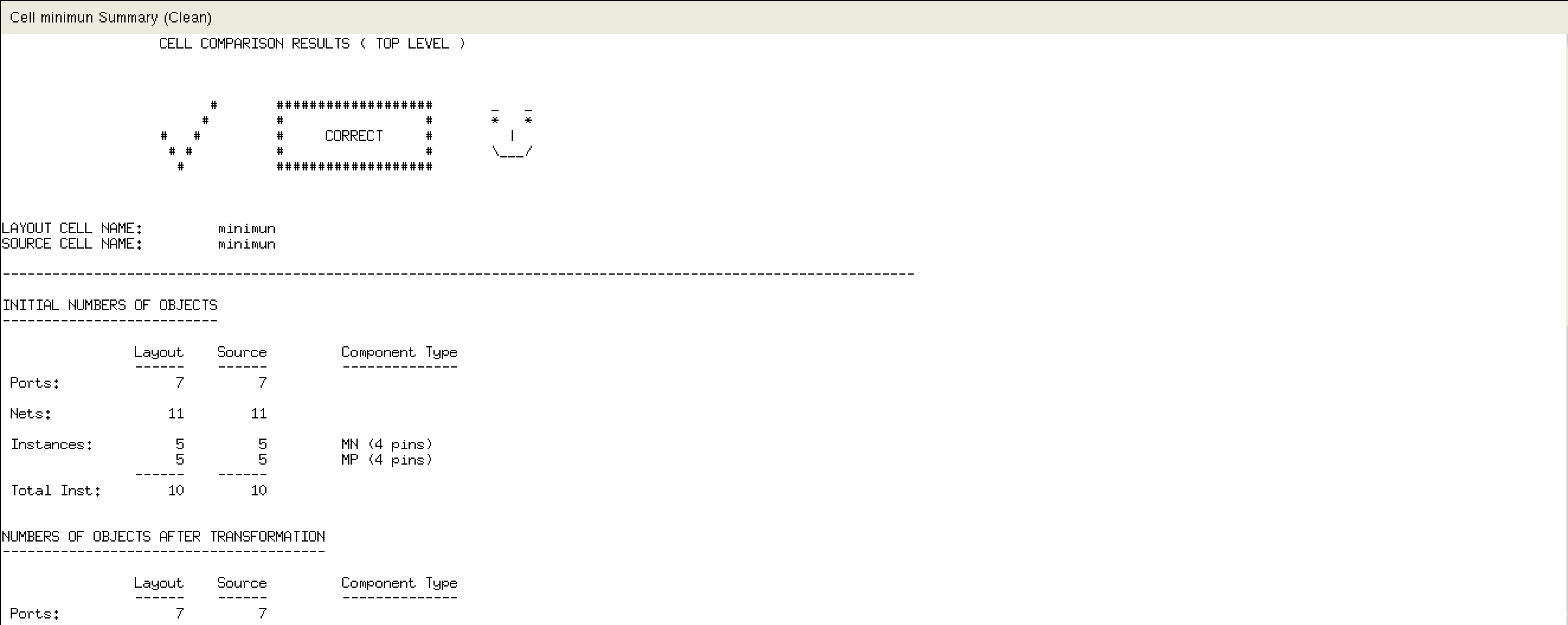
兩者使用面積差了約39%

# Based on problem 1(a),1(b), please finish DRC and LVS verification. You must attach the pictures on your report which contain layout, DRC result and LVS result.

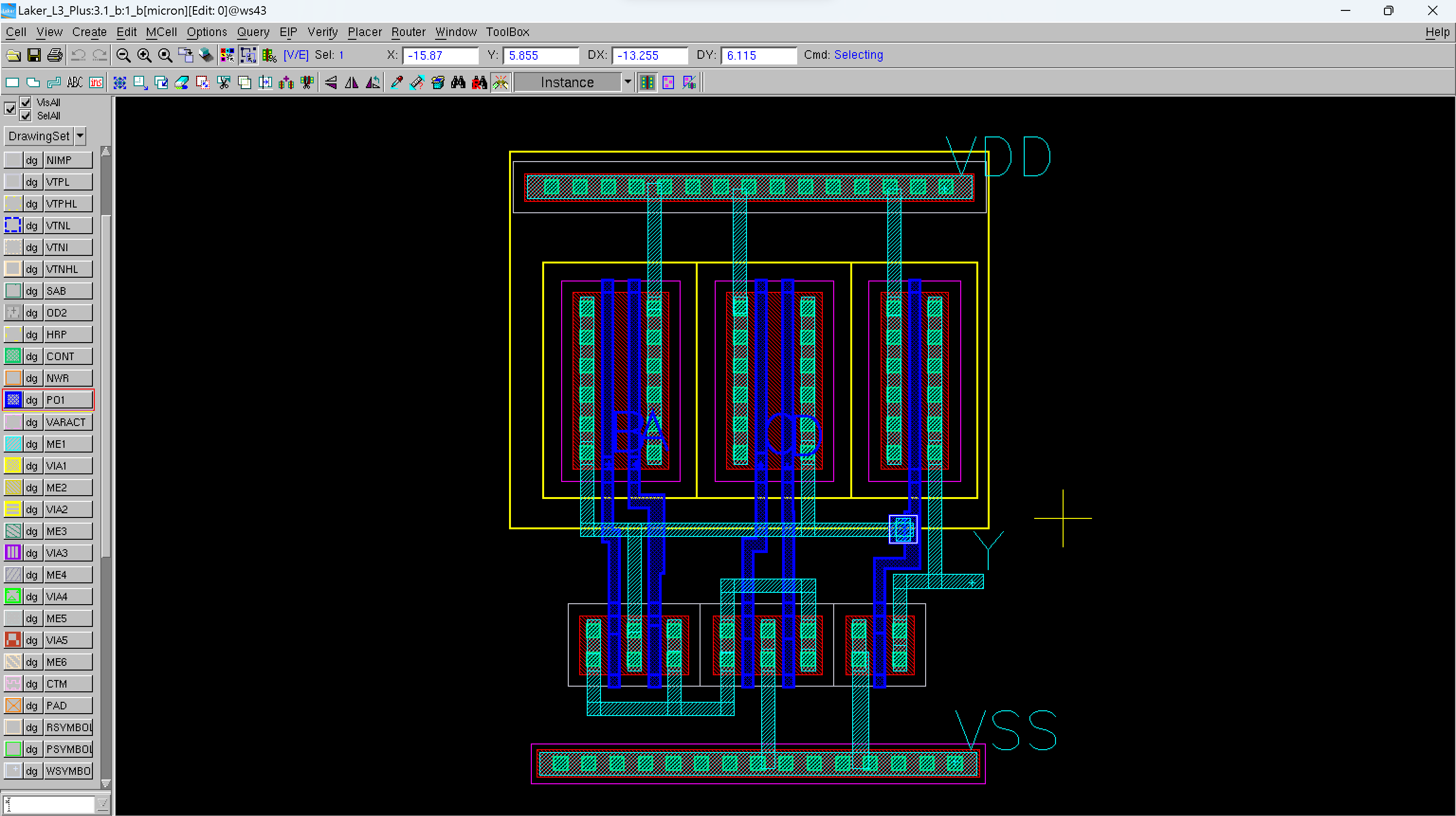
1. Y = A·B·C+D
2. Layout

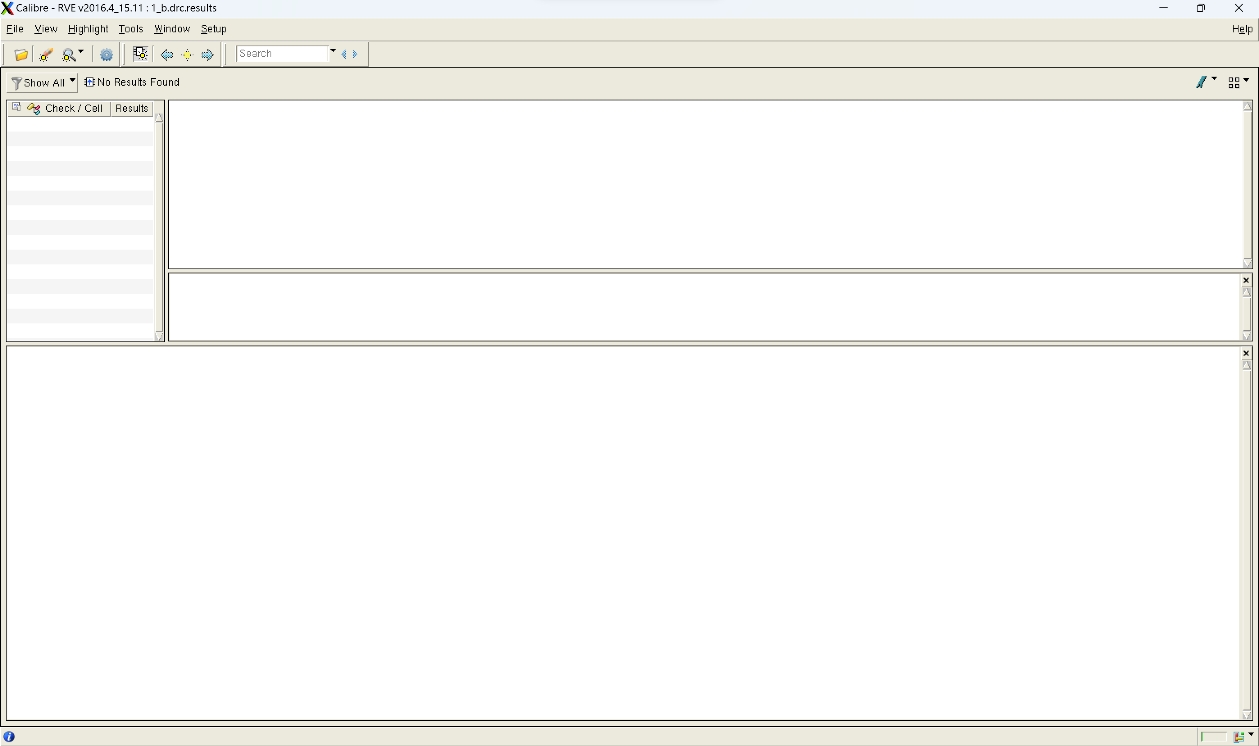


1. DRC result
2. LVS result



1. Y = (A+B)·(C+D)
2. Layout



1. DRC result
2. LVS result



1. Explain what DRC rules do you learn, please list them.
2. Minimum width of Metal line is 0.23um when transistor channel length is 0.18um.
3. If the same layer cross each other, it makes a contact.
4. If the different layer just cross, it doesn't make contact but if contact has to be made, we should mark it.
5. Minimum area of contact should be 0.23u x 0.23u when transistor channel length is 0.18um.
6. We should draw N-WELL contact to enclose PMOS and VDD(positive source).
7. Minimum distance between different layers is 0.25u.
8. Minimum NWELL overlap N+ diffusion is 0.25um
9. Minimum space between two Poly regions on field area is 0.25um.
10. Gate at 90 degree angle is not allowed.(merge them to solve)
11. Minimum PO1 width for 1.8V NMOS or PMOS or interconnect is 0.18um
12. Minimum space between two NPlus regions is 0.45um
13. Minimum space between ME1 regions is 0.24um where MET1 width < 10um

# Draw the fabrication steps of an inverter (cross section).

