**國立清華大學**

**超大型積體電路設計VLSI Design**



**Homework 2**

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目錄

[1. Run the HSPICE simulation to answer the following question, use 𝑉𝐷𝐷 = 1.5𝑉. 3](#_Toc117889280)

[(a) Please design five INVERTER gates (one for each corner) with (W/L)𝑛 = 1μm/0.2μm while (W/L)𝑝 is your design. Run the transfer curve (like Fig.1), the transition point should be 𝑉𝑂𝑈𝑇 = 0.5𝑉𝐷𝐷 @ 𝑉𝑖𝑛 = 0.5 𝑉𝐷𝐷 in 5 process corners (TT, SS, FF, SF, FS). Please comment on the differences. 3](#_Toc117889281)

[(b) Using the transfer curve you simulated in (a), calculate the value of 𝑉𝐼𝐿,𝑉𝐼𝐻, 𝑉𝑂𝐿,𝑉𝑂𝐻 and 𝑁𝑀𝐻 and 𝑁𝑀𝐿 in 5 process corners (TT, SS, FF, SF, FS). Please comment on the differences. 6](#_Toc117889282)

[(c) Using the INVERTER designed in (a) with 𝑉𝐷𝐷 = 1.5𝑉. Input signal = 0V-1.5V @2MHz with rising time / falling time = 0.1ns and loading capacitor 𝐶𝑙𝑜𝑎𝑑 = 800𝑓𝐹 at output. 9](#_Toc117889283)

[2. Run the HSPICE simulation to answer the following question, use 𝑉𝐷𝐷 = 1.5𝑉. 12](#_Toc117889284)

[(a) Please design five 2-input NAND gates (one for each corner) with (W/L)𝑛 = 3μm/0.2μm while (W/L)𝑝 is your design. (BOTH PMOS sizes should be same.) Connect the two input together to run the transfer curve (like Fig.1), the transition point should be 𝑉𝑂𝑈𝑇 = 0.5𝑉𝐷𝐷 @ 𝑉𝑖𝑛 = 0.5 𝑉𝐷𝐷 in 5 process corners. (TT, SS, FF, SF, FS). 12](#_Toc117889285)

[(b) Using the transfer curve you simulated in (a), calculate the value of 𝑉𝐼𝐿,𝑉𝐼𝐻, 𝑉𝑂𝐿,𝑉𝑂𝐻 and 𝑁𝑀𝐻 and 𝑁𝑀𝐿 in 5 process corners. (TT, SS, FF, SF, FS). 14](#_Toc117889286)

[(c) What are the differences in (W/L)𝑝/(W/L)𝑛 between Q1(a) and Q2(a)? Please comment on the difference. 15](#_Toc117889287)

[(d) Using the 2-input NAND designed in (a) with 𝑉𝐷𝐷 = 1.5𝑉. Input signal (A or B) = 0V-1.5V@2MHz with rising time / falling time = 0.1ns and loading capacitor 𝐶𝑙𝑜𝑎𝑑 = 800𝑓𝐹 at output. 16](#_Toc117889288)

[3. Complete the layout and post-sim of Inverter in Q1 @ TT corner and 2-input NAND in Q2 @ TT corner. 19](#_Toc117889289)

[(a) Finish DRC and LVS verification. Paste the pictures of layout, DRC result and LVS result in your report. 19](#_Toc117889290)

[(b) Run the post-layout simulation (post-sim) for Q1(c) and Q2(d) compare them with pre-layout simulation (pre-sim). Please comment on the differences. 21](#_Toc117889291)

# Run the HSPICE simulation to answer the following question, use 𝑉𝐷𝐷 = 1.5𝑉.

## Please design five INVERTER gates (one for each corner) with (W/L)𝑛 = 1μm/0.2μm while (W/L)𝑝 is your design. Run the transfer curve (like Fig.1), the transition point should be 𝑉𝑂𝑈𝑇 = 0.5𝑉𝐷𝐷 @ 𝑉𝑖𝑛 = 0.5 𝑉𝐷𝐷 in 5 process corners (TT, SS, FF, SF, FS). Please comment on the differences.

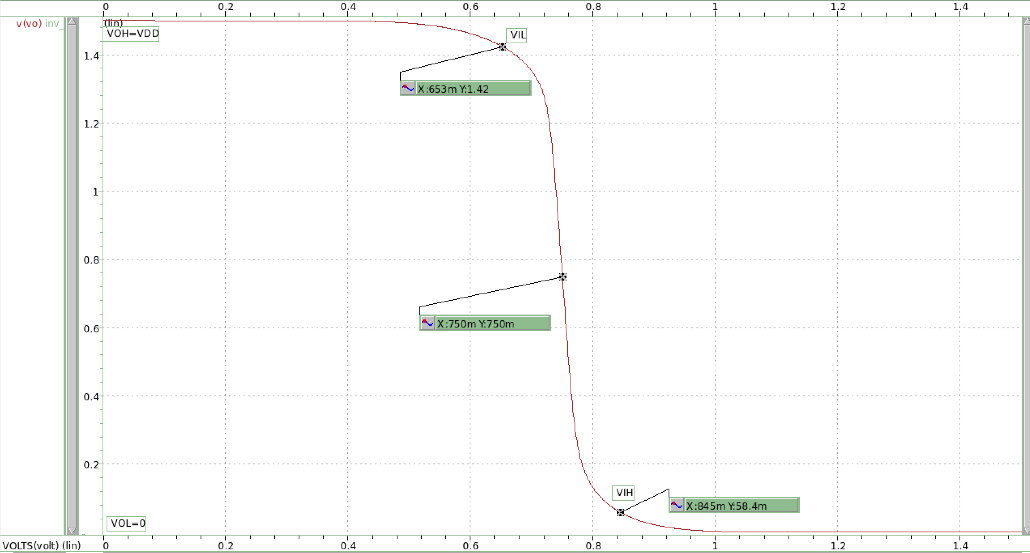


圖 1 TT Corner

W=4.15u,L=0.2u

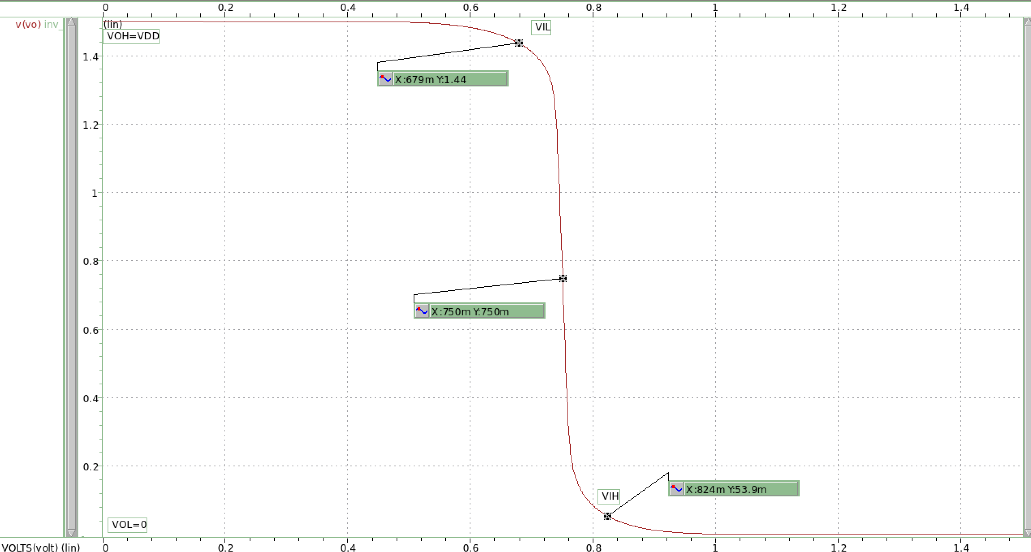


圖 2 SS corner

W=3.65u,L=0.2u

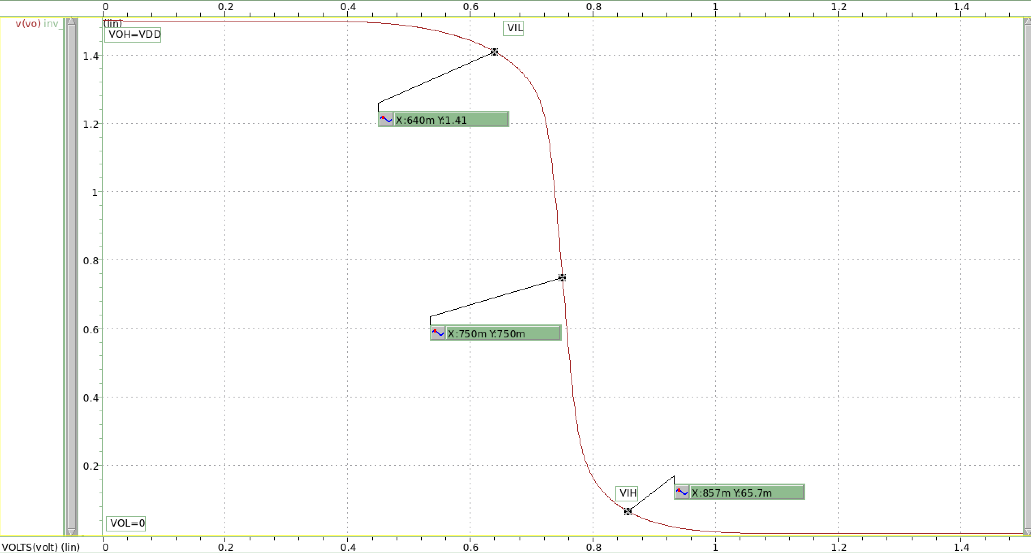


圖 3 FF Corner

W=4.11u,L=0.2u

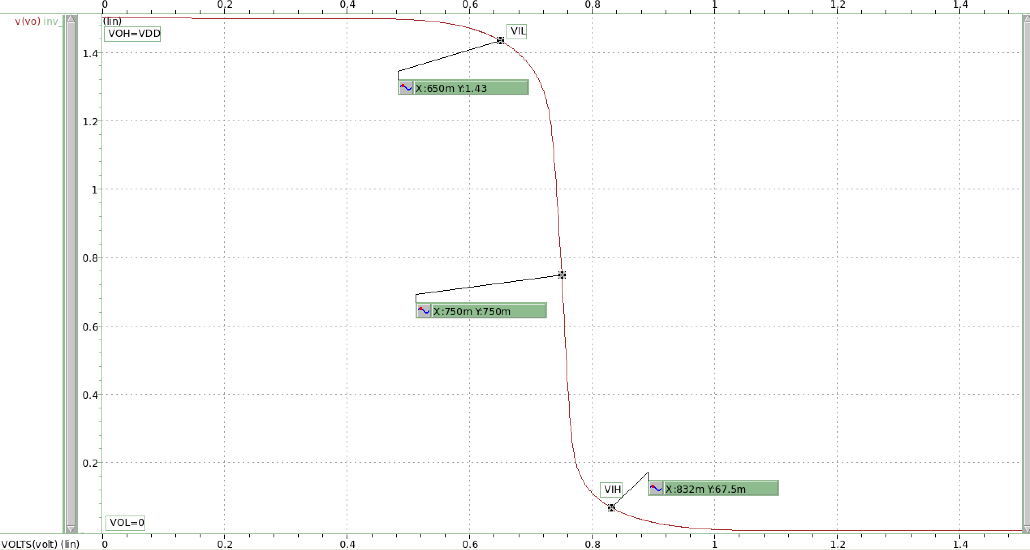


圖 4 SF Corner

W=0.914u,L=0.2u

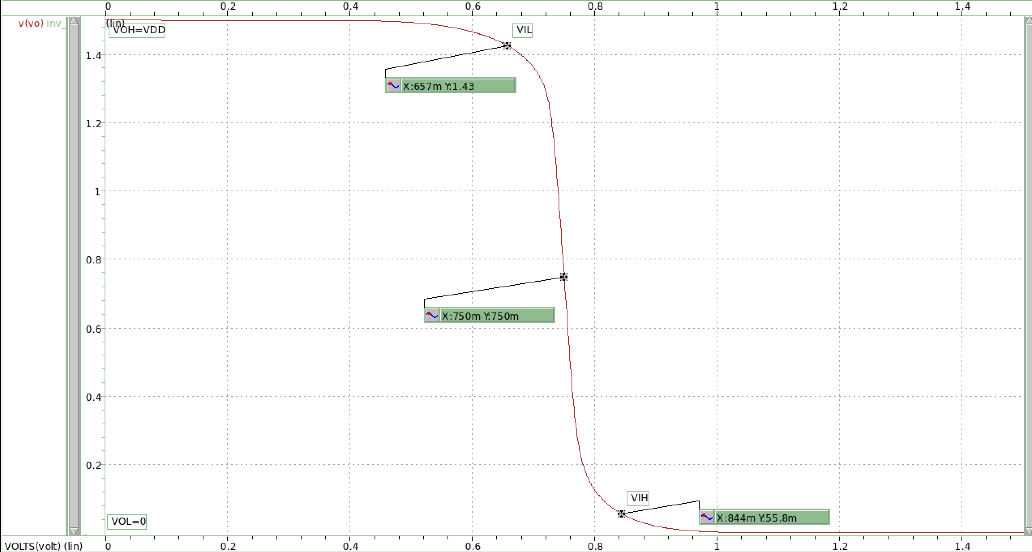


圖 5 FS Corner

W=4.16u,L=0.2u

Comment:

上面五張圖依序為TT、SS、FF、SF、FS，從圖形上可看出每個圖形的變化趨勢都有細微的差別。

TT : 圖形對稱，VIL和VIH處的二次曲線變化速度接近。

SS : 圖形對稱，VIL和VIH處的二次曲線變化速度接近。但變化速度都比TT corner快，故中間sat處直線較為陡峭。

FF : 圖形對稱，VIL和VIH處的二次曲線變化速度接近。但變化速度比TT corner慢，故中間sat處直線較為平坦。

SF : 圖形較不對稱，在VIL處的曲線變化速度較VIH處大。

FS : 圖形較不對稱，在VIL處的曲線變化速度較VIH處小。

斜線較為陡峭之corner，雖可以更快速切換高低狀態，但若要調到𝑉𝑂𝑈𝑇 = 0.5𝑉𝐷𝐷 @ 𝑉𝑖𝑛 = 0.5 𝑉𝐷𝐷，較為困難，斜率與敏感度呈正相關。而斜率較為平坦之corner則相反，各有優缺。TT為最平衡的corner。

## Using the transfer curve you simulated in (a), calculate the value of 𝑉𝐼𝐿,𝑉𝐼𝐻, 𝑉𝑂𝐿,𝑉𝑂𝐻 and 𝑁𝑀𝐻 and 𝑁𝑀𝐿 in 5 process corners (TT, SS, FF, SF, FS). Please comment on the differences.

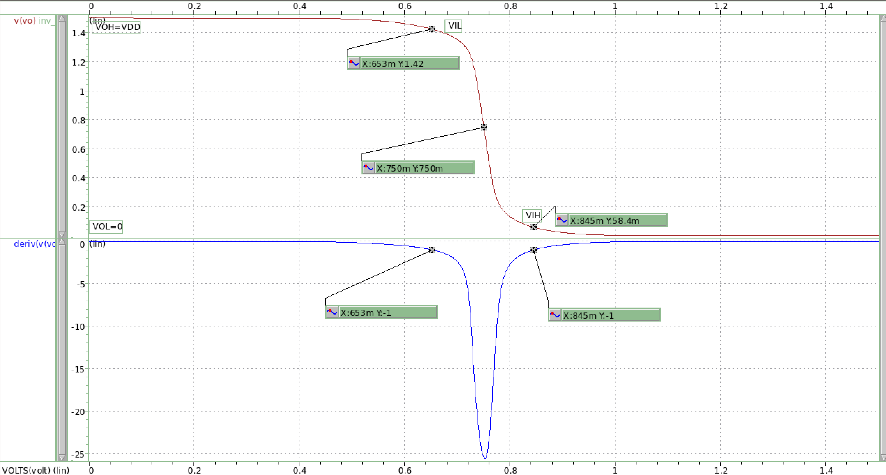


圖 6 TT Corner

VIL=653mv;VIH=845mv;VOL=0V;VOH=1.5V

NMH=VOH-VIH=655mv;NML=VIL-VOL=653mv

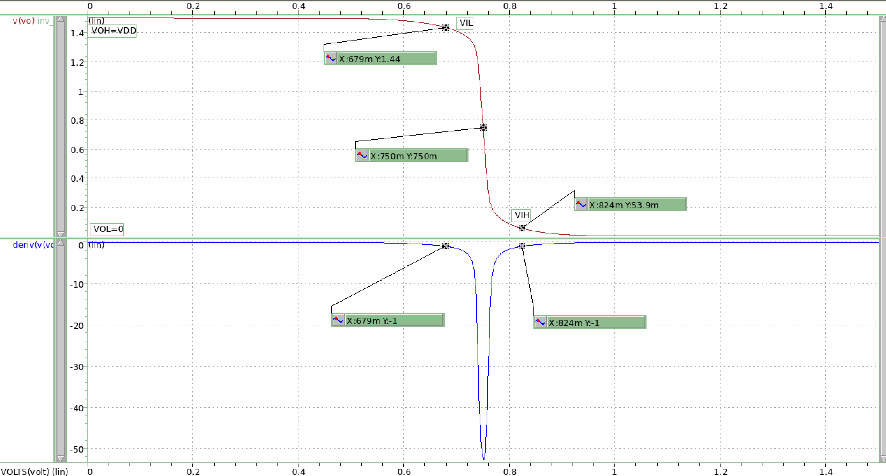


圖 7 SS Corner

VIL=679mv;VIH=824mv;VOL=0V;VOH=1.5V

NMH=VOH-VIH=676mv;NML=VIL-VOL=679mv

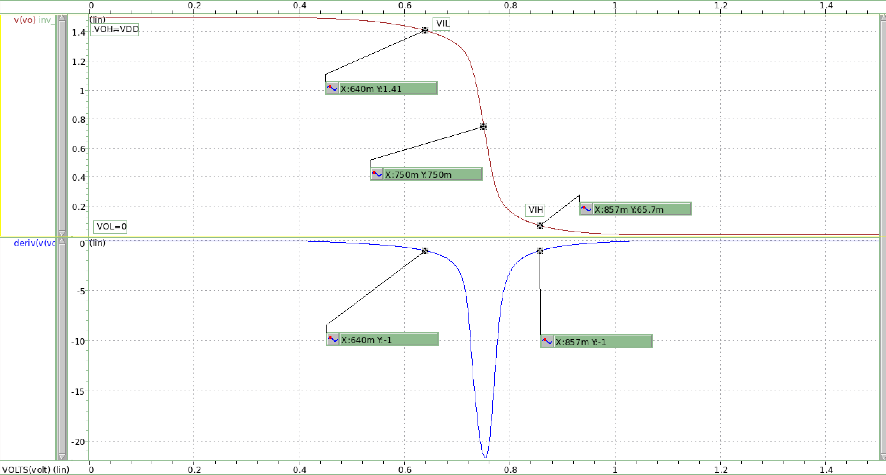


圖 8 FF Corner

VIL=640mv;VIH=857mv;VOL=0V;VOH=1.5V

NMH=VOH-VIH=643mv;NML=VIL-VOL=640mv

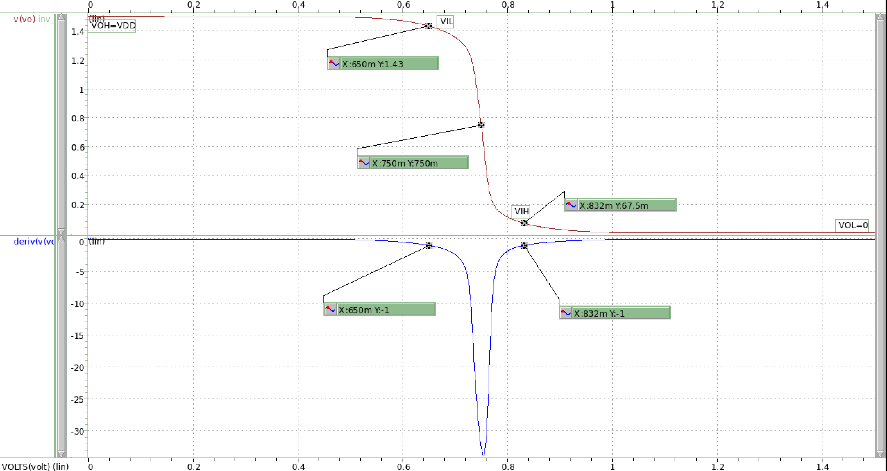


圖 9 SF Corner

VIL=650mv;VIH=832mv;VOL=0V;VOH=1.5V

NMH=VOH-VIH=668mv;NML=VIL-VOL=650mv

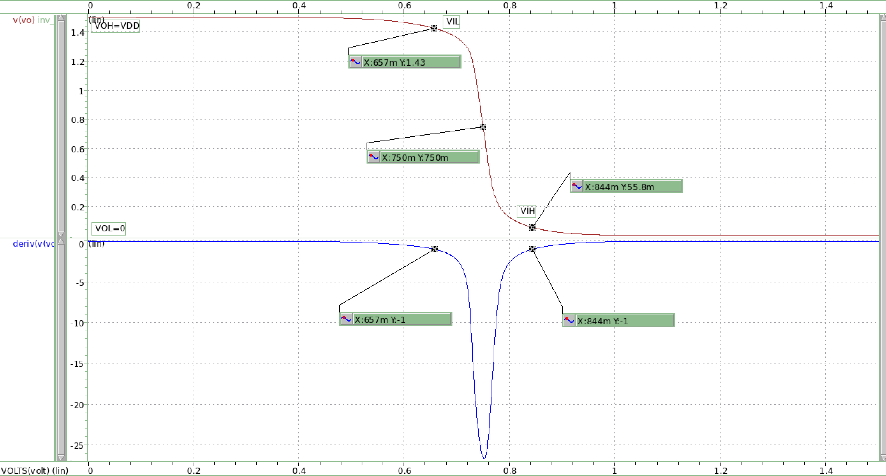


圖 10 FS Corner

VIL=657mv;VIH=844mv;VOL=0V;VOH=1.5V

NMH=VOH-VIH=656mv;NML=VIL-VOL=657mv

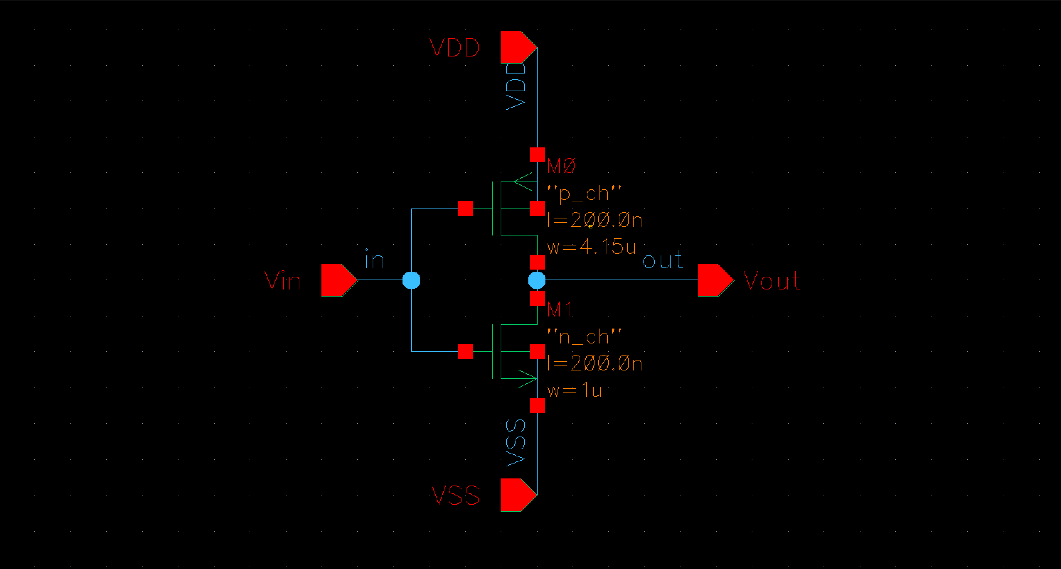


圖 11 Inverter schematic

Comment:

因S代表飽和電流小、閥值大；F代表飽和電流大、閥值小。

可從上面5張圖觀察出相較TT corner，SS corner擁有更好的Noise Margin，VIL更大、VIH更小，換句話說SS Corner可以擁有更多輸入電壓的選擇，input voltage forbidden zone也更小。

而FF Corner則相反，forbidden zone較TT大，故在選擇輸入訊號時條件更為嚴苛，但相對擁有更大的飽和電流。

SF Corner的情況也符合理論，其VIL及VIH都比TT corner小，造成其NML比較差但NMH比較好;而FS corner的VIL要比TT corner來的大，波形結果也是符合的。

## Using the INVERTER designed in (a) with 𝑉𝐷𝐷 = 1.5𝑉. Input signal = 0V-1.5V @2MHz with rising time / falling time = 0.1ns and loading capacitor 𝐶𝑙𝑜𝑎𝑑 = 800𝑓𝐹 at output.

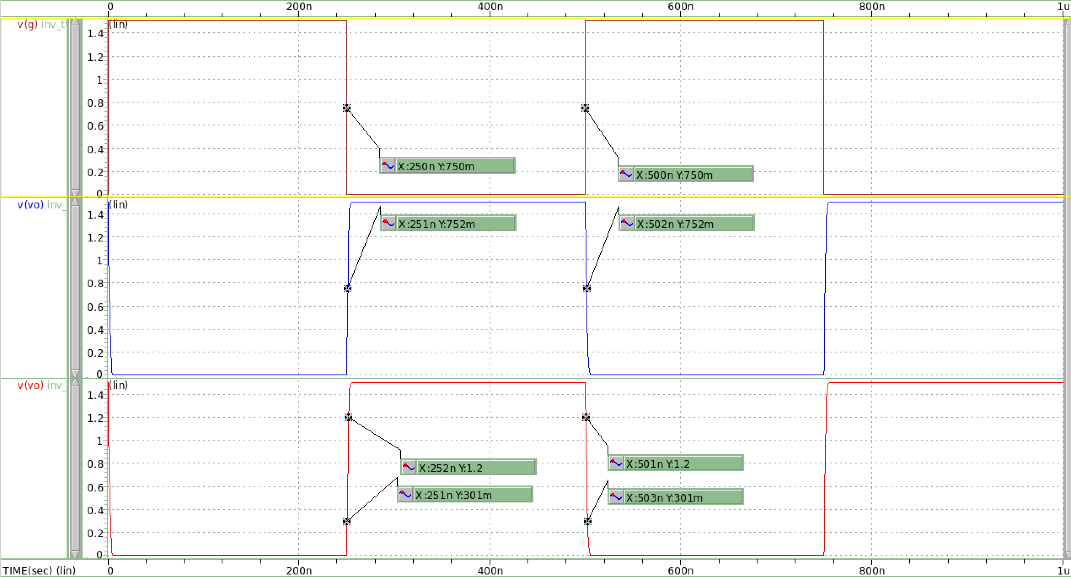


圖 12 TT Corner .tran simulation

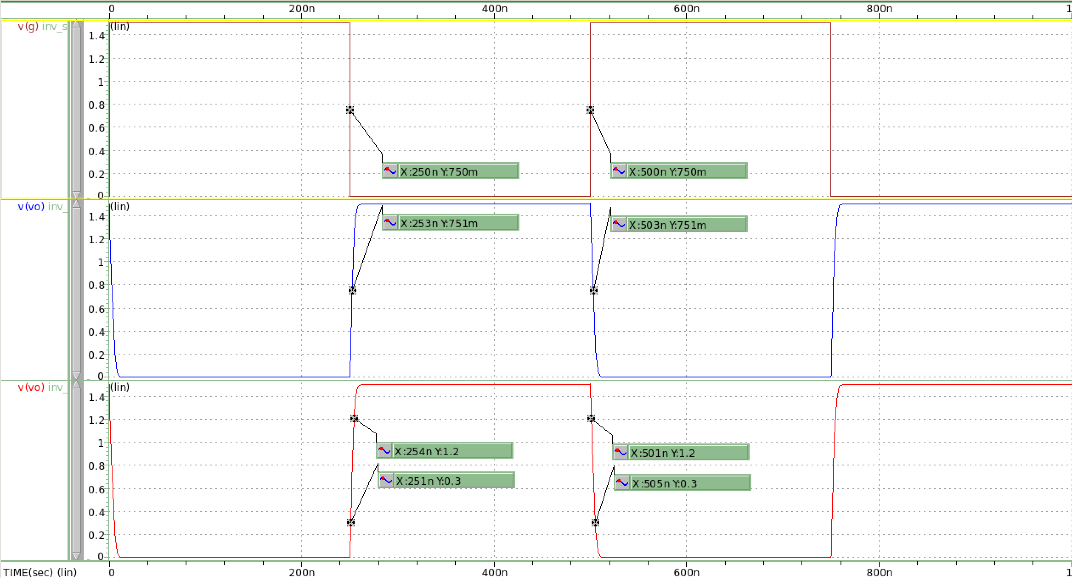


圖 13 SS Corner .tran simulation

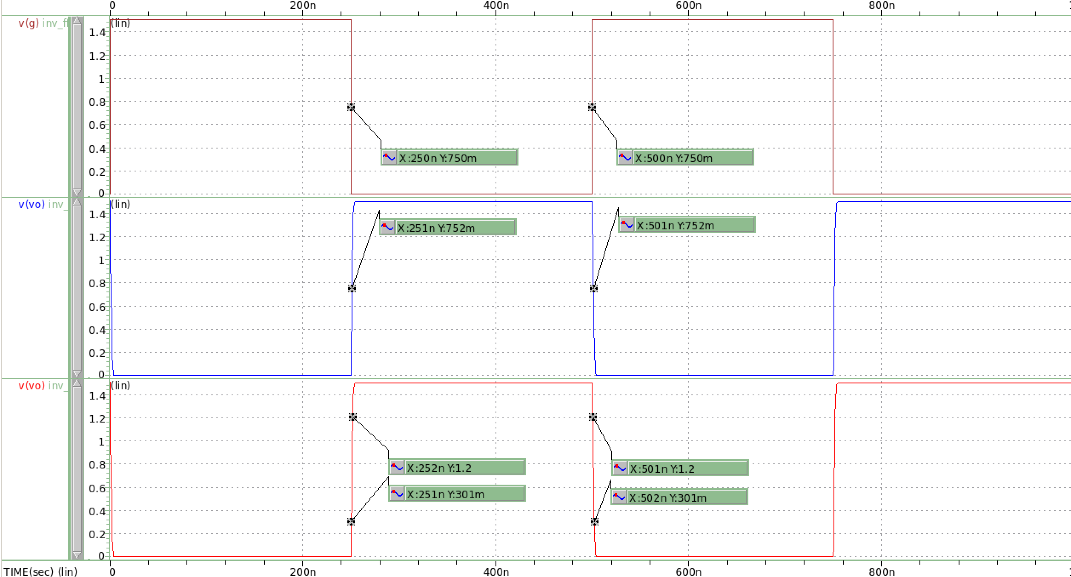


圖 14 FF Corner .tran simulation

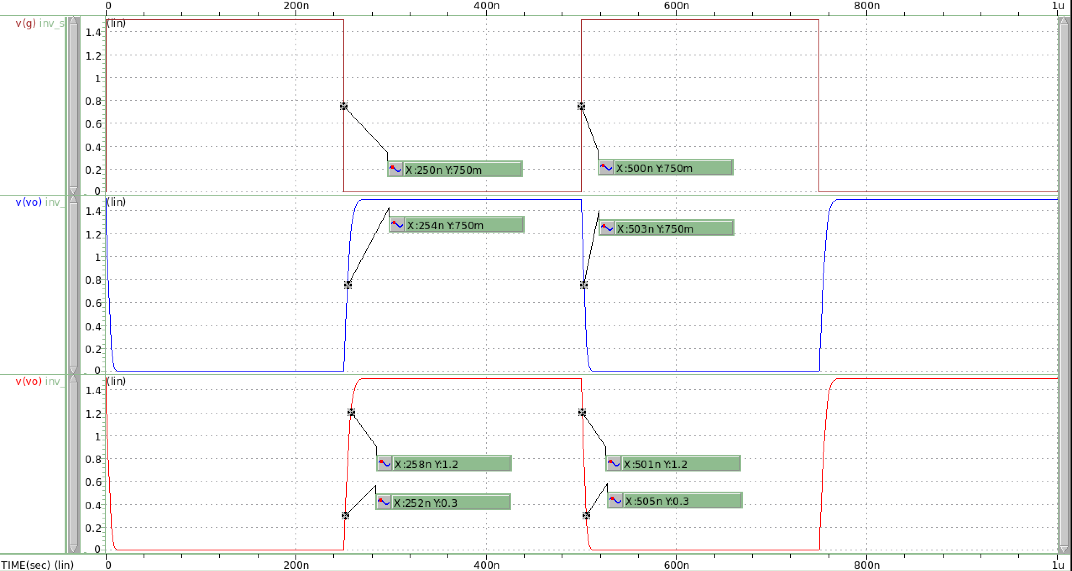


圖 15 SF Corner .tran simulation

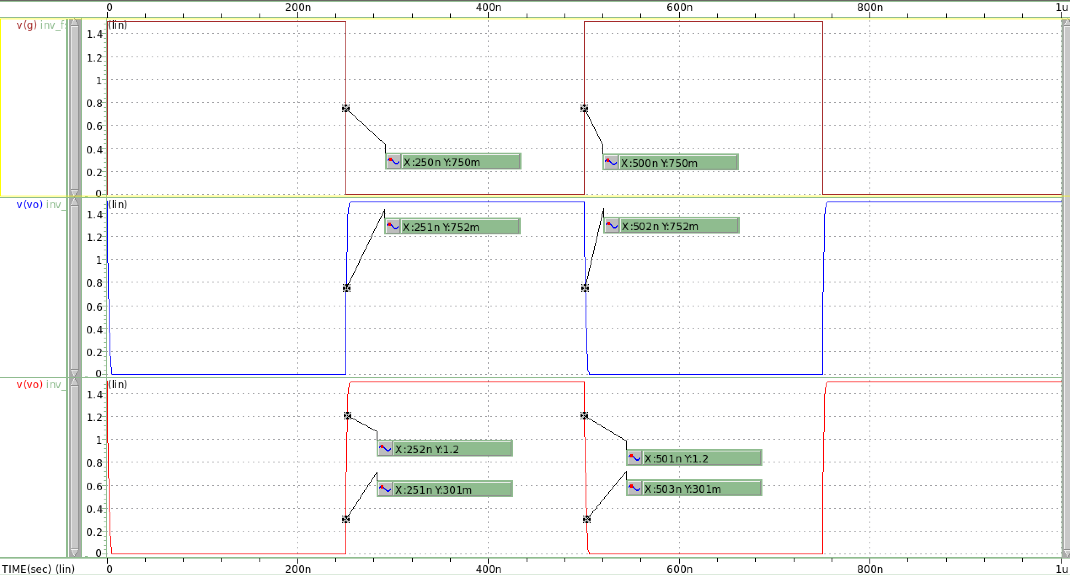


圖 16 FS Corner .tran simulation

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| INVERTER |  | | | | |
| Input | CLK@2MHZ | | | | |
| Corner | TT | SS | FF | SF | FS |
| tPHL | 2ns | 3ns | 1ns | 3ns | 2ns |
| tPLH | 1ns | 3ns | 1ns | 4ns | 1ns |
| tr | 1ns | 3ns | 1ns | 6ns | 1ns |
| tf | 2ns | 4ns | 1ns | 4ns | 2ns |

Comment:

在分析TT Corner和SS Corner結果時，因本題nMOS size為題目給定，我推測是因pMOS的Width設計稍大，導致pull-up電流較大，使得rising time比falling time小。

而SF Corner理應是slow NMOS, fast PMOS,若兩個MOS symmetric，結果應該為rising time<falling time，但實際結果卻相反，推測是在設計PMOS size時，設計較小導致其pull-up電流不夠強。

在tPHL和tPLH部分可看到FF Corner的delay是最小的。這與理想符合，而FS和SF Corner都沒有比TT Corner延遲表現出色。

# Run the HSPICE simulation to answer the following question, use 𝑉𝐷𝐷 = 1.5𝑉.

### Please design five 2-input NAND gates (one for each corner) with (W/L)𝑛 = 3μm/0.2μm while (W/L)𝑝 is your design. (BOTH PMOS sizes should be same.) Connect the two input together to run the transfer curve (like Fig.1), the transition point should be 𝑉𝑂𝑈𝑇 = 0.5𝑉𝐷𝐷 @ 𝑉𝑖𝑛 = 0.5 𝑉𝐷𝐷 in 5 process corners. (TT, SS, FF, SF, FS).

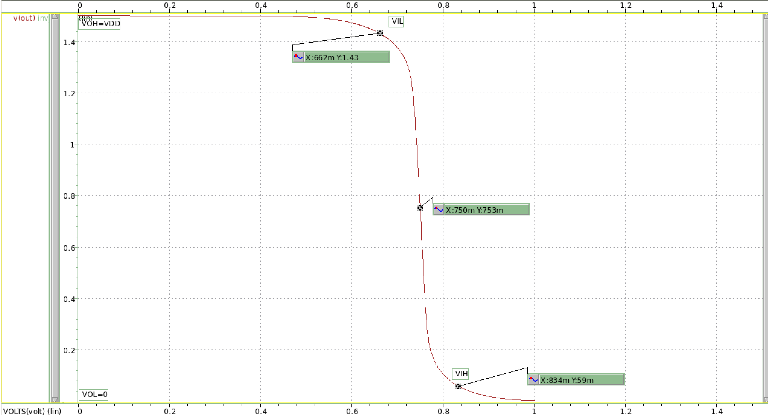


圖 17 TT Corner

W=2.86u,L=0.2u

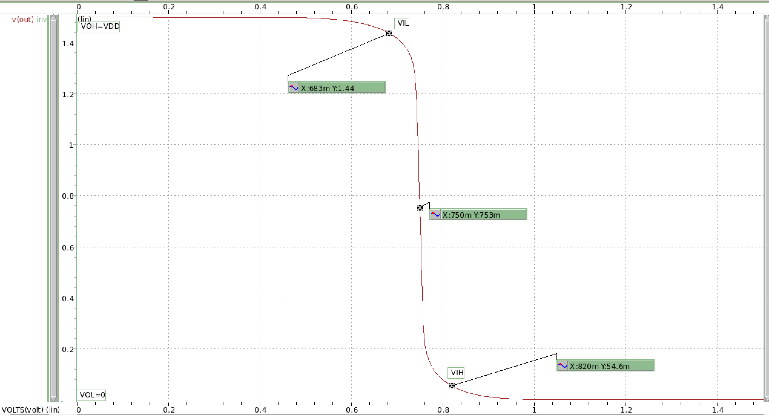


圖 18 SS Corner

W=2.99u,L=0.2u

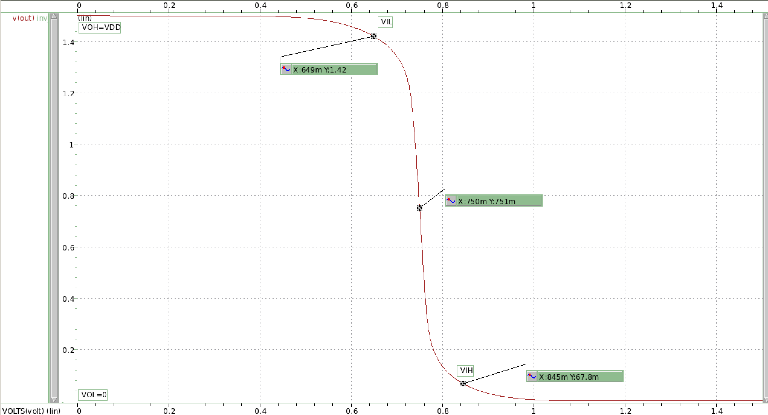


圖 19 FF Corner

W=2.79u,L=0.2u

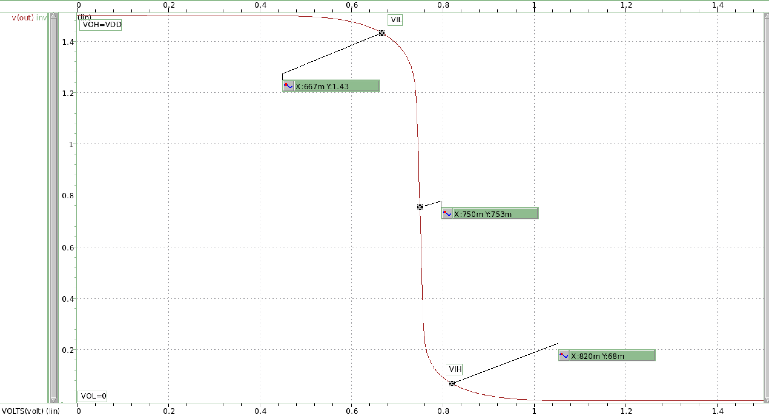


圖 20 SF Corner

W=0.7u,L=0.2u

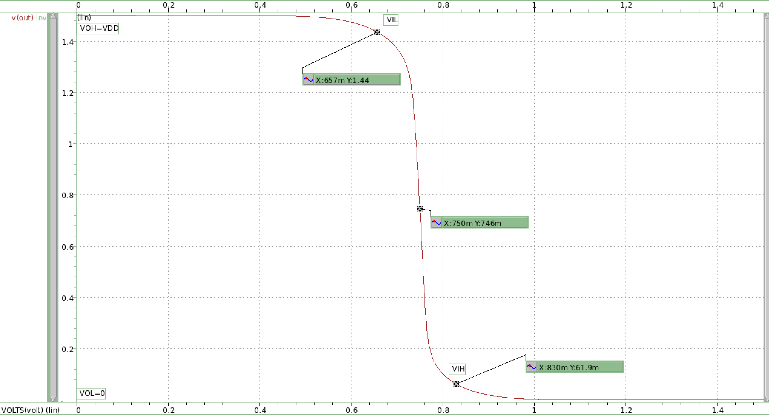


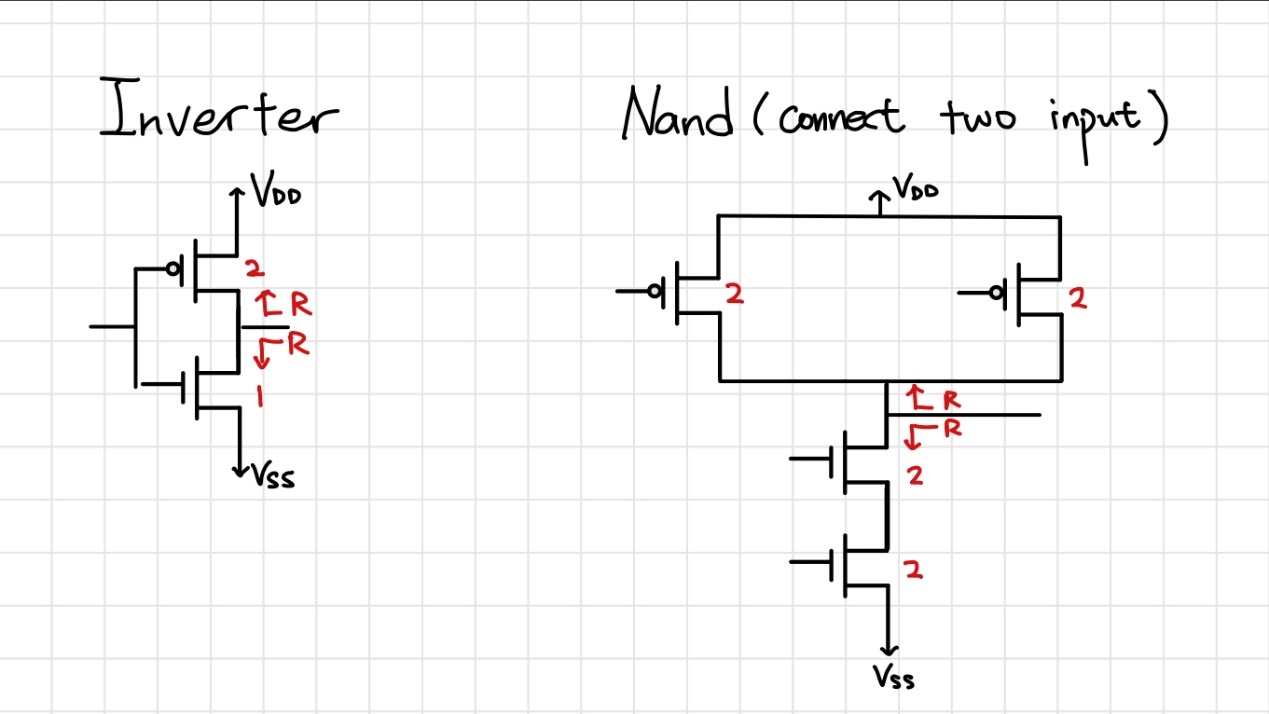
圖 21 FS Corner

W=2.95u,L=0.2u

### Using the transfer curve you simulated in (a), calculate the value of 𝑉𝐼𝐿,𝑉𝐼𝐻, 𝑉𝑂𝐿,𝑉𝑂𝐻 and 𝑁𝑀𝐻 and 𝑁𝑀𝐿 in 5 process corners. (TT, SS, FF, SF, FS).

|  |  |
| --- | --- |
| 圖 22 TT Corner | 圖 23 SS Corner |
| 圖 24 FF Corner | 圖 25 SF Corner |
| 圖 26 FS Corner | |

### What are the differences in (W/L)𝑝/(W/L)𝑛 between Q1(a) and Q2(a)? Please comment on the difference.



為使pull-up network and pull-down network symmetric, 在設計inverter電路時的MOS size與 2 input NAND會不同，從上圖大概計算一下path effort，得:

Inverter:F=GH=1

2 input NAND:F=GH=(4/3)\*2=8/3

故理論上2 input NAND delay會更嚴重。

### Using the 2-input NAND designed in (a) with 𝑉𝐷𝐷 = 1.5𝑉. Input signal (A or B) = 0V-1.5V@2MHz with rising time / falling time = 0.1ns and loading capacitor 𝐶𝑙𝑜𝑎𝑑 = 800𝑓𝐹 at output.

|  |  |
| --- | --- |
| CASE1(A:0-1.5@2MHZ,B:1.5) | CASE2(A:1.5,B:0-1.5@2MHZ) |
| 圖 27 TT Corner | 圖 28 TT Corner |
|  |  |
| 圖 29 SS Corner | 圖 30 SS Corner |
|  |  |
|  |  |

|  |  |
| --- | --- |
| CASE1(A:0-1.5@2MHZ,B:1.5) | CASE2(A:1.5,B:0-1.5@2MHZ) |
| 圖 31 FF Corner | 圖 32 FF Corner |
| 圖 33 SF Corner | 圖 34 SF Corner |
| 圖 35 FS Corner | 圖 36 FS Corner |

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| NAND2 | Case1 | | | | | Case2 | | | | |
| Input A | CLK@2MHZ | | | | | 1.5V | | | | |
| Input B | 1.5V | | | | | CLK@2MHZ | | | | |
| Corner | TT | SS | FF | SF | FS | TT | SS | FF | SF | FS |
| tPHL | 1ns | 2ns | 1ns | 2ns | 1ns | 1ns | 2ns | 1ns | 2ns | 1ns |
| tPLH | 2ns | 3ns | 2ns | 2ns | 2ns | 2ns | 3ns | 2ns | 5ns | 2ns |
| Tr | 2ns | 4ns | 2ns | 3ns | 2ns | 2ns | 4ns | 2ns | 8ns | 2ns |
| Tf | 2ns | 2ns | 1ns | 2ns | 2ns | 1ns | 2ns | 1ns | 2ns | 2ns |

一張含有 光, 黑色, 紅色, 交通號誌 的圖片

自動產生的描述

Comment:

表格數據最大差異是SF Corner，Case 2的rising time較長，推測是因為在畫transient schematic時，INPUT B因是時脈訊號，INPUT A是直流訊號(不存在延遲)而INPUT B是畫在下方的NMOS，距離輸出較遠，導致延遲較明顯。

好比有一台A車與B車要同時到達終點，而B較A慢，那當然是讓B靠近終點一點再一起出發會比較容易使得兩車同時抵達終點，而不是A車先抵達後還要等B車。

INPUT B在下方時，若為時脈訊號，將造成延遲

# Complete the layout and post-sim of Inverter in Q1 @ TT corner and 2-input NAND in Q2 @ TT corner.

#### Finish DRC and LVS verification. Paste the pictures of layout, DRC result and LVS result in your report.

INVERTER:

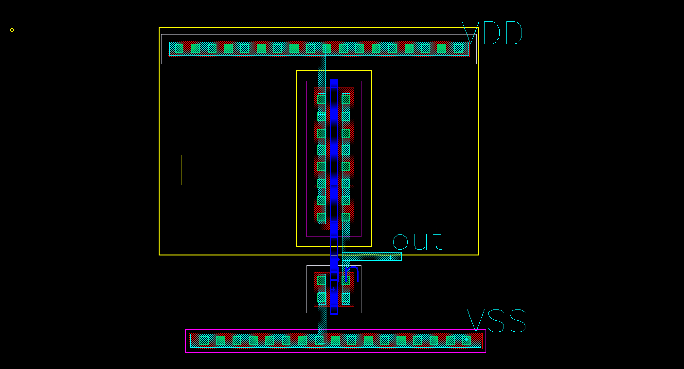


圖 37 Layout

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自動產生的描述

圖 38 DRC result

一張含有 文字 的圖片

自動產生的描述

圖 39 LVS result

2 INPUT NAND:

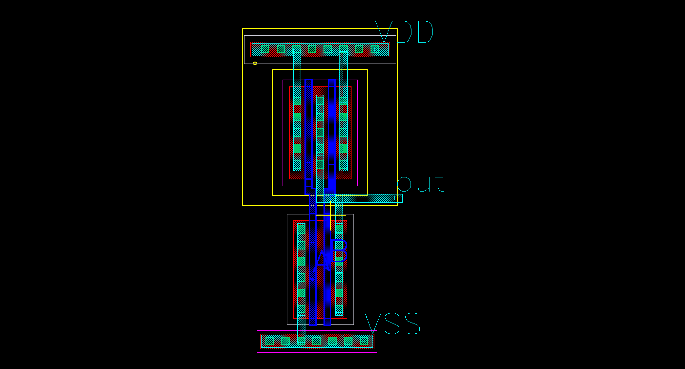


圖 40 Layout

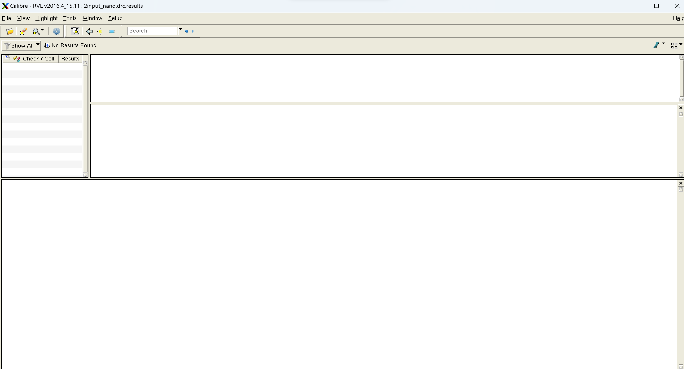


圖 41 DRC result



圖 42 LVS result

#### Run the post-layout simulation (post-sim) for Q1(c) and Q2(d) compare them with pre-layout simulation (pre-sim). Please comment on the differences.

|  |  |  |
| --- | --- | --- |
|  | Presim | Postsim |
| INVERTER |  |  |
| 2-INPUT NAND(CASE1) |  |  |
| 2-INPUT NAND(CASE2) |  |  |

COMMENT:

上圖對比可發現POSTSIM的輸出波型相較PRESIM往左移，推測是因POSTSIM加入了寄生參數，與實際工作情況更為貼近，但不論是inverter還是2 -input NAND，波形都與PRESIM時沒太大差異，仍是具有反向器功能的電路設計。