**國立清華大學**

**超大型積體電路設計VLSI Design**



**Homework 3**

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目錄

[1. Run an inverter buffer (out = 𝑖𝑛̅ ) with output loading 75pF with VDD = 1.8V, as shown in Fig 1. (The size of the first inverter has been assigned.) (the rising time and falling time of input is 0.01ns & input frequency = 5MHz). 3](#_Toc119674373)

[(a) Please find the unit inverter, calculate the g and p and use the parameter to calculate the optimum p with the simulation result and your normalization condition. 3](#_Toc119674374)

[(b) Please design the size and stage of the inverter chain to reach tpdf and tpdr < 1ns 5](#_Toc119674375)

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[(e) What is the difference between (c) and (d), and comment on it. 9](#_Toc119674380)

[(f) Change the output loading to 120pF, fix the stage of the inverter chain, and compare the simulated oscillation frequency between the different output loading. 10](#_Toc119674381)

[2. Please design a 3-to-8 decoder with output loading 300fF at each output node (as shown in Fig. 2) and try to add an inverter buffer to minimize the delay from input to output of the decoder. VDD = 1.8V, and the size of the first inverter has been assigned. 13](#_Toc119674382)

[(a) Describe how you design the inverter buffer and the other device size in detail. 13](#_Toc119674383)

[(b) Finish the layout(whole circuit, from “A” to “Out”), DRC, and LVS. Paste the photo of the layout, DRC result, and LVS result in your report. Please mark the length and width on the layout and calculate the area(𝑢𝑚2 ). 16](#_Toc119674384)

[(c) Run the post-layout simulation and compare it with the pre-sim. 17](#_Toc119674385)

# Run an inverter buffer (out = 𝑖𝑛̅ ) with output loading 75pF with VDD = 1.8V, as shown in Fig 1. (The size of the first inverter has been assigned.) (the rising time and falling time of input is 0.01ns & input frequency = 5MHz).

## Please find the unit inverter, calculate the g and p and use the parameter to calculate the optimum p with the simulation result and your normalization condition.

**UNIT INVERTER SIZE:**

|  |  |  |
| --- | --- | --- |
| **Unit inverter** | **W/L** | **m** |
| **PMOS** | 0.6u/0.2u | 3 |
| **NMOS** | 0.401u/0.2u | 1 |

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自動產生的描述

圖 1 unit inverter schematic

在選定unit inverter size時，有兩組size:

1. P:828n/200n,m=3;N:600n/200n,m=1
2. P:600n/200n,m=3;N:401n/200n,m=1

但第二組得到的g會比較小，故optimize delay時選擇第二組unit inverter較佳



圖 2 unit unverter transfer curve(β=1)

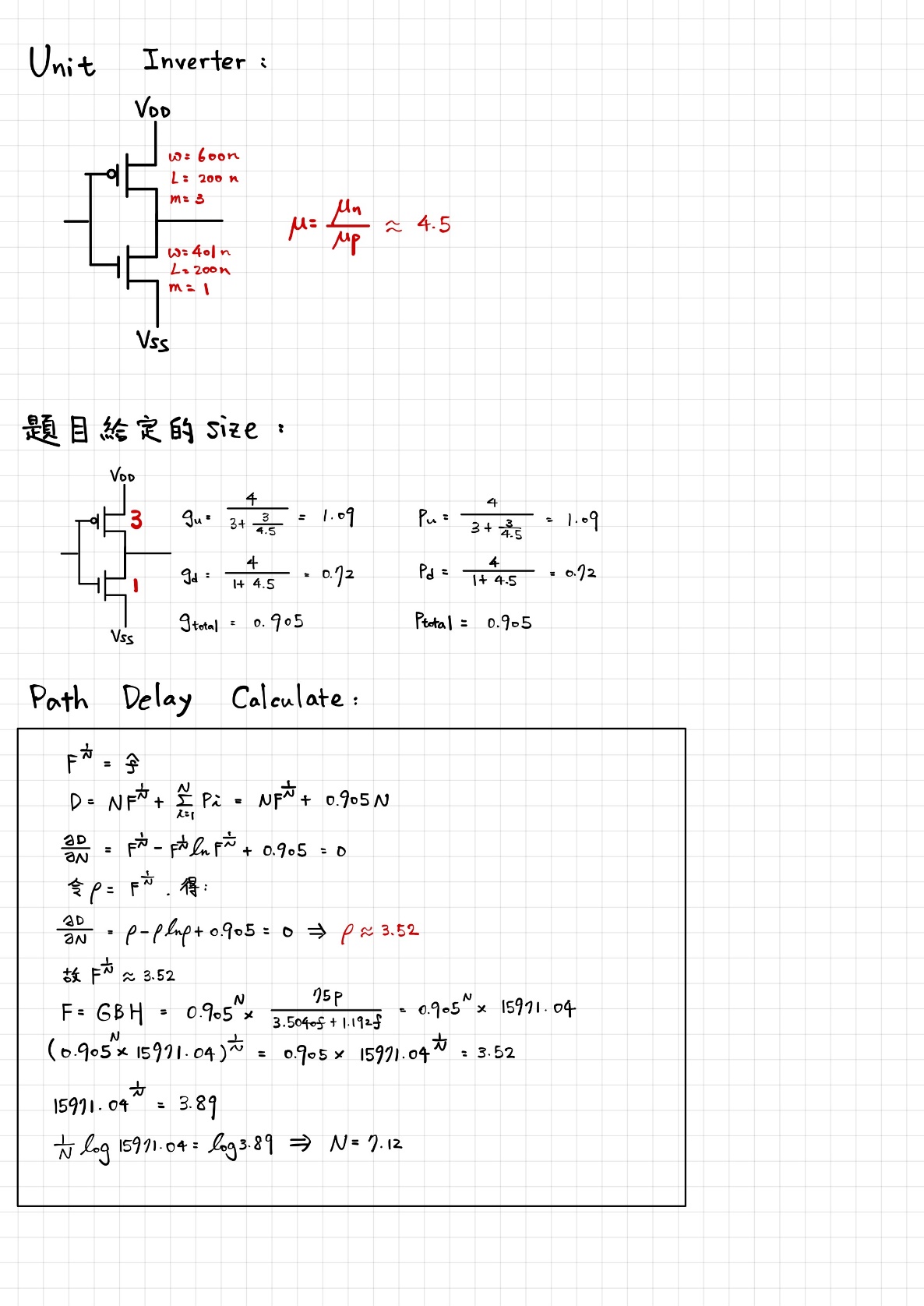
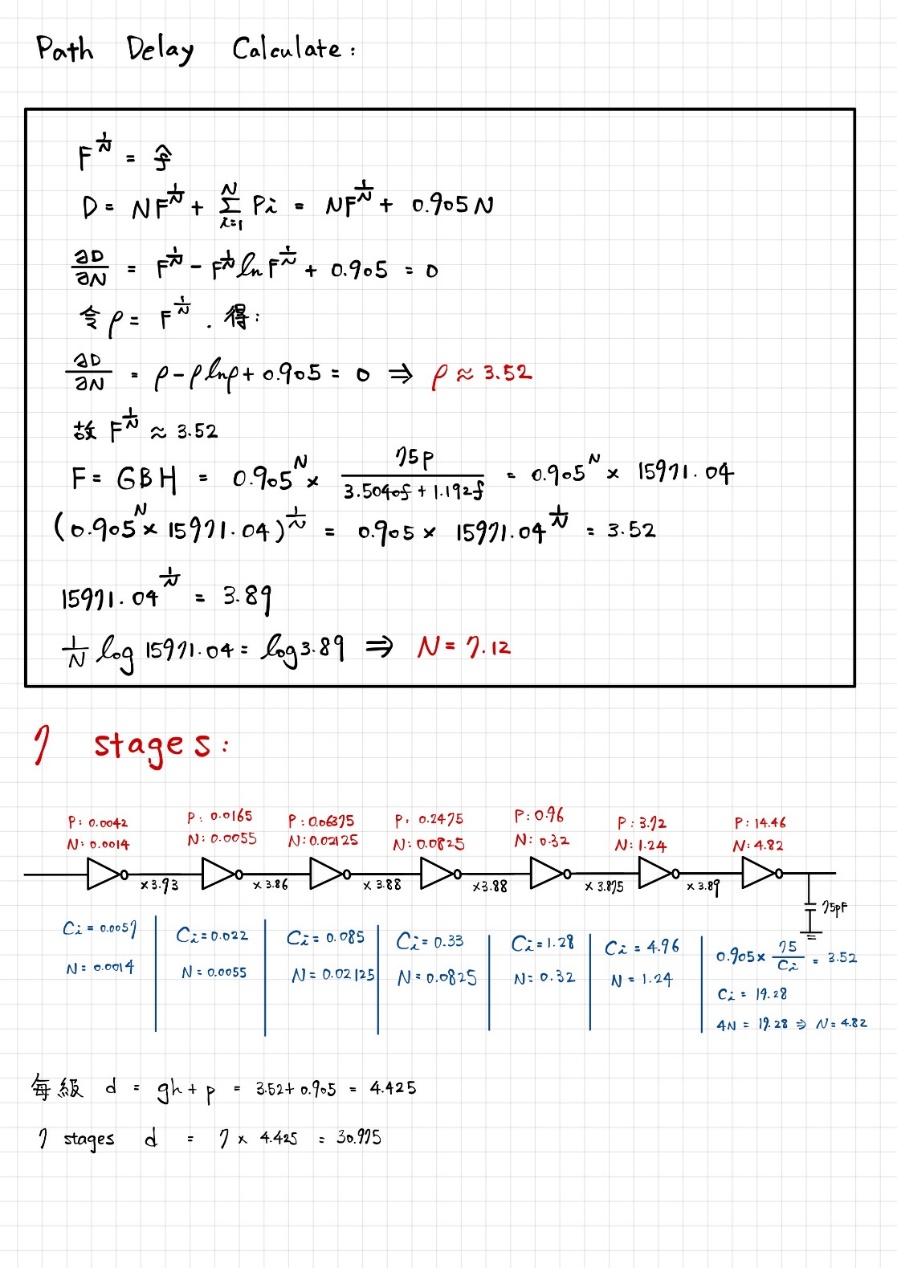


圖 3 g and p calculate

**g=0.905;p=0.905**

## Please design the size and stage of the inverter chain to reach tpdf and tpdr < 1ns



上方紅字**P,N size**並非真實的size，此計算過程只為了**得到stage之間的size放大倍率**，每級間放大倍率約莫落在3.8～3.9。而計算過程中的**H是題目給定的load capacitance與spice模擬出的(cgs+cgd)之比值。(Cin=Cgs+Cgd=4.696f)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Number of stage** | **Parasitic delay(p)** | **Effort delay(f=gh)** | **Stage delay(d=f+p)** | **Path delay** |
| **7** | **0.905** | **3.52** | **4.425** | **30.975** |

Part1—Schematic Design

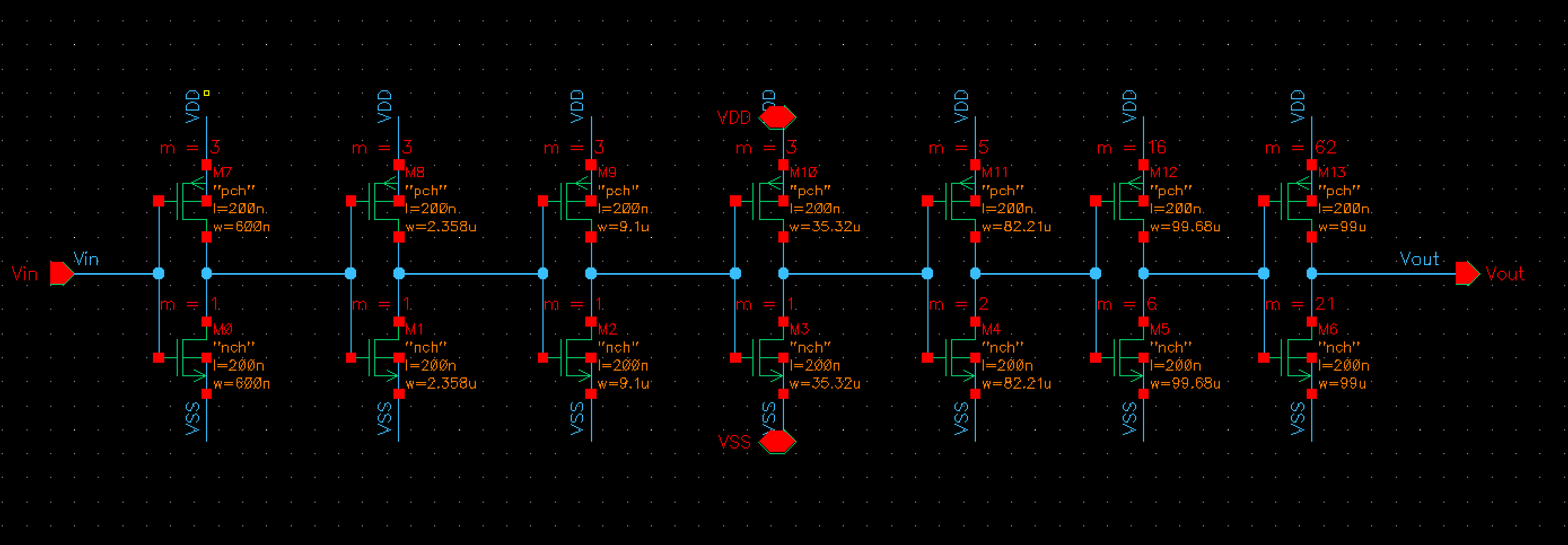


圖 4 inverter buffer schematic

**表格 1 NMOS stage size**

|  |  |  |
| --- | --- | --- |
| **NMOS** | **W(L=2um)** | **m** |
| **First stage** | 0.6u | 1 |
| **Second stage** | 2.358u | 1 |
| **Third stage** | 9.1u | 1 |
| **Fourth stage** | 35.32u | 1 |
| **Fifth stage** | 82.21u | 2 |
| **Sixth stage** | 99.68u | 6 |
| **Seventh stage** | 99u | 21 |

**表格 2 PMOS stage size**

|  |  |  |
| --- | --- | --- |
| **PMOS** | **W(L=2um)** | **m** |
| **First stage** | 0.6u | 3 |
| **Second stage** | 2.358u | 3 |
| **Third stage** | 9.1u | 3 |
| **Fourth stage** | 35.32u | 3 |
| **Fifth stage** | 82.21u | 5 |
| **Sixth stage** | 99.68u | 16 |
| **Seventh stage** | 99u | 62 |

Part2—Simulation and Waveview

數據定義:

Tpdf\_0.5VDD: **input@0.5VDD** to **falling output@0.5vdd** propagation delay

Tpdr\_0.5VDD: **input@0.5VDD** to **rising output@0.5vdd** propagation delay

Tpdf: **input@0.1VDD** to **falling output@0.1vdd** propagation delay

Tpdr: **input@0.9VDD** to **rising output@0.9vdd** propagation delay

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圖 5 propagation delay

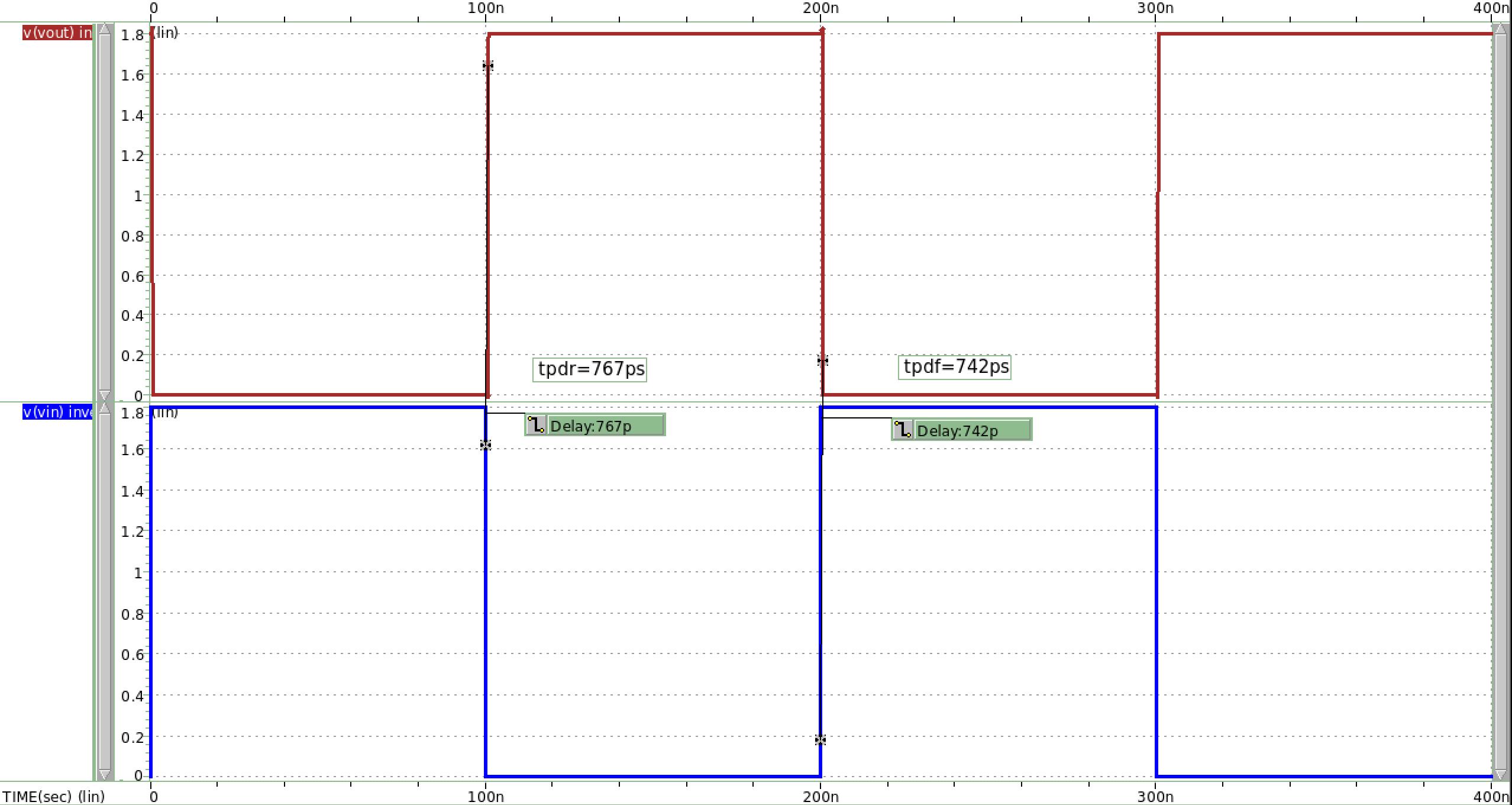


圖 6 output input waveview(.tran)

Tpdr=767ps;tpdf=742ps

**Propagation delay = = 754.5ps<0.1ns**

## Calculate the oscillation frequency based on the simulated parameters.

## Simulate the oscillation frequency

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自動產生的描述

圖 7 oscillation freq

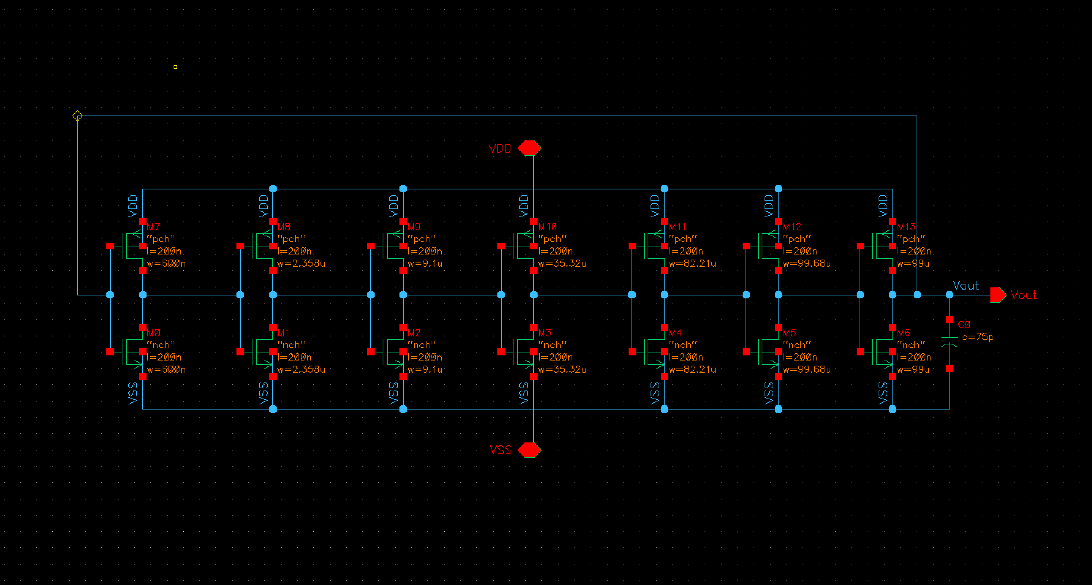


圖 8 oscillator schematic

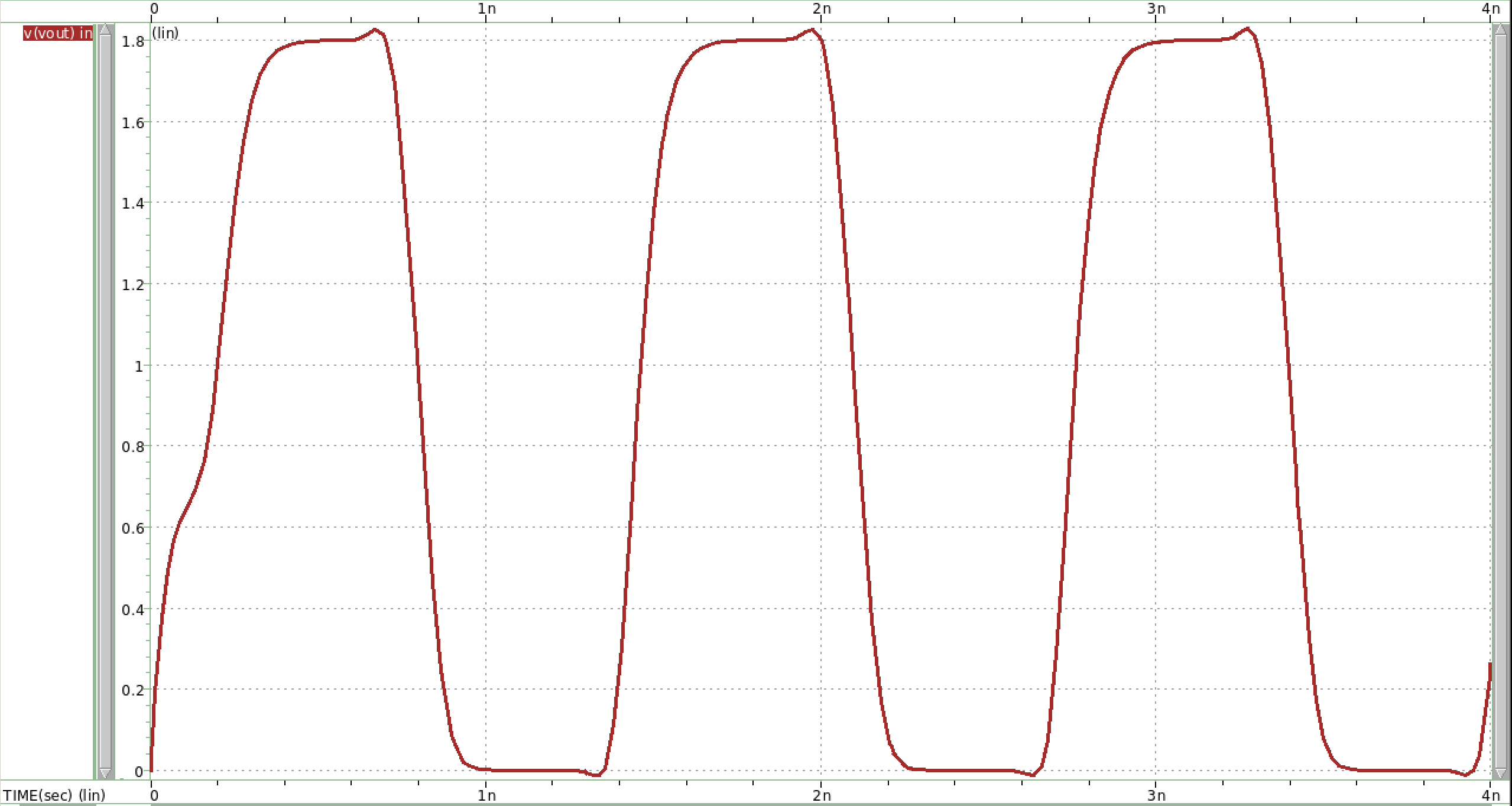


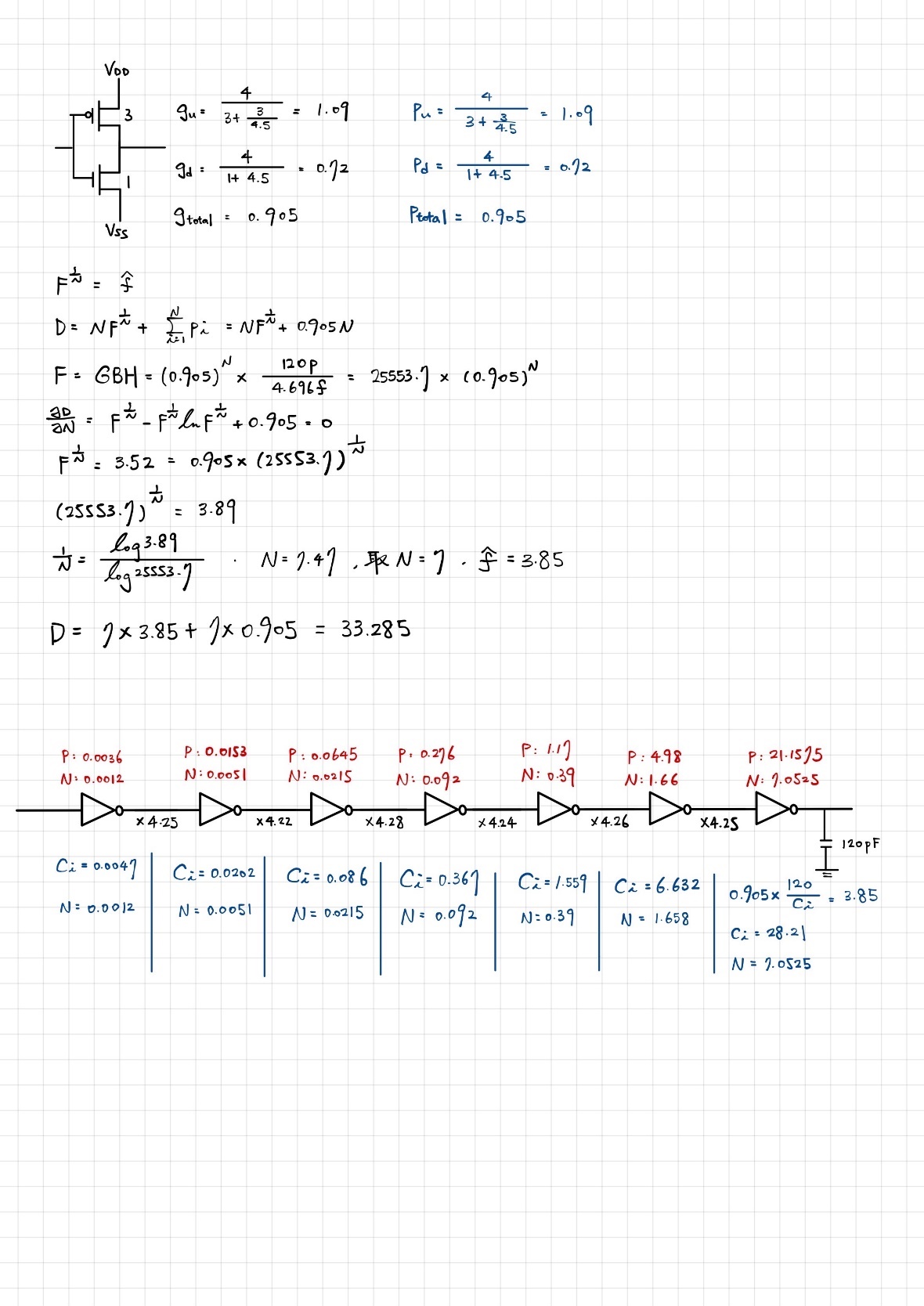
圖 9 oscillator waveview(.tran)

## What is the difference between (c) and (d), and comment on it.

本次作業tpdr和tpdf的定義較特別，分別定義在rising output=0.9VDD處和fallinf output=0.1VDD處，與都是0.5VDD處不同。

Simulation時，分別觀察兩組定義的結果，發現定義在0.5VDD處的delay較小，**而的d是定義在0.5VDD的propogation delay，在手算時，我是採用定義為0.5VDD之propagation delay計算**，所以c小題頻率會較d小題頻率小。

## Change the output loading to 120pF, fix the stage of the inverter chain, and compare the simulated oscillation frequency between the different output loading.



與(b)相同，此計算過程只為了**得到stage之間的size放大倍率**，每級間放大倍率約為4.25。而計算過程中的**H是題目給定的load capacitance與spice 模擬出的(cgs+cgd)之比值。(Cin=Cgs+Cgd=4.696f)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Number of stage** | **Parasitic delay(p)** | **Effort delay(f=gh)** | **Stage delay(d=f+p)** | **Path delay(D)** |
| **7** | **0.905** | **3.85** | **4.755** | **33.285** |

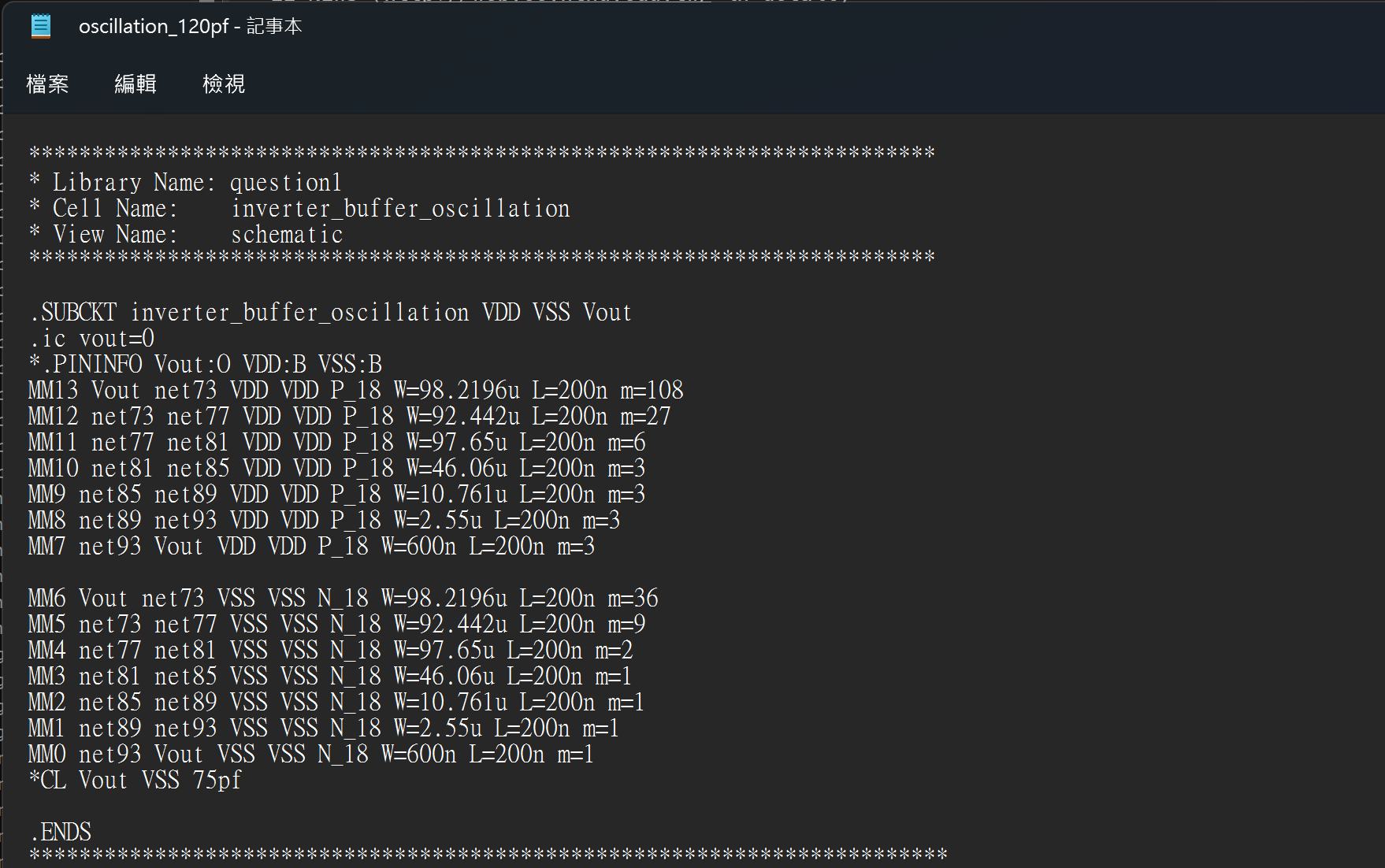


圖 10 CL=120pf oscillation sp file

**表格 3 NMOS stage size**

|  |  |  |
| --- | --- | --- |
| **NMOS** | **W(L=2um)** | **M** |
| **First stage** | 0.6u | 1 |
| **Second stage** | 2.55u | 1 |
| **Third stage** | 10.761u | 1 |
| **Fourth stage** | 46.06u | 1 |
| **Fifth stage** | 97.65u | 2 |
| **Sixth stage** | 92.442u | 9 |
| **Seventh stage** | 98.22u | 36 |

**表格 4 PMOS stage size**

|  |  |  |
| --- | --- | --- |
| **PMOS** | **W(L=2um)** | **m** |
| **First stage** | 0.6u | 3 |
| **Second stage** | 2.55u | 3 |
| **Third stage** | 10.761u | 3 |
| **Fourth stage** | 46.06u | 3 |
| **Fifth stage** | 97.65u | 6 |
| **Sixth stage** | 92.442u | 27 |
| **Seventh stage** | 98.22u | 108 |

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圖 11 oscillation 120pf frequency

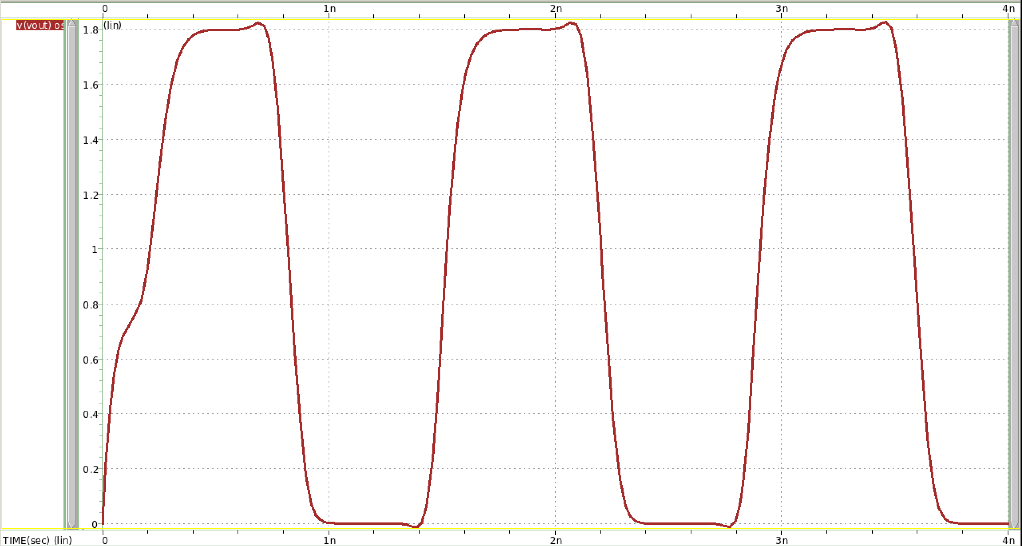


圖 12 CL=120pf oscillator waveview

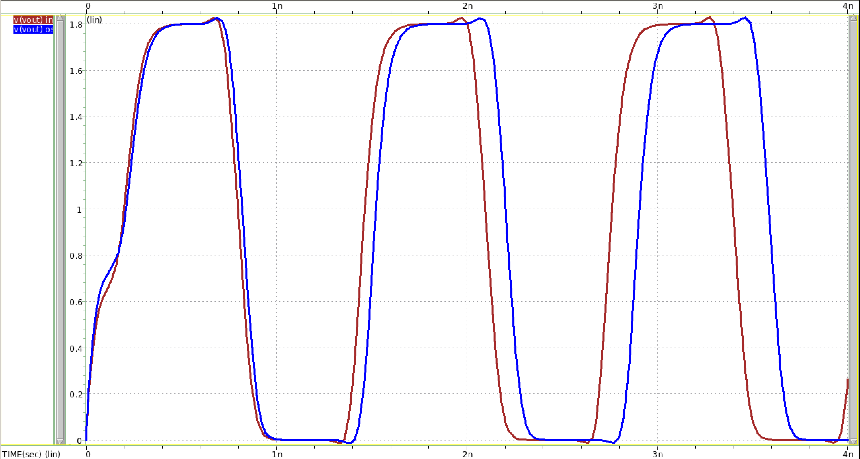


圖 13 compare between 75pf and 120pf oscillator

presim(紅) vs postsim(藍)

**Bigger load capacitance cause H being larger**.因為delay與H成正比，所以120pf當load capacitance會使propogation delay變大。

# Please design a 3-to-8 decoder with output loading 300fF at each output node (as shown in Fig. 2) and try to add an inverter buffer to minimize the delay from input to output of the decoder. VDD = 1.8V, and the size of the first inverter has been assigned.

#### Describe how you design the inverter buffer and the other device size in detail.

**Step1** :

hspice simulation，得到unit inverter size後，得到μ並計算題目給定first stage inverter的logic effort。

**Step2:**

利用上一步得到之μ，設計一個3 input nand，並計算logic effort。

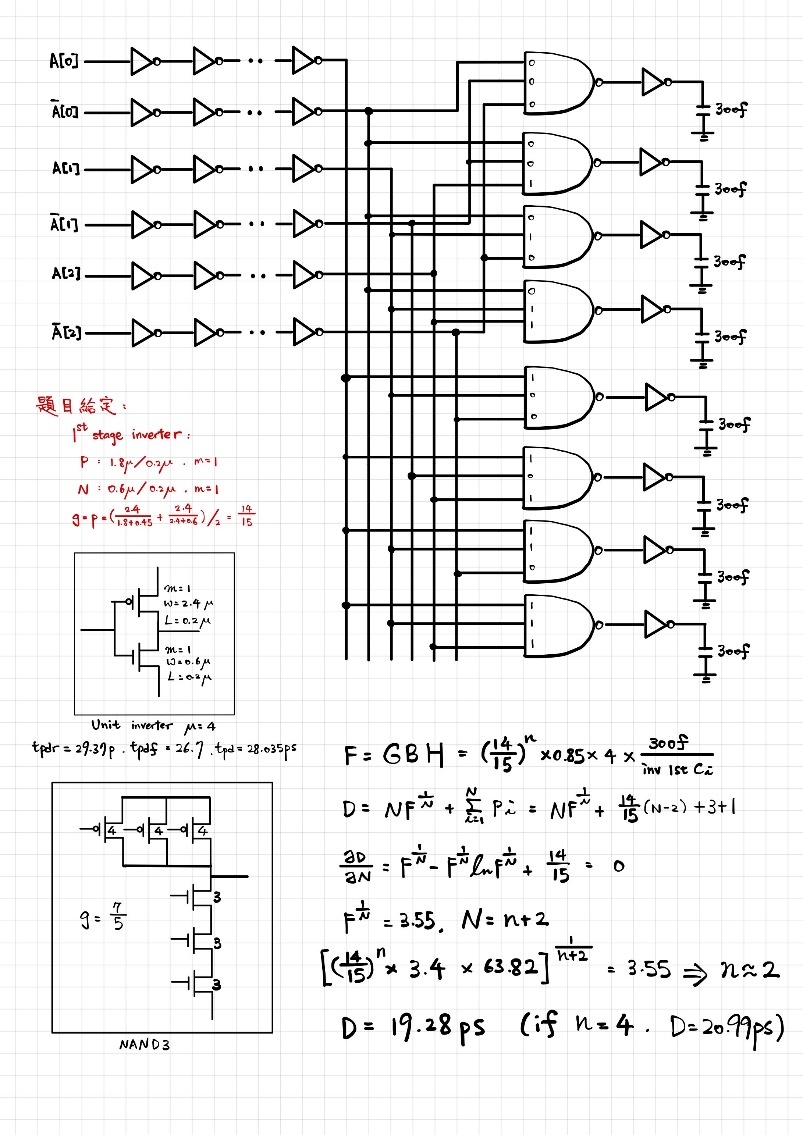
**Step3**:

題目給定之size，使整個inverter buffer的Wp/Wn比例固定為3，故也可利用μ計算出inverter buffer的logic effort。

**Step4**:

現在我們有inverter buffer、3 input nand的logic effort and parasitic delay，便可計算出Path effort，透過微分可得到最佳number of stage to minimum the delay。

(下頁有hand calculate過程)



透過實際simulation paramerter得到**N=2時會有最小delay**。

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 一張含有 文字, 黑色, 紅色, 光 的圖片  自動產生的描述  圖 14 unit inverter schematic |  |  |  |  | 一張含有 文字, 光, 紅色 的圖片  自動產生的描述  圖 15 3 input nand schematic |

|  |  |  |
| --- | --- | --- |
|  | **Unit inverter** | **3 input NAND** |
| **(W/L)p** | 2.4u/0.2u | 0.8u/0.2u |
| **(W/L)n** | 0.6u/0.2u | 0.6u/0.2u |

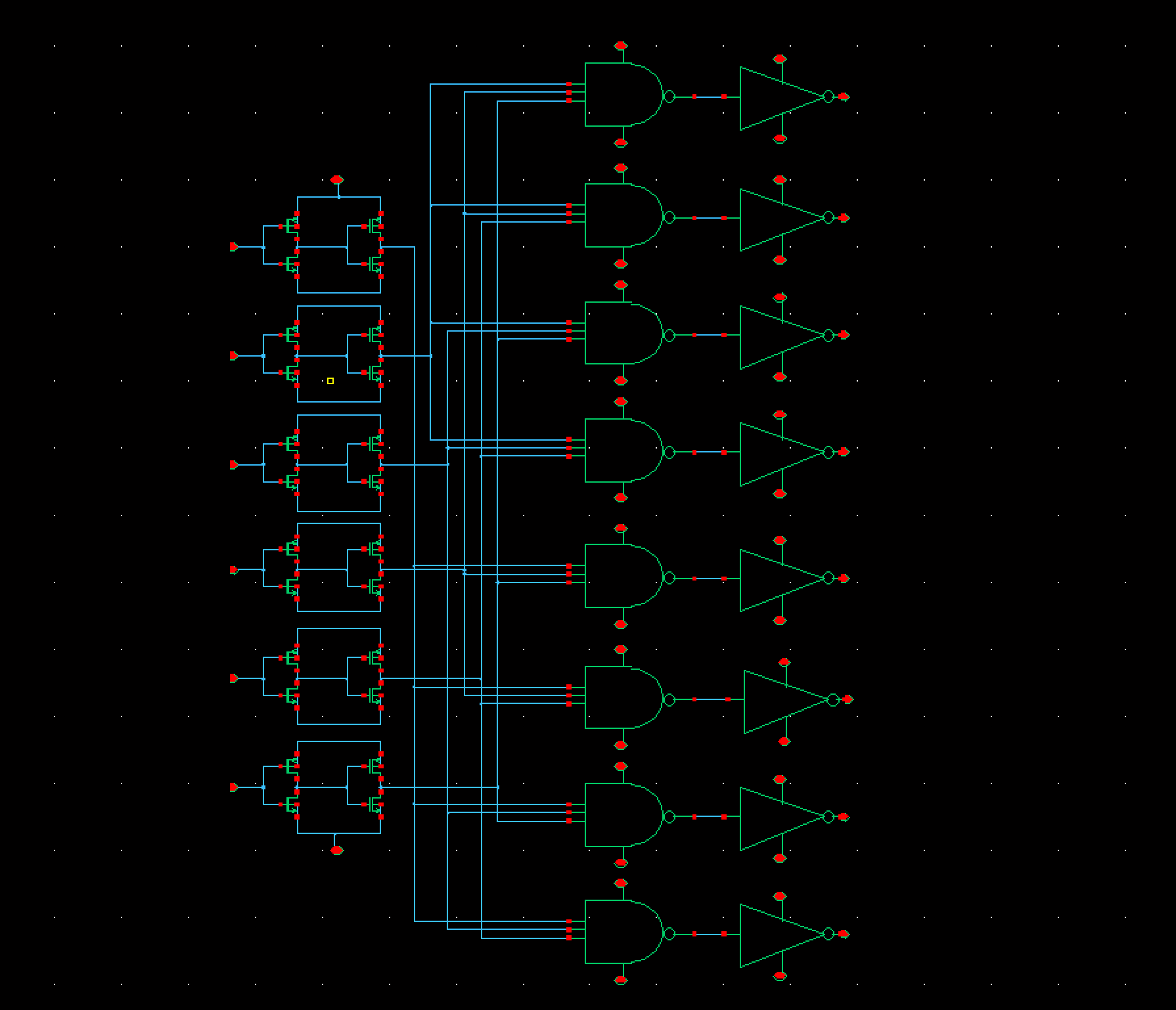


圖 16 3-8 decoder schematic

表格 5 each stage size

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **1st inverter** | **2nd inverter** | **Nand3** | **Unit inverter** |
| **(W/L)p\*m** | 1.8u/0.2u\*1 | 1.8u/0.2u\*4 | 0.8u/0.2u\*1 | 2.4u/0.2u\*1 |
| **(W/L)n\*m** | 0.6u/0.2u\*1 | 0.6u/0.2u\*4 | 0.6u/0.2u\*1 | 0.6u/0.2u\*1 |

#### Finish the layout(whole circuit, from “A” to “Out”), DRC, and LVS. Paste the photo of the layout, DRC result, and LVS result in your report. Please mark the length and width on the layout and calculate the area(𝑢𝑚2 ).

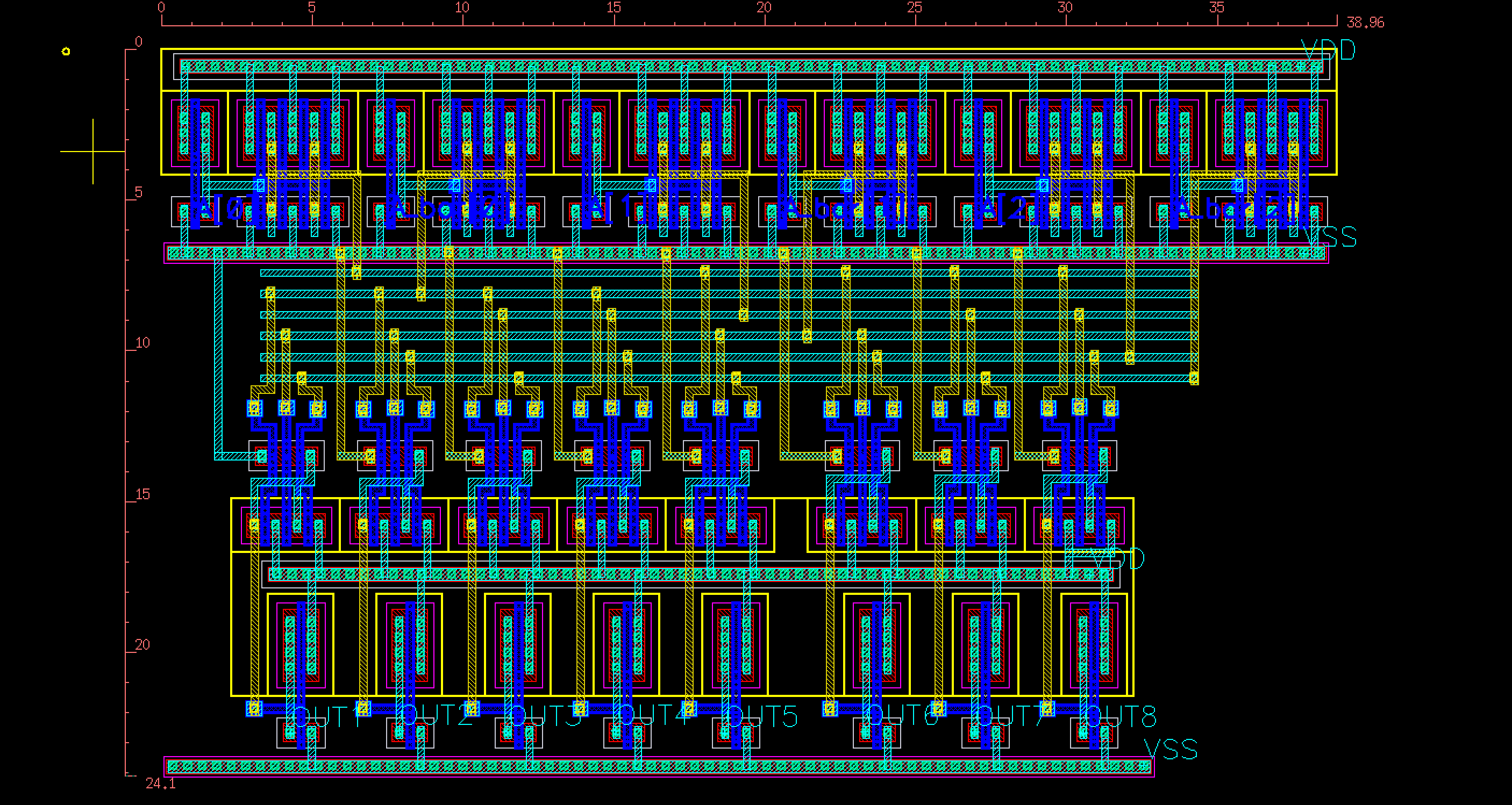


圖 17 3-8decoder layout

**用Distance計算後，layout面積為39.64\*24.565 = 973.7566μm^2**

|  |  |
| --- | --- |
| 圖 18 layout DRC result | 一張含有 桌 的圖片  自動產生的描述  圖 19 layout LVS result |

#### Run the post-layout simulation and compare it with the pre-sim.

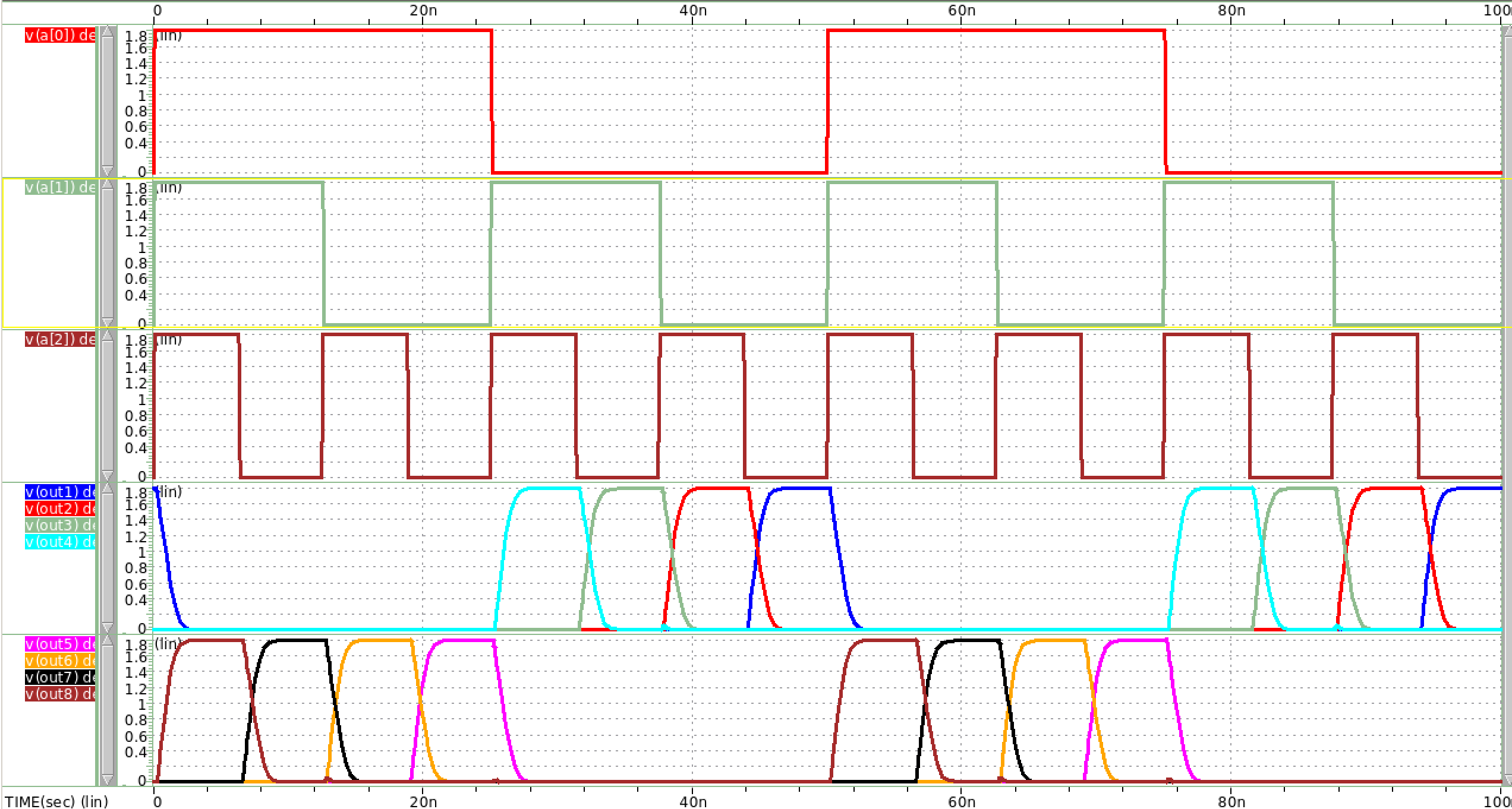


圖 20 presim waveview

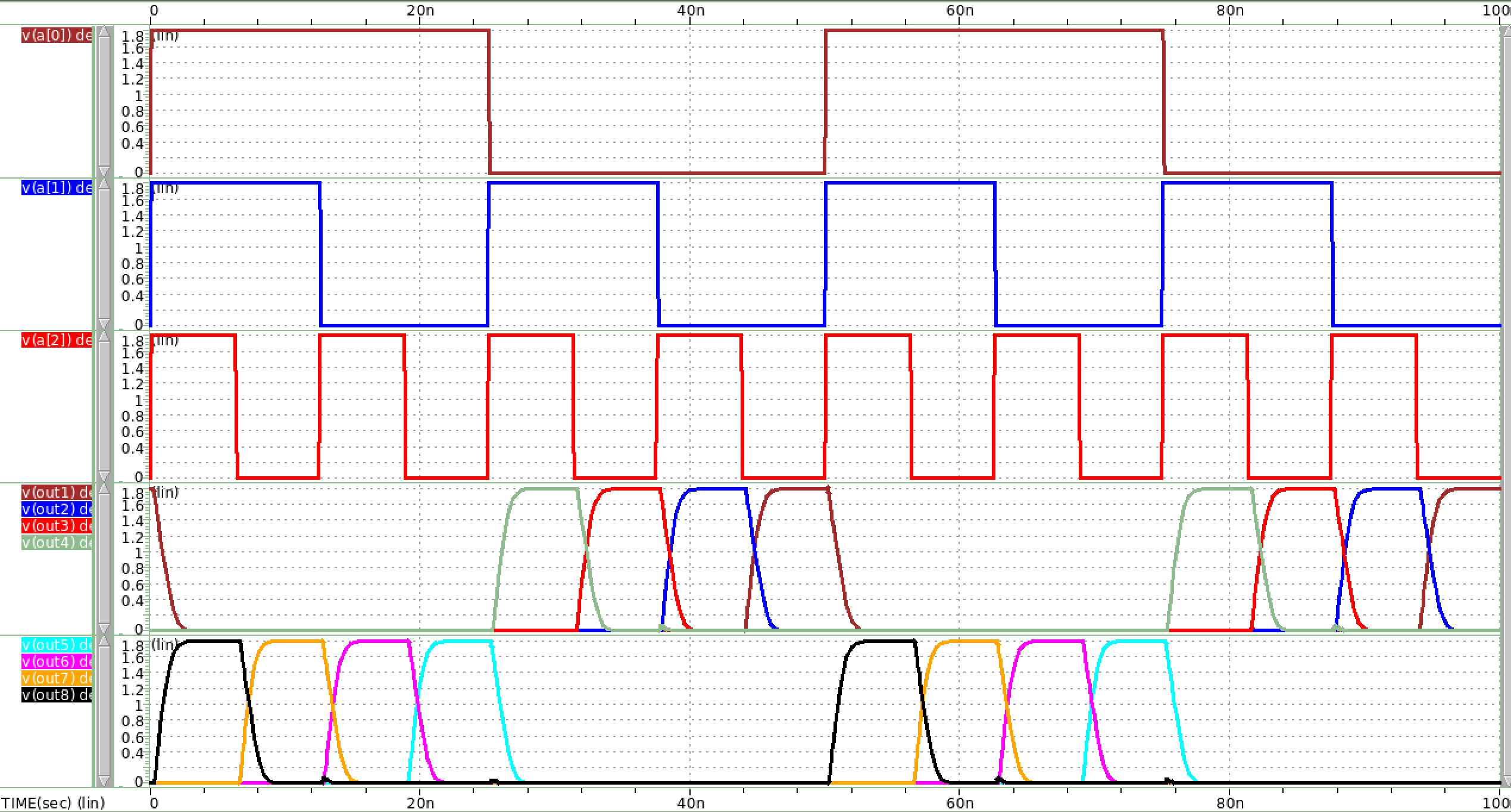


圖 21 postsim waveview

波形由上到下，分別為:

1. input A[0], is 0.01ns & input frequency = 20MHz
2. input A[1], is 0.01ns & input frequency = 40MHz
3. input A[2], is 0.01ns & input frequency = 80MHz
4. out1,out2,out3,out4(由左到右)
5. out5,out6,out7,out8,(由左到右)

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圖 22 presim(紅) vs postsim(藍)

**Postsim過後的波形(以out8為例)，delay較presim大。推測是因為postsim過後，更貼近實際情況，電容更多，導致每級的p略微提升，進而影響整體delay表現。**