**國立清華大學**

**超大型積體電路設計VLSI Design**



**Homework 5**

**學號:111063548**

**姓名:蕭方凱**

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[2. Please design a 3 bit pseudo-random-bit-sequence (PRBS) generator with Linear Feedback Shift Register (LFSR) with clock frequency CLK = 200MHz, VDD = 1.8V, VSS = 0V. Try to minimize the power consumption of the PRBS generator. 8](#_Toc122562859)

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# Please design a 4 bit binary synchronous up counter with clock frequency CLK = 200MHz, VDD = 1.8V (default) , VSS = 0V. You can use any architecture to complete the design. Try to minimize the power consumption of the counter. You can adjust the value of VDD for minimizing the power meanwhile the counter works correctly, and the maximum glitch should be less than 80ps.

## Please describe how you design the counter and how to reduce the glitch and power consumption of counter.

Counter Design

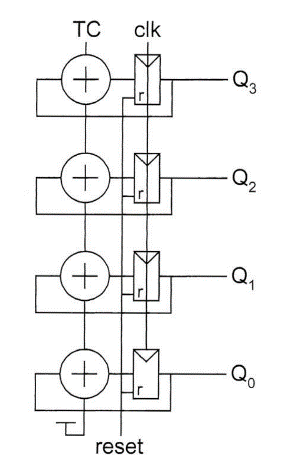
設計想法:

將一個一次只加1的電路(incrementer)與暫存器電路結合，即可實現counter計數器功能。概念圖如左下，其增值表如右下。

|  |  |
| --- | --- |
| 圖 1 synchronous counter | 圖 2 synchronous counter truth table |

實際設計電路:

參考講義上的synchronous counter，本次作業以下圖為實際設計電路。



此電路組成，左邊為half adder，提供carry bit 和sum bit，右邊則為D Flip-Flop，提供暫存功能，每個Flip-Flop一次暫存1 bit。

**Schematic :**

左下圖為4 bits synchronous up counter，其中DFF沿用上次作業的設計，half adder為右上圖，half adder內部的XOR gate則為左下圖。

|  |  |
| --- | --- |
| 一張含有 文字, 黑色, 光, 夜晚 的圖片  自動產生的描述  圖 3 4 bits synchronous up counter | 一張含有 文字, 光, 交通, 紅色 的圖片  自動產生的描述  圖 4 half adder |
| 一張含有 文字, 光, 室外, 夜晚 的圖片  自動產生的描述  圖 5 XOR gate |

設計完成後，模擬結果如下:

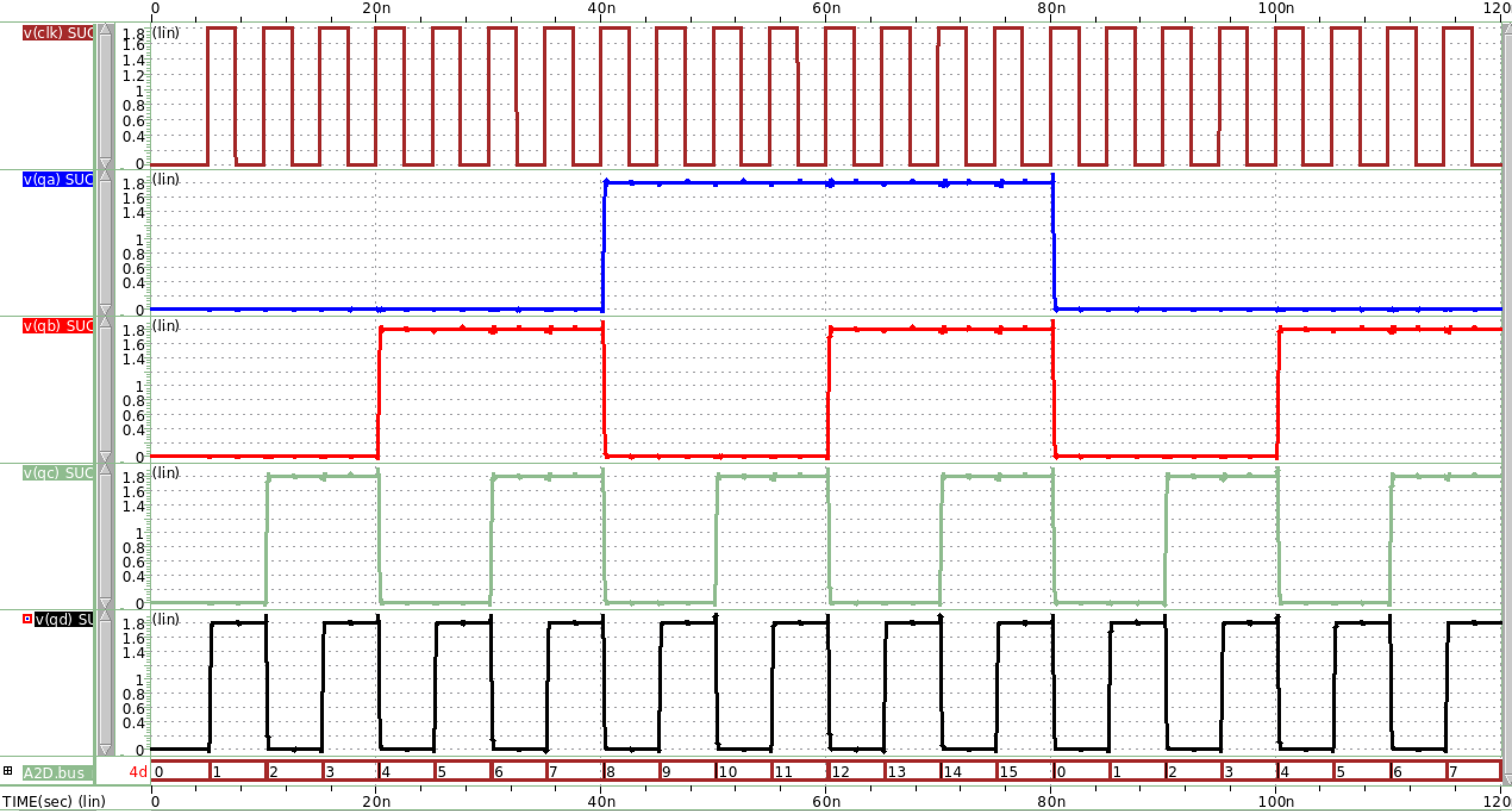


圖 6 4 bits synchronous up counter waveview

一張含有 文字 的圖片

自動產生的描述

Glitch皆發生在odd number to even number之間，從truth table可以解釋此現象，因1 to 2(0001 →0010)、3 to 4(0011 →0100)、 5 to 6(0101 →0110)…等，皆不只一個bit轉態，且每個bit轉態時間不同，導致glitch現象(1 to 2中間出現3、3 to 4 中間出現7…等)。

Glitch and power consumption reducing way

1. Reduce power consumption的方法:

降低transistor size。將transistor size(以unit inverter為例)設為

pmos width=0.6μm;nmos width=0.3μm。模擬後如下:

一張含有 文字 的圖片

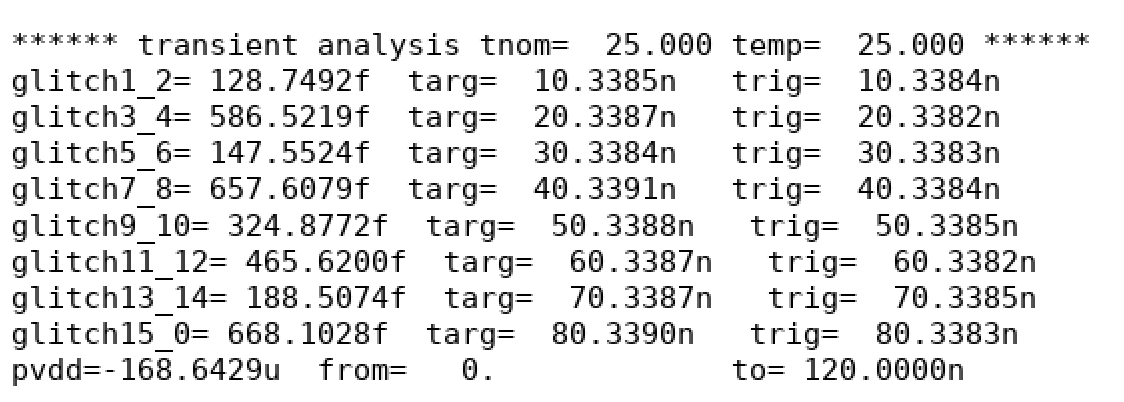
自動產生的描述

**Power consumption=127.9μ;**

Power consumption從原本的412.4095μ降低到127.9099μ，但glitch增加了，因glitch發生的原因是current state 轉態時間(falling time)與next state轉態時間(rising time)存在delay。

1. Glitch reduce:

因glitch發生的原因是current state 轉態時間(falling time)與next state轉態時間(rising time)存在delay。故要降低glitch time須提高pull down network的能力(reduce falling time)，將nmos width增加即可做到。我將XOR gate 的nmos width=1.25μm，其餘不變，模擬結果如下:



Glitch降至femto等級，雖然power consumption有略微上升，但仍比最一開始設計時表現還佳。

## Please list the glitch in each number (0 ~ 15) and find the maximum glitch.

|  |  |  |
| --- | --- | --- |
| Number to number | Glitch Value | Glitch Time |
| 0-1 | NA | 0s |
| 1-2 | 3 | 128.75fs |
| 2-3 | NA | 0s |
| 3-4 | 7 | 586.52fs |
| 4-5 | NA | 0s |
| 5-6 | 7 | 147.55fs |
| 6-7 | NA | 0s |
| 7-8 | 15 | 657.61fs |
| 8-9 | NA | 0s |
| 9-10 | 11 | 324.88fs |
| 10-11 | NA | 0s |
| 11-12 | 15 | 465.62fs |
| 12-13 | NA | 0s |
| 13-14 | 15 | 188.51fs |
| 14-15 | NA | 0s |
| 16-0 | NA | 668.1fs |
| **Maximum Glitch** | | |
| **668.1fs** | | |

## Please measure the power of the counter.

一張含有 文字 的圖片

自動產生的描述

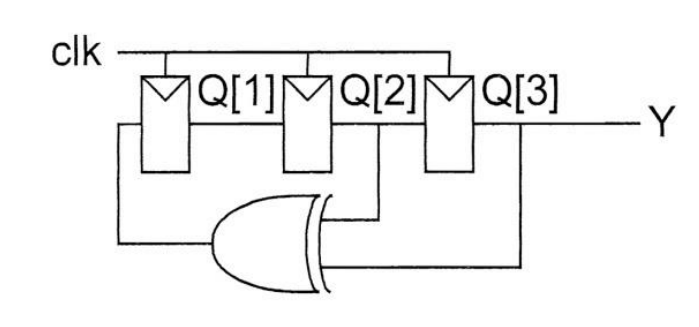
**Power consumption=168.6429μW**

# Please design a 3 bit pseudo-random-bit-sequence (PRBS) generator with Linear Feedback Shift Register (LFSR) with clock frequency CLK = 200MHz, VDD = 1.8V, VSS = 0V. Try to minimize the power consumption of the PRBS generator.

#### Please describe how you design the PRBS generator and show the pseudo-random sequence result to prove your design.

PRBS Design

參考講義上pseudo-random sequence的電路如下:



其Q[1]、Q[2]、Q[3]會依照下表進行循環:

一張含有 桌 的圖片

自動產生的描述

題目要求設計3 bits的pseudo random bit sequence，完成此功能之電路，需要三個Flip-Flop提供暫存功能及一個XOR gate，因本題為3 bits，對應到的characteristics polynomial 為1+x2+x3，故設計電路時，須將第二個Flip-Flop的輸出與第三個Flip-Flop的輸出作為XOR gate的輸入。

實際設計電路:

沿用上次作業的master slave based ET DFF作為提供暫存器功能的電路，以及上題採用的XOR gate，完成3 bits pseudo random bit sequence的電路設計。

**Schematic :**

一張含有 文字, 光, 室外, 交通 的圖片

自動產生的描述

圖 7 3 bit pseudo-random-bit-sequence (PRBS) generator

模擬結果如下:

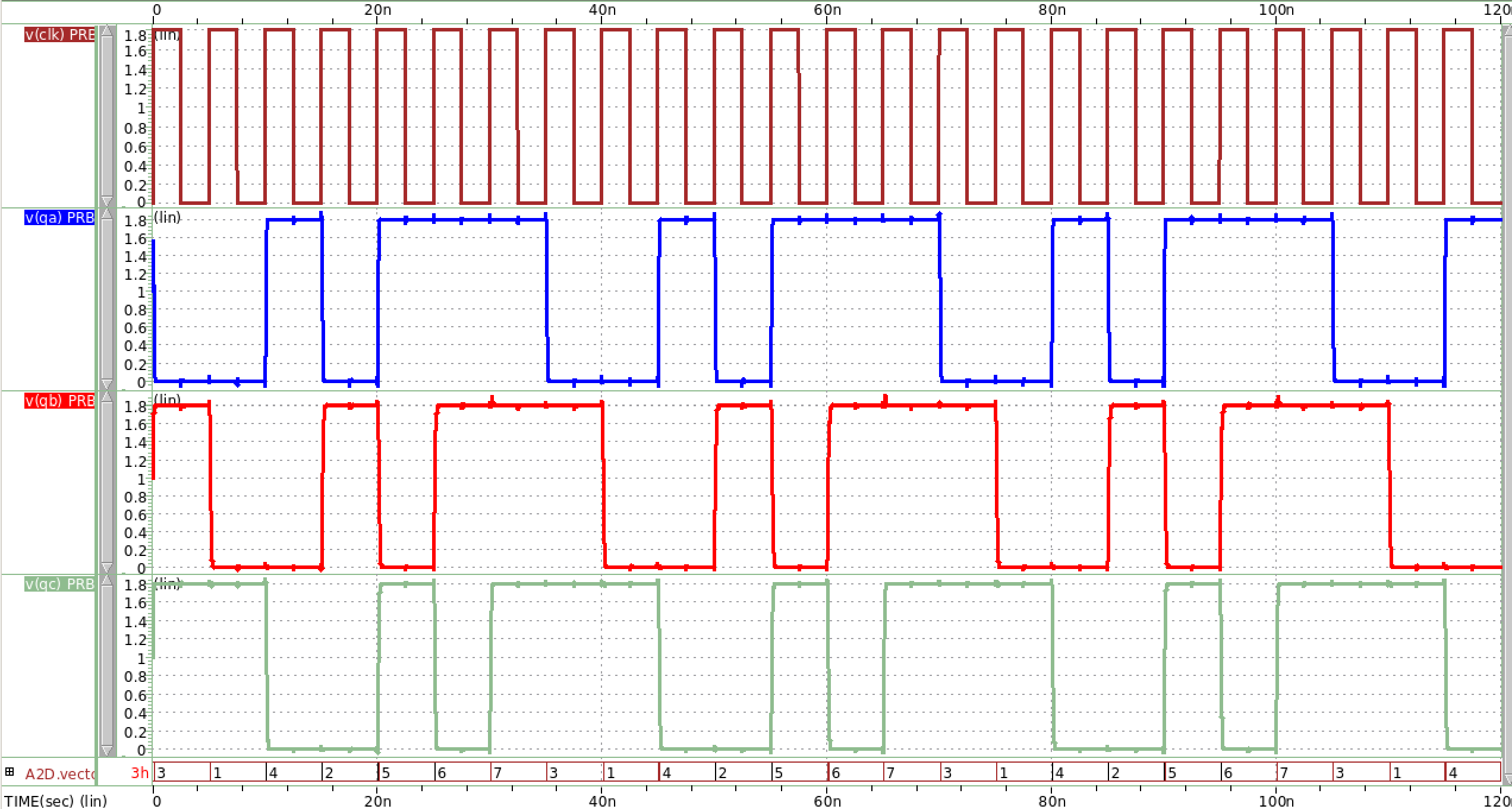
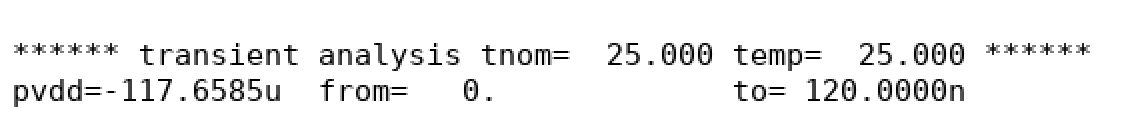


圖 8 pseudo random bit sequence waveview

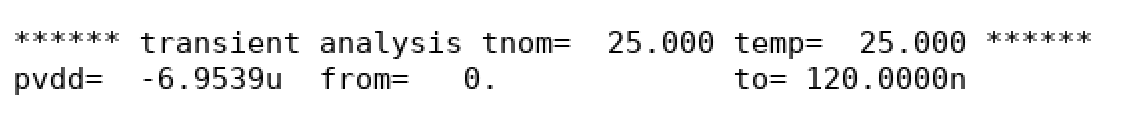
The way to minimize the power

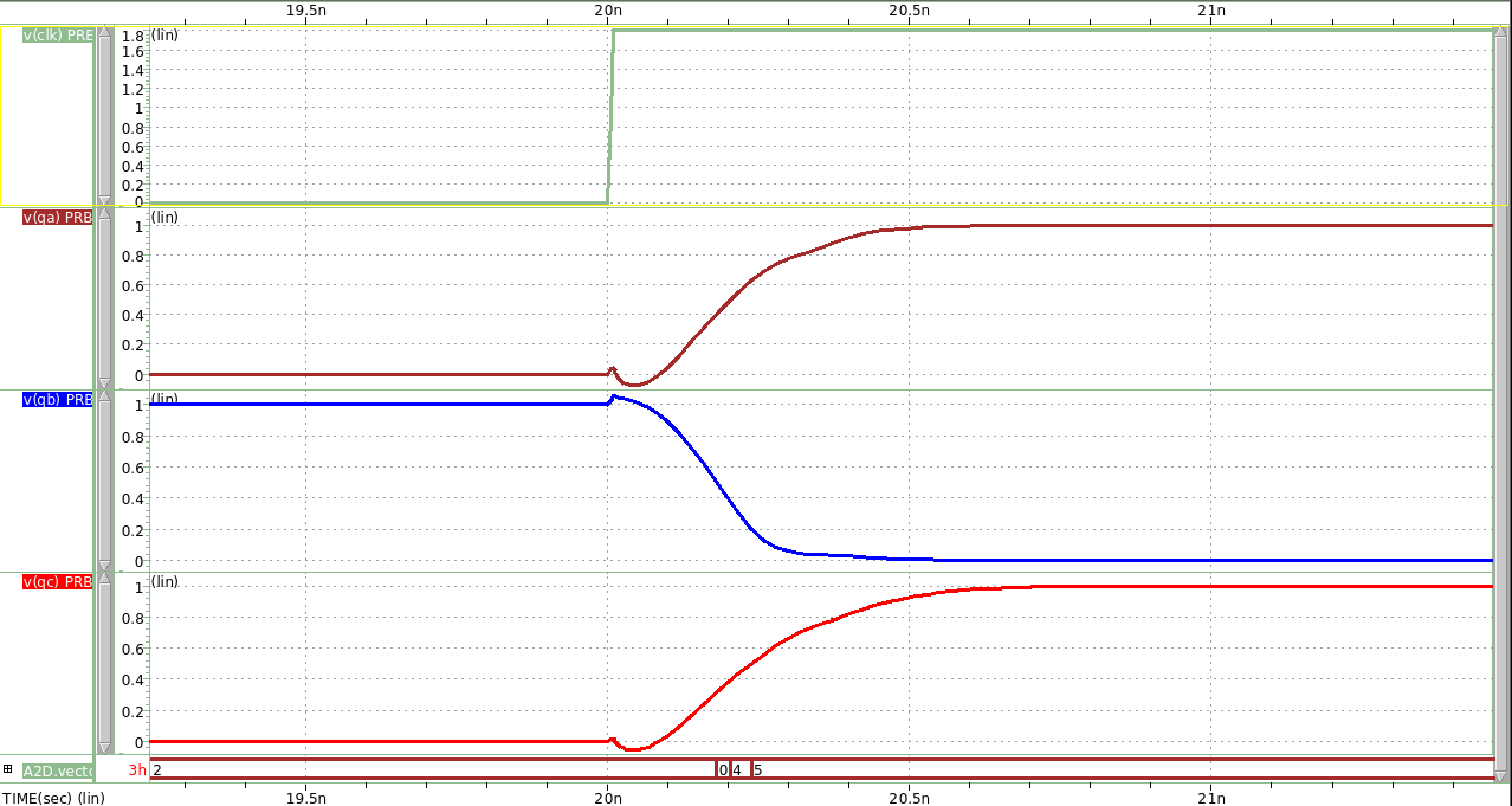
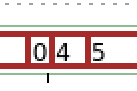
設計3 bits的pseudo random bit sequence的mos parameter，原先採用的mos大小為nmos width=1μm，pmos width=2μm進行設計，模擬後得到的power consumption如下:



1. 方法一:降低VDD

將VDD從1.8V降至1V，模擬結果如下:

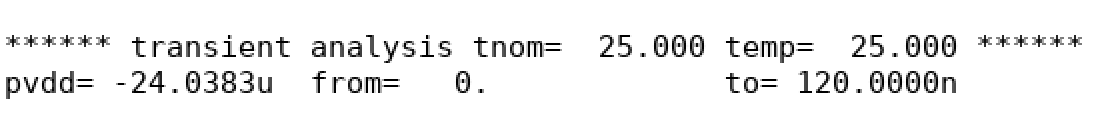




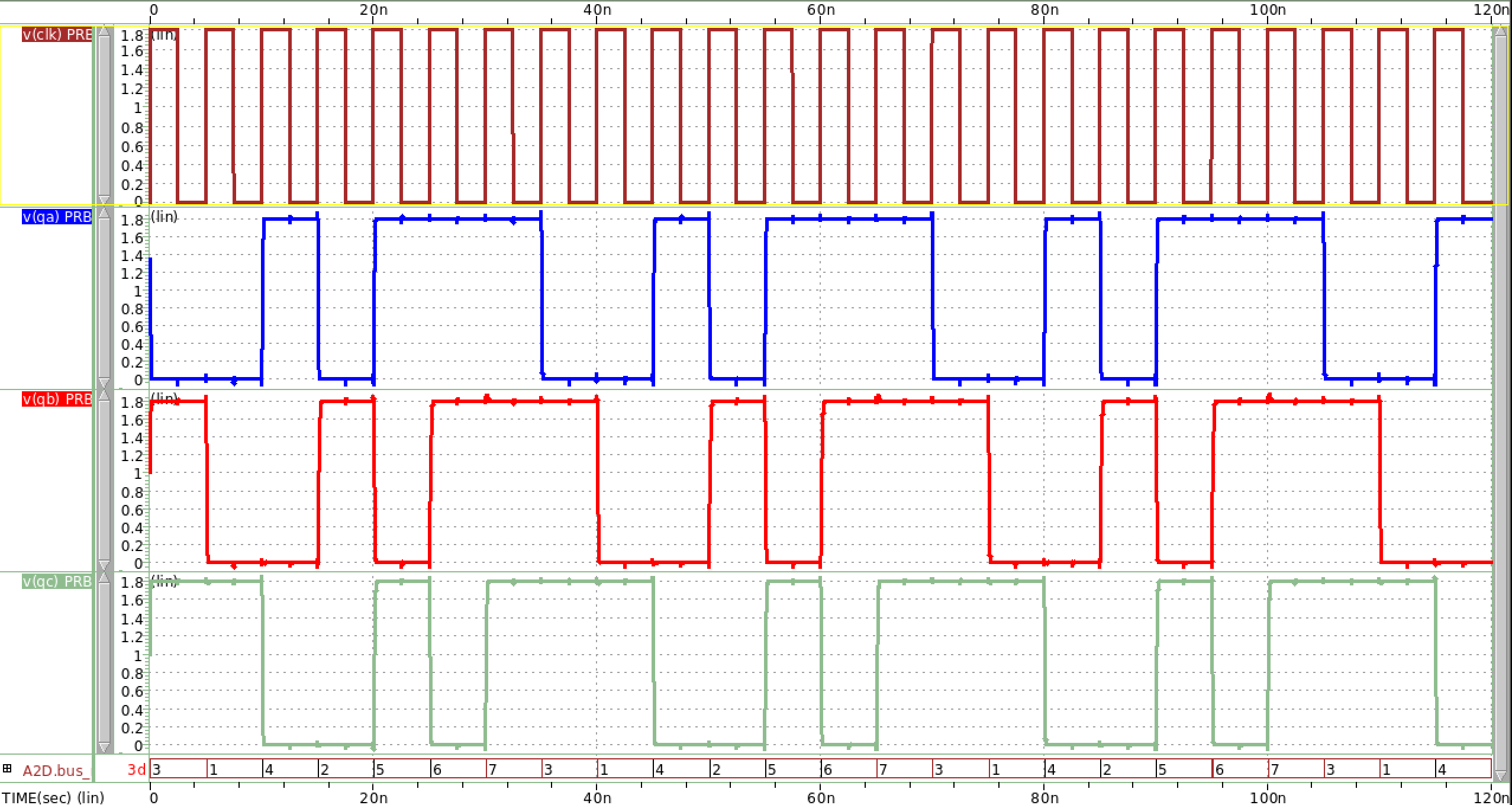
雖然power consumption降低到非常小，但電路的glitch更大，超過80ps，固本題不採用降低VDD的方法去降低power consumption。

1. 方法二:降低mos size

將整體mos size降低，nmos width=0.25μm，pmos width=0.3μm，得到的power consumption如下:



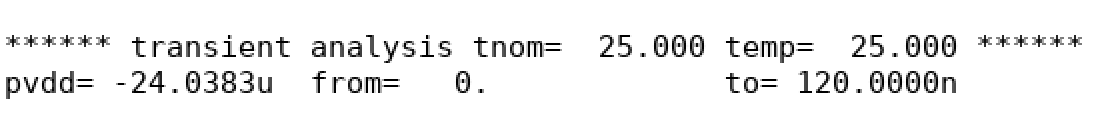
電路功能也可正常運作:



**結論:**

**雖然降低VDD會得到更好的功耗表現，但也影響電路功能，而調低mos size雖然沒有比直接調整VDD來的更有成效，但仍可明顯降低power consumption。**

#### Please measure the power of the PRBS generator.



**Power consumption=24.0483μW**