

1. Description

1.1. Project

Project Name	Nucleo-F401_Code
Board Name	NUCLEO-F401RE
Generated with:	STM32CubeMX 6.2.0
Date	03/22/2021

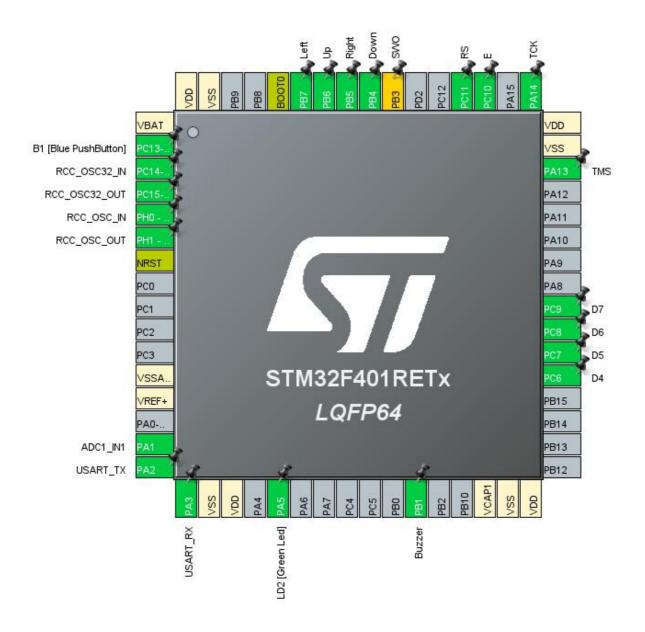
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F401
MCU name	STM32F401RETx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration



3. Pins Configuration

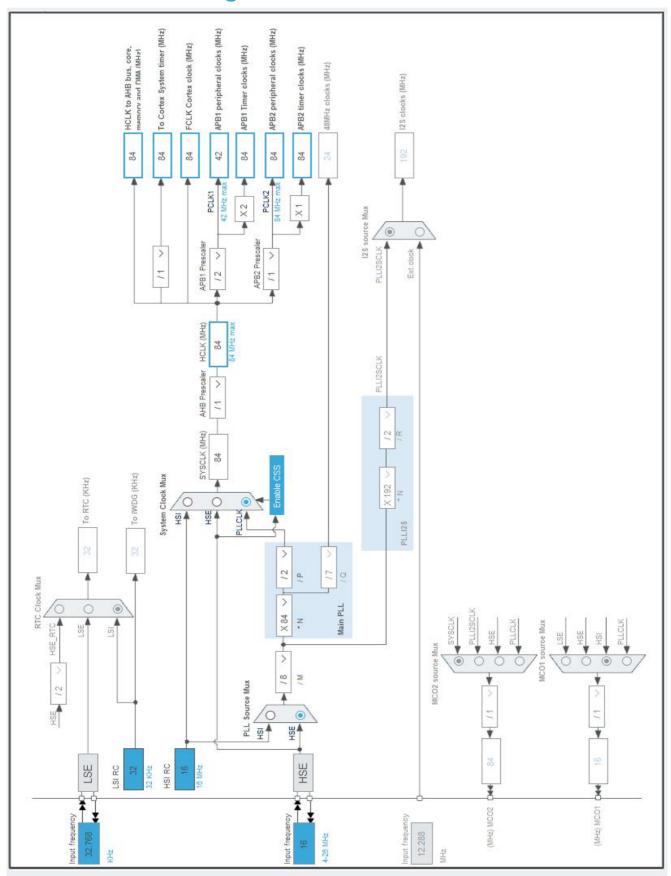
Pin Number LQFP64	Pin Name (function after	Pin Type	Alternate Function(s)	Label
LQII 04	reset)		i dilotion(3)	
1	VBAT	Power		
2	PC13-ANTI_TAMP	I/O	GPIO_EXTI13	B1 [Blue PushButton]
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PH0 - OSC_IN	I/O	RCC_OSC_IN	
6	PH1 - OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
12	VSSA/VREF-	Power		
13	VREF+	Power		
15	PA1	I/O	ADC1_IN1	
16	PA2	I/O	USART2_TX	USART_TX
17	PA3	I/O	USART2_RX	USART_RX
18	VSS	Power		
19	VDD	Power		
21	PA5 *	I/O	GPIO_Output	LD2 [Green Led]
27	PB1 *	I/O	GPIO_Output	Buzzer
30	VCAP1	Power		
31	VSS	Power		
32	VDD	Power		
37	PC6 *	I/O	GPIO_Output	D4
38	PC7 *	I/O	GPIO_Output	D5
39	PC8 *	I/O	GPIO_Output	D6
40	PC9 *	I/O	GPIO_Output	D7
46	PA13	I/O	SYS_JTMS-SWDIO	TMS
47	VSS	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	TCK
51	PC10 *	I/O	GPIO_Output	Е
52	PC11 *	I/O	GPIO_Output	RS
55	PB3 **	I/O	SYS_JTDO-SWO	SWO
56	PB4 *	I/O	GPIO_Input	Down
57	PB5 *	I/O	GPIO_Input	Right
58	PB6 *	I/O	GPIO_Input	Up
59	PB7 *	I/O	GPIO_Input	Left
60	воото	Boot		
63	VSS	Power		

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
64	VDD	Power		

^{*} The pin is affected with an I/O function

^{**} The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	Nucleo-F401_Code
Project Folder	D:\CORTEX_M\STM32F401\Nucleo-F401_Code
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.26.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_USART2_UART_Init	USART2
5	MX_ADC1_Init	ADC1

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F401
MCU	STM32F401RETx
Datasheet	DS10086_Rev3

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

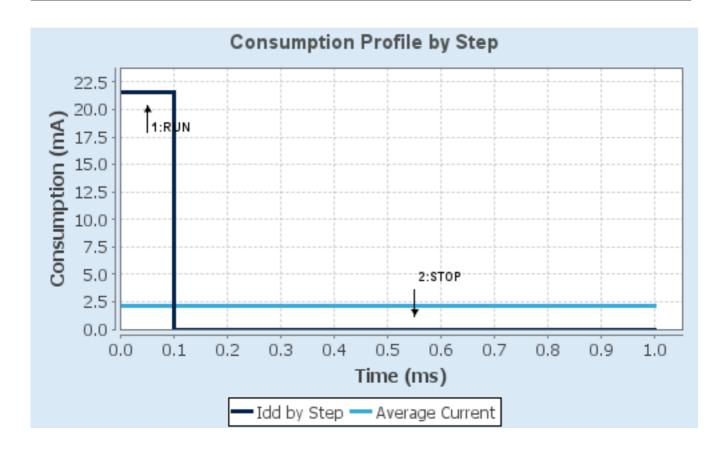
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale2-Medium	No Scale
Fetch Type	FLASH/ART/PREFETCH	n/a
CPU Frequency	84 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LPLV Flash-
		PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	21.6 mA	10 μΑ
Duration	0.1 ms	0.9 ms
DMIPS	105.0	0.0
Ta Max	101.44	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	2.17 mA
Battery Life	2 months, 4 days,	Average DMIPS	105.0 DMIPS
	8 hours	_	

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. ADC1 mode: IN1

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

DMA Continuous Requests

Clock Prescaler PCLK2 divided by 4

Resolution 12 bits (15 ADC Clock cycles)

Data Alignment

Scan Conversion Mode

Continuous Conversion Mode

Disabled

Enabled *

Discontinuous Conversion Mode

Disabled

End Of Conversion Selection EOC flag at the end of single channel conversion

Enabled *

ADC_Regular_ConversionMode:

Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None
Rank 1

Channel Channel 1
Sampling Time 84 Cycles *

ADC_Injected_ConversionMode:

Number Of Conversions 0

WatchDog:

Enable Analog WatchDog Mode false

7.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator Low Speed Clock (LSE): Crystal/Ceramic Resonator

7.2.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Instruction Cache Enabled
Prefetch Buffer Enabled

Data Cache Enabled

Flash Latency(WS) 2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value 16

TIM Prescaler Selection Disabled
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000

Power Parameters:

Power Regulator Voltage Scale Power Regulator Voltage Scale 2

7.3. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.4. **USART2**

Mode: Asynchronous

7.4.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples

^{*} User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA1	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	
RCC	PC14- OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15- OSC32_OU T	RCC_OSC32_O UT	n/a	n/a	n/a	
	PH0 - OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1 - OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS- SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK- SWCLK	n/a	n/a	n/a	TCK
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	USART_TX
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	USART_RX
Single Mapped Signals	PB3	SYS_JTDO- SWO	n/a	n/a	n/a	SWO
GPIO	PC13- ANTI_TAMP	GPIO_EXTI13	External Interrupt Mode with Falling edge trigger detection	No pull-up and no pull-down	n/a	B1 [Blue PushButton]
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [Green Led]
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Buzzer
	PC6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	D4
	PC7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	D5
	PC8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	D6
	PC9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	D7
	PC10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Е
	PC11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RS
	PB4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Down
	PB5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Right
	PB6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Up
	PB7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Left

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA2_Stream0	Peripheral To Memory	Low

ADC1: DMA2_Stream0 DMA request Settings:

Mode: Circular *
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: Enable *
Peripheral Data Width: Half Word
Memory Data Width: Half Word

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA2 stream0 global interrupt	true	0	0
PVD interrupt through EXTI line 16		unused	
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 global interrupt	unused		
USART2 global interrupt	unused		
EXTI line[15:10] interrupts	unused		
FPU global interrupt	unused		

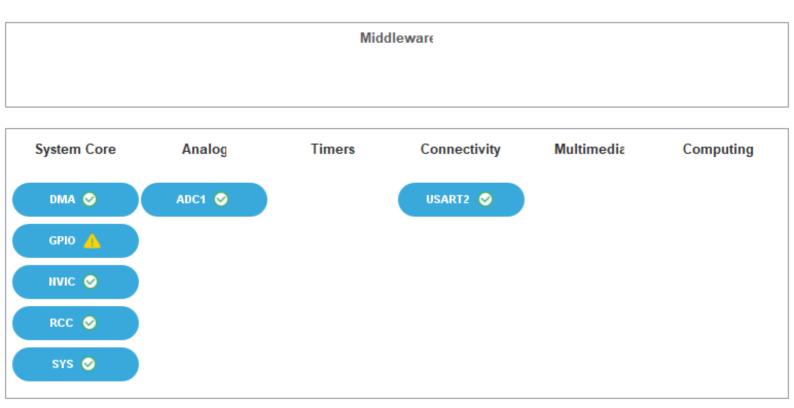
8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA2 stream0 global interrupt	false	true	true

* User modified value

9. System Views

- 9.1. Category view
- 9.1.1. Current



10. Docs & Resources

Type Link

Datasheet http://www.st.com/resource/en/datasheet/DM00102166.pdf

Reference http://www.st.com/resource/en/reference_manual/DM00096844.pdf

manual

Programming http://www.st.com/resource/en/programming manual/DM00046982.pdf

manual

Errata sheet http://www.st.com/resource/en/errata_sheet/DM00158624.pdf

Application note http://www.st.com/resource/en/application_note/CD00167594.pdf

Application note http://www.st.com/resource/en/application_note/CD00211314.pdf

Application note http://www.st.com/resource/en/application_note/CD00249778.pdf

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Application note http://www.st.com/resource/en/application_note/CD00264342.pdf

Application note http://www.st.com/resource/en/application_note/CD00264379.pdf

Application note http://www.st.com/resource/en/application_note/DM00024853.pdf

Application note http://www.st.com/resource/en/application_note/DM00040802.pdf

Application note http://www.st.com/resource/en/application_note/DM00040808.pdf

Application note http://www.st.com/resource/en/application_note/DM00042534.pdf

Application note http://www.st.com/resource/en/application_note/DM00046011.pdf

Application note http://www.st.com/resource/en/application_note/DM00072315.pdf

Application note http://www.st.com/resource/en/application_note/DM00073742.pdf

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