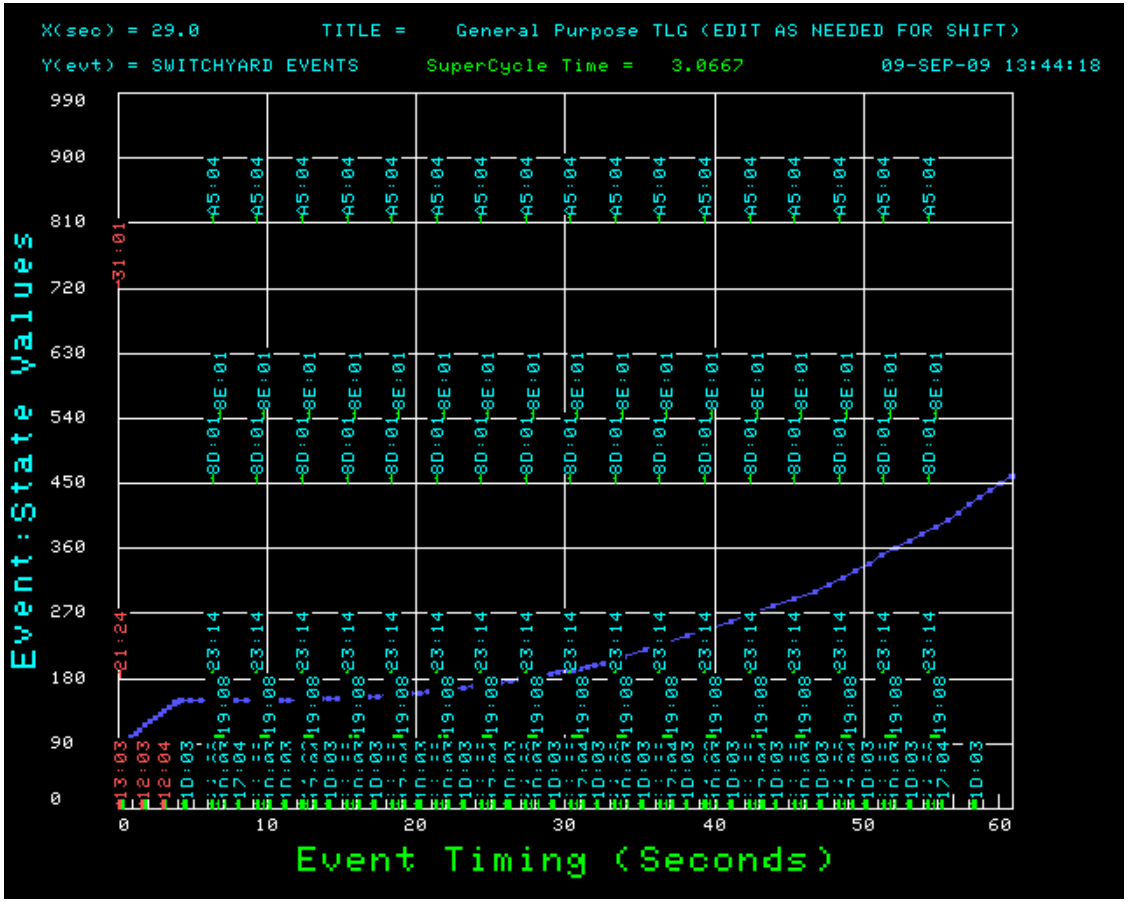
Fermi Timing Systems and Project X

- Multi-Level System Timing
  - TCLK
    - High Level Machine Coordination
  - Beam Sync Clocks
    - Machine Specific Bunch Level Timing
  - Machine State on data links
    - MDAT
    - Ethernet

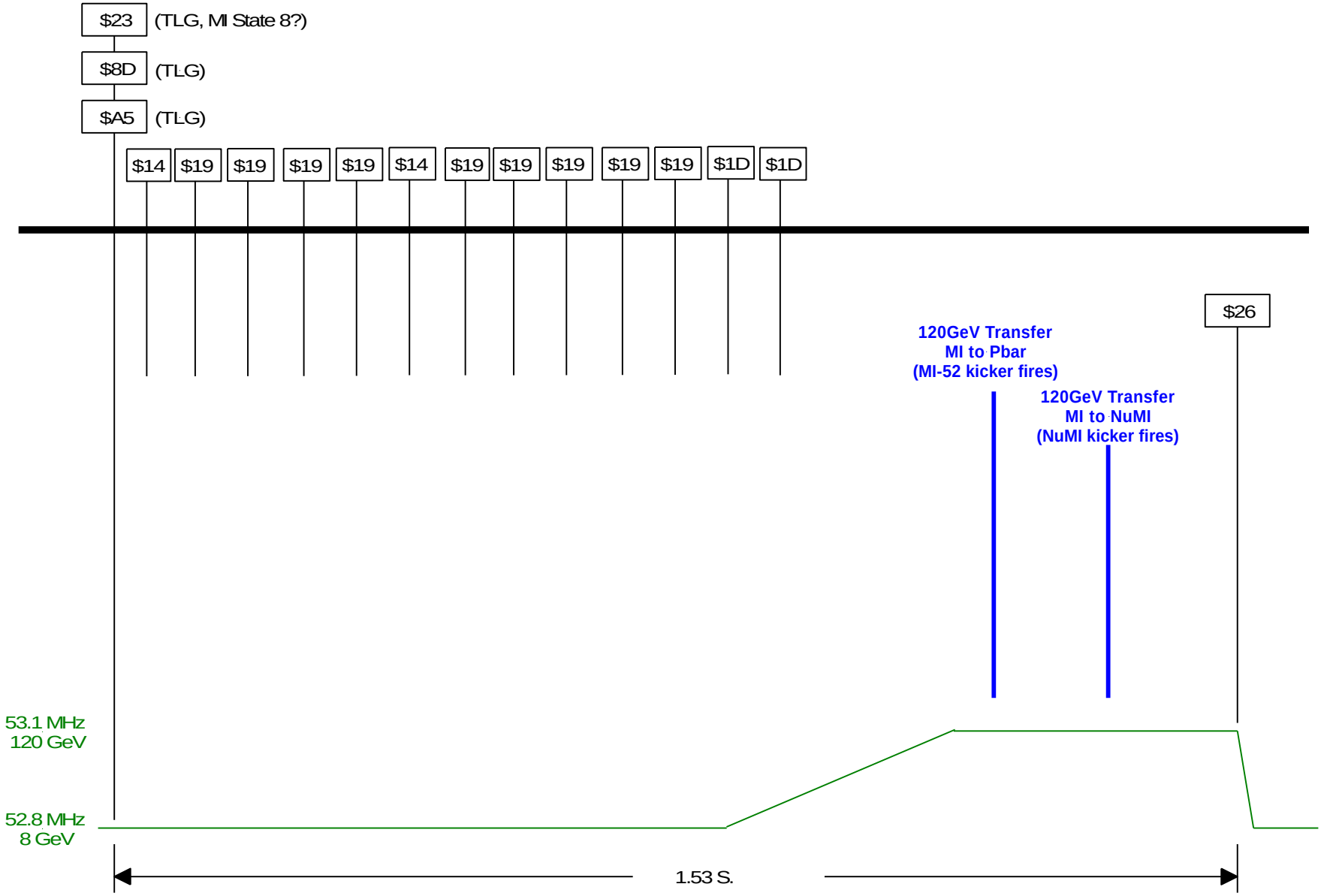
- TCLK
  - Provides high level machine coordination for complex
    - Overall complex timing set via Timeline Generator (TLG)
  - Available in all machine locations
  - 10MHz Carrier
  - Modified Manchester Encoding
  - 10 bit event frame
    - Start bit (0)
    - 8 bit event data (256 events)
    - Parity bit
  - 2 carrier cycle minimum event spacing
    - Minimum event spacing 1.2 uS
  - Event prioritization
  - Jitter ~1nS (multimode fiber transmission)

- Timeline Generator (TLG)
  - Provides primary TCLK system interface via D69 application
    - Allows quick reconfiguration of operational scenario(s) for accelerator complex
  - Supercycle
  - Timeline
    - Continuous timelines
    - One shot timeline function
    - Sequencer loading
  - Timeline Modules
    - Multimode modules
    - Intermixing modules


D69 TLG(VME) Released 07-AUG-2001 11:40:00 08-SEP-09 11:04:34 ♦Pgm_Tools♦
TIMELINES
modules
module states
misc
TLG F/E STATUS WINDOW
Current : 15) General Purpose TLG (EDIT AS NEEDED FOR SHIFT) 60 REPEAT RUNNING
Next : NONE
TLG F/E : Responding SuperCycle Time : 16.8 Sec(s)
♦Status♦
♦COMMANDS♦
TIMELINE EDIT WINDOW
BOO: 6.5 9.7 Hz ♦Plot♦ ♦Save♦ ♦Activate♦ ♦Delete♦ ♦Cycle Length♦ 60
NTF: 92 90 %
♦ TIMELINE NAME ♦ <General Purpose TLG (EDIT AS NEEDED FOR SHIFT)> ID = -<15 >+
♦Computed Values♦
♦Diagnostics♦
Click On Module To Select
Modules
♦Expand♦ ♦Devices♦
Repeat Rate
Start Time
Times
End Time
Total Time
1 Tevatron Ramp reset (Collider) 219 0 0 ♦fixd♦ 0 xxx.xxxx
* 2 120 Gev extraction to SY 4.2s FT 65 0 0 ♦fixd♦ 0 xxx.xxxx
* 3 Collider Protons to Tevatron 60 30 0 ♦fixd♦ 30 xxx.xxxx
* 4 NuMi Target -- SIX BATCH 10 16.8 0 ♦fixd♦ 16.8 xxx.xxxx
* 5 Slip Stacking to Pbar target 2 0 0 ♦fixd♦ 0 xxx.xxxx
* 6 Slip stacking to NuMi and Pbar ta 3 0 20 ♦pack♦ 60 59.2667
* 7 NuMi only 11 batch slip stacking 2.2 0 0 ♦fixd♦ 0 xxx.xxxx
8 MiniBoone Test - single 1D 10 0 0 ♦fixd♦ 0 xxx.xxxx
9 Booster study 5 3.867 10 ♦fixd♦ 62.87 58.0667
10 MINIBOONE (0X12, 0X12, 0X1D) GENE .2 1.733 20 ♦pack♦ 60 60
11 MINIBOONE (0X1D) GENERATED BY F/E .06667 .8667 40 ♦pack♦ 60 60
1:12 of 12
Messages
[PM1723] : Initializing TLG.....COMPLETED
[PM1723] : Initializing TLG.....STARTED


X(sec) = 29.0
TITLE = General Purpose TLG (EDIT AS NEEDED FOR SHIFT)
Y(evt) = SWITCHYARD EVENTS
SuperCycle Time = 3.0667
09-SEP-09 13:44:18
Event:State Values
990
900
810
720
630
540
450
360
270
180
90
0
0
10
20
30
40
50
60
Event Timing (Seconds)

Sample Timeline for Mixed Mode NuMI Cycles



- Beam Sync Clock(s)
  - Machine Specific
    - Separate clocks for MI, RR & Tevatron
  - Provides bunch level timing
    - Kickers, BPMs, etc.
  - Turn Markers
  - Beam transfer events
  - Machine rf/7 carrier
  - Modified Manchester encoding
  - 10 bit event frame
    - Start bit (0)
    - 8 bit event data
    - Parity bit
  - Minimum event spacing ~1.6 uS
  - Jitter ~1nS (multimode fiber transmission)

- Machine State on Data Links
  - MDAT Link
    - Carries data frames for ramps, intensities, machine states, etc.
    - Frames update/repeat at 720 Hz.
    - Continuous transmission
  - Ethernet Multicast
    - Single Ethernet broadcast on change in machine state

- Project X Clock System Configurations

  - 8 GeV Linac
    - Project X Clock
      - TCLK available to legacy equipment
    - RRBS provided to source for synchronization

  - 2 GeV Linac with Rapid Cycling Synchrotron (RCS)
    - Project X Clock
      - TCLK available to legacy equipment
    - RCS Beam Sync Clock provided to source for Linac to RCS synchronization
    - RRBS provided to RCS for RCS to Recycler synchronization

- Project X Clock (ACLK/XCLK?)
  - Upgrade/eventual replacement for TCLK
    - Will provide high level machine coordination for complex
    - Will need to be synchronized with TCLK to provide support for existing hardware (MI, RR, NuMI, etc.)
  - Gigabit (or faster)
  - 16 bit clock events
    - $0000 - $00FF match existing TCLK event definitions
  - Event count (16/32 bit?)
    - Allows for unique Event & Count for data sorting
  - Sourced by new TLG
    - Also source TCLK to enforce synchronization
  - Open frame space under TCLK event frames may be used to broadcast non-TCLK events ($0100-$FFFF)
  - Transmission path through Linac opposite beam

- RCS Beam Sync Clock
  - Provide bunch level timing
    - Kickers, BPMs, etc.
  - Turn Markers
  - Beam transfer events
  - Machine rf carrier (50-52.8 MHz)
  - Modified Manchester encoding
  - 10 bit event frame
    - Start bit (0)
    - 8 bit event data
    - Parity bit
  - Minimum 2 rf cycle between event frames
    - Minimum event spacing ~240 nS