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Reviews

Very good e-book and helpful one. It is among the most awesome publication we have read. Its been developed in an remarkably simple way in fact it is simply right after i finished reading this book through which basically transformed me, affect the way i really believe.
(Prof. Kacey O'Hara)

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RareBooksClub. Paperback. Book Condition: New. This item is printed on demand. Paperback. 66 pages. Original publisher: Aberdeen Proving Ground, MD : Army Research Laboratory, 1999 OCLC Number: (OCoLC)311097378 Subject: Computational fluid dynamics. Excerpt: . . . This report will discussh ow this effect was SGI Power Challengea ndo n the ConvexE xemplar approachedw, hat the resultsw ere, and the reasonf or thoser esults. 2. The Architecture of the SGI Power Challenge Beforeo ne can discussth e resultso f this effort, it is helpful to have a short introduction to the architectureisn volved. TheS GI PowerC hallengec anb e thoughto f ast he prototypicalR ISC-based cache-coherensth aredm emory SMP. As such, it will be discussedf irst. From the hardware perspectivei, t hast he following properties: (1) Powerful RISC-basedp rocessors. I n this case, R SOOOpr ocessorsra ted at 300 MFLOPS each. (2) This versiono f the PowerC hallengeh ad up to 18 processorsa ndu p to 16 GB of memory, althougho nec ouldn ot configurea systemw ith both 18 processorsa nd 16 GB of memory. (3) Eachp rocessohr ada largeo ff-chip cache (4 MB). (4) Hardwarep rotocolsm aintaint he coherencyb etweena ll of the cachesa nd main memory. This is a key requiremenitf sharedm emoryi s to be implementede ntirelyi n hardware. (5) Sharedm emoryi s entirelyi mplementedin hardware. All of the boardsa re connectedb y a commons ystemb ust hat implementsa snoopyb us protocol for cachec oherency. T his bus gives a The speedo f the bus is a key limiting factor in uniform memory access time. determiningh ow manyp rocessorsc anr un in a systema t one time without running out of memory busb andwidth. This item ships from La Vergne,TN. Paperback.

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