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# Generative AI for Analog/RF Integrated Circuit Design and Netlist Synthesis: Evolving Methodologies and Emerging Applications

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**ABSTRACT** Electronic Design Automation (EDA) in analog Integrated Circuits (ICs) continues to be a critical research area, yet its widespread adoption significantly lags behind its digital counterpart due to inherent complexities. This extended systematic review updates recent contributions in the last five years, specifically highlighting cutting-edge methods that address persistent domain-specific challenges such as data scarcity, efficient topology exploration, robust parameter optimization considering process-voltage-temperature (PVT) variations, and accurate layout parasitic management. Our primary objective is to equip researchers new to this rapidly evolving domain with a comprehensive collection of references, a refined understanding of current challenges, and practical application guidelines. We provide an in-depth methodological review of state-of-the-art machine learning (ML) and generative AI approaches—including Graph Neural Networks (GNNs), Large Language Models (LLMs), and Variational Autoencoders (VAEs)—which are increasingly applied across various analog circuit design tasks, from topology synthesis to parameter sizing and validation. Notably, this survey expands on previous works by integrating discussions on newer, comprehensive frameworks like FALCON and MenTeR, which introduce end-to-end design, multi-agent workflows, and advanced layout-aware optimization. To the best of the authors' knowledge, this is the second review after [1] to comprehensively explore these latest applications of generative AI models in analog IC circuit design, charting their evolution and impact. We conclude by identifying key future research directions, emphasizing few-shot learning, multi-modal AI, and advanced multi-agent systems to further simplify human-tool interaction and guide design space exploration for industrial-scale analog ICs.

**INDEX TERMS** Analog integrated circuits (ICs), electronic design automation (EDA), generative artificial intelligence (GenAI), graph neural networks (GNNs), large language models (LLMs), machine learning (ML), netlist synthesis, parameter optimization, layout-aware sizing, topology synthesis, variational autoencoders (VAEs).

## I. INTRODUCTION

THE escalating complexity and diverse performance requirements of modern analog systems underpin advancements in crucial technologies such as generative AI, 5G/6G communication, and quantum computing. *"analog genie"* These demands necessitate full-flow automation to effectively manage the intricate trade-offs between numerous performance parameters, a task where traditional manual approaches are notoriously time-consuming and heavily reliant on scarce expert knowledge. While digital design automation has witnessed extensive development and widespread adoption across both industry and academia, the automation of analog IC design continues to face significant challenges.

Researchers have made concerted efforts to automate various stages of the analog design flow*"genAI paper"*. Conventionally, the process is segmented into three primary areas at the circuit level: topology selection, circuit sizing, and layout generation, often with complex feedback loops, as clearly shown in Fig. 1. Although remarkable progress has been achieved in layout generation tools, such as MAGICAL and ALIGN, and in certain aspects of digital IC design with generative AI, the development of scalable and robust solu-

tions for analog circuit sizing and comprehensive topology design remains a formidable challenge. Furthermore, a truly practical automation flow at each stage must inherently account for the interdependencies across design stages*"5,6,7 from genAI paper"*; for instance, the initial selection of a topology must proactively consider potential layout parasitics and their subsequent impact on performance metrics.

The fundamental challenge arises from the intricate design complexities of analog ICs. Unlike digital ICs that can be universally and hierarchically abstracted into Boolean logic representations and easily described with high-level hardware description languages (e.g., Verilog and VHDL) or programming languages (e.g., C), analog ICs remain intractable to such abstraction due to their lack of systematic hierarchical representation and the heuristic and knowledge-intensive nature of their design process [1]. This makes automating analog IC design using programming languages similar to those for digital ICs extremely difficult. As such, domain experts have followed a longstanding manual flow to design analog ICs. This process involves a number of time-consuming stages, such as selecting/creating an existing (new) circuit topology (i.e., defining the connections between devices), optimizing device parameters based on the topology to achieve desired performance, and designing the physical layout of the optimized circuit for manufacturing. Importantly, the topology generation stage is the foundation and most creative part of the analog IC design process, posing a formidable and perennial challenge to design automation. Addressing it is the key to accelerating the development of analog ICs.

In response to these challenges, machine learning (ML) has emerged as a promising solution. Learning-based methods, which leverage simulation data for training, offer more efficient design space exploration. ML techniques can be applied individually or in combination to facilitate decision-making, function approximation, and black-box optimization. Recent breakthroughs in generative AI, a subset of ML, have presented transformative opportunities to expedite these conventional design flows. Models such as Graph Neural Networks (GNNs) have shown significant advantages for handling graph-structured circuit data, while Variational Autoencoders (VAEs) are being explored to learn underlying data distributions for tasks like topology optimization. Furthermore, Large Language Models (LLMs), traditionally used for natural language processing, have demonstrated remarkable adaptability to large-scale design problems, including layout automation, optimization, and topology generation.

Despite these advances, many prior studies on ML-driven analog circuit design have often focused on isolated subtasks or simple, homogeneous circuits, overlooking the complexities of real-world heterogeneous systems. *"AI Circuit,* The persistent lack of comprehensive, generic, and diverse datasets with robust metrics has been a major impediment to thoroughly evaluating and improving ML algorithms in the analog domain. Moreover, many early generative AI approaches for topology generation were limited in scale, producing single types of small or conventional ICs, or suffered from ambiguous representations. This has encouraged the recent works to try bridging these gaps by proposing more holistic frameworks that integrate multiple design stages, leverage multi-agent systems, and incorporate layout-aware optimization to better reflect practical design scenarios. *"AI Circuit, FALCON, MenTeR "ADO-LLM", "Analog-GENIE", "AMP-AGENT"*

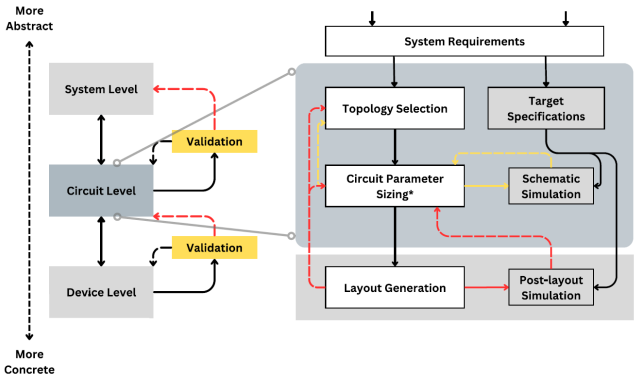


**FIGURE 1. Analog design automation flow, focusing on circuit-level automation. Dashed lines indicate dependencies between design stages.**

This paper aims to bridge these gaps by providing an updated and expanded systematic review of generative AI applications in analog IC design. We particularly focus on recent developments that push the boundaries of automation across the entire design pipeline, addressing shortcomings such as data scarcity, limited scalability, and inadequate layout awareness. Specifically, this review will integrate analysis of groundbreaking new frameworks like:

- **AnalogGenie**: A generative engine focused on the automatic discovery of diverse, large, and unseen analog circuit topologies using a scalable sequence-based graph representation and an augmented dataset.
- **AnalogCoder**: The first training-free LLM agent that designs analog circuits through Python code generation, employing feedback-enhanced flows and a circuit tool library.
- **SPICEPilot**: A framework leveraging LLMs to generate Python-based SPICE code, addressing data scarcity by automating dataset creation and providing standardized benchmarking.
- **AnalogXpert**: An LLM-based agent for subcircuit-level SPICE code generation that incorporates circuit design expertise through a proofreading strategy for iterative error correction.
- **MenTeR**: A fully-automated multi-agent workflow for end-to-end RF/Analog circuit netlist design, emphasizing specification understanding, collaborative optimization, and test bench validation through Chain-of-Stage reasoning and Diagram-Aware RAG.
- **FALCON**: A unified ML framework enabling fully automated, specification-driven analog circuit synthesis through performance-driven topology selection, GNN-

based parameter inference, and layout-constrained optimization, validated with industrial-grade simulations.
- **AICircuit**: A multi-level dataset and benchmark that facilitates the development and evaluation of ML algorithms for both homogeneous and heterogeneous analog and RF circuit designs.
- **AMSNet**: A netlist dataset for Analog and Mixed-Signal (AMS) circuits, which consists of 734 topologies and has been utilized for LLM-based AMS circuit auto-design and netlist generation.
- **AnalogCoderPro**: A training-free, end-to-end multimodal LLM framework that unifies topology generation and device sizing. It advances AnalogCoder by incorporating a multimodal diagnosis-and-repair feedback loop that uses simulation logs and waveform images for autonomous error correction.

These frameworks represent significant strides toward achieving holistic, human-competitive, and even superhuman capabilities in analog IC design.

The main contributions of this paper are as follows:

- **Comprehensive Survey of Recent Advancements**: Examine and compare recent advancements in generative AI for analog circuit design, with a particular focus on evolving techniques that address topology exploration, scalable parameter sizing, robust PVT variations, and realistic layout parasitics.
- **Methodological Review of State-of-the-Art Techniques**: Provide a methodological review of state-of-the-art generative AI techniques applied in analog circuit design automation, including Graph Neural Networks (GNNs), Large Language Models (LLMs), and Variational Autoencoders (VAEs), showcasing their latest applications and interconnections.
- **Analysis of Novel Comprehensive Frameworks**: Integrate and analyze new, comprehensive frameworks such as FALCON, MenTeR, AnalogGenie, AnalogCoder, SPICEPilot, and AnalogXpert, which were not thoroughly covered in previous surveys, providing insights into their unique contributions and synergistic potential.
- **Practical Resource Compilation**: Collect and synthesize abundant resources, open-source codes, and application guidelines to serve as a practical reference for researchers new to or advancing within the field of analog circuit automation.

The remainder of this paper is structured as follows: section II summarizes and compares previous review papers in terms of their automation scope and the ML techniques covered, highlighting the gaps addressed by this work. section III introduces fundamental IC design challenges and outlines how these challenges shape the automation task for generative AI. section IV provides the fundamentals of generative AI relevant to recent research, including detailed discussions on GNNs, LLMs, and VAEs. section V comprehensively compares significant research works, focusing on their methodologies, key problems they attempt to solve, and their contributions to the evolving landscape of analog design automation. Finally, section VI outlines future research directions and challenges for large-scale industrial adoption, including discussions on multi-agent systems and multi-modal AI.

## II. RELATED WORKS AND SURVEY LANDSCAPE

The rapid evolution of Artificial Intelligence (AI) and foundation models has spurred numerous systematic reviews aimed at capturing the state-of-the-art in Electronic Design Automation (EDA) "To add all previous survery papers".

This section summarizes the scope of previous survey papers and highlights the critical gaps that this work addresses, particularly concerning the application of generative AI to the complex domain of analog integrated circuits (ICs).

### A. TAXONOMY OF PRIOR AI FOR EDA SURVEYS

Existing reviews on AI for EDA can generally be categorized into two major types based on the AI paradigm they cover "A survey of circuit foundation models":

#### 1) Supervised Predictive AI Techniques

This category represents the mainstream of earlier AI for EDA solutions "circuit foundation model, generative AI for analog IC", focusing on supervised predictive models tailored for specific tasks, such as early prediction of design quality metrics (e.g., timing, area, power). These works have been extensively studied and covered in earlier surveys "put all previous surveys". However, they often fall short in addressing the unique challenges of analog IC design, which requires more than just predictive accuracy. The need for creativity in topology generation and the handling of continuous parameter spaces are aspects that these surveys do not fully explore.

#### 2) Foundation AI Techniques (Circuit Foundation Models - CFMs)

This emerging trend focuses on models characterized by pretraining on large datasets followed by fine-tuning for specific applications, enhancing generalization and generative capabilities "put survey of circuit foundation models here". The concept of Circuit Foundation Models (CFMs) encompasses two primary approaches: encoder-based and decoder-based models. Encoder-based models, such as Graph Neural Networks (GNNs), are adept at learning representations from graph-structured data, making them suitable for tasks like topology classification and parameter prediction. Decoder-based models, including Variational Autoencoders (VAEs) and Large Language Models (LLMs), excel in generating new designs by learning the underlying distribution of existing circuits.

Most recent surveys on second type CFMs have primarily focused on decoder-based models, specifically Large Language Models (LLMs) for EDA "search of relevant papers in the survey paper". This focus reflects the immense generative potential demonstrated by LLMs in areas like Hardware De-

scription Language (HDL) code generation, verification, and debugging "search of relevant papers in the survey paper".

### B. COMPARISON OF COVERAGE AND GAPS

A direct comparison reveals that existing surveys often suffer from limitations in scope, depth of analog coverage, or model inclusivity "pick relevant papers from previous surveys".

**TABLE 1. Comparison of Survey Focus and Gaps**

| Survey | ML/AI Techniques | Gaps Addressed |
|---|---|---|
| **Traditional Analog Surveys** | Bayesian Optimization (BO), Evolutionary Algorithms (EA), Deep Neural Networks (DNNs), Convolutional Neural Networks (CNNs) | Lack coverage of generative AI (LLMs, VAEs) and end-to-end integration; often overlook post-layout effects |
| **LLM-EDA** | Decoder LLMs | Lacks encoders (GNNs); digital bias; limited analog focus |
| **Recent Perspectives** | Encoder/Decoder LLMs | Missing latest GenAI & multi-agent analog applications |

Specific Gaps in Previous Literature:

#### 1) Model Inclusivity:

Model inclusivity addresses whether a survey covers the necessary range of AI paradigms critical for analog circuit automation, specifically encompassing both generative and predictive models. The majority of LLM-focused surveys covered only decoder-based LLMs. This survey, in contrast, incorporates both encoder-based GNNs (used for generalized circuit representation learning and predictive tasks like design quality evaluation) and decoder-based LLMs (used for generative tasks) into a unified CFM framework.

- **CFM Survey:** (to adjust the link) This work is highly model-inclusive. It systematically defines and categorizes all works within the foundation model paradigm into two primary types: encoder-based methods (which typically learn generalized representations for predictive tasks, e.g., Graph Neural Networks (GNNs)) and decoder-based methods (which leverage Large Language Models (LLMs) for generative tasks). This approach inherently covers the diverse model architectures used across the digital and analog EDA flows.
- **LLM for EDA Survey (The Leak):** The primary limitation of this survey is its exclusive focus on Large Language Models (LLMs), which are decoder-based foundation models. This narrow scope results in a critical omission of foundational encoder-based methods. Many breakthroughs in analog automation rely on non-LLM techniques, such as Graph Neural Networks (GNNs) and Variational Autoencoders (VAEs), which are fundamental for tasks like parasitic modeling and topology generation (e.g., CktGNN). By concentrating solely on LLMs, this survey overlooks a substantial and active segment of foundational analog AI research.
- **Analog AI Survey:** This paper aims to provide a comprehensive methodological review encompassing GNNs, LLMs, and VAEs as applied to analog circuit sizing and automation.

#### 2) Analog Depth:

Analog circuit design poses unique challenges, such as complexity due to diverse components, intricate interconnections, and the necessity of direct device-level representation, unlike the high-level abstraction available in digital design.

- **AnalogGenAI Survey**: The AnalogGenAI survey offers the deepest focus, dedicated entirely to analog IC design methodologies and applications. It effectively highlights core analog challenges including data scarcity, topology exploration, PVT variations, and layout parasitics. This survey is particularly rich in techniques for circuit sizing, reinforcement learning, and layout-aware automation. However, much of the research discussed focuses on relatively simple circuits like Op-Amps, with complex systems such as PLLs and power amplifiers being comparatively underexplored.
- **CFM and LLM4EDA Surveys**: Both CFM and LLM4EDA dedicate sections to analog circuits. The CFM survey lists recent works like AnalogGenie, AnalogCoder, and LaMAGIC. The LLM4EDA survey details contributions in initial specification/topology selection, schematic design/simulation (e.g., AnalogCoder, ADO-LLM, LaMAGIC), and layout design (e.g., LLANA, LayoutCopilot).

**Gap and Contribution:** While previous surveys acknowledge the analog domain, detailed coverage of advanced generative capabilities, especially those focusing on scalable and flexible topology discovery, is often summarized. Our survey will emphasize recent breakthroughs that address fundamental analog design difficulties:

- **Scalable Topology Discovery**: We highlight approaches like AnalogGenie, which addresses scalable and general analog design by broadening the variety of ICs and increasing device counts. AnalogGenie introduces a sequence-based, pin-level graph representation to efficiently capture large analog circuit topologies, enabling the discovery of diverse and unseen topologies.
- **Practical Topology Synthesis**: We examine specialized LLM agents like AnalogXpert, which moves toward practical topology synthesis by formulating it as a subcircuit-level SPICE code generation problem. AnalogXpert achieves significantly higher success rates (40% on synthetic data, 23% on real data) compared to baselines like AnalogCoder (8% and 6%, respectively) due to its use of a subcircuit library and a human experience-based proofreading strategy.

#### 3) Emerging Frameworks and Methodologies

Despite the advancements in analog design automation, several challenges remain unaddressed. These include:

- **End-to-End Automation**: End-to-end automation, spanning from specifications to layout-aware netlists, is identified as a critical future direction across all three existing surveys.
  **Gap and Contribution:** The current literature often tackles topology generation and parameter optimization as separate, sequential stages, which can lead to suboptimal results when inherent topological constraints are ignored during sizing. Our survey highlights new efforts that unify these stages:
  - **Unified Generation and Optimization**: AnalogCoder-Pro is introduced as a training-free, multimodal LLM framework designed for end-to-end analog circuit design, jointly performing topology generation and device sizing. It focuses on transforming natural-language design objectives into optimized netlists.
  - **Layout-Constrained Synthesis**: FALCON unifies topology selection, parameter inference, and layout-aware optimization in a single end-to-end pipeline. It guides parameter inference using a differentiable layout cost, integrating schematic and physical considerations.
- **Multi-Agent and Feedback Systems**: The use of autonomous agents and sophisticated feedback loops is crucial for handling the complexity and iterative nature of analog design.
  The LLM4EDA survey notes the trend toward LLM autonomous agents that iteratively improve code quality by incorporating feedback. It specifically mentions LayoutCopilot as an LLM-powered multi-agent collaborative framework for analog layout design. AnalogCoder employs a feedback-enhanced design flow to refine generated circuits based on functional checks and simulation results.
  **Gap and Contribution:** Recent advancements incorporate multi-modal inputs and highly specialized agents to improve robustness and efficiency beyond basic feedback loops:
  - **Multi-Modal Diagnosis:**:AnalogCoder-Pro advances the feedback loop by incorporating a multimodal diagnosis-and-repair feedback loop that utilizes simulation error messages and waveform images to autonomously correct design errors.
  - **Specialized Multi-Agent Systems:** MenTeR proposes a fully-automated multi-agent workflow integrated into an end-to-end analog design framework. It uses specialized agents for specification understanding, design refinement via Chain-of-Stage (CoS) reasoning, and diagram-aware retrieval, demonstrating significant performance improvements over single-agent approaches, even tackling complex circuits like the CMOS Bandgap Reference. Similarly, AmpAgent is an LLM-based multi-agent system specifically for multi-stage amplifier schematic design.
- **Data Scarcity Solutions**: The lack of large, high-quality, and publicly available analog circuit datasets remains a fundamental bottleneck.
  All three existing surveys recognize this challenge. The CFM survey explicitly discusses synthetic dataset generation and advanced data augmentation techniques as necessary paths forward. The AnalogGenAI survey advocates for the creation of open-source datasets and testbenches like AICircuit.
  **Gap and Contribution:** Our survey highlights critical recent efforts focused on generating large-scale, automated, and multi-modal analog datasets, which are essential for training robust foundation models.
  - **Generative Dataset Creation:** We discuss new automated frameworks designed to extract data at scale. AnalogGenie addressed this gap by building an extensive dataset of over 3,000 distinct analog circuit topologies with diverse functionalities, expanded by over 70x using data augmentation.
  - **Automated Schematic-to-Netlist Extraction:** We review frameworks dedicated to overcoming the image-to-netlist conversion barrier. Masala-CHAI is a fully automated framework leveraging LLMs and custom deep network models to generate SPICE netlists from schematic images, resulting in the largest curated open-source dataset of ∼7,500 SPICE netlists from textbooks. Similarly, AMSnet 2.0 uses deep-learning-based image instance segmentation for robust net detection to generate netlists and subsequently reconstruct digital schematics, overcoming the limitations of previous heuristic methods on noisy schematics. These tools directly address the deficiency of SPICE netlist data compared to digital HDL code and don't need to forget SPICEPilot; which is based on LLM-generated SPICE datasets.

By focusing on these specific advancements—particularly the deep integration of multi-modal data, multi-agent reasoning, unified topology-sizing optimization, and large-scale dataset generation—our survey provides a current and comprehensive understanding of the Generative AI landscape for complex analog circuit design, building upon and extending the scope of the existing literature.

By incorporating over 130 relevant works, spanning both predictive (encoder-based) and generative (decoder-based) methodologies, this survey provides a comprehensive collection of resources and application guidelines for researchers targeting industrial-scale analog IC design challenges.

## III. FUNDAMENTAL ANALOG IC DESIGN CHALLENGES

The quest for automating Analog Integrated Circuit (IC) design is obstructed by several foundational challenges inherent to continuous-signal processing, which contrast sharply with the structured nature of digital design. These challenges drive

the complexity of the design cycle and necessitate advanced generative AI solutions.

### A. DESIGN STAGES: TOPOLOGY SELECTION, CIRCUIT SIZING, AND LAYOUT GENERATION

The conventional manual flow segments the design into three critical, tightly coupled stages: topology selection, circuit sizing (parameter inference), and layout generation. A persistent challenge is the inherent strong interdependency across these stages. The performance of a circuit hinges on the topological choices, parameter values, and eventual physical implementation, where optimization in one stage often restricts success in the next.

1) **Topology Selection and Synthesis:** This is widely regarded as the most creative and challenging initial phase. Automation efforts must overcome the immense design space and the lack of a universal, scalable representation method for circuits. Frameworks like AnalogGenie address this by proposing models that can automatically discover diverse, large, and previously unseen circuit topologies.
2) **Circuit Sizing and Parameter Optimization:** This stage involves setting precise physical dimensions (W/L ratios, component values) to meet specific performance targets. As the number of parameters increases, optimization becomes computationally intensive and prone to local minima.
3) **Layout Generation:** The final stage demands adherence to complex manufacturing constraints while mitigating physical effects.

### B. INTRICATE TRADE-OFFS AND NON-LINEARITY

Analog circuits must successfully navigate numerous, often contradictory, performance requirements simultaneously, such as Power, Performance, Area (PPA), in addition to noise, gain, and linearity.

1) **Conflicting Metrics and Application Specificity:** Improving one metric often degrades another (e.g., increasing device size improves noise performance but increases parasitics and reduces speed). Moreover, analog IC design is highly application-specific, relying on designer intuition to define context-dependent Figures of Merit (FoM) and acceptable compromises.
2) **High Non-Linearity:** The relationship between circuit parameters and performance metrics is often highly non-linear, especially in complex circuits. AICircuit highlights this issue, noting that metrics such as phase noise in Voltage-Controlled Oscillators (VCOs) and performance metrics in Power Amplifiers (PAs) are difficult for even advanced models (MLPs, Transformers) to learn effectively.

### C. ABSTRACTION GAP AND DESIGN COMPLEXITY

Analog circuits exhibit a fundamental complexity rooted in the continuous nature of signals and their low-level representation:

1) **Low-Level Representation:** Unlike digital circuits, which can be abstracted hierarchically into Boolean logic using high-level Hardware Description Languages (HDLs), analog circuits resist such simplification. Analog design inherently operates at the device level. Even basic functions, such as an analog adder, require explicit configuration and wiring of multiple MOSFETs and resistors, unlike a succinct digital implementation.
2) **Combinatorial Complexity:** Analog circuits comprise a diverse mixture of voltage sources, MOSFETs, resistors, and capacitors. The intricate interconnections mean that even minor parameter adjustments can drastically alter functionality, potentially leading to a combinatorial explosion in the design search space.
3) **Heterogeneous Systems:** Scaling solutions to real-world, complex heterogeneous circuits (systems combining blocks with distinct functionalities, like a transmitter combining a VCO and a PA) remains challenging. Critically, AICircuit demonstrated that models trained on individual homogeneous circuits cannot generalize well to large heterogeneous systems due to load effects and strong coupling between blocks.

### D. DATA SCARCITY AND ACQUISITION BOTTLENECK

The scarcity of large, comprehensive analog circuit datasets is a severe barrier to applying generative AI methods.

1) **Proprietary Data and Language Scarcity:** Semiconductor companies protect proprietary designs, leading to few publicly available datasets. Furthermore, SPICE (Simulation Program with Integrated Circuit Emphasis), the predominant language for analog netlists, has a much smaller footprint in public code repositories compared to digital HDLs (like Verilog), complicating LLM domain learning.
2) **Schema-to-Netlist Bottleneck:** Much of the available analog design information exists only as schematic diagrams in papers and textbooks. Converting these schematic images into executable SPICE netlists typically requires painstaking manual transcription.
3) **Addressing Data Needs:**
   - **AMSnet 2.0**: Directly tackles this data bottleneck by constructing a large-scale database comprising transistor-level schematics, SPICE netlists, and component positional information. This resource is crucial for training Multimodal Large Language Models (MLLMs) to recognize and understand schematics.
   - **AICircuit**: Provides a comprehensive, high-fidelity, multi-level benchmark dataset covering both homogeneous and complex heterogeneous circuits simulated using commercial tools.
   - **AnalogGenie**: Addressed data scarcity by collecting an extensive dataset of over 3,000 diverse circuit topologies and employing data augmentation

techniques to expand it substantially.

- **Frameworks like AnalogCoder and SPICEPilot**: Utilize LLMs to generate functional Python/PySpice code, effectively generating synthetic data and accelerating dataset creation.

### E. PVT VARIATIONS AND ROBUSTNESS

Analog designs must be robust against Process, Voltage, and Temperature (PVT) variations. A design optimized under nominal conditions may fail under worst-case scenarios, necessitating computationally expensive PVT corner analysis to ensure design viability.

### F. LAYOUT PARASITICS AND PHYSICAL AWARENESS

The transition from schematic-level design to physical layout introduces parasitic effects that critically influence performance, especially in high-frequency (RF/mm-wave) and advanced technology nodes. Ignoring these effects leads to schematic-to-layout mismatch.

1) **Unified Layout Constraints:** The FALCON framework unifies the schematic and physical domain by incorporating layout constraints directly into the optimization loop. It uses a differentiable layout model to analytically compute area penalties and enforce design rules during gradient-based parameter inference, guiding the optimization toward physically realizable solutions.
2) **Multimodal Diagnosis:** AnalogCoder-Pro addresses the challenge of layout-sensitive performance by integrating a multimodal diagnosis-and-repair feedback loop. This system can analyze complex non-textual data, such as waveforms and frequency response images, to diagnose issues related to physical effects that textual logs might miss, improving the design refinement process.

### G. AMBIGUITY, HEURISTICS, AND THE NEED FOR UNIFIED FLOWS

The reliance on expert intuition and heuristic decision-making in analog design makes formalizing the design process for AI challenging.

1) **Topology-Sizing Decoupling:** Traditionally, topology generation and device sizing are treated sequentially, often resulting in suboptimal choices that lead to expensive, iterative redesigns.
2) **Unified and Agentic Approaches:** Generative AI aims to capture and operationalize this expertise:
   - **AnalogCoder-Pro:** addresses the decoupling challenge by aiming for a unified framework that combines topology generation and device sizing, supported by multimodal feedback and a circuit tool library for managing component reuse.
   - **AnalogCoder:** introduced a training-free LLM agent utilizing a prompt engineering and a feedback-enhanced flow to achieve automated design and self-correction.
   - **AnalogXpert:** focuses on incorporating human expertise by formulating topology synthesis as a subcircuit-level task complemented by a proofreading strategy that allows the LLM agent to iteratively correct errors based on predefined design rules.
   - **MenTeR:** uses a multi-agent framework powered by Chain-of-Stage (CoS) reasoning to decompose complex problems and employs Diagram-Aware RAG (DA-RAG) to retrieve information, ensuring that expert knowledge embedded in diagrams is effectively used throughout the design flow.

## IV. ML AND LLM FUNDAMENTALS IN ANALOG EDA

Please don't use the `{eqnarray}` equation environment. Use `{align}` or `{IEEEeqnarray}` instead. The `{eqnarray}` environment leaves unsightly spaces around relation symbols.

Please note that the `{subequations}` environment in LaTeX will increment the main equation counter even when there are no equation numbers displayed. If you forget that, you might write an article in which the equation numbers skip from (17) to (20), causing the copy editors to wonder if you've discovered a new method of counting.

BibTeX does not work by magic. It doesn't get the bibliographic data from thin air but from .bib files. If you use BibTeX to produce a bibliography you must send the .bib files.

LaTeX can't read your mind. If you assign the same label to a subsubsection and a table, you might find that Table I has been cross referenced as Table IV-B3.

LaTeX does not have precognitive abilities. If you put a `\label` command before the command that updates the counter it's supposed to be using, the label will pick up the last counter to be cross referenced instead. In particular, a `\label` command should not go before the caption of a figure or a table.

Do not use `\nonumber` inside the `{array}` environment. It will not stop equation numbers inside `{array}` (there won't be any anyway) and it might stop a wanted equation number in the surrounding equation.

## V. SOME COMMON MISTAKES

The word "data" is plural, not singular. The subscript for the permeability of vacuum $\mu_0$ is zero, not a lowercase letter "o." The term for residual magnetization is "remanence"; the adjective is "remanent"; do not write "remnance" or "remnant." Use the word "micrometer" instead of "micron." A graph within a graph is an "inset," not an "insert." The word "alternatively" is preferred to the word "alternately" (unless you really mean something that alternates). Use the word "whereas" instead of "while" (unless you are referring to simultaneous events). Do not use the word "essentially" to mean "approximately" or "effectively." Do not use the word "issue" as a euphemism for "problem." When compositions are not specified, separate chemical symbols by en-dashes; for example, "NiMn" indicates the intermetallic compound

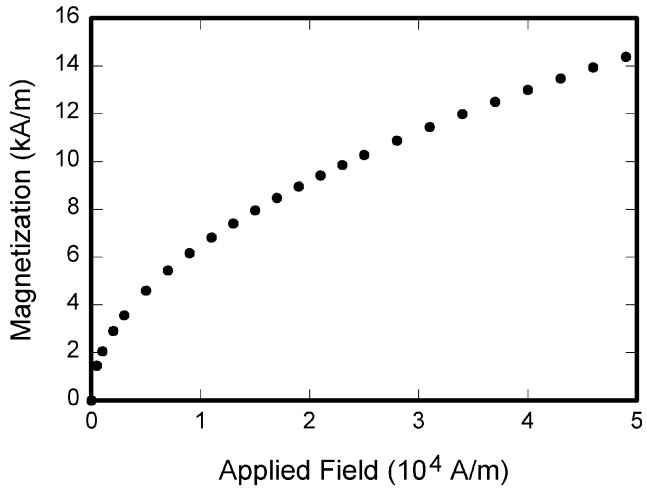


**FIGURE 2.** **Magnetization as a function of applied field. It is good practice to explain the significance of the figure in the caption.**

$Ni_{0.5}Mn_{0.5}$ whereas "Ni–Mn" indicates an alloy of some composition $Ni_xMn_{1-x}$.

Be aware of the different meanings of the homophones "affect" (usually a verb) and "effect" (usually a noun), "complement" and "compliment," "discreet" and "discrete," "principal" (e.g., "principal investigator") and "principle" (e.g., "principle of measurement"). Do not confuse "imply" and "infer."

Prefixes such as "non," "sub," "micro," "multi," and "ultra" are not independent words; they should be joined to the words they modify, usually without a hyphen. There is no period after the "et" in the Latin abbreviation "*et al.*" (it is also italicized). The abbreviation "i.e.," means "that is," and the abbreviation "e.g.," means "for example" (these abbreviations are not italicized).

A general IEEE styleguide is available at http://www.ieee.org/authortools.

**TABLE 2.** **Units for Magnetic Properties**

| Symbol | Quantity | Conversion from Gaussian and CGS EMU to SI [a] |
|---|---|---|
| $\Phi$ | magnetic flux | 1 Mx $\rightarrow 10^{-8}$ Wb $= 10^{-8}$ V·s |
| $B$ | magnetic flux density, magnetic induction | 1 G $\rightarrow 10^{-4}$ T $= 10^{-4}$ Wb/m$^2$ |
| $H$ | magnetic field strength | 1 Oe $\rightarrow 10^3/(4\pi)$ A/m |
| $m$ | magnetic moment | 1 erg/G $=$ 1 emu $\rightarrow 10^{-3}$ A·m$^2$ $= 10^{-3}$ J/T |
| $M$ | magnetization | 1 erg/(G·cm$^3$) $=$ 1 emu/cm$^3$ $\rightarrow 10^3$ A/m |
| $4\pi M$ | magnetization | 1 G $\rightarrow 10^3/(4\pi)$ A/m |
| $\sigma$ | specific magnetization | 1 erg/(G·g) $=$ 1 emu/g $\rightarrow$ 1 A·m$^2$/kg |
| $j$ | magnetic dipole moment | 1 erg/G $=$ 1 emu $\rightarrow 4\pi \times 10^{-10}$ Wb·m |
| $J$ | magnetic polarization | 1 erg/(G·cm$^3$) $=$ 1 emu/cm$^3$ $\rightarrow 4\pi \times 10^{-4}$ T |
| $\chi, \kappa$ | susceptibility | $1 \rightarrow 4\pi$ |
| $\chi_\rho$ | mass susceptibility | 1 cm$^3$/g $\rightarrow 4\pi \times 10^{-3}$ m$^3$/kg |
| $\mu$ | permeability | $1 \rightarrow 4\pi \times 10^{-7}$ H/m $= 4\pi \times 10^{-7}$ Wb/(A·m) |
| $\mu_r$ | relative permeability | $\mu \rightarrow \mu_r$ |
| $w, W$ | energy density | 1 erg/cm$^3$ $\rightarrow 10^{-1}$ J/m$^3$ |
| $N, D$ | demagnetizing factor | $1 \rightarrow 1/(4\pi)$ |

Vertical lines are optional in tables. Statements that serve as captions for the entire table do not need footnote letters.

[a]Gaussian units are the same as cg emu for magnetostatics; Mx = maxwell, G = gauss, Oe = oersted; Wb = weber, V = volt, s = second, T = tesla, m = meter, A = ampere, J = joule, kg = kilogram, H = henry.

## VI. GUIDELINES FOR GRAPHICS PREPARATION AND SUBMISSION

### A. TYPES OF GRAPHICS

The following list outlines the different types of graphics published in IEEE journals. They are categorized based on their construction, and use of color/shades of gray:

#### 1) Color/Grayscale figures

Figures that are meant to appear in color, or shades of black/gray. Such figures may include photographs, illustrations, multicolor graphs, and flowcharts. For multicolor graphs, please avoid any gray backgrounds or shading, as well as screenshots, instead export the graph from the program used to collect the data.

#### 2) Line Art figures

Figures that are composed of only black lines and shapes. These figures should have no shades or half-tones of gray, only black and white.

#### 3) Author photos

Author photographs should be included with the author biographies located at the end of the article underneath References.

#### 4) Tables

Data charts which are typically black and white, but sometimes include color.

### B. MULTIPART FIGURES

Figures compiled of more than one sub-figure presented side-by-side, or stacked. If a multipart figure is made up of multiple figure types (one part is lineart, and another is grayscale or color) the figure should meet the stricter guidelines.

### C. FILE FORMATS FOR GRAPHICS

Format and save your graphics using a suitable graphics processing program that will allow you to create the images as PostScript (.PS), Encapsulated PostScript (.EPS), Tagged Image File Format (.TIFF), Portable Document Format (.PDF), Portable Network Graphics (.PNG), or Metapost (.MPS), sizes them, and adjusts the resolution settings. When submitting your final paper, your graphics should all be submitted individually in one of these formats along with the manuscript.

### D. SIZING OF GRAPHICS

Most charts, graphs, and tables are one column wide (3.5 inches/88 millimeters/21 picas) or page wide (7.16 inches/181 millimeters/43 picas). The maximum depth a graphic can be is 8.5 inches (216 millimeters/54 picas). When choosing the depth of a graphic, please allow space for a caption. Figures can be sized between column and page widths if the author chooses, however it is recommended that figures are not sized less than column width unless when necessary.

There is currently one publication with column measurements that do not coincide with those listed above. Proceedings of the IEEE has a column measurement of 3.25 inches (82.5 millimeters/19.5 picas).

The final printed size of author photographs is exactly 1 inch wide by 1.25 inches tall (25.4 millimeters $\times$ 31.75 millimeters/6 picas $\times$ 7.5 picas). Author photos printed in editorials measure 1.59 inches wide by 2 inches tall (40 millimeters $\times$ 50 millimeters/9.5 picas $\times$ 12 picas).

### E. RESOLUTION

The proper resolution of your figures will depend on the type of figure it is as defined in the ''Types of Figures'' section. Author photographs, color, and grayscale figures should be at least 300dpi. Line art, including tables should be a minimum of 600dpi.

### F. VECTOR ART

In order to preserve the figures' integrity across multiple computer platforms, we accept files in the following formats: .EPS/.PDF/.PS. All fonts must be embedded or text converted to outlines in order to achieve the best-quality results.

### G. COLOR SPACE

The term color space refers to the entire sum of colors that can be represented within the said medium. For our purposes, the three main color spaces are Grayscale, RGB (red/green/blue) and CMYK (cyan/magenta/yellow/black). RGB is generally used with on-screen graphics, whereas CMYK is used for printing purposes.

All color figures should be generated in RGB or CMYK color space. Grayscale images should be submitted in Grayscale color space. Line art may be provided in grayscale OR bitmap colorspace. Note that ''bitmap colorspace'' and ''bitmap file format'' are not the same thing. When bitmap color space is selected, .TIF/.TIFF/.PNG are the recommended file formats.

### H. ACCEPTED FONTS WITHIN FIGURES

When preparing your graphics IEEE suggests that you use of one of the following Open Type fonts: Times New Roman, Helvetica, Arial, Cambria, and Symbol. If you are supplying EPS, PS, or PDF files all fonts must be embedded. Some fonts may only be native to your operating system; without the fonts embedded, parts of the graphic may be distorted or missing.

A safe option when finalizing your figures is to strip out the fonts before you save the files, creating ''outline'' type. This converts fonts to artwork what will appear uniformly on any screen.

### I. USING LABELS WITHIN FIGURES

#### 1) Figure Axis labels

Figure axis labels are often a source of confusion. Use words rather than symbols. As an example, write the quantity ''Magnetization,'' or ''Magnetization M,'' not just ''M.'' Put units in parentheses. Do not label axes only with units. As in Fig. 1, for example, write ''Magnetization (A/m)'' or ''Magnetization ($A{\cdot}m^{-1}$),'' not just ''A/m.'' Do not label axes with a ratio of quantities and units. For example, write ''Temperature (K),'' not ''Temperature/K.''

Multipliers can be especially confusing. Write ''Magnetization (kA/m)'' or ''Magnetization ($10^3$ A/m).'' Do not write ''Magnetization (A/m) $\times$ 1000'' because the reader would not know whether the top axis label in Fig. 1 meant 16000 A/m or 0.016 A/m. Figure labels should be legible, approximately 8 to 10 point type.

#### 2) Subfigure Labels in Multipart Figures and Tables

Multipart figures should be combined and labeled before final submission. Labels should appear centered below each subfigure in 8 point Times New Roman font in the format of (a) (b) (c).

### J. FILE NAMING

Figures (line artwork or photographs) should be named starting with the first 5 letters of the author's last name. The next characters in the filename should be the number that represents the sequential location of this image in your article. For example, in author ''Anderson's'' paper, the first three figures would be named ander1.tif, ander2.tif, and ander3.ps.

Tables should contain only the body of the table (not the caption) and should be named similarly to figures, except that '.t' is inserted in-between the author's name and the table number. For example, author Anderson's first three tables would be named ander.t1.tif, ander.t2.ps, ander.t3.eps.

Author photographs should be named using the first five characters of the pictured author's last name. For example, four author photographs for a paper may be named: oppen.ps, moshc.tif, chen.eps, and duran.pdf.

If two authors or more have the same last name, their first initial(s) can be substituted for the fifth, fourth, third. . . letters of their surname until the degree where there is differentiation. For example, two authors Michael and Monica Oppenheimer's photos would be named oppmi.tif, and oppmo.eps.

### K. REFERENCING A FIGURE OR TABLE WITHIN YOUR PAPER

When referencing your figures and tables within your paper, use the abbreviation ''Fig.'' even at the beginning of a sentence. Figures should be numbered with Arabic Numerals. Do not abbreviate ''Table.'' Tables should be numbered with Roman Numerals.

### L. SUBMITTING YOUR GRAPHICS

Figures should be submitted individually, separate from the manuscript in one of the file formats listed above in Section IV-C. Place figure captions below the figures; place table titles above the tables. Please do not include captions as part of the figures, or put them in ''text boxes'' linked to the figures. Also, do not place borders around the outside of your figures.

### M. COLOR PROCESSING/PRINTING IN IEEE JOURNALS

All IEEE Transactions, Journals, and Letters allow an author to publish color figures on IEEE *Xplore*® at no charge, and automatically convert them to grayscale for print versions. In most journals, figures and tables may alternatively be printed in color if an author chooses to do so. Please note that this service comes at an extra expense to the author. If you intend to have print color graphics, include a note with your final paper indicating which figures or tables you would like to be handled that way, and stating that you are willing to pay the additional fee.

## VII. CONCLUSION

Although a conclusion may review the main points of the paper, do not replicate the abstract as the conclusion. A conclusion might elaborate on the importance of the work or suggest applications and extensions.

If you have multiple appendices, use the \appendices command below. If you have only one appendix, use \appendix[Appendix Title]

## APPENDIX A
## FOOTNOTES

Number footnotes separately in superscript numbers.[1] Place the actual footnote at the bottom of the column in which it is cited; do not put footnotes in the reference list (endnotes). Use letters for table footnotes (see Table 2).

[1]It is recommended that footnotes be avoided (except for the unnumbered footnote with the receipt date on the first page). Instead, try to integrate the footnote information into the text.

## APPENDIX B
## SUBMITTING YOUR PAPER FOR REVIEW

### A. FINAL STAGE

When your article is accepted, you can submit the final files, including figures, tables, and photos, per the journal's guidelines through the submission system used to submit the articlle. You may use *Zip* for large files, or compress files using *Compress, Pkzip, Stuffit,* or *Gzip.*

In addition, designate one author as the ''corresponding author.'' This is the author to whom proofs of the paper will be sent. Proofs are sent to the corresponding author only.

### B. REVIEW STAGE USING IEEE AUTHOR PORTAL

Article contributions to IEEE Access should be submitted electronically on the IEEE Author Portal. For more information, please visit https://ieeeaccess.ieee.org/.

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## APPENDIX C
## IEEE PUBLISHING POLICY

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for publication, nor is under review for another refereed publication. The submitting author must disclose all prior publication(s) and current submissions when submitting a manuscript. Do not publish ''preliminary'' data or results. To avoid any delays in publication, please be sure to follow these instructions. Final submissions should include source files of your accepted manuscript, high quality graphic files, and a formatted pdf file. If you have any questions regarding the final submission process, please contact the administrative contact for the journal. author is responsible for obtaining agreement of all coauthors and any consent required from employers or sponsors before submitting an article.

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## APPENDIX D
## PUBLICATION PRINCIPLES

Authors should consider the following points:

1) Technical papers submitted for publication must advance the state of knowledge and must cite relevant prior work.
2) The length of a submitted paper should be commensurate with the importance, or appropriate to the complexity, of the work. For example, an obvious extension of previously published work might not be appropriate for publication or might be adequately treated in just a few pages.
3) Authors must convince both peer reviewers and the editors of the scientific and technical merit of a paper; the standards of proof are higher when extraordinary or unexpected results are reported.
4) Because replication is required for scientific progress, papers submitted for publication must provide sufficient information to allow readers to perform similar experiments or calculations and use the reported results. Although not everything need be disclosed, a paper must contain new, useable, and fully described information. For example, a specimen's chemical composition need not be reported if the main purpose of a paper is to introduce a new measurement technique. Authors should expect to be challenged by reviewers if the results are not supported by adequate data and critical details.
5) Papers that describe ongoing work or announce the latest technical achievement, which are suitable for presentation at a professional conference, may not be appropriate for publication.

## APPENDIX E
## REFERENCE EXAMPLES

- *Basic format for books:*
  J. K. Author, ''Title of chapter in the book,'' in *Title of His Published Book, x*th ed. City of Publisher, (only U.S. State), Country: Abbrev. of Publisher, year, ch. *x*, sec. *x*, pp. *xxx–xxx.*
  See [1], [2].
- *Basic format for periodicals:*
  J. K. Author, ''Name of paper,'' *Abbrev. Title of Periodical*, vol. *x, no. x*,pp. *xxx–xxx,* Abbrev. Month, year, DOI. 10.1109.*XXX*.123456.
  See [3]– [5].
- *Basic format for reports:*
  J. K. Author, ''Title of report,'' Abbrev. Name of Co., City of Co., Abbrev. State, Country, Rep. *xxx*, year.
  See [6], [7].
- *Basic format for handbooks:*
  *Name of Manual/Handbook, x* ed., Abbrev. Name of Co., City of Co., Abbrev. State, Country, year, pp. *xxx–xxx.*
  See [8], [9].
- *Basic format for books (when available online):*
  J. K. Author, ''Title of chapter in the book,'' in *Title of Published Book*, *x*th ed. City of Publisher, State, Country: Abbrev. of Publisher, year, ch. *x*, sec. *x*, pp. *xxx–xxx*. [Online]. Available: http://www.web.com
  See [10]– [13].
- *Basic format for journals (when available online):*
  J. K. Author, ''Name of paper,'' *Abbrev. Title of Periodical*, vol. *x*, no. *x*, pp. *xxx–xxx*, Abbrev. Month, year. Accessed on: Month, Day, year, DOI: 10.1109.*XXX*.123456, [Online].
  See [14]– [16].
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  Name of the invention, by inventor's name. (year, month day). Patent Number [Type of medium]. Available: site/path/file
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  J. K. Author, ''Title of paper,'' in *Abbreviated Name of Conf.*, City of Conf., Abbrev. State (if given), Country, year, pp. *xxxxxx.*
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- *Basic format for patents*:
  J. K. Author, "Title of patent," U.S. Patent *x xxx xxx*, Abbrev. Month, day, year.
  See [24].
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  1) J. K. Author, "Title of thesis," M.S. thesis, Abbrev. Dept., Abbrev. Univ., City of Univ., Abbrev. State, year.
  2) J. K. Author, "Title of dissertation," Ph.D. dissertation, Abbrev. Dept., Abbrev. Univ., City of Univ., Abbrev. State, year.

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- *Basic format for the most common types of unpublished references:*
  1) J. K. Author, private communication, Abbrev. Month, year.
  2) J. K. Author, "Title of paper," unpublished.
  3) J. K. Author, "Title of paper," to be published.

  See [27]– [29].
- *Basic formats for standards:*
  1) *Title of Standard*, Standard number, date.
  2) *Title of Standard*, Standard number, Corporate author, location, date.

  See [30], [31].
- *Article number in reference examples:*
  See [32], [33].
- *Example when using et al.:*
  See [34].

## ACKNOWLEDGMENT

The preferred spelling of the word "acknowledgment" in American English is without an "e" after the "g." Use the singular heading even if you have many acknowledgments. Avoid expressions such as "One of us (S.B.A.) would like to thank . . . ." Instead, write "F. A. Author thanks . . . ." In most cases, sponsor and financial support acknowledgments are placed in the unnumbered footnote on the first page, not here.

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**SECOND B. AUTHOR** (M'76–SM'81–F'87) and all authors may include biographies. Biographies are often not included in conference-related papers. This author became a Member (M) of IEEE in 1976, a Senior Member (SM) in 1981, and a Fellow (F) in 1987. The first paragraph may contain a place and/or date of birth (list place, then date). Next, the author's educational background is listed. The degrees should be listed with type of degree in what field, which institution, city, state, and country, and year the degree was earned. The author's major field of study should be lower-cased.

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**THIRD C. AUTHOR, JR.** (M'87) received the B.S. degree in mechanical engineering from National Chung Cheng University, Chiayi, Taiwan, in 2004 and the M.S. degree in mechanical engineering from National Tsing Hua University, Hsinchu, Taiwan, in 2006. He is currently pursuing the Ph.D. degree in mechanical engineering at Texas A&M University, College Station, TX, USA.

From 2008 to 2009, he was a Research Assistant with the Institute of Physics, Academia Sinica, Tapei, Taiwan. His research interest includes the development of surface processing and biological/medical treatment techniques using nonthermal atmospheric pressure plasmas, fundamental study of plasma sources, and fabrication of micro- or nanostructured surfaces.

Mr. Author's awards and honors include the Frew Fellowship (Australian Academy of Science), the I. I. Rabi Prize (APS), the European Frequency and Time Forum Award, the Carl Zeiss Research Award, the William F. Meggers Award and the Adolph Lomb Medal (OSA).