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EXPERIMENT 4 – Flip Flops and Sequential Circuits 2

I. Introduction

A. Objectives

In this experiment, you will get familiar with the basic operational principles of flip flops and shift registers.

II. Preliminary Work

1. Figure 1 shows a circuit constructed with elementary gates and JK flip-flops, in which all of the flip-flops are positive edge triggered. Write down the present states of $Q_{1,n}$, $Q_{2,n}$, and $Q_{3,n}$ in terms of the previous states $Q_{1,n-1}$, $Q_{2,n-1}$, $Q_{3,n-1}$. Prepare a table showing the state of the circuit after each clock pulse, starting from the state (1, 1, 1).

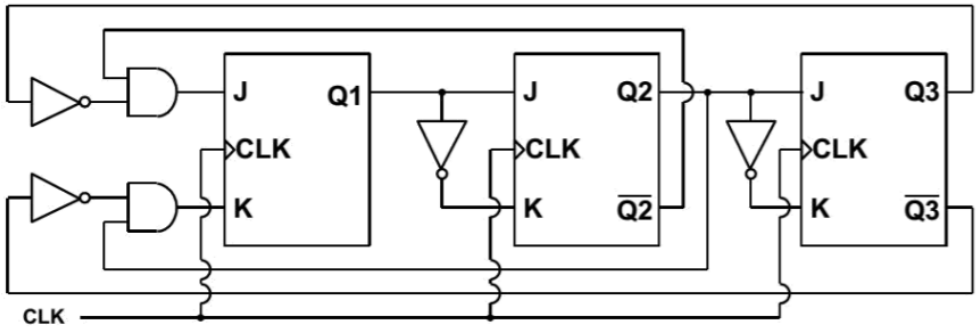

Figure 1: Schematic for preliminary work Q1.

2. Design a 4-bit shift register using 4 D flip flops. Your circuit should have one clock input pin, one serial data input pin, one serial data output pin and a 4-bit parallel data output pin. At each clock pulse, the 4-bit state should be shifted right and the MSB should be set as serial input, i.e, $\mathbf{Q_{3,n}Q_{2,n}Q_{1,n}Q_{0,n} = SIQ_{3,n-1}Q_{2,n-1}Q_{1,n-1}}$. Serial output is the new LSB, $\mathbf{Q_{0,n}}$.

3. Design an 4-bit shift register with parallel load capability in Verilog. Your module should have one clock input, one serial data input, one 4-bit parallel data input, a load signal, one serial data output, an 4-bit parallel data output. When the load signal is LOW, the module should work like a regular shift register. When the load signal is HIGH, state of the shift register is set to the parallel data input, $Q_3Q_2Q_1Q_0 = PI_3PI_2PI_1PI_0$, when a clock pulse occurs.

4. Design a test bench in Verilog for your shift register in Q3. Your test bench should illustrate the parallel load and shift capabilities of your shift register.

III. Experimental Work

1. Implement the circuit in Figure 1 on Quartus. Make a functional simulation to find the state of the circuit after each clock pulse, starting from the state (1, 1, 1). **Note:** Initial state of the flip flops is 0 on Quartus. To initialize the state to (1, 1, 1), you could add a Preset pin to the circuit, which is connected to the PRN inputs of the FFs, and send a LOW pulse on this pin before the clock signal starts.

2. Implement the shift register that you designed in preliminary work Q2 on Quartus. Create a symbol for this shift register. Using this symbol and elementary gates, implement a circuit where a single HIGH output circulates through the registers. That is, the parallel output of the shift register goes like 1000, 0100, 0010, 0001, 1000, 0100, … **Note** that initially the state is 0000 for one clock period. **Do not** use PRN or CLRN inputs of the flip flops. Make a functional simulation.

3. Implement your 4-bit shift register with parallel load capability in Verilog. Also implement your test bench for this shift register. Run the test bench to verify the shift register's operation.