## **EE447 EXPERIMENT 4 PRELIMINARY WORK**

## Part 1

## In which mode is TIMEROA used?

Periodic Mode. TAMR is set to 0x02. (Count Down)

Calculation of low and high values:

In the PULSE\_INIT, clk is divided to 16 through TAPR. Therefore it becomes 1 Mhz meaning timer is increased by each 1 microseconds. To achieve 20 kHz frequency, 50 microsec should be provided.

50 usec/1 usec gives 50 as a period. (in decimal) Therefore, HIGH value should 50/5=10 (A in hex) and LOW value should be 10\*4=40 (28 in hex)

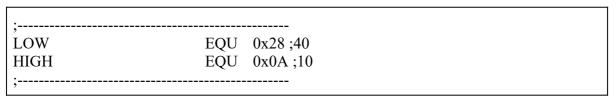


Figure 1. Low and High values to ensure 20% duty cycle

```
AREA MAIN, CODE, READONLY, ALIGN=2
THUMB
EXTERN PULSE_INIT
EXPORT __main

__main PROC

BL PULSE_INIT
MOV R6, #0

Final B Final
ENDP
ALIGN
END
```

Figure 2. Main Code for Part 1

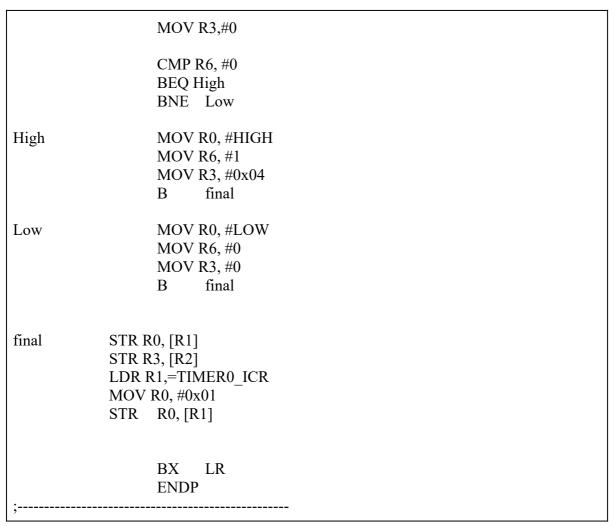


Figure 3. My Timer0A Handler ISR code

Since 20kHz can not be observed with naked eye, Debug is used to observation. Below Figure shows the TAILR register value for 20% cycle.

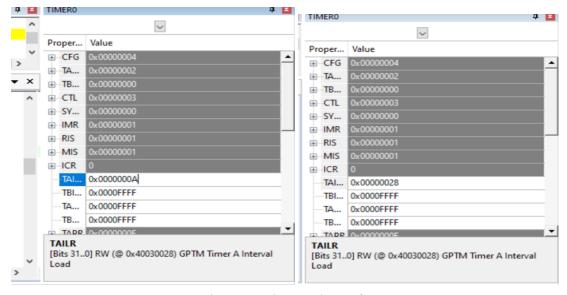


Figure 4. Timer Register values of TIMER0A

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## Part 2

In this part, pulse.s is included directly to the code. Then another Timer is created, for this purpose TIMER3 is chosen, which is created thorugh PB2. Pb2 is assigned as input and it takes values of pulse train to achieve this PF2 is connected with a jumper to PB2. Moreover, Convrt.s (from Exp1) and OutStr.s subroutines added to the code

```
;Timer Init.s
; 16/31 Timer Registers
TIMER3 CFG EQU 0x40033000
TIMER3 TAMR EQU 0x40033004
TIMER3 CTL EQU 0x4003300C
TIMER3 IMR EQU 0x40033018
TIMER3 RIS EQU 0x4003301C; Timer Interrupt Status
TIMER3 ICR EQU 0x40033024; Timer Interrupt Clear
TIMER3 TAILR EQU 0x40033028; Timer interval
TIMER3 TAPR EQU 0x40033038
TIMER3 TAR EQU 0x40033048; Timer register
;GPIO Registers B ile degistir!
GPIO PORTB DATA EQU 0x40005010; Access BIT2
GPIO PORTB DIR EOU 0x40005400 : Port Direction
GPIO PORTB AFSEL EQU 0x40005420; Alt Function enable
GPIO PORTB DEN EQU 0x4000551C; Digital Enable
GPIO PORTB AMSEL EQU 0x40005528; Analog enable
GPIO PORTB PCTL EQU 0x4000552C; Alternate Functions
; System Registers
SYSCTL RCGCGPIO EQU 0x400FE608; GPIO Gate Control
SYSCTL RCGCTIMER EQU 0x400FE604; GPTM Gate Control
COUNTER MAX VALEQU
                               0xFFFFFFF
                              AREA Timer3 init, CODE, READONLY
                              THUMB
                              EXPORT Timer init
Timer init PROC
                  LDR R1 ,=SYSCTL RCGCGPIO ; start GPIO clock
                  LDR R0, [R1]
                  ORR R0, R0, \#0x02; set bit [1] for port B
                  STR R0, [R1]
                  NOP; allow clock to settle
                  NOP
                  NOP
                  LDR R1, =GPIO PORTB DIR; set direction of PB2
                  LDR R0, [R1]
                  BIC R0, R0, #0x04; clear bit 2 for input
```

```
STR R0, [R1]
LDR R1, =GPIO PORTB AFSEL; regular port function
LDR R0, [R1]
ORR R0, R0, #0x04
STR R0, [R1]
LDR R1, =GPIO PORTB PCTL; Timer3A alternate func select
LDR R0, [R1]
ORR R0, R0, #0x00000700
STR R0, [R1]
LDR R1, =GPIO PORTB AMSEL; disable analog
MOV R0, #0
STR R0, [R1]
LDR R1, =GPIO PORTB DEN; enable port digital
LDR R0, [R1]
ORR R0, R0, #0x04
STR R0, [R1]
LDR R1, =SYSCTL RCGCTIMER; Start Timer3
LDR R2, [R1]
ORR R2, R2, #0x08;1000
STR R2, [R1]
NOP; alow clock to settle
NOP
NOP
LDR R1, =TIMER3 CTL; disable timer during setup
BIC R2, R2, #0x08
STR R2, [R1]
LDR R1, =TIMER3 CFG; set 16 bit mode
MOV R2, #0x04
STR R2, [R1]
LDR R1, =TIMER3_TAMR
MOV R2, #0x17;
STR R2, [R1]
LDR R1, =TIMER3 CTL; initialize match clocks
LDR R2,[R1]
ORR R2,R2,#0x0C
STR R2, [R1]
LDR R1, =TIMER3 TAILR
MOV R2, #COUNTER MAX VAL
STR R2, [R1]
```

```
LDR R1 ,=TIMER3_TAPR
MOV R2 ,#15 ; divide clock by 16 to
STR R2 , [R1] ; get 1 us clocks

LDR R1 ,=TIMER3_IMR ; disable timeout interrupt
MOV R2 ,#0x00
STR R2 , [R1]

; Enable timer

LDR R1 ,=TIMER3_CTL
LDR R2 , [R1]
ORR R2 ,R2 ,#0x03 ; set bit 0 to enable
STR R2 , [R1];
BX LR ; return
ENDP
```

Figure 5. Timer Init.s code

```
; Program Directives.s
.********************
LOW EQU 0x00000028;
FIRST EQU 0x20000400
; 16/31 Timer Registers
TIMER3 CFG EQU 0x40033000
TIMER3 TAMR EQU 0x40033004
TIMER3 CTL EQU 0x4003300C
TIMER3 IMR EQU 0x40033018
TIMER3 RIS EQU 0x4003301C; Timer Interrupt Status
TIMER3 ICR EQU 0x40033024; Timer Interrupt Clear
TIMER3 TAILR EQU 0x40033028; Timer interval
TIMER3 TAPR EQU 0x40033038
TIMER3 TAR EQU 0x40033048; Timer register
GPIO Registers B access
GPIO PORTB DATA EQU 0x40005010; Access BIT2
; Program section
.********************
;LABEL
              DIRECTIVE VALUE
                                       COMMENT
              AREA
                        main, READONLY, CODE
              THUMB
                             PULSE INIT
              EXTERN
                             Timer init
              EXTERN
              EXTERN
                             OutStr
              EXTERN
                             Convrt
                        main; Make available
              EXPORT
         PROC
 main
```

BL PULSE\_INIT BL Timer\_init MOV R8,#LOW

start MOV R4,#0x00 ;counter for edges

read flag LDR R1,=TIMER3 RIS ;polling for RIS

LDR R0,[R1] STR R0,[R4]

CMP R0,#0x04 ;if capture flag is high

BNE read flag

BEQ flag\_high ;go to flag\_high

flag high

ADDS R4,#1 ;add counter by 1 LDR R1,=TIMER3 ICR ;clear capture flag

MOV R0,#0xFF STR R0,[R1]

LDR R1,=TIMER3\_TAR ;loading current TAR value

LDR R2,[R1]

CMP R4,#1

BEQ first\_val ;first edge value

CMP R4,#2

BEQ second val ;second edge value

CMP R4,#3

BEQ third\_val ;third edge value

CMP R4,#4 ;when counter is 4 go to exit

BEQ display

first val MOV R12,R2 ;copying TAR value at the first edge

B read flag

second val MOV R6,R2 ;copying TAR value at the second edge

B read flag

third val MOV R10,R2 ;copying TAR value at the third edge

B read flag

display

SUB R6,R12; led is high i.e. pulse width

LDR R5,=FIRST MOV R4,R6 BL Convrt

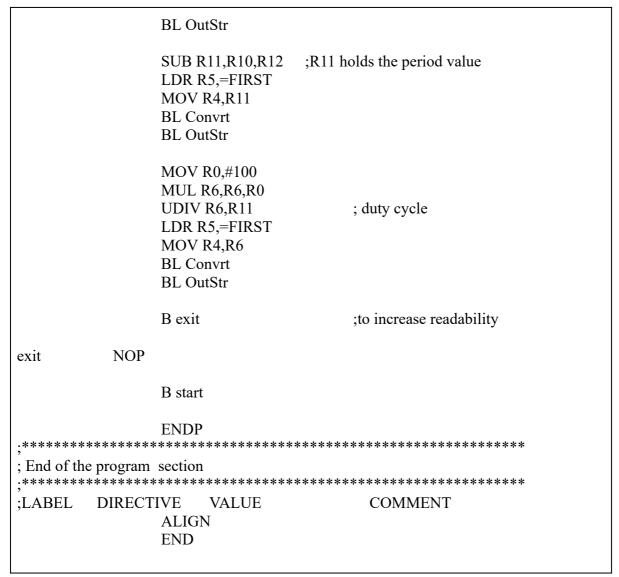


Figure 6. Program Directive Code

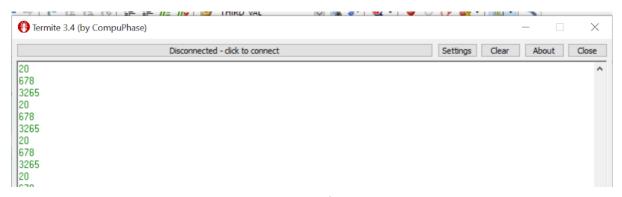


Figure 7. Termite Output

In Fig. 7 pulse width is 678, period is 3265 and the duty cycle is 20.

678 is calculated by substracting the second edge TAR value from the first edge TAR value. 3265 is calculated by sybstracting the thirs edge TAR value from the first edge TAR value.

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Duty cycle is calculated by dividing the pwm cycle to period, and multipled with 100. Here, I couln't convert the pulse width and period values into seconds. Termit prints only the TAR current value differences.

```
.*********************
; Convrt.s
; Def: Converts max 32-bit hex number's decimal equivalent to ascii
; Writes the ascii result sstarting from [R5] address
.*********************
; Constants
ASCII
          EQU
                           0x030
; Program section
.**********************
;LABEL
                DIRECTIVE VALUE
                                           COMMENT
                AREA convert, READONLY, CODE
                THUMB
                EXPORT Convrt; Reference external subroutine
Convrt
                PROC
                :LDR
                                R5,=FIRST
                PUSH
                           {R0,R1,R2,R3,R4,R5,R6,R7,R8}
                MOV
                                R1,#0x0A
                MOV
                           R6,#0
                     R2, R4,R1; divide by ten, div->R2
start
          UDIV
                MUL
                                R3, R2,R1 ;multiply div*10 -> R3
                SUB
                                R0,R4,R3; Least significant digit -> R0
                                R0,#ASCII ;convert digits to ascii
                ADD
                PUSH
                           {R0}
                MOV
                                R4,R2
                CMP
                           R2.#0
                                R6,#0x01; counts how many decimal digits
                ADD
exists in the number
                BNE
                ;ascii equivalent of digits are pushed to stack, then write to location
of R5
write reg
          SUB
                     R6,#0x01
                           {R7}
                POP
                STRB R7,[R5],#1
                CMP
                           R6,#0x00
                BNE
                           write reg
                           R0,#0x0D
                MOV
                STRB R0,[R5],#1
                           R0,#0x04
                MOV
                STRB R0,[R5]
```

POP {R0,R1,R2,R3,R4,R5,R6,R7,R8}
BX LR
ENDP
ALIGN
END

Figure 8. Convrt.s code