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EXPERIMENT 2. Elementary Gate Networks

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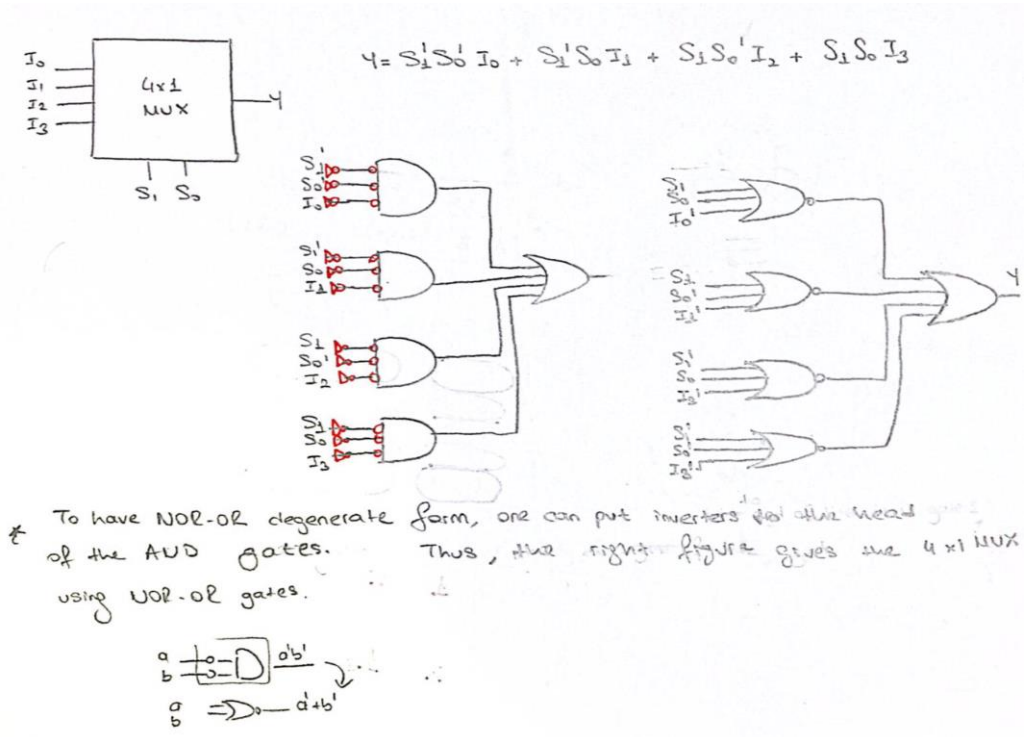
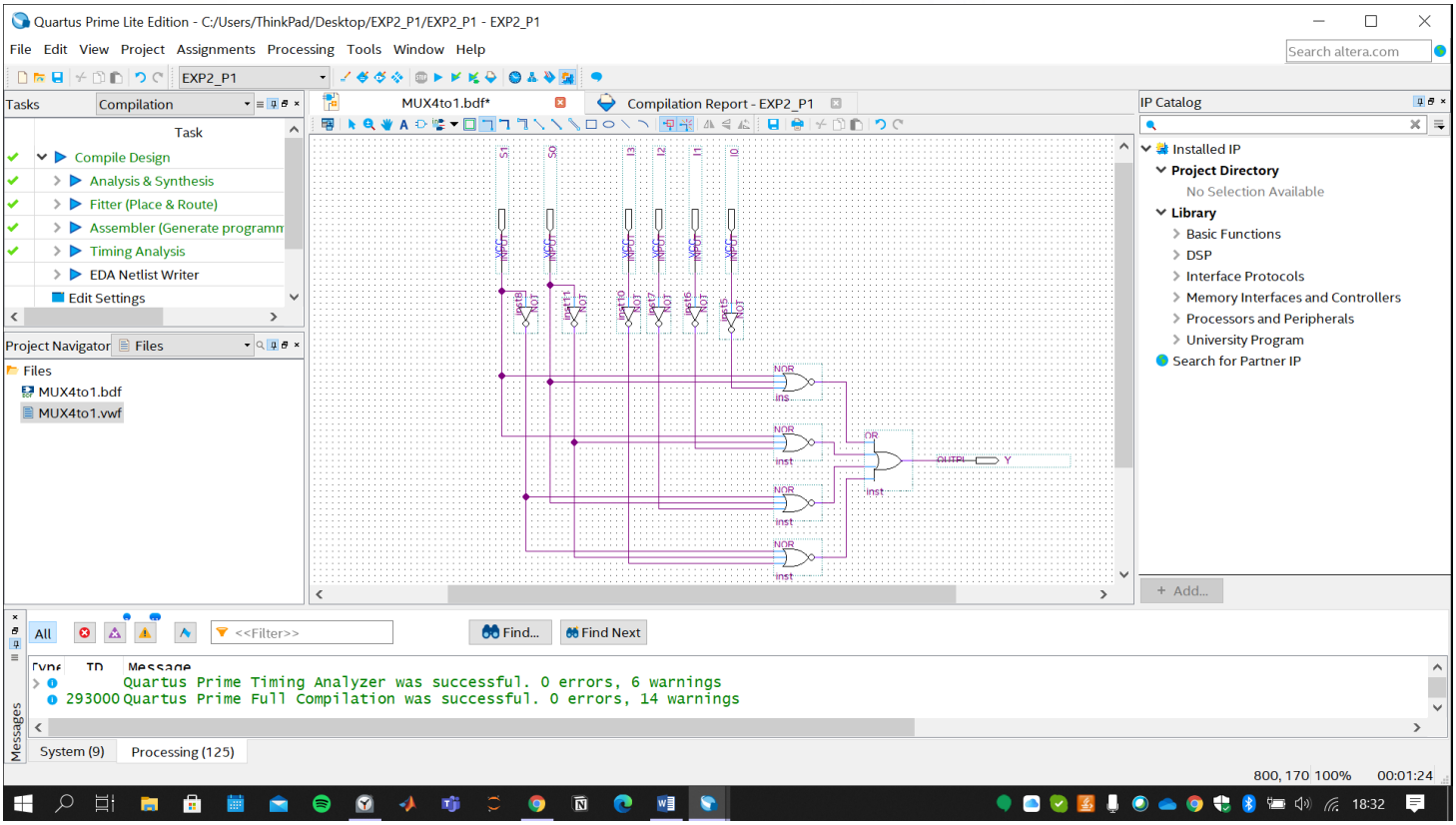
Important Notes:

- You will be expected to provide screenshots of your designs and simulation results. You have to take full screenshots for all of them. You can use the full-screen mode of the Snipping Tool for this. **DO NOT crop** any image.
- If the image is too dense or too small that makes it difficult to view, then add zoomed-in images as EXTRAS (again full screenshots).
- You will name your report as "**Exp# _ Report_StudentID.pdf**
- You may make comments if any discrepancy occurs between your results and your expectations. You can write your expectations, possible reasons of that discrepancy, etc. below related section. **In addition to this report, DO NOT FORGET to upload your project files at the end of each part.**

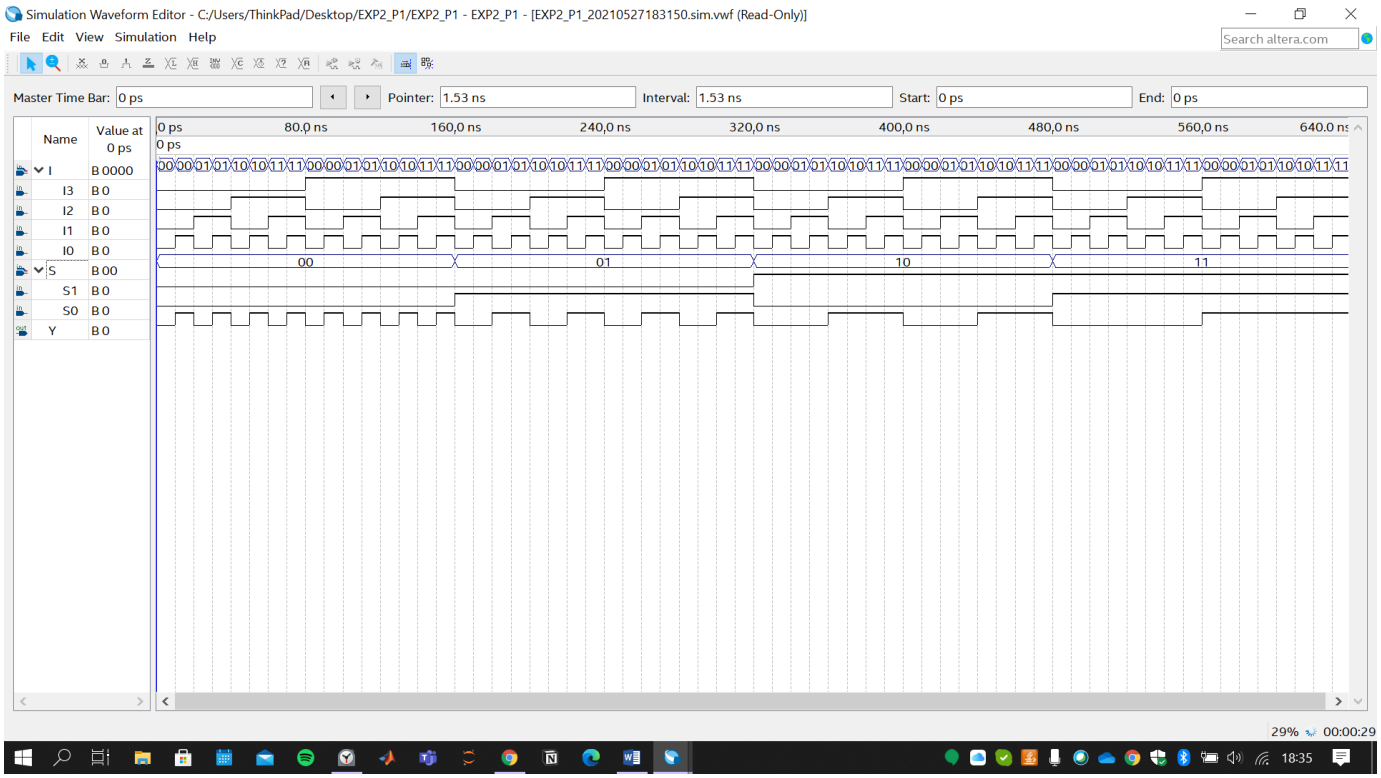
A. 4-to-1 MUX

A1) Please post the screenshot of the block diagram of the 4-to-1 multiplexer that you have designed. Make sure the blocks and the wiring are clearly visible. Briefly explain the methodology behind your design.





A2) Put the screenshot of the simulation results of the 4-to-1 multiplexer. Please make sure there are enough examples of each condition in the sample set, which are clearly visible in the screenshot.



B. 16-to-1 MUX

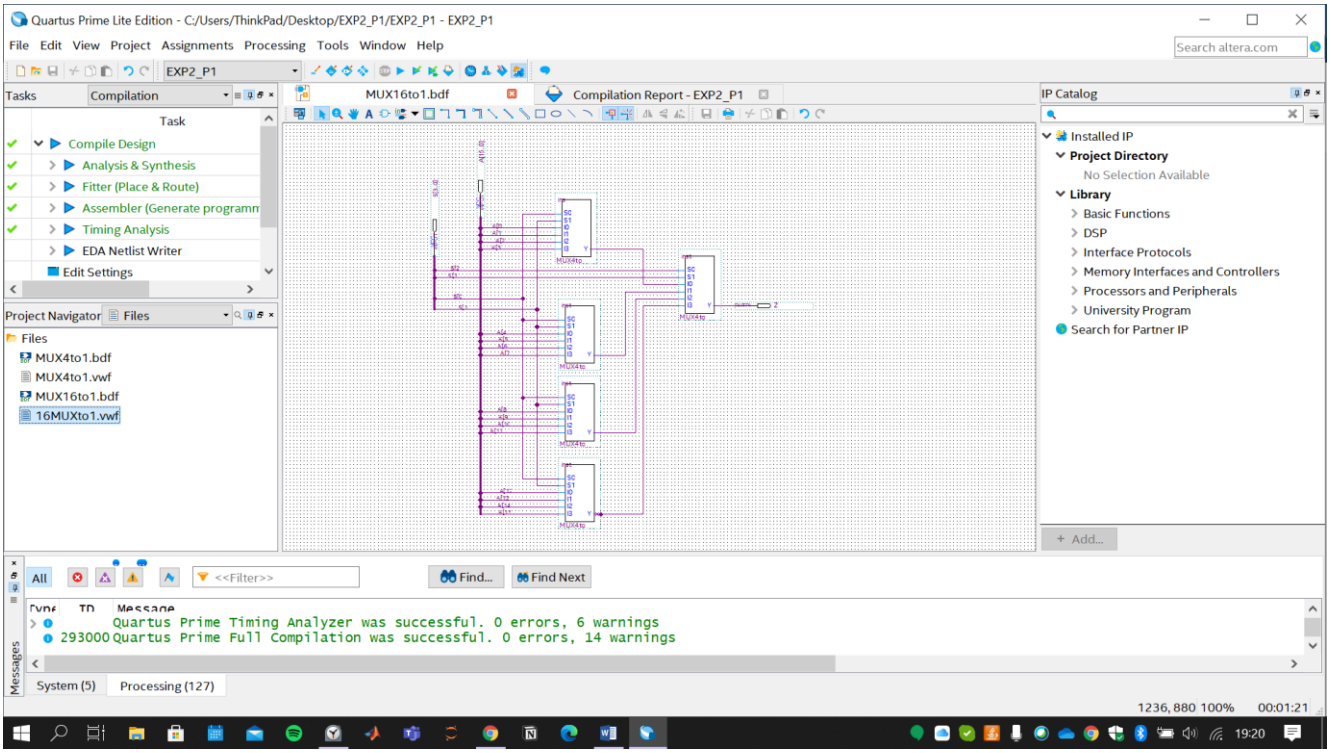
B1) Please put the screenshot of the 16-to-1 multiplexer that you have implemented via the 4-to-1 multiplexers. Pay attention to the clear demonstration of the blocks and the wiring between the blocks. Briefly explain your approach on the design task.

To implement 16-to-1 MUX, firstly four 4-to-1 MUX are used to connect 16 inputs and select inputs (S1, S0). Inputs are generated from one 16-bit-bus.

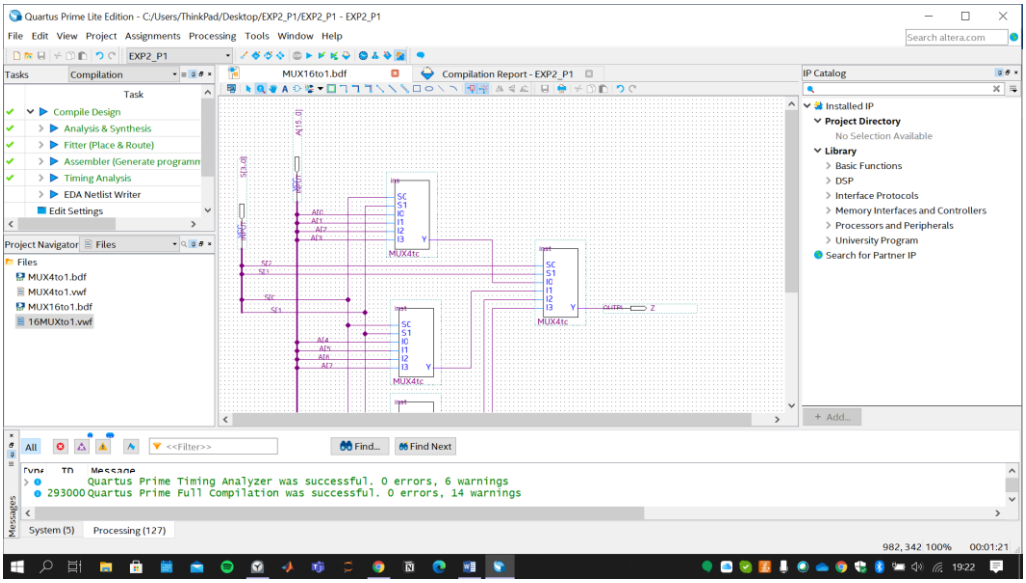
Then, outputs coming from these MUXs are connected to the fifth MUX as inputs to create final output with selects inputs (S3, S2).

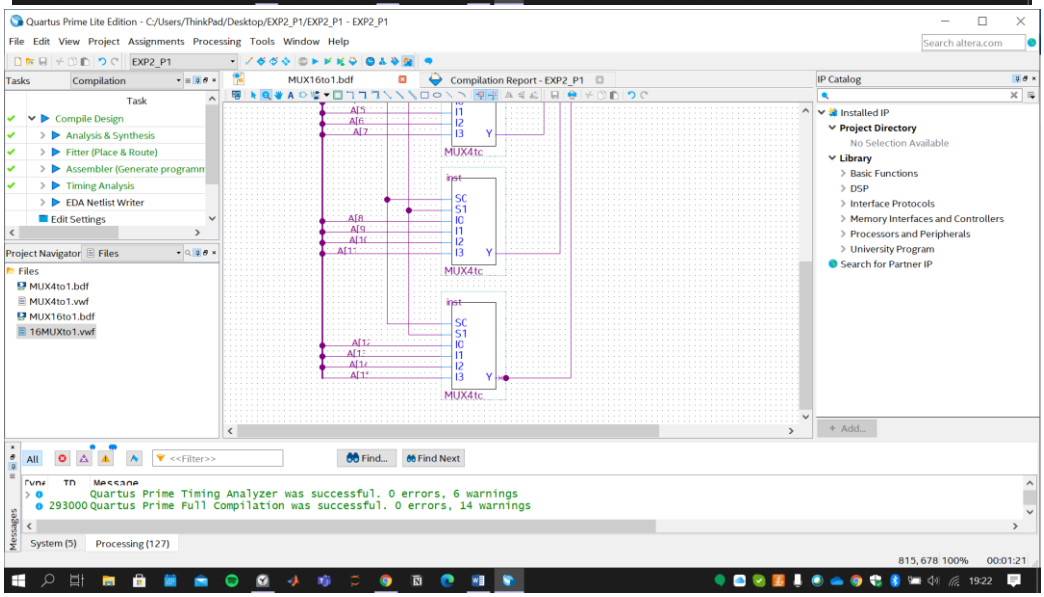
Here, *select inputs* plays crucial role while constructing bigger MUXs. With the help of four select inputs (S3, S2, S1, S0) one can generate sixteen states.

Thus, from connected input bus; we can select the desired input by determining related select inputs.

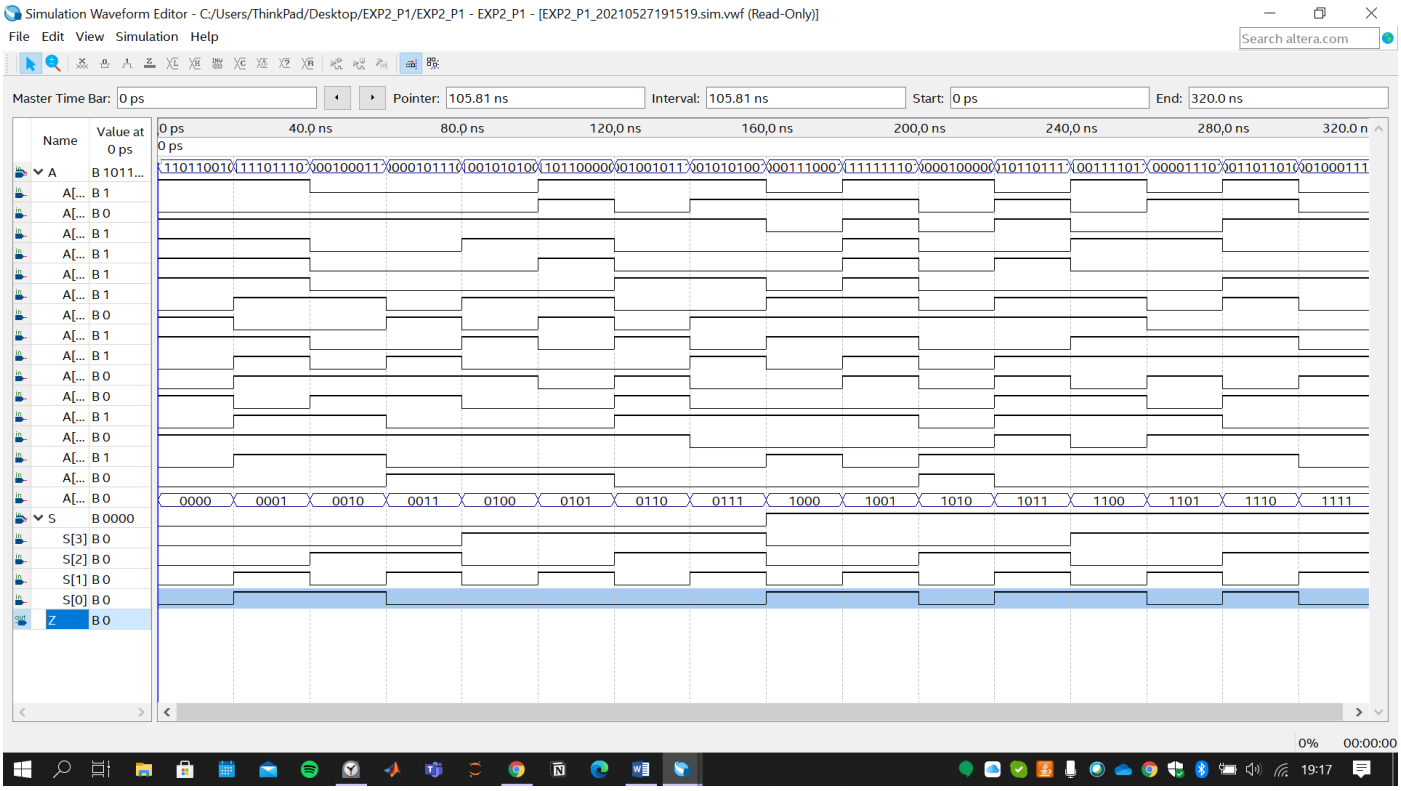


Zoomed-In Pictures:





B2) Put the screenshot of the functional simulation results. Make sure that you have provided the proper operation for each select input configuration.



In this simulation, sixteen states are determined since we have four select inputs (S3, S2, S1,S0). Here, inputs coming from A Bus are *randomly* chosen. From output (Z) we can observe that the result meets the expectation. According to the select input state, related A[i] input is reflected to the output. For instance: S=1000 -> Z=1 where A[8]=1.

C. Implementation of the Function

C1) Please write down the function that you are asked to implement with using 4-to-1 multiplexers.

$$f(w,x,y,z) = (xy + x'y')(wz + w'z')$$

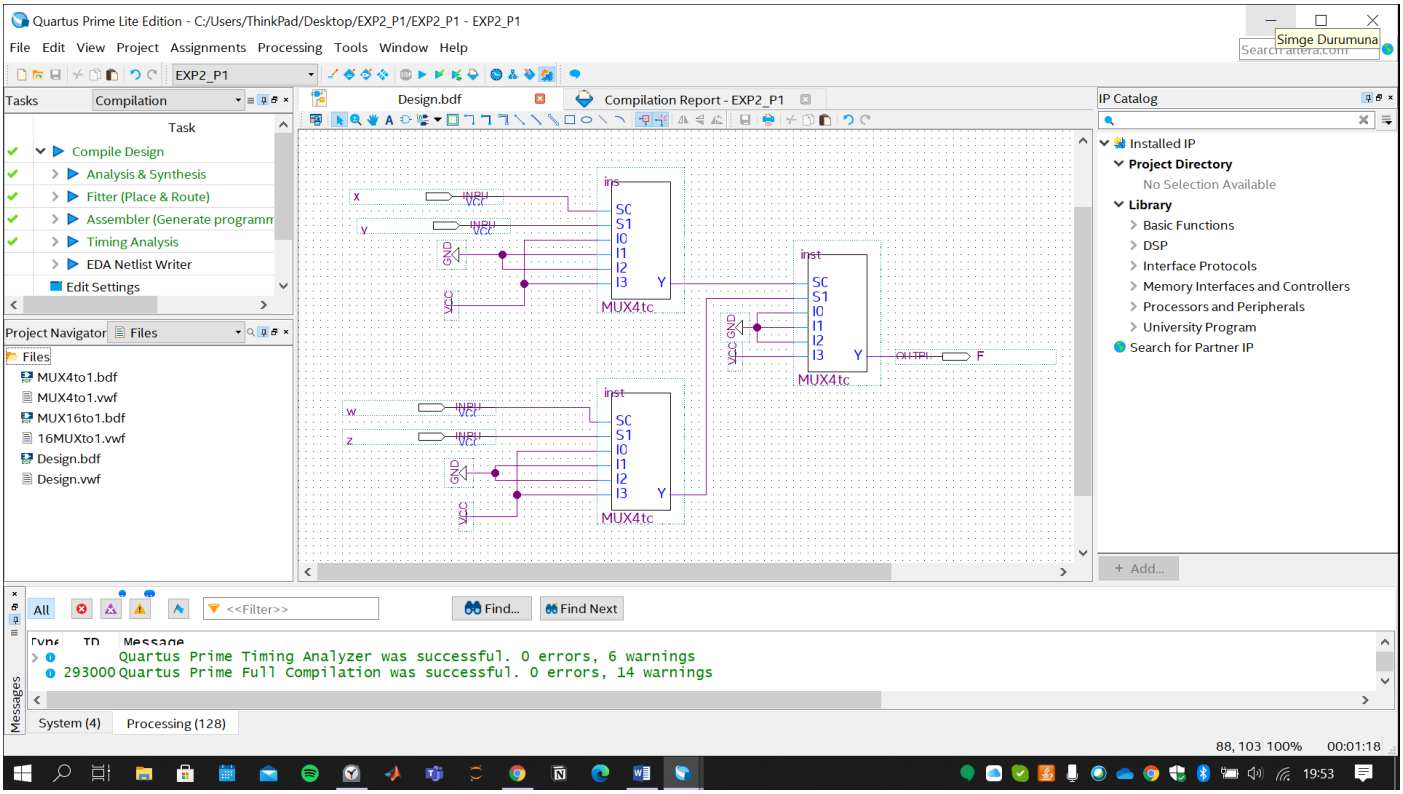
C2) Please post the screenshot of the final schematic of your design. Pay attention to the visibility of the blocks and the wiring. Explain your design methodology.

f can be divided into two equations being $(xy + x'y')$ and $(wz + w'z')$

Using x and y as select inputs for one 4-to-1 MUX, $(xy + x'y')$ can be obtained as output.

Similarly, using w and z as select inputs for the other 4-to-1 MUX, $(wz + w'z')$ can be obtained as output. For both case I0 and I3 should be Logic 1 and I2 and I1 should be 0.

Afterwards, to apply AND gates I3 is connected to the Logic 1 whereas, others are grounded. Thus, connecting $(xy + x'y')$ and $(wz + w'z')$ to the select inputs of the last 4-to-1 MUX yields F as the output.



C3) Put the screenshot of the proper simulation results of your design. Make sure you properly demonstrate the correct operation of your circuitry.