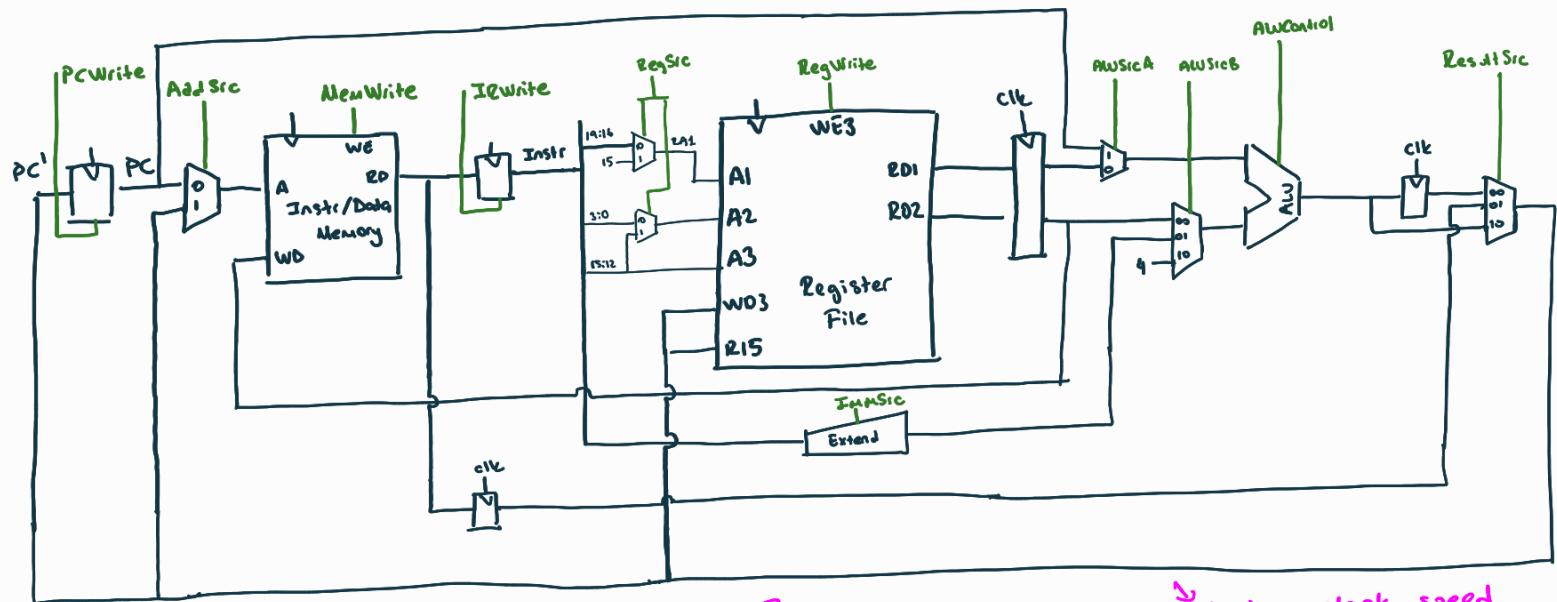


MULTI CYCLE PROCESSOR

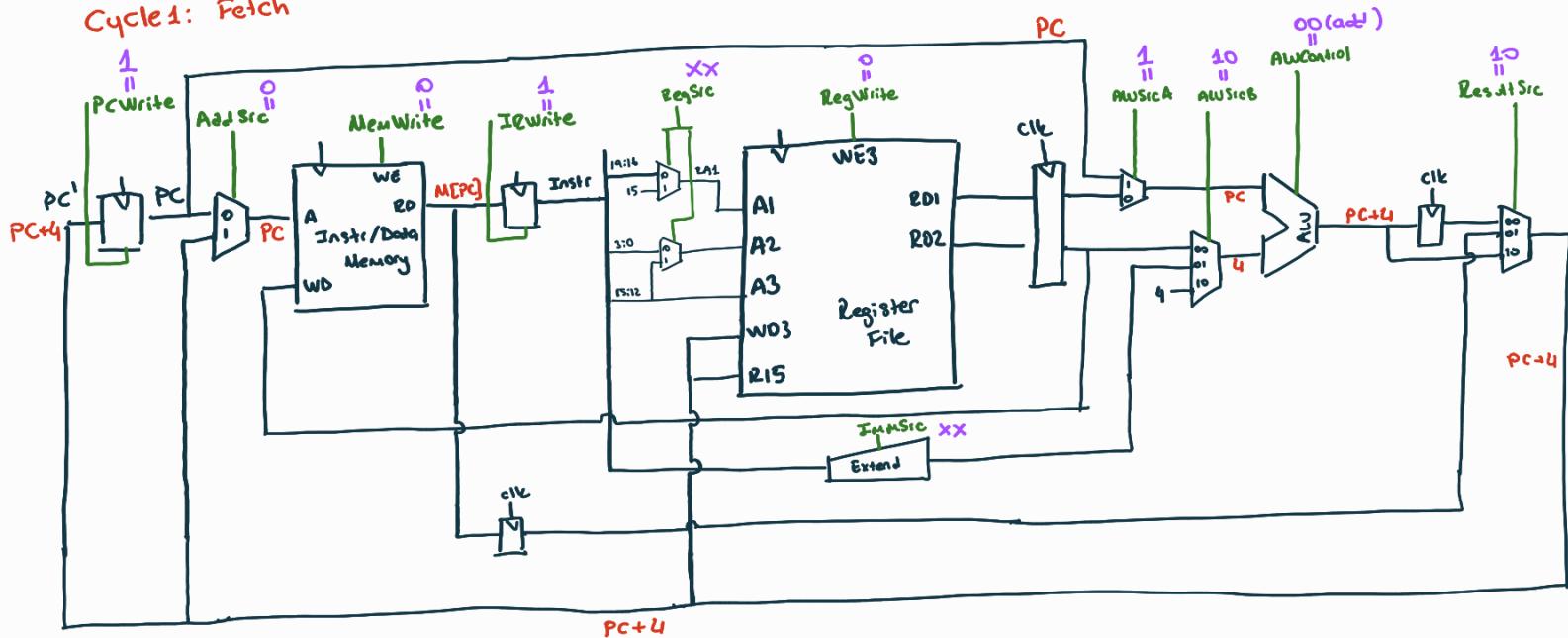
Reference: Ece GÜRAN SCHMITT'S EE441
lecture Notes (Harris Book)



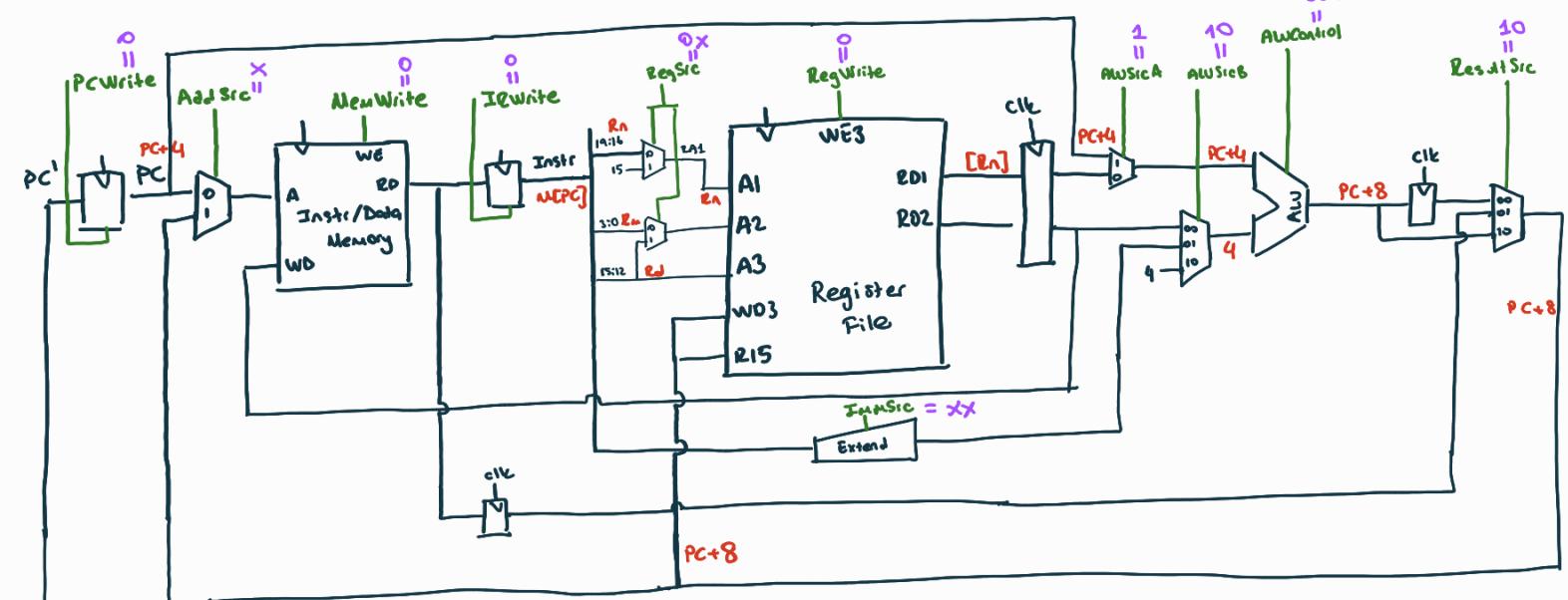
MEMORY PROCESS \rightarrow LDR Rd , [Rn, imm12]

higher clock speed

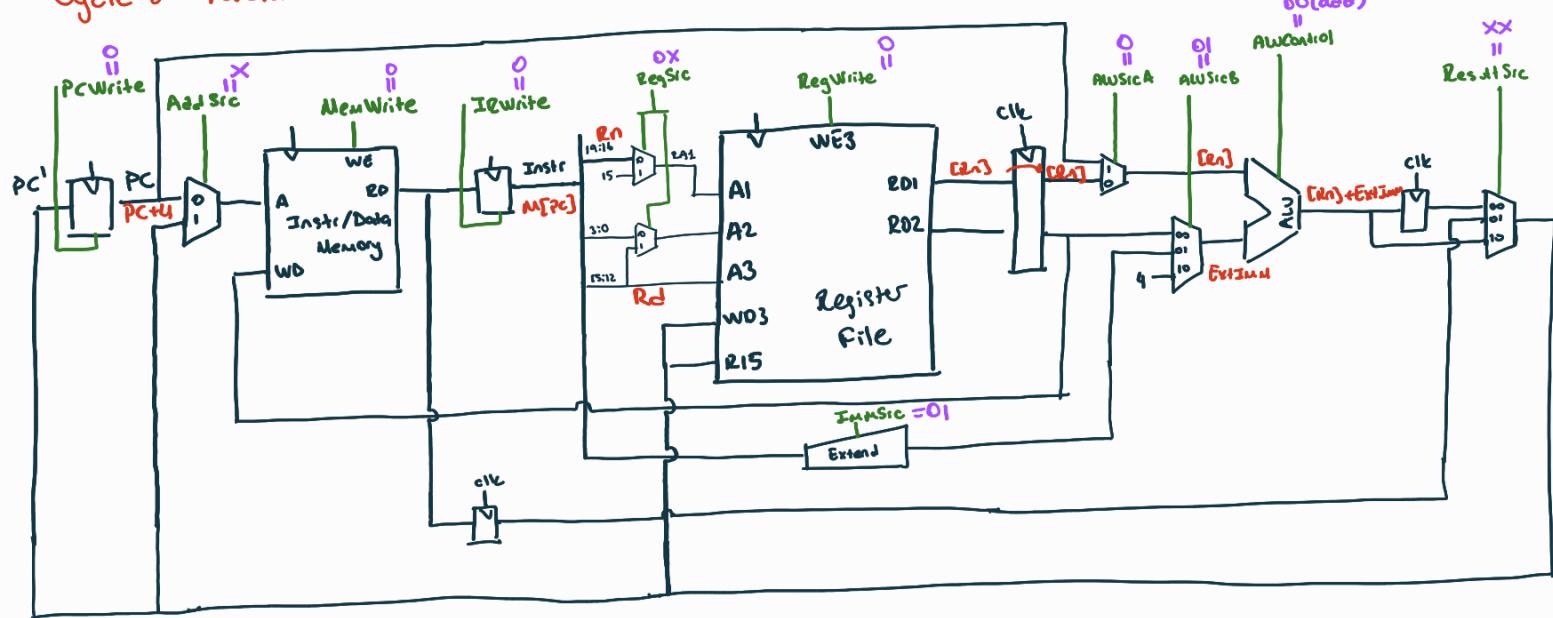
Cycle 1: Fetch



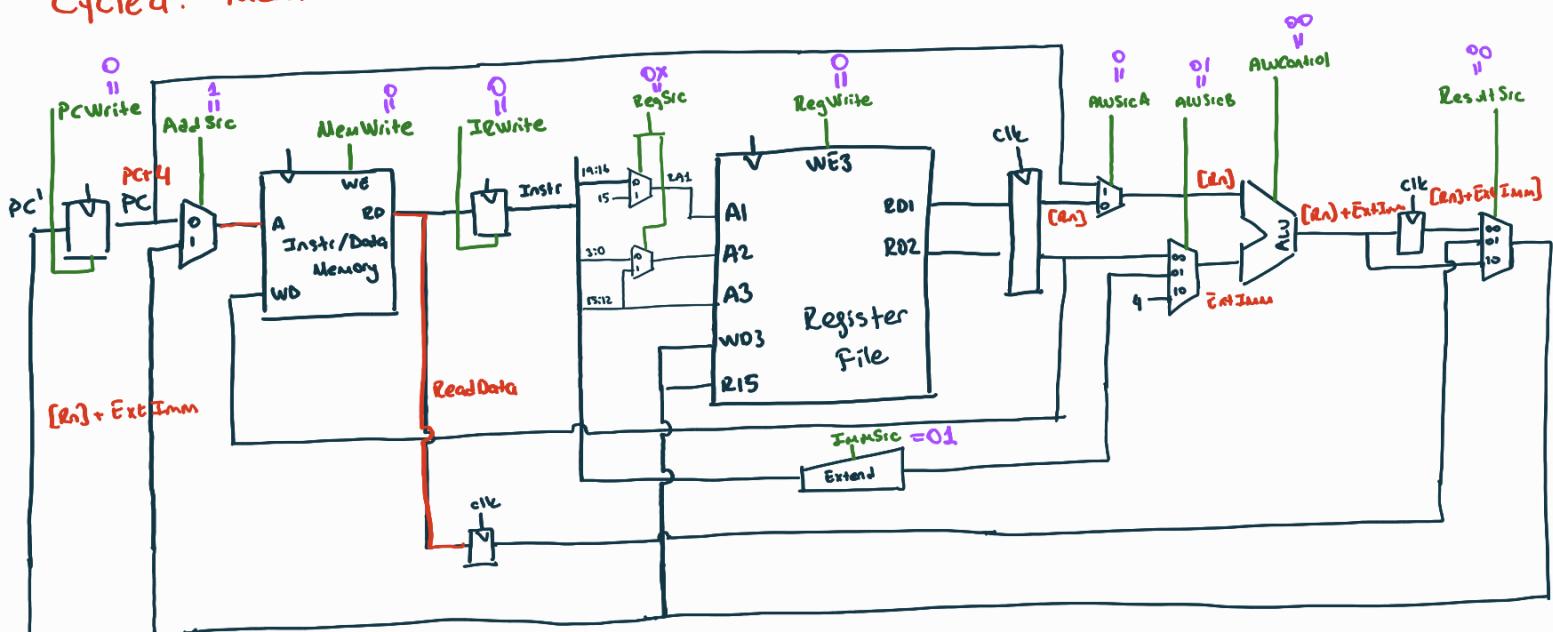
Cycle 2: Decode



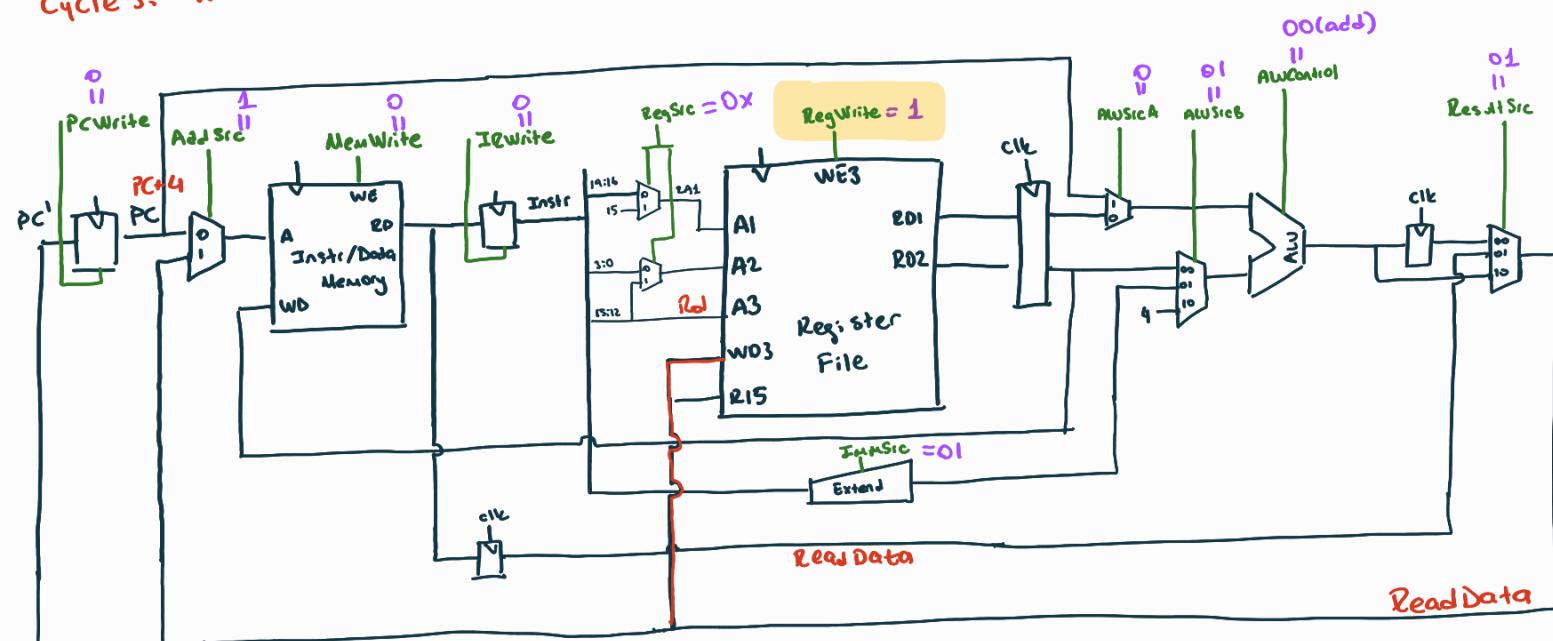
Cycle 3: Mem Addr (Execute ALU)



Cycle 4: Mem Read

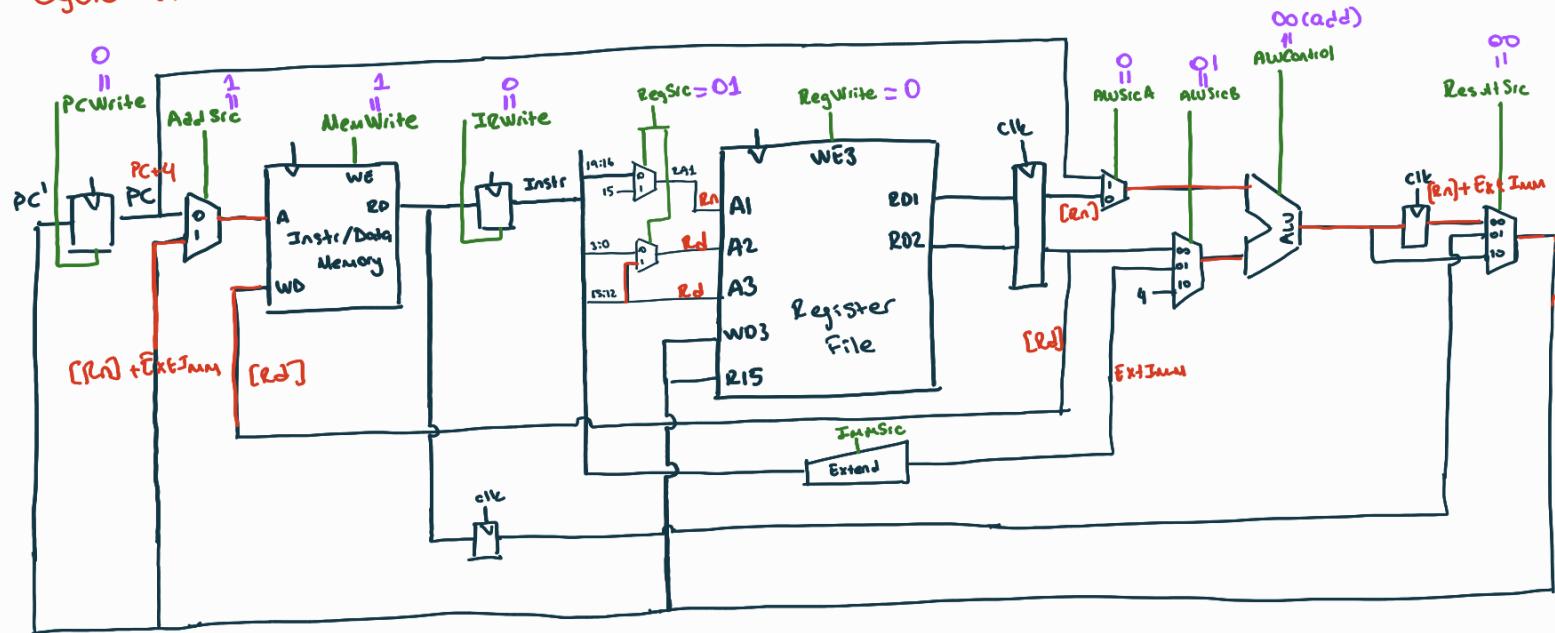


Cycle 5: Writeback



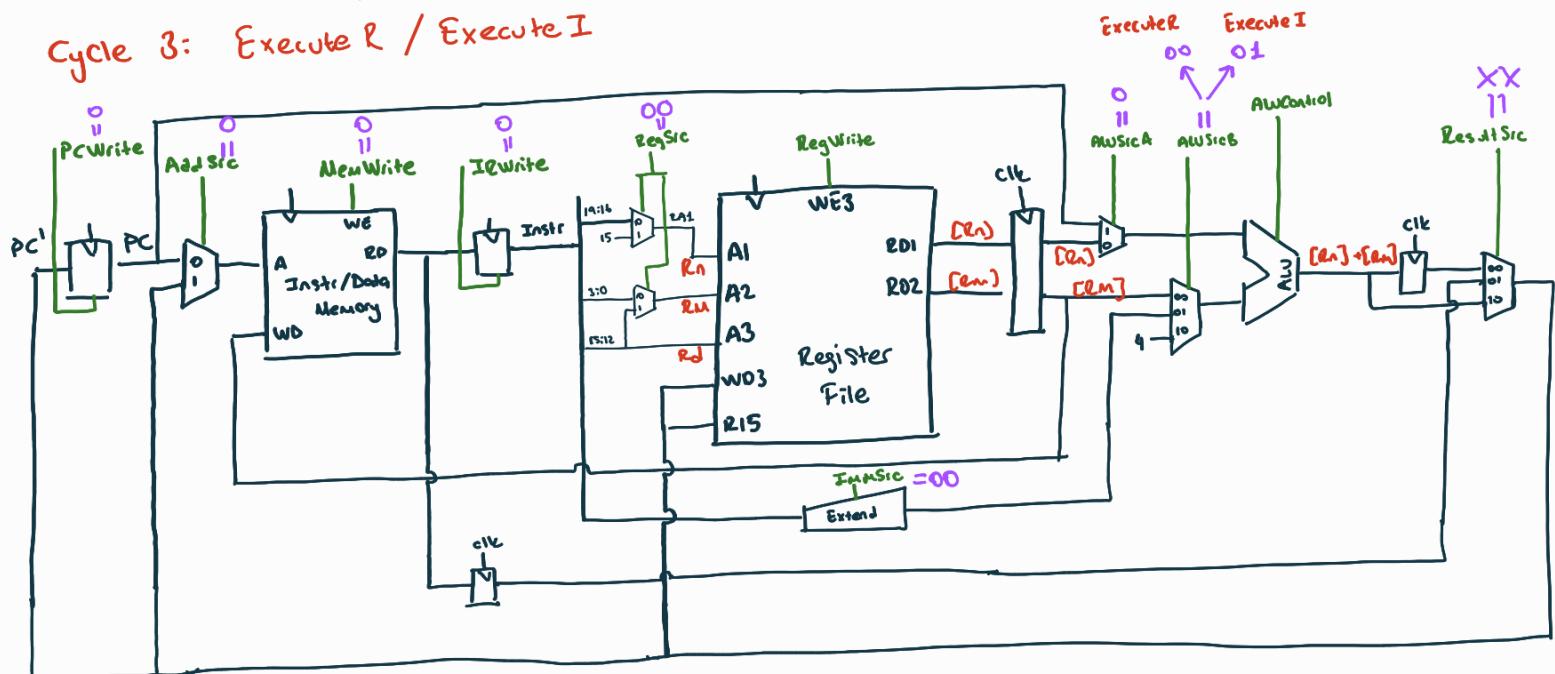
MEMORY PROCESS: STR Rd, [Rn, imm12]

Cycle 4: MemWrite

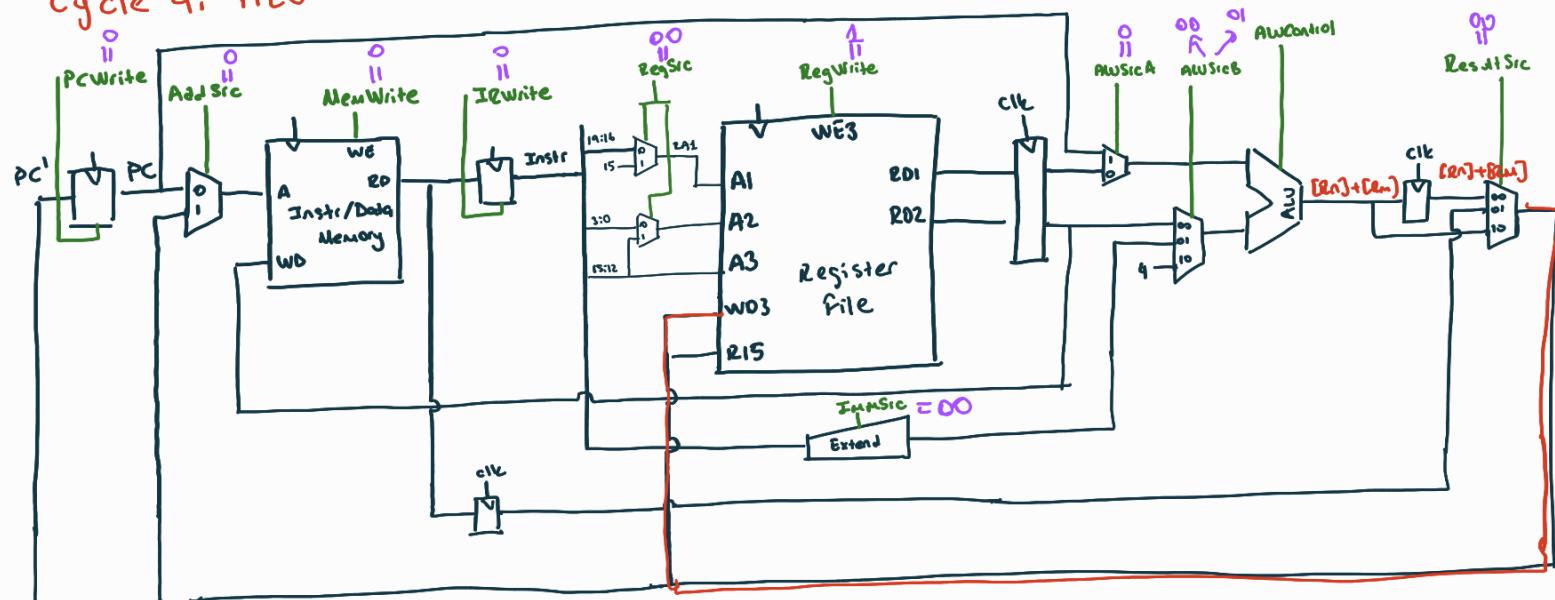


DATA PROCESS: ADD Rd, Rn, Rm
ADD Rds, Rn, Imm

Cycle 3: Execute R / Execute I

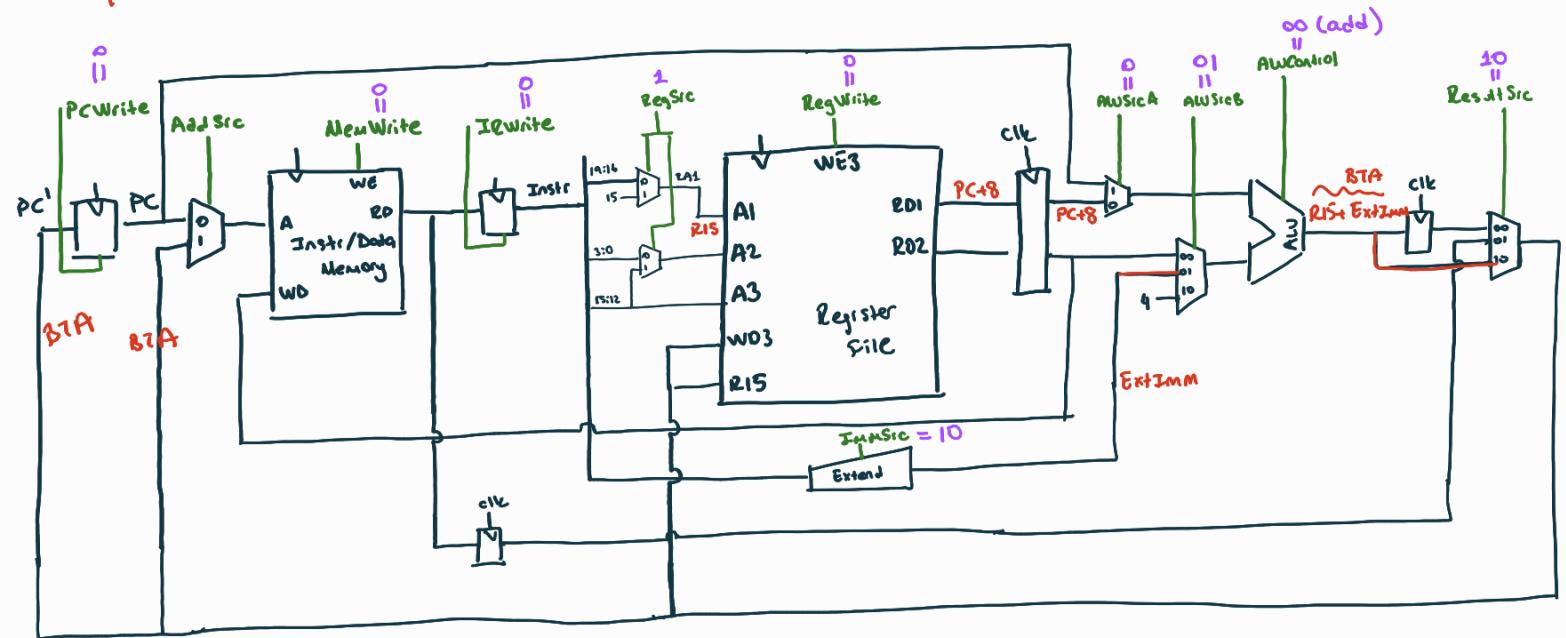


Cycle 4: ALUWriteback

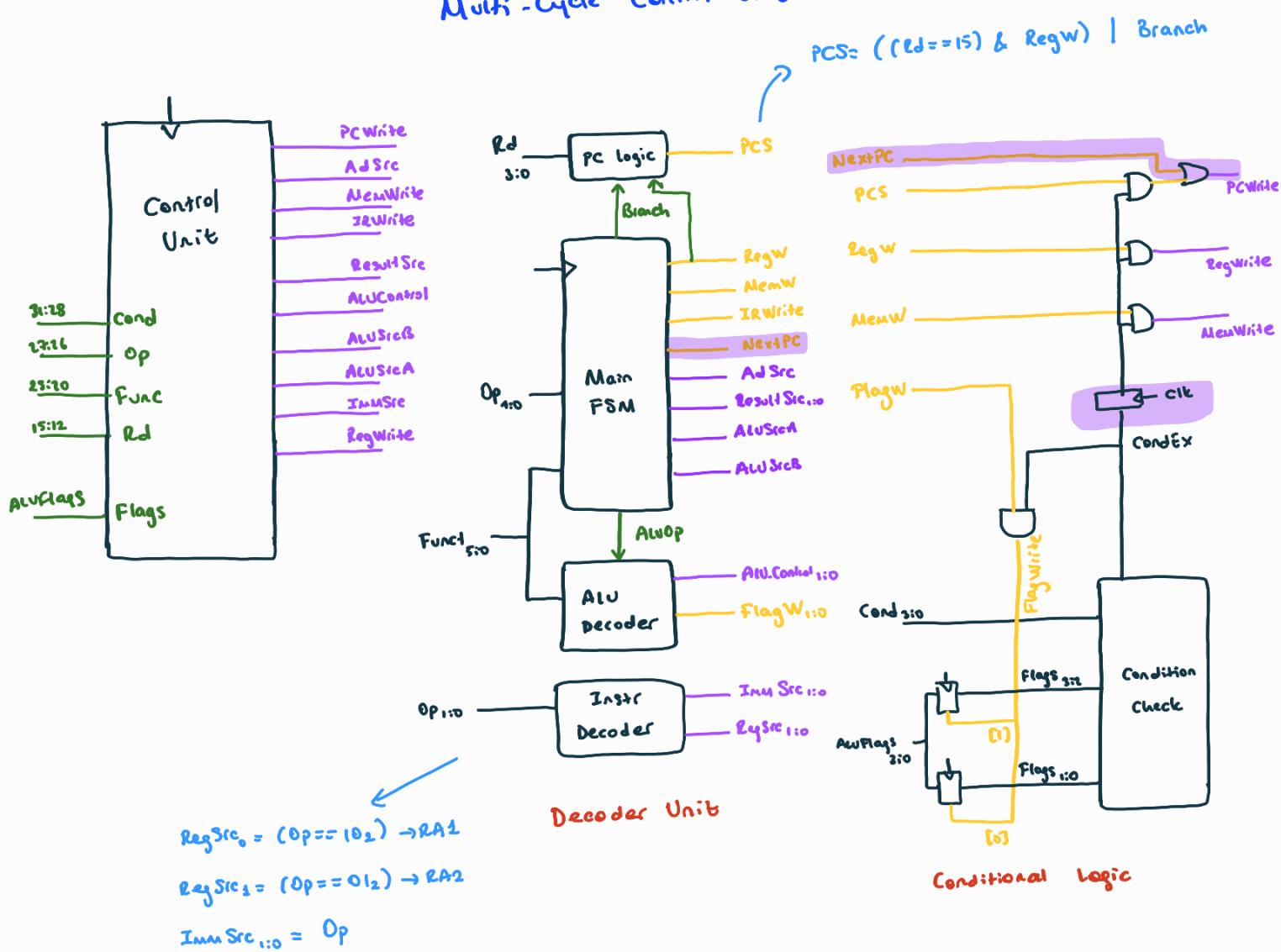


BRANCH

Cycle 3: Branch



Multi-Cycle Control Unit



Multi-PSM



Multi Cycle Performance

3 cycles : B

4 cycles : DP , 8TR

5 cycles : LDR

$$T_{C2} = t_{PCQ} + 2t_{MUX} + \max(t_{AW}, t_{MEM}) + t_{Setup}$$

↓
multicycle critical path

| Ex | %25 | loads | { } |
|-----------------------|-----|---|-----|
| | %10 | stores | |
| | %13 | branches | |
| | %52 | R-type | |
| SPECINT2000 benchmark | | Average CPI = $(0.13) \times 3 + (0.52 + 0.10) \times 4 + 0.15 \times 5 = 4.12$ | |

$$\text{Execution Time} = (\# \text{ instructions}) \times \text{CPI} \times T_c$$

clock cycle time

* It is slower than the single-cycle processor

Question 1

PC = 0xA184

CPSR_{31:18} = 1001

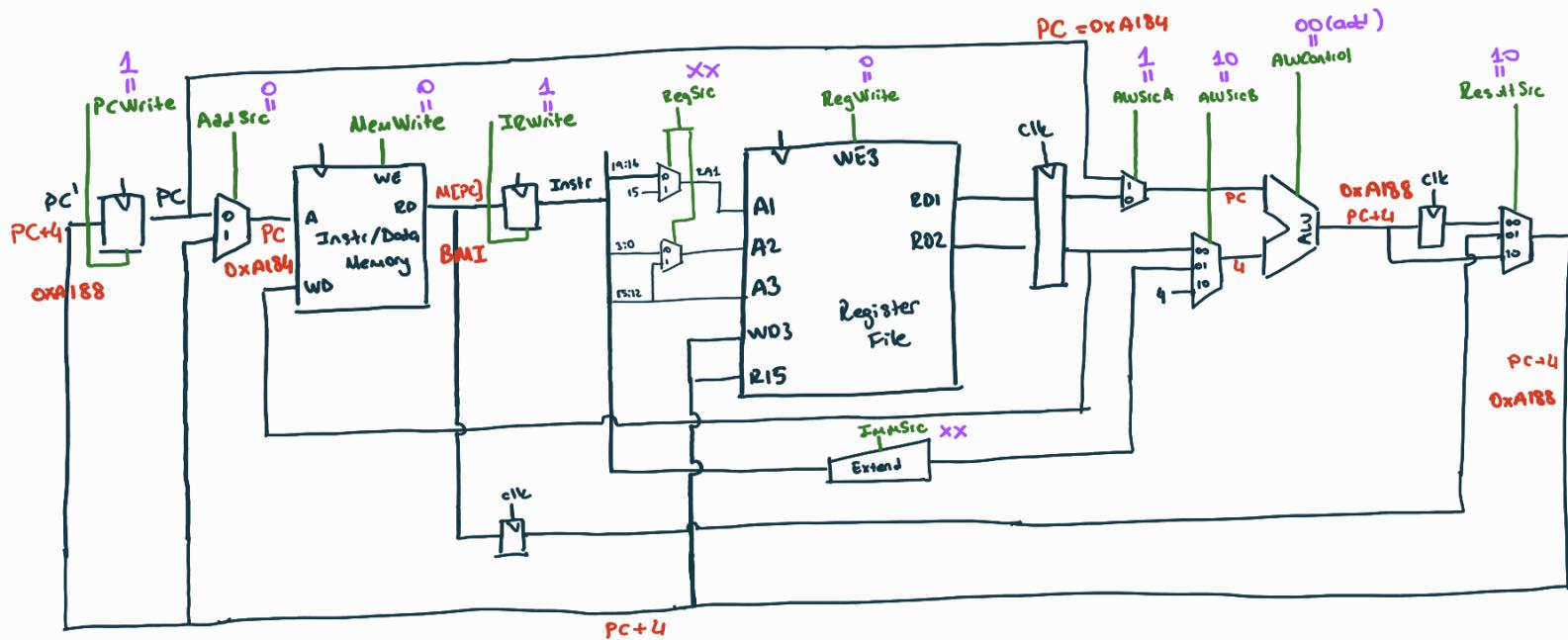
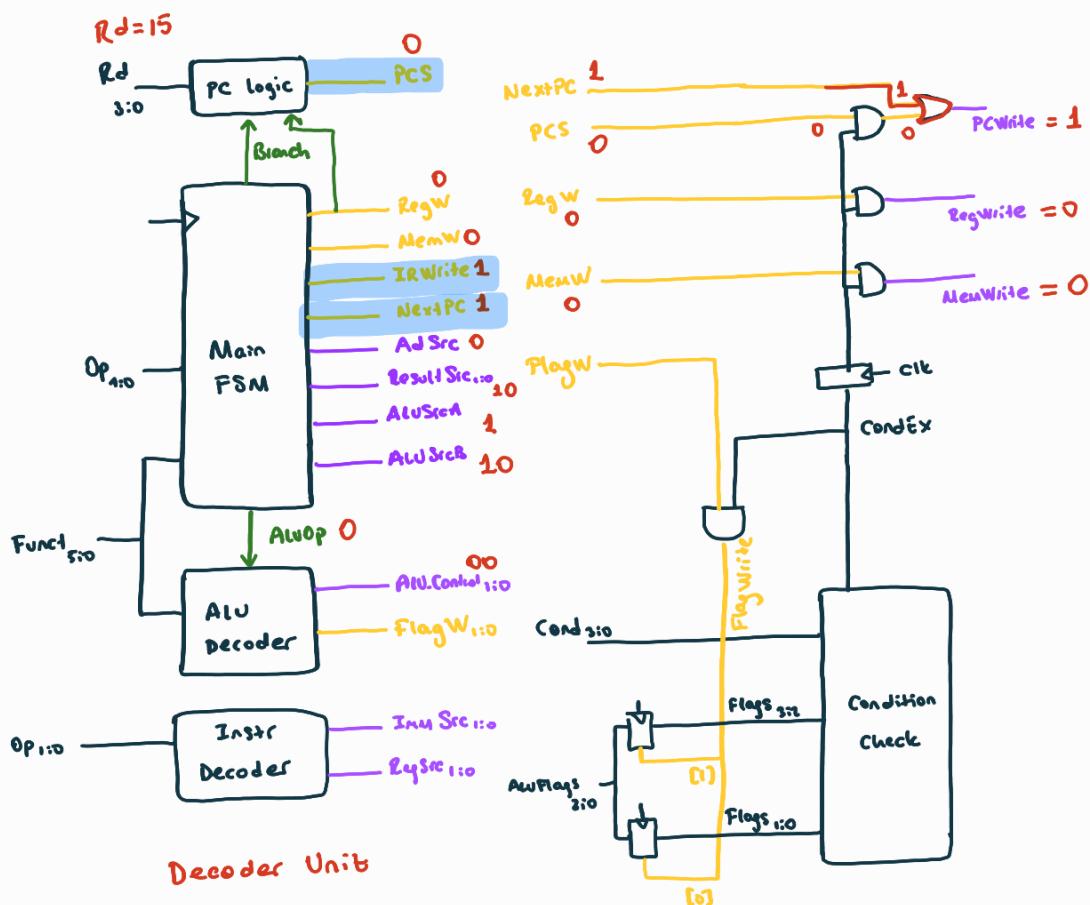
and the ARM assembly code

0xA184 BMI BTA Branch Target Address

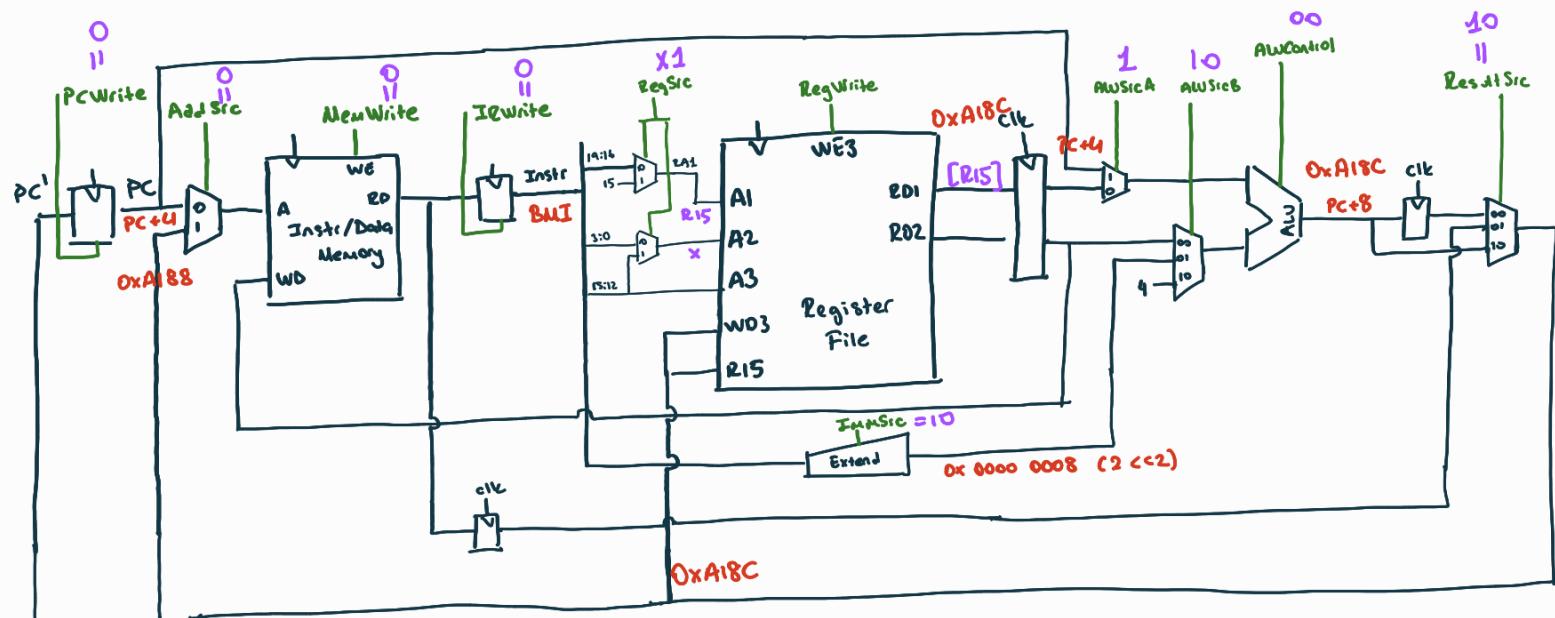
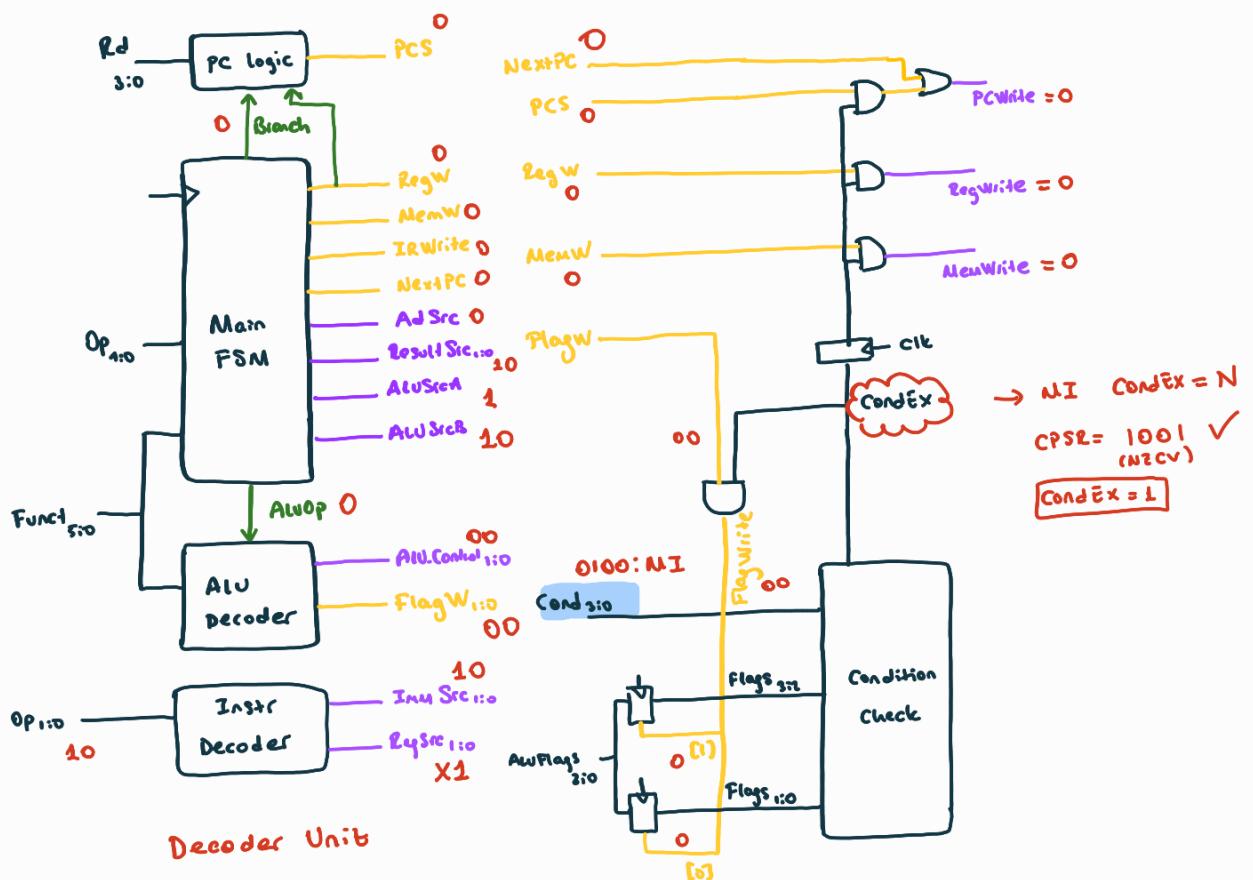
Instruction = 0x4A00 0002

- a) Show all signals in the control and datapath
 b) what are the values of the following after the instruction is executed at the beginning of the + cycle? (PC, CPSR, RIS) input

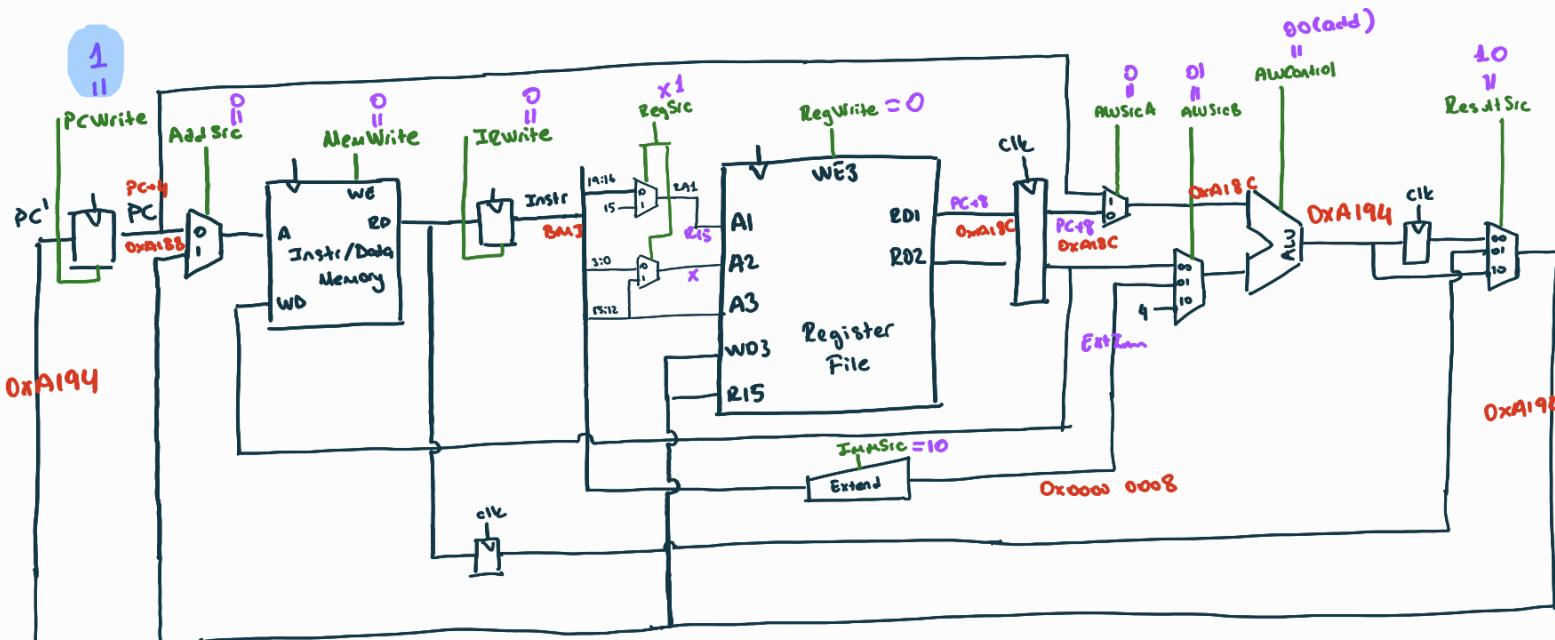
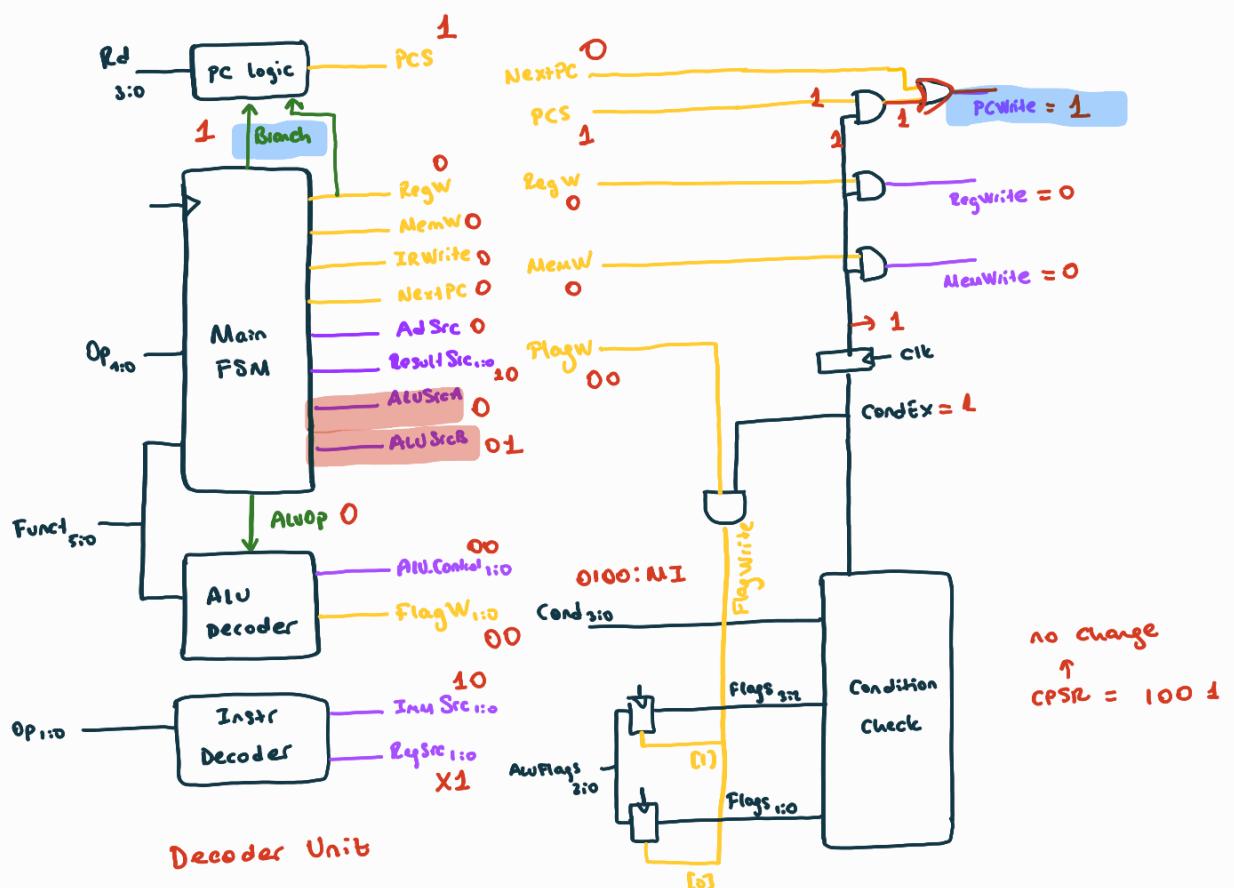
Cycle 1: Fetch



Cycle2: Decode



Cycle 3: Branch



b) At the next fetch cycle

$$PC = 0xA194$$

$CPSR = 1001$ (unchanged)

$$R15 = PC+4 = 0xA198$$

Question 2

Given PC = 0xA100

CPSR_{31:28} = 1100

NZCV = 1100

Instruction: 0x00 95 9003

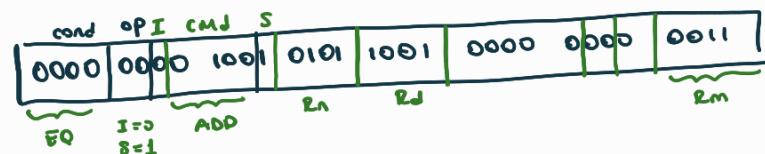
R9 = 0x0000 0000

RS = 0x0000 1EDC

R3 = 0x0000 0000

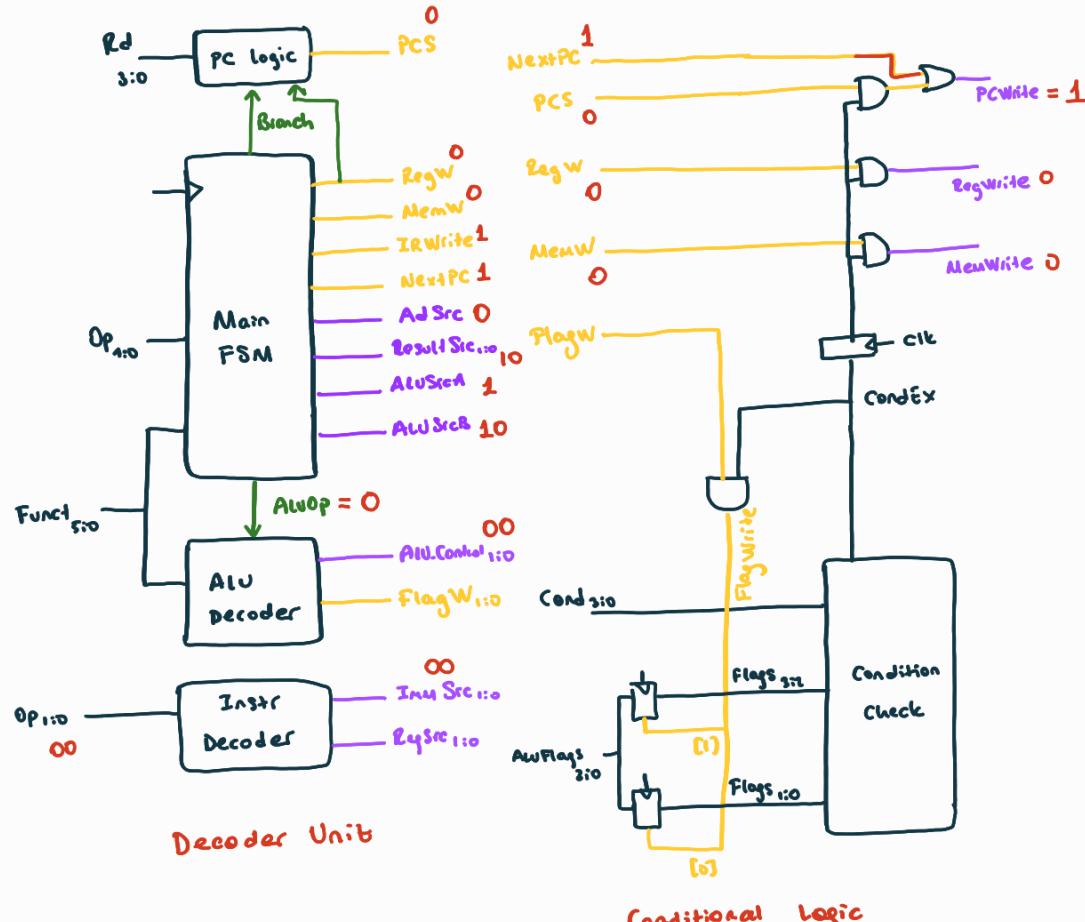
a) Show all signals on control and datapath

b) At the next fetch cycle, values of PC, CPSR, R15, RG

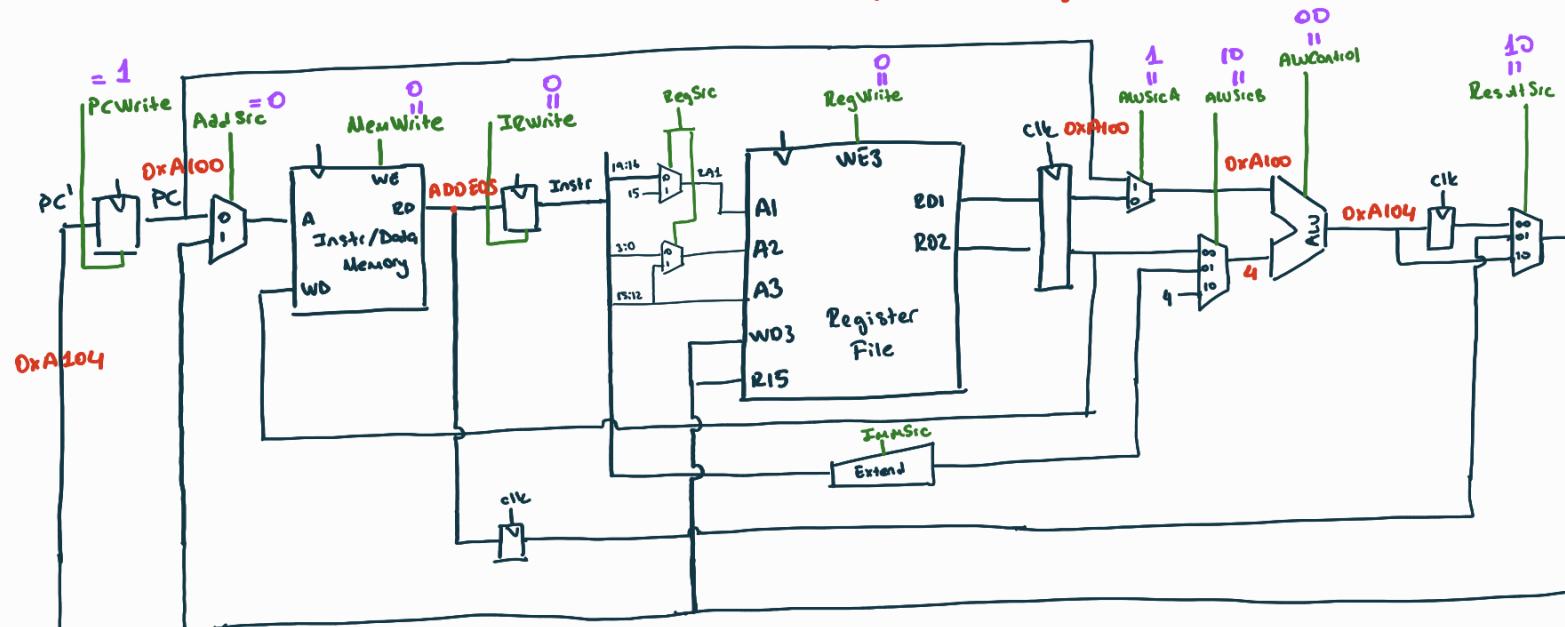


$$\text{CPSR} = 1100 \\ \text{if } Z=1 \quad \checkmark$$

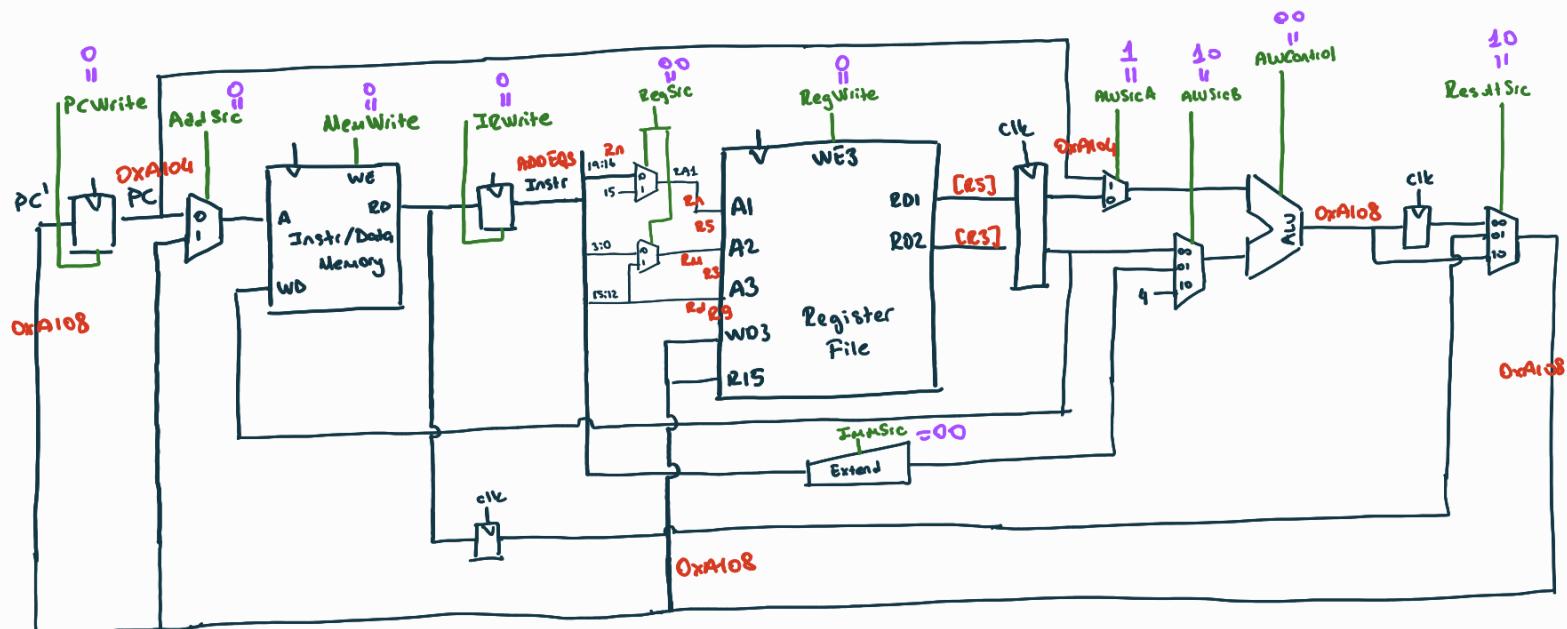
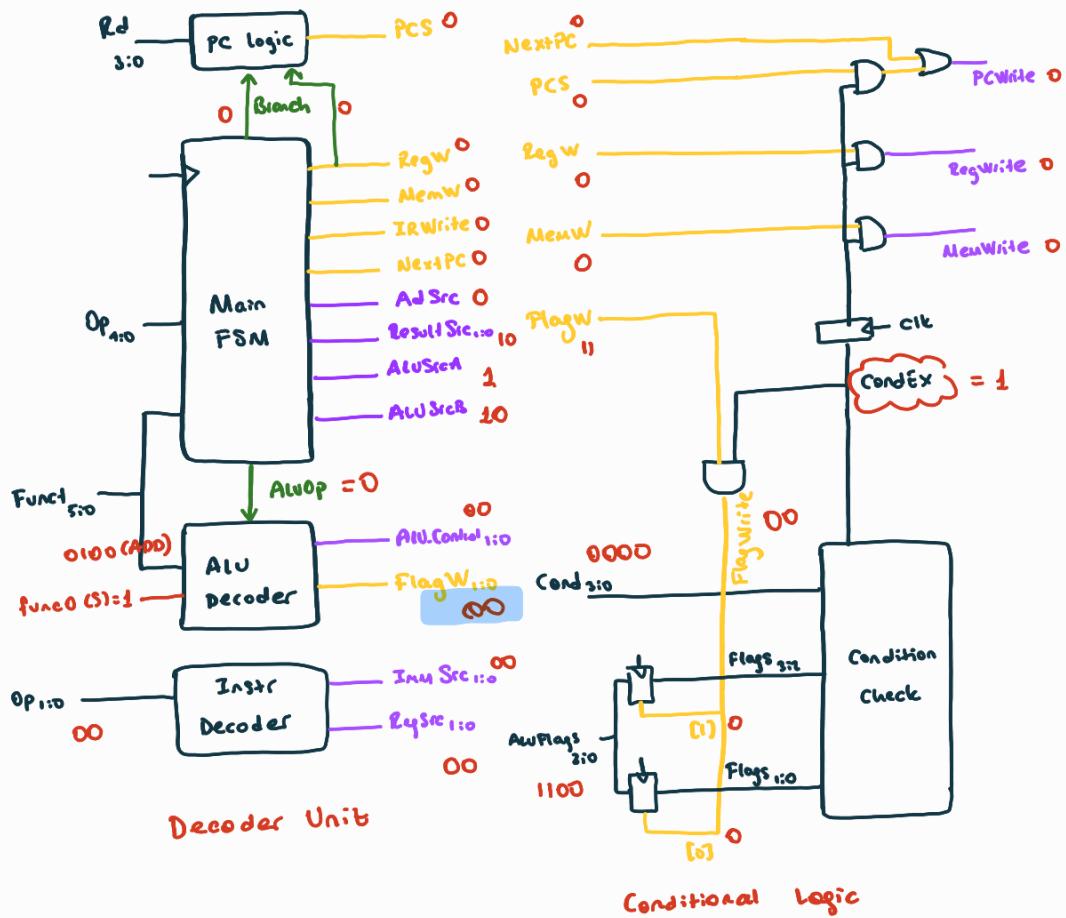
Cycle 1: Fetch



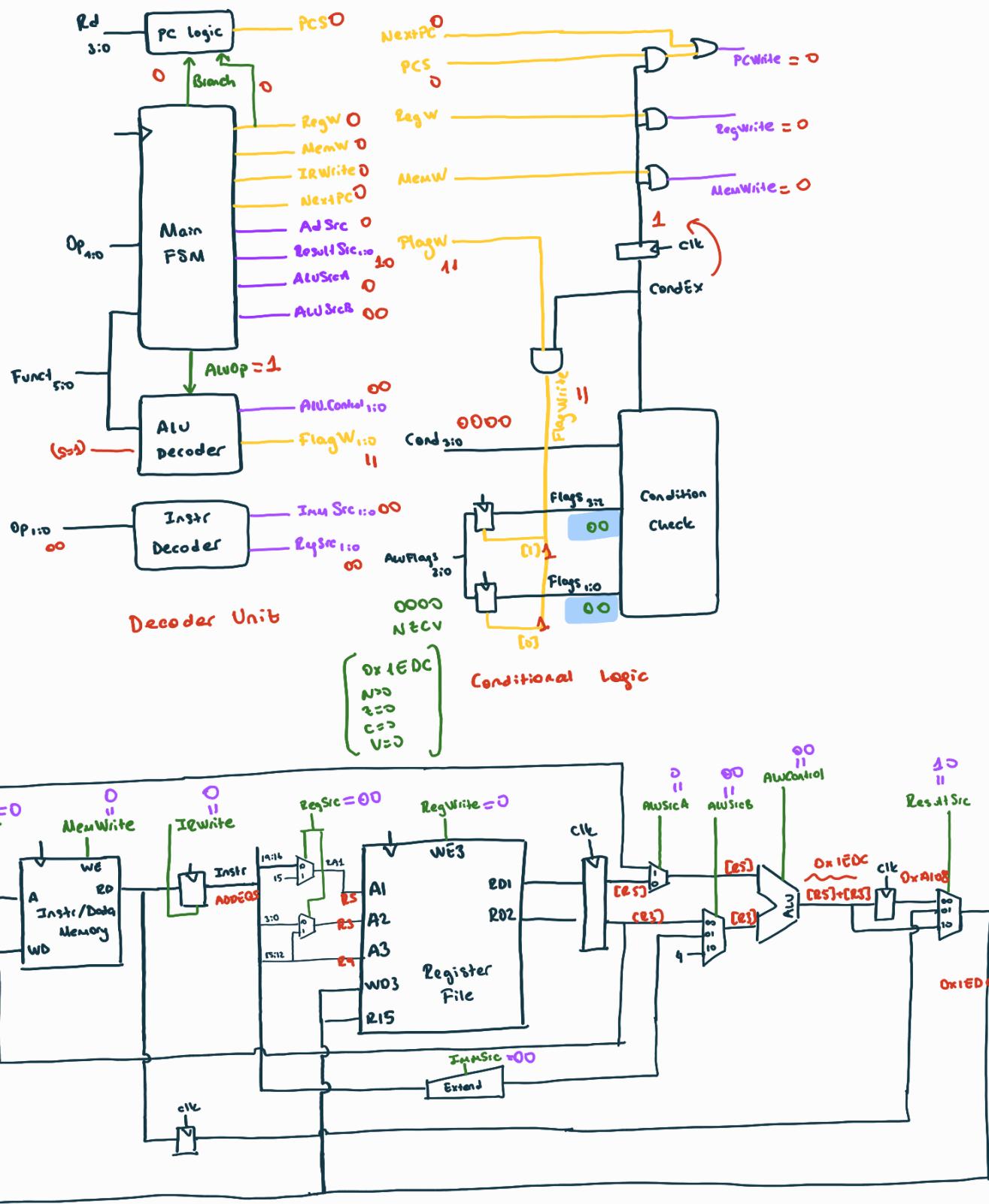
Conditional Logic



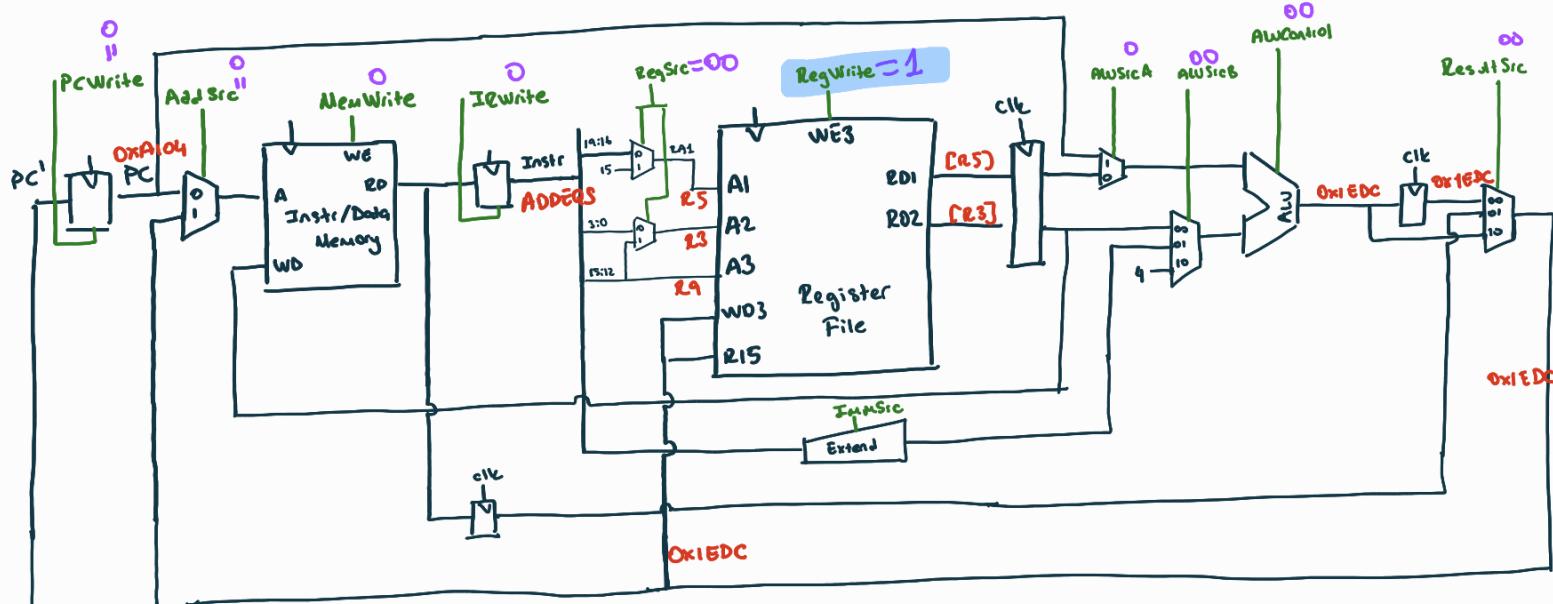
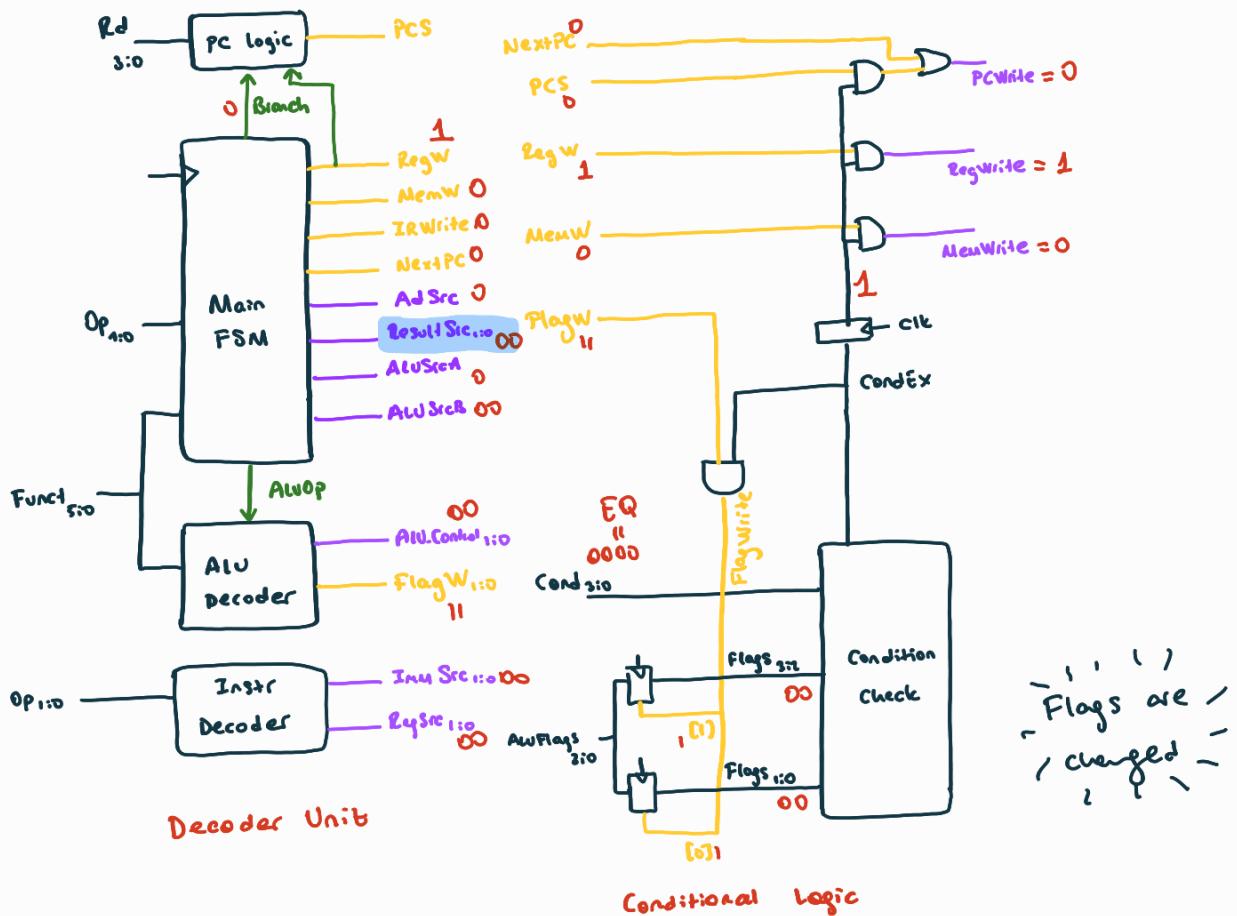
Cycle 2: Decode



Cycle 3: Execute R



Cycle 4: ALU Writeback



$$b) \quad PC = 0xA104$$

$CPSR = 0x0000 \rightarrow \text{changed}$

$$R15 = PC + 4 = 0xA108$$

Question 3

BL (branch with link)

$$LR \leftarrow (PC + 8) - 4 ; PC \leftarrow (PC + 8) + (imm24 \ll 2)$$

