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EXPERIMENT 4. Flip Flops and Sequential Circuits 2

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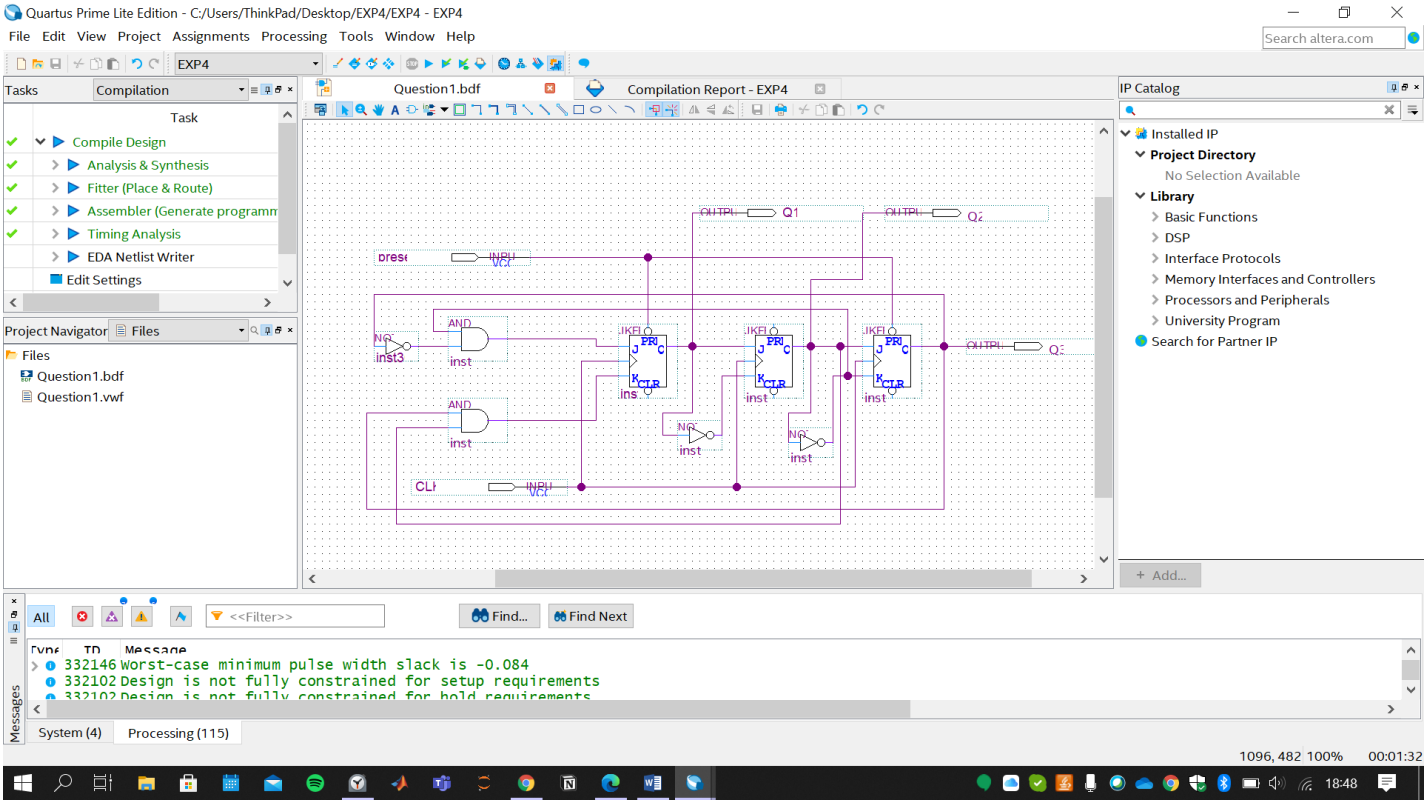
Important Notes:

- You will be expected to provide screenshots of your designs and simulation results. You have to take full screenshots for all of them. You can use the full-screen mode of the Snipping Tool for this. **DO NOT crop** any image.
- If the image is too dense or too small that makes it difficult to view, then add zoomed-in images as EXTRAS (again full screenshots).
- You will name your report as "**Exp# _ Report_StudentID.pdf**
- You may make comments if any discrepancy occurs between your results and your expectations. You can write your expectations, possible reasons of that discrepancy, etc. below related section. **In addition to this report, DO NOT FORGET to upload your project files at the end of each part.**

Part 1.

A) Put the screenshot of the designed circuit schematic. Make sure the blocks and the wiring are clearly visible. Briefly explain the methodology behind your design. Implement **III.1** in **Experimental Work** on Quartus. Starting from the initial state of $Q_3Q_2Q_1$ = 101, make a functional simulation observing the output for **20 clock pulses**. How does it differ from the one in the **III.1**?



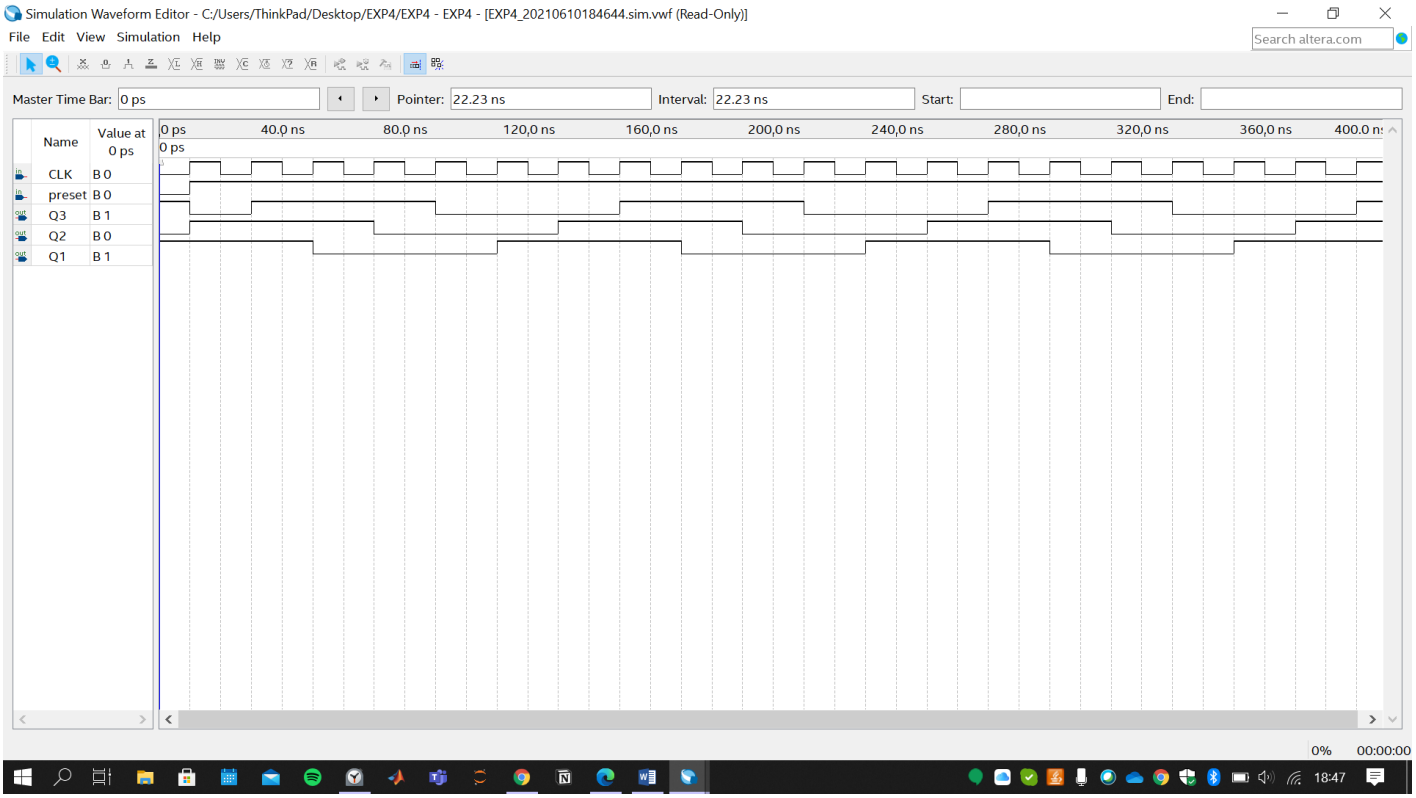
This design is implemented from the Fig.1 of the Exp 4 Manuel.

To implement desired initial states additional (Q3Q2Q1=101) preset input is introduced.

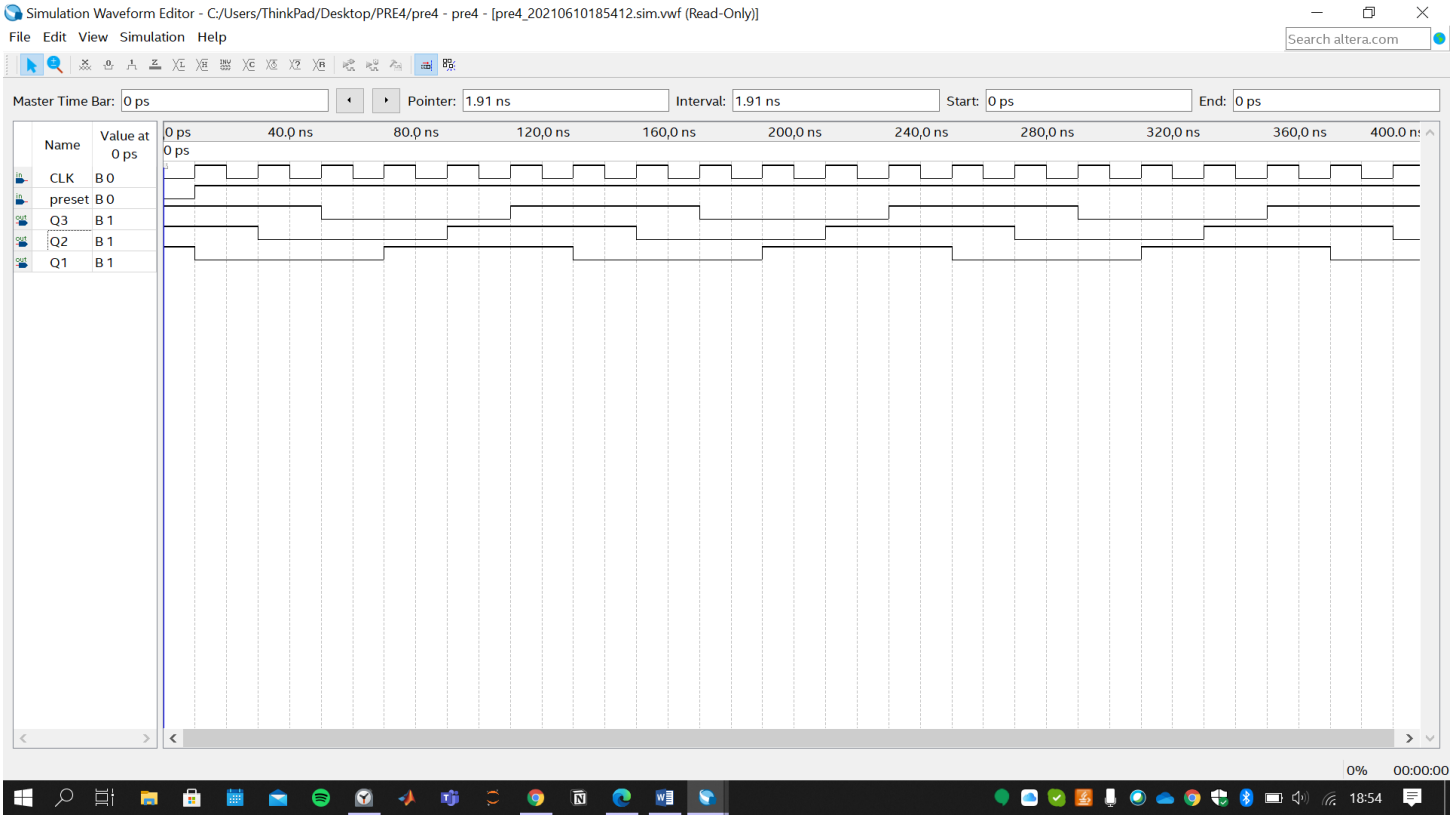
Preset is connected to the PRN inputs of the first and third FFs.

When the LOW input is applied from the Preset input before the first clock pulse, initial states of 1st and 3rd FFs become 1. 2nd is initially zero due to the Quartus property.

B) Put the screenshot of the required simulation result. Please make sure there are enough examples of each condition in the sample set, which are clearly visible in the screenshot.



Functional Simulation of the Circuit When The Input is Q3Q2Q1=101



Functional Simulation of the Circuit When the Input is Q3Q2Q1=111

Comment:

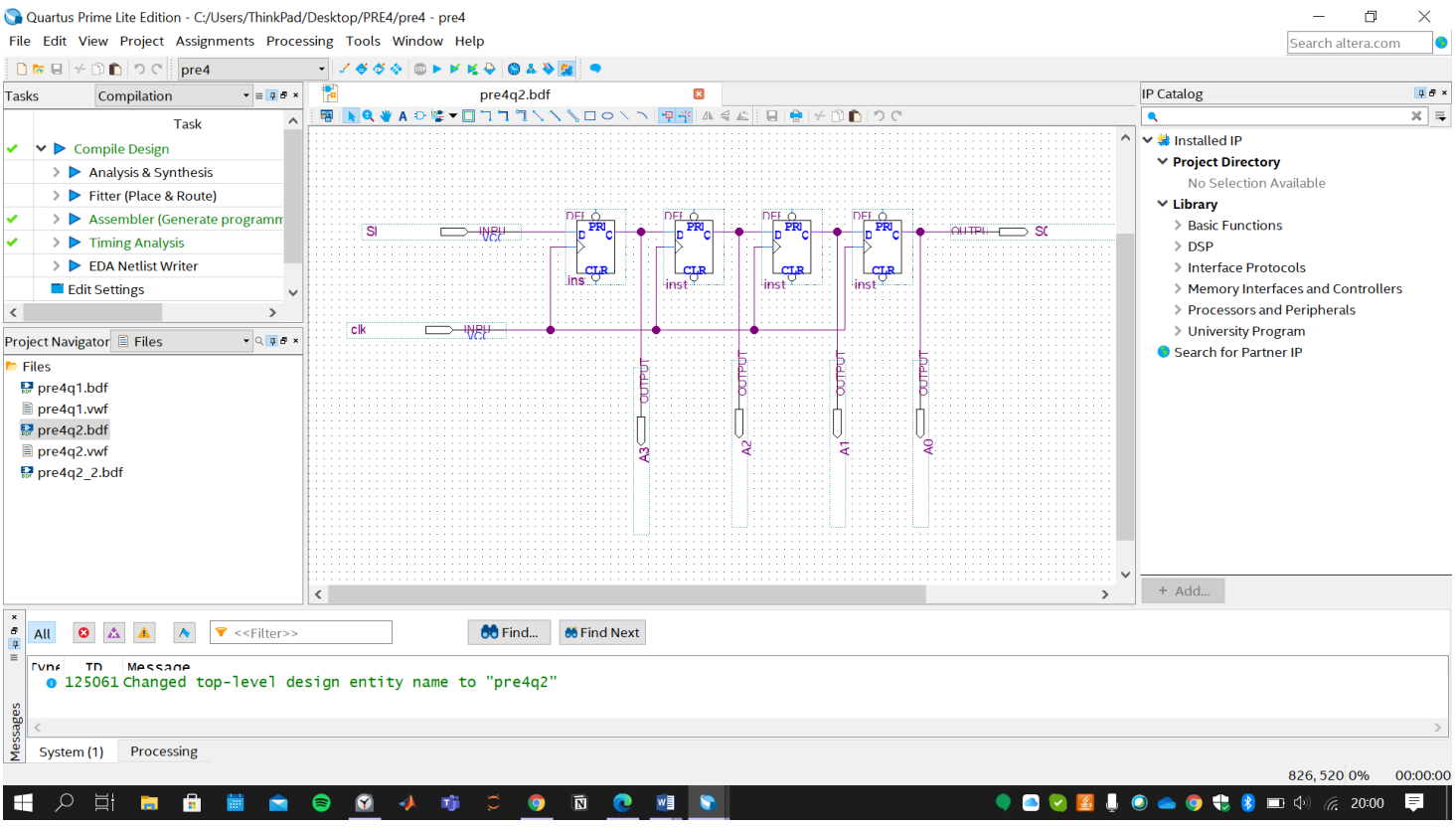
Time	Q1Q2Q3
0	111
1	011
2	001
3	000
4	100
5	110
6	111
7	011
8	001

Time	Q1Q2Q3
0	101
1	110
2	111
3	011
4	000
5	100
6	110
7	110
8	111

Initial state with Q1Q2Q3=101 is similar to initial state (1,1,1) case.
It is the two clock pulse delayed version of (1,1,1)case.
Looking at the state tables, one can say six pulse periodic pulses are generated

Part 2.

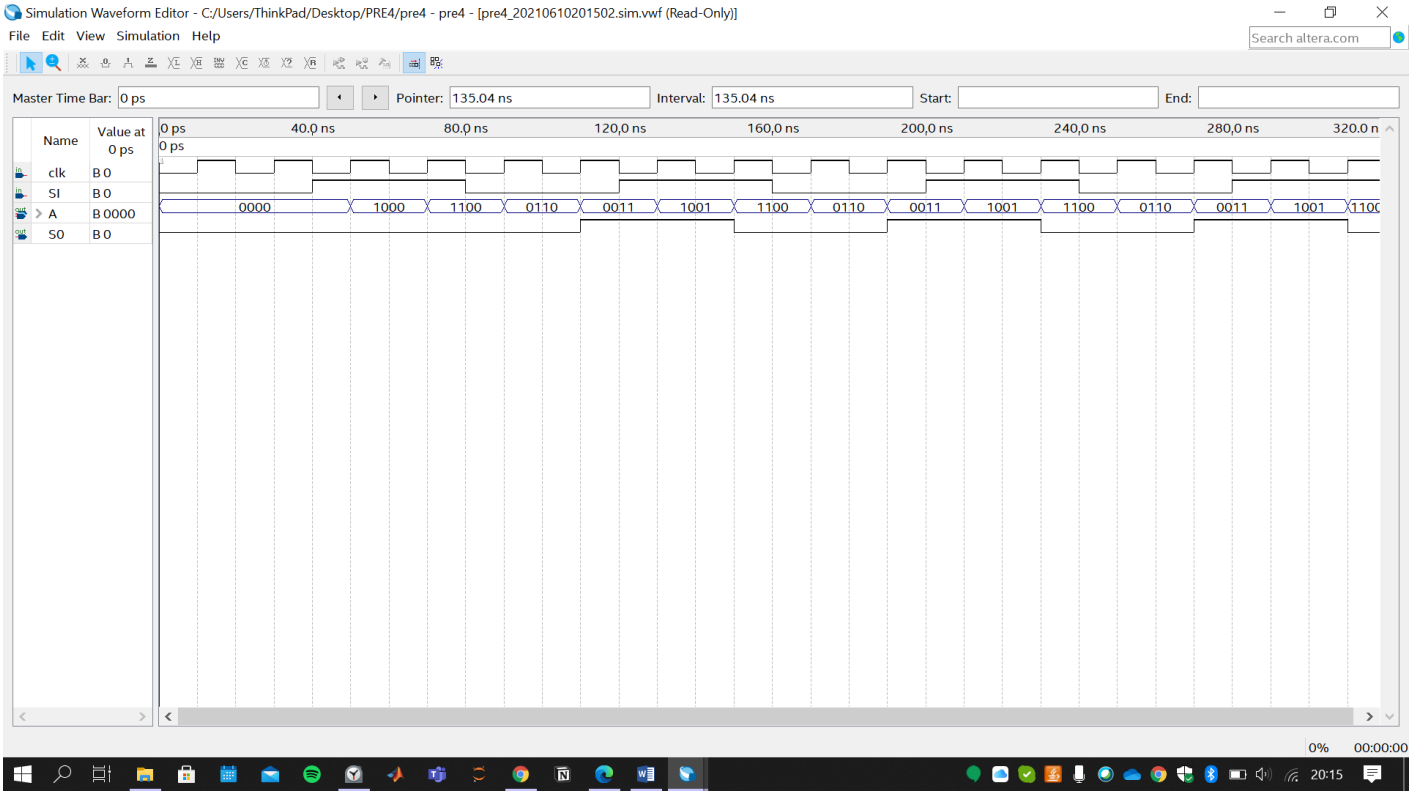
A) Put the screenshot of the designed circuit schematic of **III.2** of **Experimental Work**. Pay attention to the clear demonstration of blocks and wiring between blocks. Briefly explain your approach on the required task.



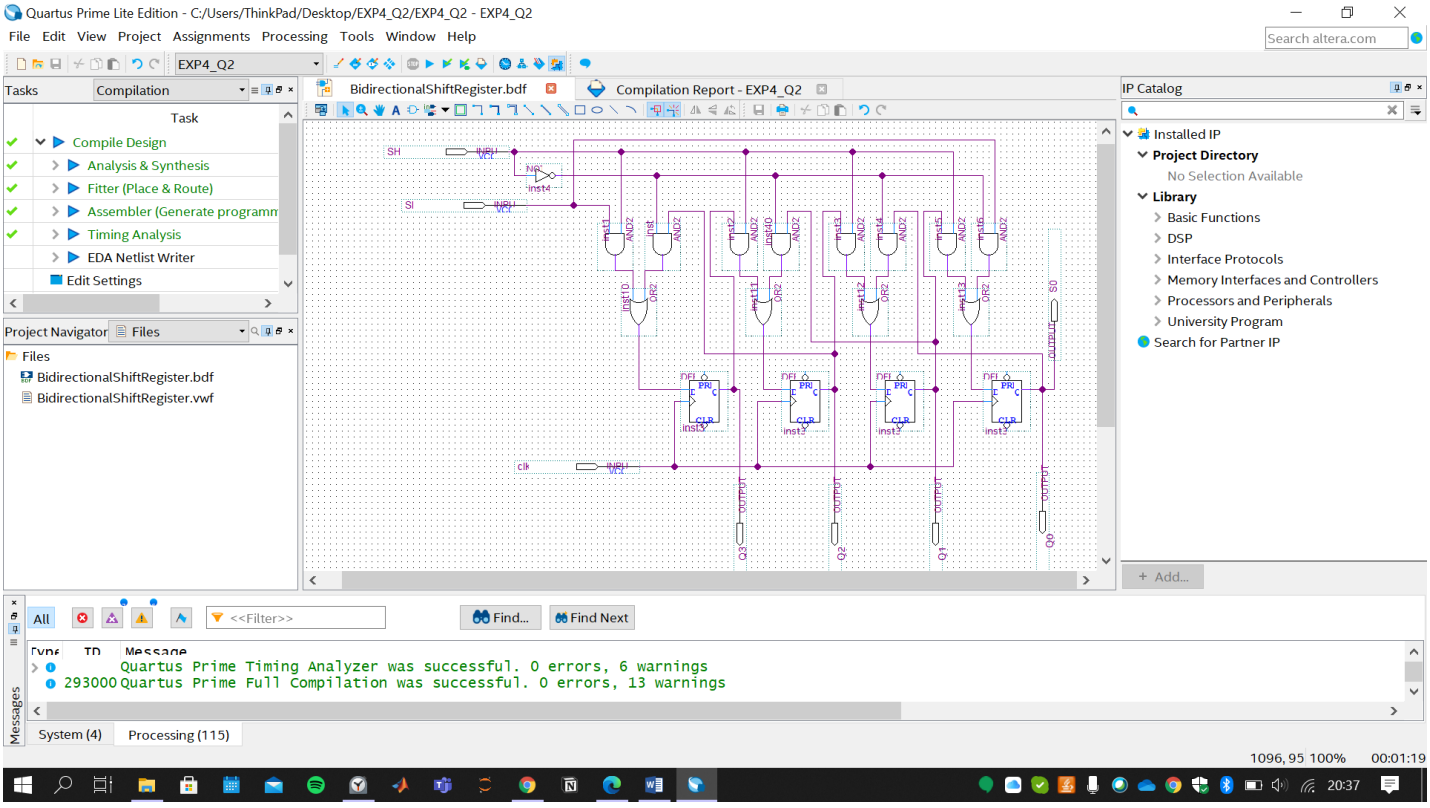
Approach: To obtain a right shif register serial input is directly connected to the last (D3) FF.

Outputs of the FFs is connected to the D input of the previous FFs.
(Q3->D2, Q2->D1, Q1->D0). LSB is attained as Serial Output as well.

B) Put the screenshot of the required simulation result of design in **A**. Please make sure there are enough examples of each condition in the sample set, which are clearly visible in the screenshot.



C) Put the screenshot of the designed circuit schematic of **4-bit bidirectional shift register** in **Take Home Design Question 2 part A**. Pay attention to the clear demonstration of blocks and wiring between blocks. Briefly explain your approach on the required task.



Approach: To implement the 4-bit bidirectional shift register, additional SH input is used. This input determines whether shift register shifts left or right.

At each input basic 2x1 MUX circuit is connected. When SH is LOW to obtain left shift and otherwise to obtain right shift:

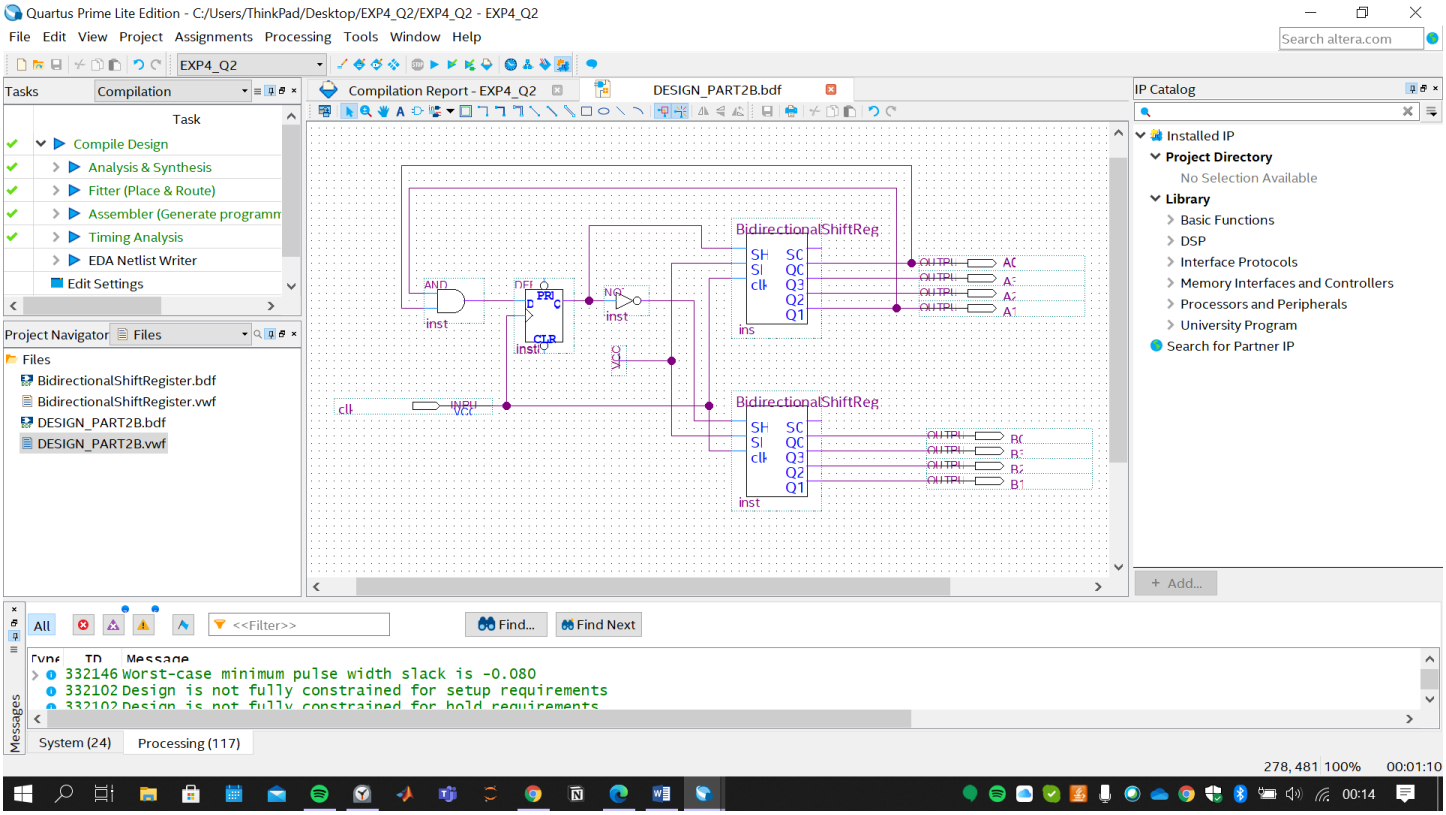
2x1 MUX's select input is SH, I0 is Q (previous Flip Flop outputs) I1 is Q (next Flip Flop outputs)
Y is the D input of the related FF.

For instance, lets look at the second FF case:

2x1 MUX of second FF: S=SH, I0=Q1, I1=Q3, Y=D2.

To apply Serial Input, SI is introduced. And SI is both connected to the third and zeroth FF's inputs.

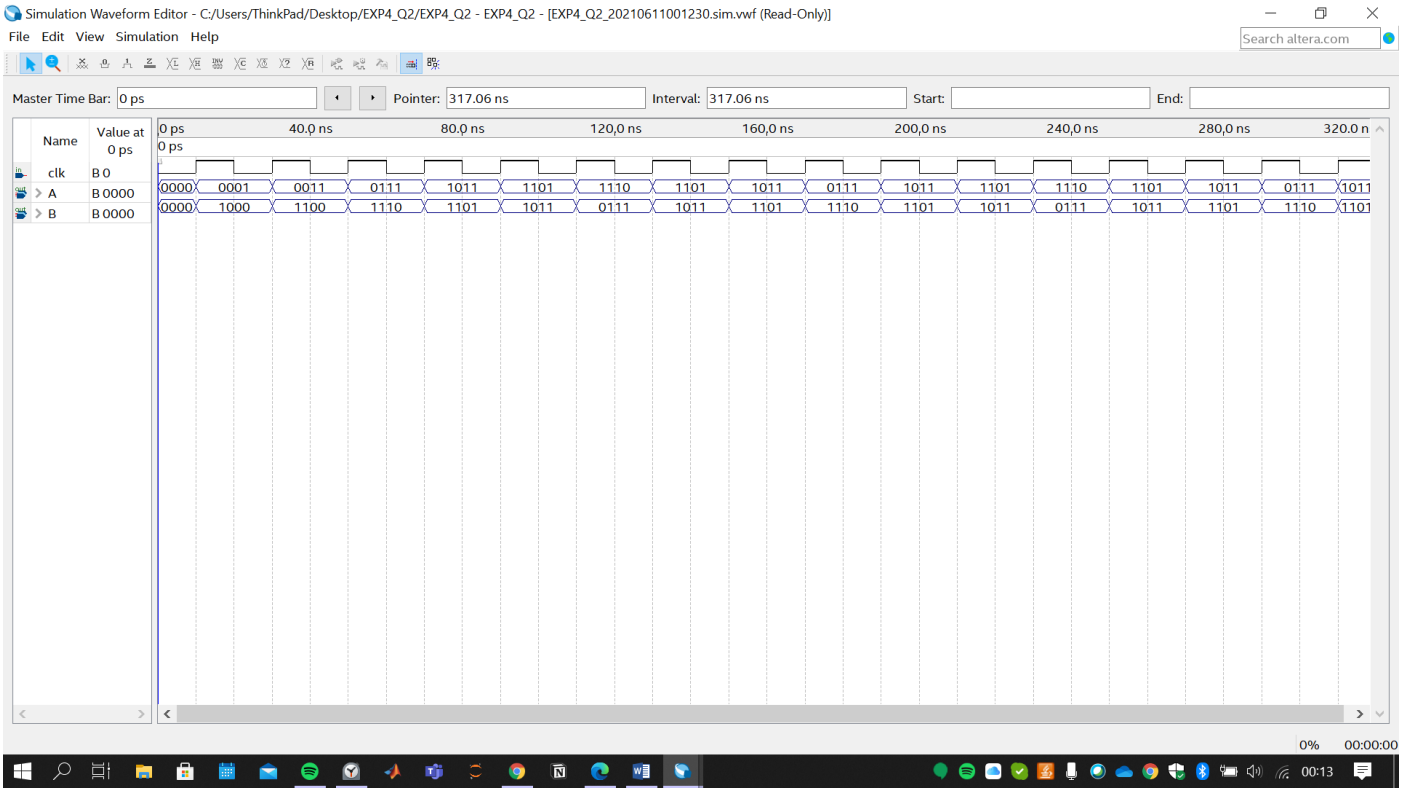
D) Put the screenshot of the designed circuit schematic in **Take Home Design Question 2 part B**. Pay attention to the clear demonstration of blocks and wiring between blocks. Briefly explain your approach on the required task.



Clock Hits	A3A2A1A0	SH(A)	D FF	B3B2B1B0	SH(B)
+	0000	0	0	0000	1
+	0001	0	0	1000	1
+	0011	0	1	1100	1
+	0111	1	1	1110	0
+	1011	1	1	1101	0
+	1101	1	0	1011	0
+	1110	0	0	0111	1
+	1101	0	0	1011	1
+	1011	0	1	1101	1
+	0111	1	1	1110	0
+	1011	1	1	1101	0
+	1101	1	0	1011	0

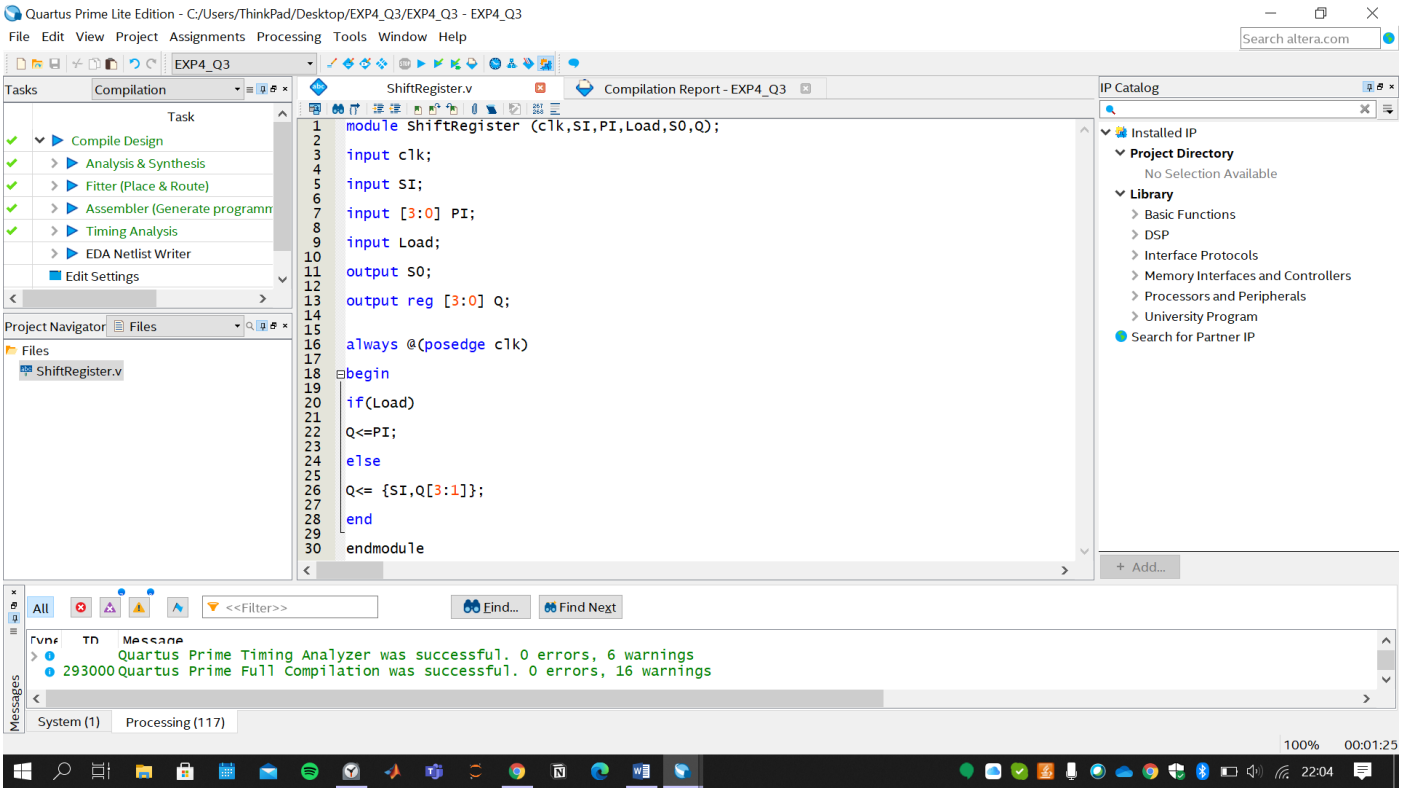
From the above table, it can be seen that SH input of A and B are complement of each other. We can achieve related SH input using D ff. If State of Q yields SH(A), SHA should be the delayed version of D input. Since D=Q(t+1).
To achieve D input, Karnaugh Map can be implemented. From K-Map, D results as A0 AND A1.
Part E shows the expected result.

E) Put the screenshot of the required simulation result of design in **D**. Please make sure there are enough examples of each condition in the sample set, which are clearly visible in the screenshot



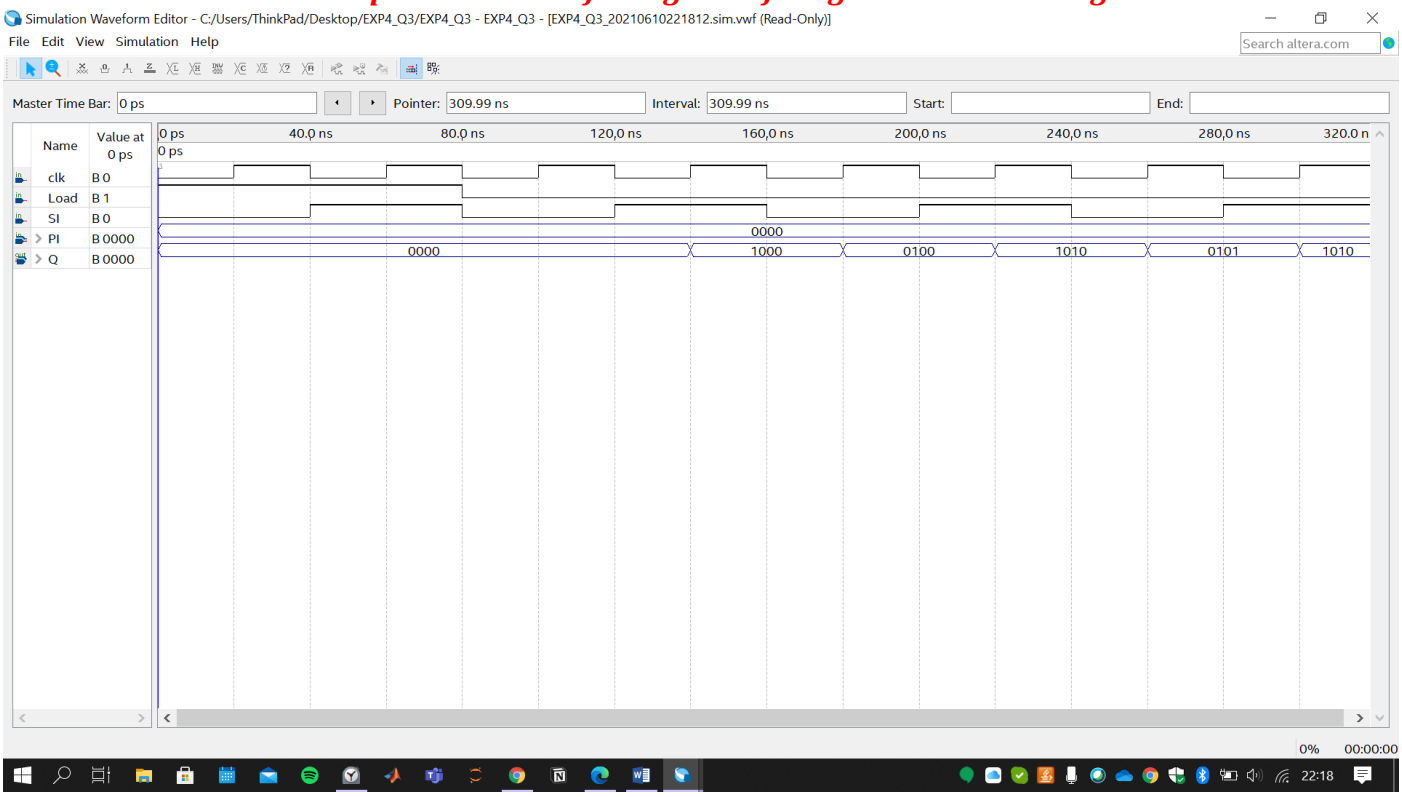
Part 3.

A) Put a screenshot of your Verilog code for **III.3** of **Experimental Work** and describe it briefly.

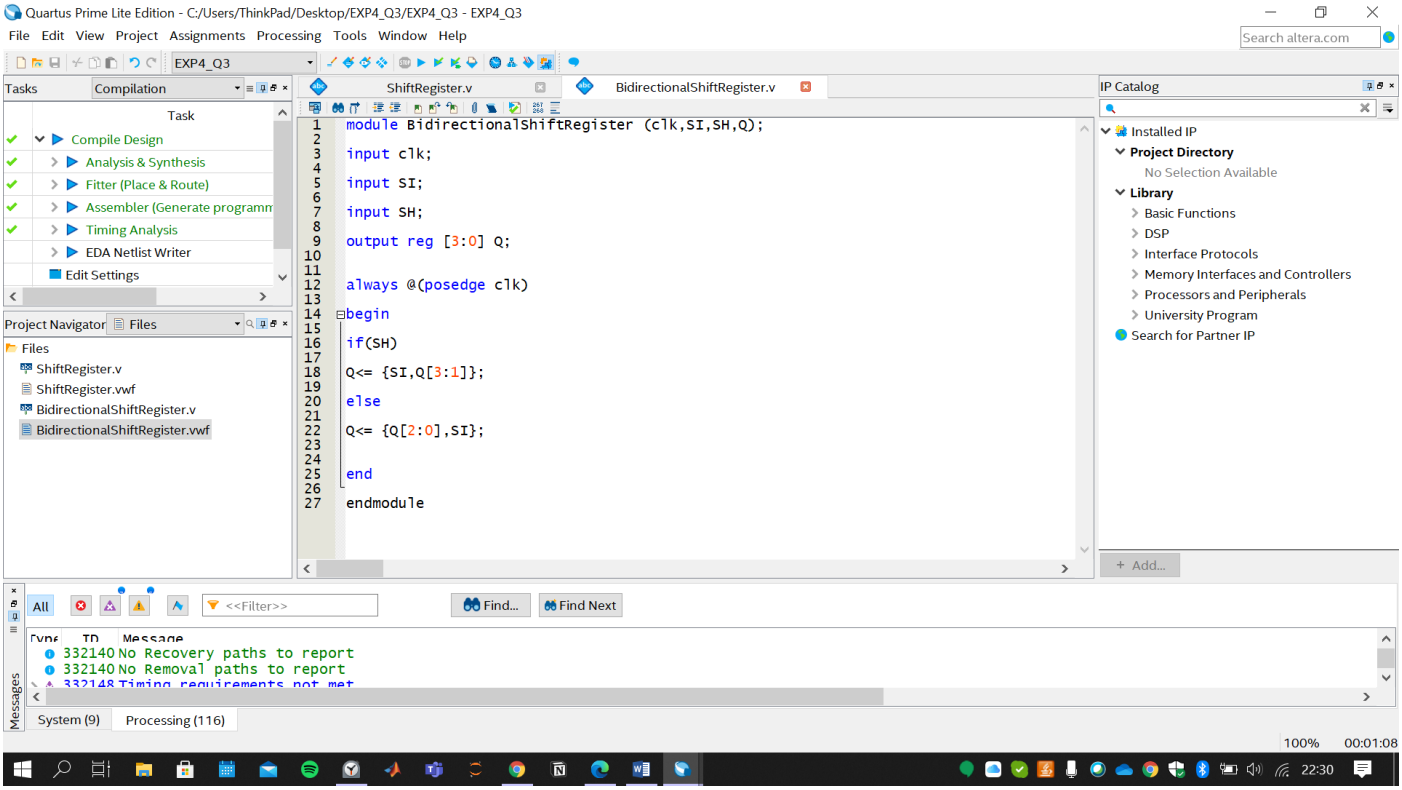


Description: When positive clock pulse hits, according to Load Input; the circuit is going to implement right shift register or data loading.
Using if else and non blocking statements for sequential circuits (<=) assignments are done.
When Load is High, parallel input is loaded whereas Load is LOW, right shifting occurs. (inside the else statement, constructing with the concatenation)

Example Simulation for Right Shift Register with Loading



B) Implement **4-bit bidirectional shift register** in **Take Home Design Question 2 part A** in Verilog. Put a screenshot of your Verilog code below.



Similar to Part3A, there is additional shift left implementing inside the else block. Q<= {Q[2:0],SI};

Example Simulation for Bidirectional Shift Register with Loading