Course Objectives:
In the Digital Electronics Laboratory course, hands-on experience based on course materials covered within the corequisite course EE348 Introduction to Logic Design will be the primary objective. The course will cover an introduction to logic circuits, parallel adders, subtractors, complementers, multiplexers, code converters, flip flops, counters, and introduction to hardware description languages (Verilog-HDL).
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Course Assistants:

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Course Details:
This course is highly coupled with EE348, Logic Design courses. All experiments will be on the subjects covered in EE348. Although the schedule is planned such that theoretical background is covered in the corequisite course, before the lab sessions in EE314, there may be times where you need to do some preliminary readings for this course. All experiments will be conducted remotely. There will be five experiments in which you are going to have an online quiz at the beginning of the experiment and prepare a report on your design question with necessary background information and experimental data. Moreover, there will be a term project. Project descriptions and any changes and updates on the deadlines will be announced later on.

Course Rules:
Laboratory work will be performed **on Thursday** between **17:30 - 23:30** for all sessions. An online *quiz* will be carried out on ODTUClass *in the first 30 minutes*. After the online quiz session, laboratory work will be performed offline except for special situations such as people who need to connect to laboratory computers remotely.
You will be assigned preliminary works; however, they will not be collected, but quizzes will be related to the preliminary works. Besides, the grades you get from quizzes will affect your report grades for each laboratory session. Scaling will be done as the following,

Q/Q_{tot}: Quiz Grade/ Total Quiz Grade R: Report Grade

$$R_{final} = R \quad if \quad Q \geq Q_{tot} * 0.5$$
$$R_{final} = 0.8 * R \quad if \quad Q < Q_{tot} * 0.5$$

Although the preliminary works are not collected, you are **strongly recommended to carefully perform the tasks given in the preliminary works *by yourself*.** Paying the necessary attention to the preliminary works will significantly enhance your learning through the experiments and increase your success in the quizzes.

During the laboratory work, you will write a report related to the work you performed. In your report, you will provide your simulation results and comments on your results. Reports will be written on computers and submitted with the designed project to

assignments opened on ODTUClass. In each experiment you will be assigned different group and have a different experimental design from other groups.

METU Honor Code:
By being a METU student, you accept the university's honor code, which is provided below. Please read it carefully. Any behavior against the honor code will result in disciplinary action against you.
"The members of the METU community are reliable, responsible and honorable people who embrace only the success and recognition they deserve and act with integrity in their use, evaluation, and presentation of facts, data, and documents."

Make-Up Lab Sessions:
With legal excuse, you can miss up to two experiments. There will be make-up sessions for you to complete your missed experiments. Missing three experiments will result in an automatic FF grade.

Term Project:
Project topics will be announced in May. We will form groups of 5 students such that at least one student from each group can be at METU in person during 14th-25th June. We prefer this student to have a residence in Ankara or its vicinity. Each group will be given the FPGA board they can be use for the term project. The details on the term project will be given in May.

Experiment Schedule:

17^{th} *May*	Verilog Recitation
20^{th} *May*	Experiment 1: Parallel Adders, Subtractors, and Complementers
27^{th} *May*	Experiment 2: Elementary Gate Networks
3^{rd} *June*	Experiment 3: Flip Flops and Sequential Circuits
10^{th} *June*	Experiment 4: Shift Registers and Counters
17^{th} *June*	Experiment 5: Introduction to Verilog
21^{st} *June* – 25^{th} *June*	Term Project Demonstration
28^{th} *June*	Make-Ups

Grading: Experiments: 14% each (4% for quiz and 10% for experiment)
Project: 30 % (details will be announced later)