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EXPERIMENT 3 – Flip Flops and Sequential Circuits

I. Introduction

A. Objectives

In this experiment, you will get familiar with the basic operational principles of flip flops and counters.

B. Background: 7-Segment Displays

7-segment display is a simple and effective form for visualizing decimal digits. The DE1-SoC board has six 7-segment displays, HEX0 through HEX5. Each display is interfaced to the FPGA using 7 signals, one signal for each segment. Interface to HEX0 is illustrated in Figure 1. **The display is common anode, that is, when the corresponding signal is 0 the LED is on, and when the signal is 1 the LED is off.** FPGA pin names associated with 7-segment displays are given in the Appendix.

7-segment decimal digits are given in Figure 2. You can see that for the digit 0, segments 0, 1, 2, 3, 4 and 5 are on, and segment 6 is off. That is, the 7-bit HEX0[6..0] signal is 7'b1000000.

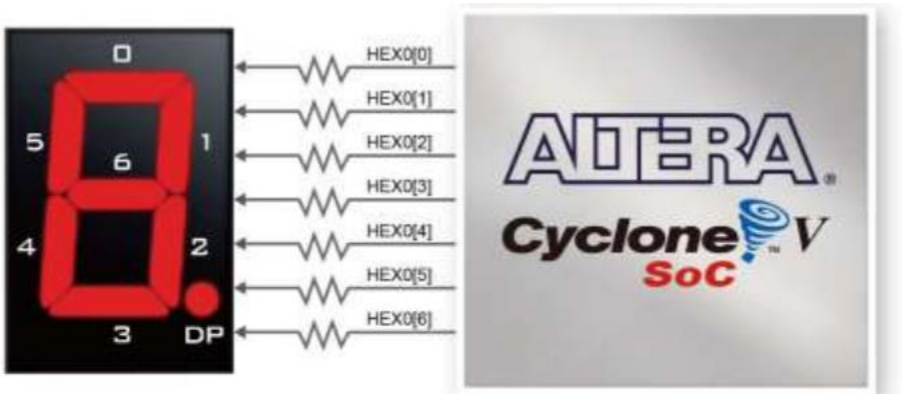

Figure 1: FPGA to 7-segment display interface.

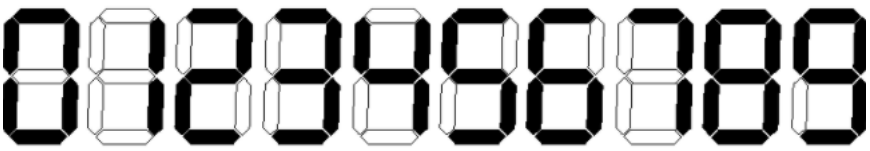

Figure 2: Decimal digits on a 7-segment display.

II. Preliminary Work

1. Design a circuit with three inputs and one output, i.e. X, Y, clk and Q_n, which has the truth table given in Table 1, using a single JK flip flop and any number of elementary logic gates.

Table 1: Truth table for preliminary work Q1

X	Y	Q_n
0	0	Q_{n-1}'
0	1	1
1	0	0
1	1	Q_{n-1}

2. Design a frequency divider circuit using only 4 JK flip flops. Your circuit should have one input clock with frequency f_{clk}, and four output clocks with frequencies $f_{clk}/2$, $f_{clk}/4$, $f_{clk}/8$ and $f_{clk}/16$. Assume that negated outputs, Q', of flip flops are not available. Flip flops are positive edge triggered.

3. The circuit you designed in Q2 is known as a 'ripple down counter'. Modify the circuit by adding elementary gates so that it counts up and has an active high *clear* input. When the clear input is high, all outputs should become low.

4. Design a BCD counter using the 4-bit ripple up counter that you designed in Q3 and elementary gates.

5. Design a BCD counter in Verilog. **Hint:** You can use *always* blocks and *if-else* statements.

6. Design a BCD to 7-segment display decoder in Verilog. Your circuit should have one 4 bit input, the BCD number, and one 7 bit output, the HEX0 signal that is explained in Background section. The output should change whenever the input changes. **Hint:** You can use *always* @* and *case* statements.

III. Experimental Work

1. Implement the circuit that you designed in preliminary work Q1 on Quartus. You can add the JK flip flop as jkff under primitives>storage in the Symbol tool. Make a functional simulation with appropriate inputs.

2. Design the frequency divider that you designed in preliminary work Q2 on Quartus. The output clocks should be grouped together as a bus, where the clock with frequency $f_{clk}/2$ is the MSB and the clock with frequency $f_{clk}/16$ is the LSB. Make a functional simulation to show that your design counts down.

3. Implement the ripple up counter with clear input that you designed in preliminary work Q3. The output should be a 4 bit bus. Create a symbol file for this counter. Using this symbol, implement the BCD counter that you designed in preliminary work Q4. Make a functional simulation to show that your design counts up the BCD numbers.

4. Implement the BCD counter in Verilog. Make a functional simulation to show that your module counts up the BCD numbers.

5. Implement the BCD to 7-segment decoder in Verilog. Make a functional simulation to show that your module works.

IV. Appendix: FPGA pin assignments of 7-segment displays

If you were to upload your design to DE1-SoC board, you would need to assign your design's inputs and outputs to actual FPGA pins. Pin names associated with 7-segment displays on DE1-SoC board are as follows.

Signal Name	FPGA Pin No.	Description	I/O Standard
HEX0[0]	PIN_AE26	Seven Segment Digit 0[0]	3.3V
HEX0[1]	PIN_AE27	Seven Segment Digit 0[1]	3.3V
HEX0[2]	PIN_AE28	Seven Segment Digit 0[2]	3.3V
HEX0[3]	PIN_AG27	Seven Segment Digit 0[3]	3.3V
HEX0[4]	PIN_AF28	Seven Segment Digit 0[4]	3.3V
HEX0[5]	PIN_AG28	Seven Segment Digit 0[5]	3.3V
HEX0[6]	PIN_AH28	Seven Segment Digit 0[6]	3.3V
HEX1[0]	PIN_AJ29	Seven Segment Digit 1[0]	3.3V
HEX1[1]	PIN_AH29	Seven Segment Digit 1[1]	3.3V
HEX1[2]	PIN_AH30	Seven Segment Digit 1[2]	3.3V
HEX1[3]	PIN_AG30	Seven Segment Digit 1[3]	3.3V
HEX1[4]	PIN_AF29	Seven Segment Digit 1[4]	3.3V
HEX1[5]	PIN_AF30	Seven Segment Digit 1[5]	3.3V
HEX1[6]	PIN_AD27	Seven Segment Digit 1[6]	3.3V
HEX2[0]	PIN_AB23	Seven Segment Digit 2[0]	3.3V
HEX2[1]	PIN_AE29	Seven Segment Digit 2[1]	3.3V
HEX2[2]	PIN_AD29	Seven Segment Digit 2[2]	3.3V
HEX2[3]	PIN_AC28	Seven Segment Digit 2[3]	3.3V
HEX2[4]	PIN_AD30	Seven Segment Digit 2[4]	3.3V
HEX2[5]	PIN_AC29	Seven Segment Digit 2[5]	3.3V
HEX2[6]	PIN_AC30	Seven Segment Digit 2[6]	3.3V
HEX3[0]	PIN_AD26	Seven Segment Digit 3[0]	3.3V
HEX3[1]	PIN_AC27	Seven Segment Digit 3[1]	3.3V
HEX3[2]	PIN_AD25	Seven Segment Digit 3[2]	3.3V
HEX3[3]	PIN_AC25	Seven Segment Digit 3[3]	3.3V
HEX3[4]	PIN_AB28	Seven Segment Digit 3[4]	3.3V
HEX3[5]	PIN_AB25	Seven Segment Digit 3[5]	3.3V
HEX3[6]	PIN_AB22	Seven Segment Digit 3[6]	3.3V
HEX4[0]	PIN_AA24	Seven Segment Digit 4[0]	3.3V
HEX4[1]	PIN_Y23	Seven Segment Digit 4[1]	3.3V
HEX4[2]	PIN_Y24	Seven Segment Digit 4[2]	3.3V
HEX4[3]	PIN_W22	Seven Segment Digit 4[3]	3.3V
HEX4[4]	PIN_W24	Seven Segment Digit 4[4]	3.3V
HEX4[5]	PIN_V23	Seven Segment Digit 4[5]	3.3V
HEX4[6]	PIN_W25	Seven Segment Digit 4[6]	3.3V
HEX5[0]	PIN_V25	Seven Segment Digit 5[0]	3.3V
HEX5[1]	PIN_AA28	Seven Segment Digit 5[1]	3.3V
HEX5[2]	PIN_Y27	Seven Segment Digit 5[2]	3.3V
HEX5[3]	PIN_AB27	Seven Segment Digit 5[3]	3.3V
HEX5[4]	PIN_AB26	Seven Segment Digit 5[4]	3.3V
HEX5[5]	PIN_AA26	Seven Segment Digit 5[5]	3.3V
HEX5[6]	PIN_AA25	Seven Segment Digit 5[6]	3.3V