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DEPARTMENT OF ELECTRICAL AND
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EXPERIMENT 1. Parallel Adders, Subtractors, and Complementors

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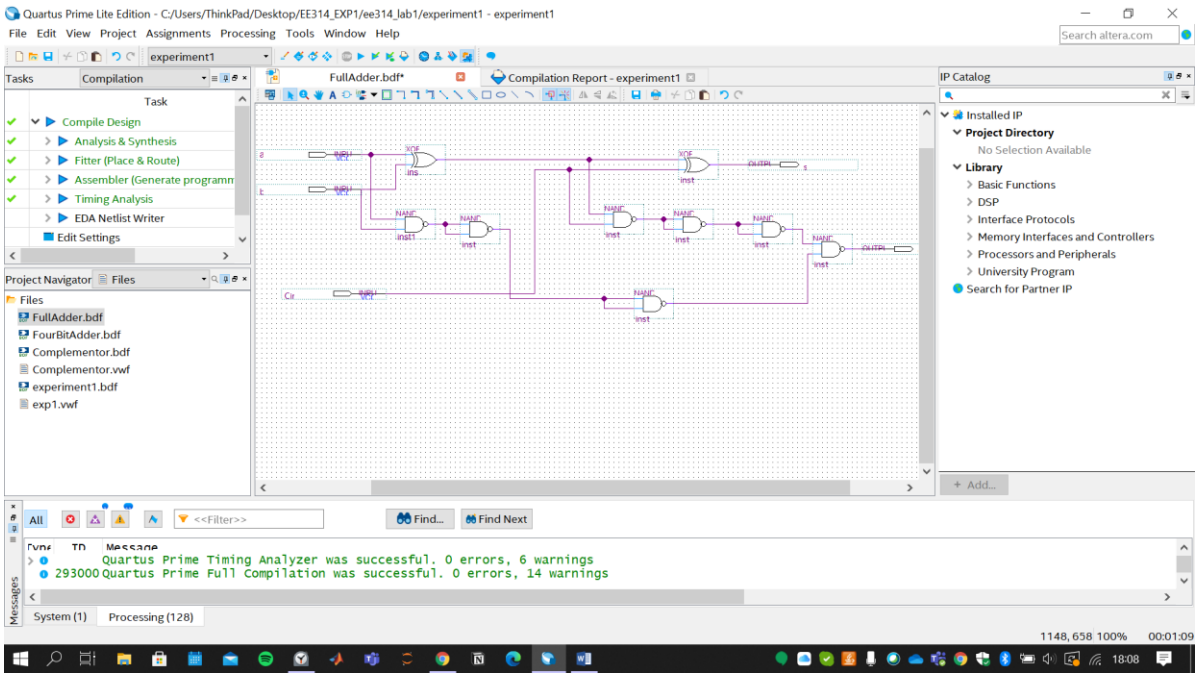
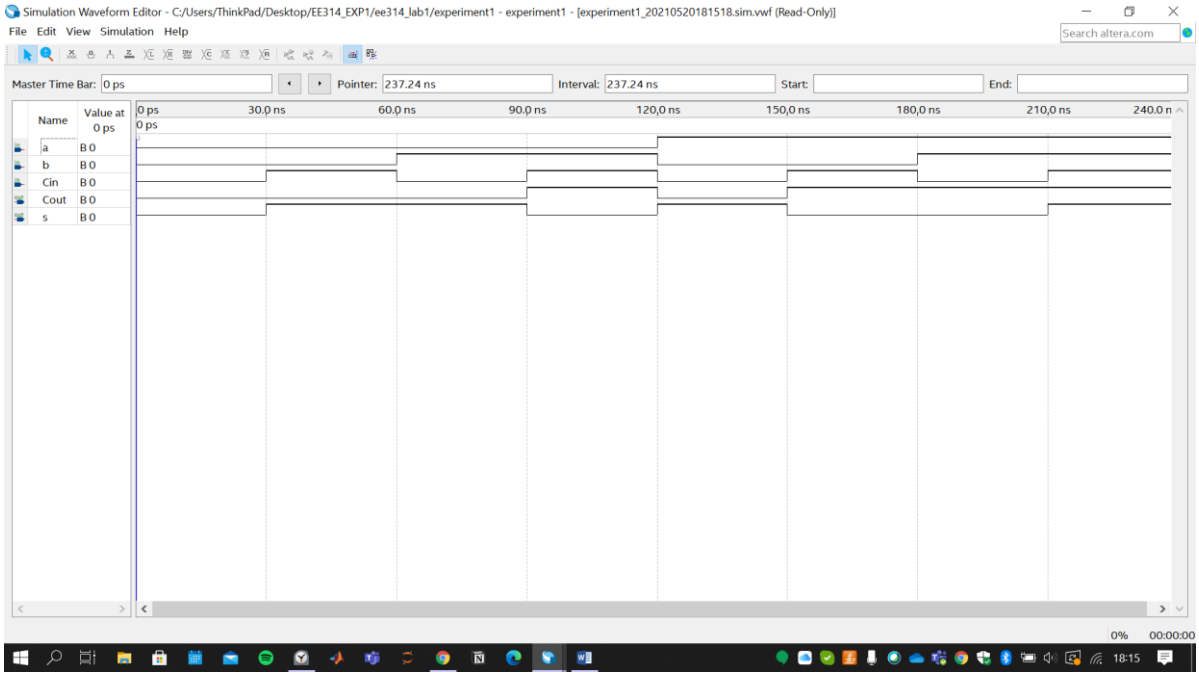
A. Implementation of the Full Adder

A1) Based on the logic circuit you designed in your preliminary work part3 construct the full adder using the minimum number of two-input NAND and two-input XOR gates and take a screenshot of the schematic from Quartus II.

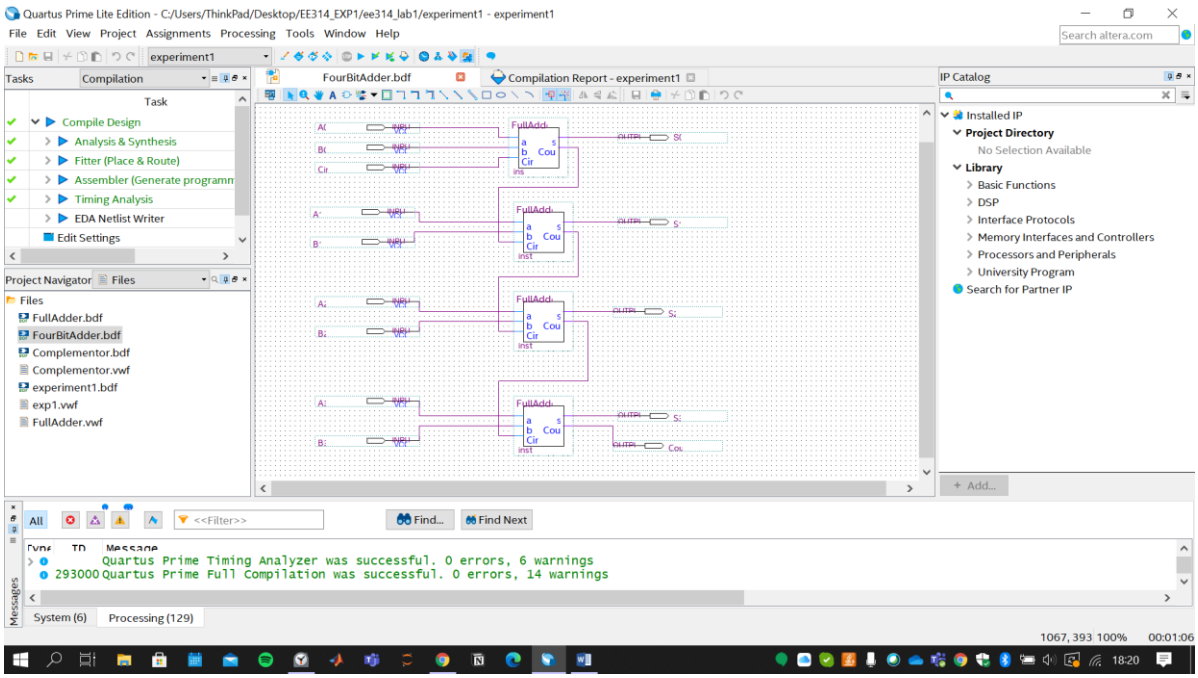


A2) Draw the proper input test waveforms, run the functional simulation to verify the operation of your circuit. Then, take the screenshot of the simulation from Quartus II.

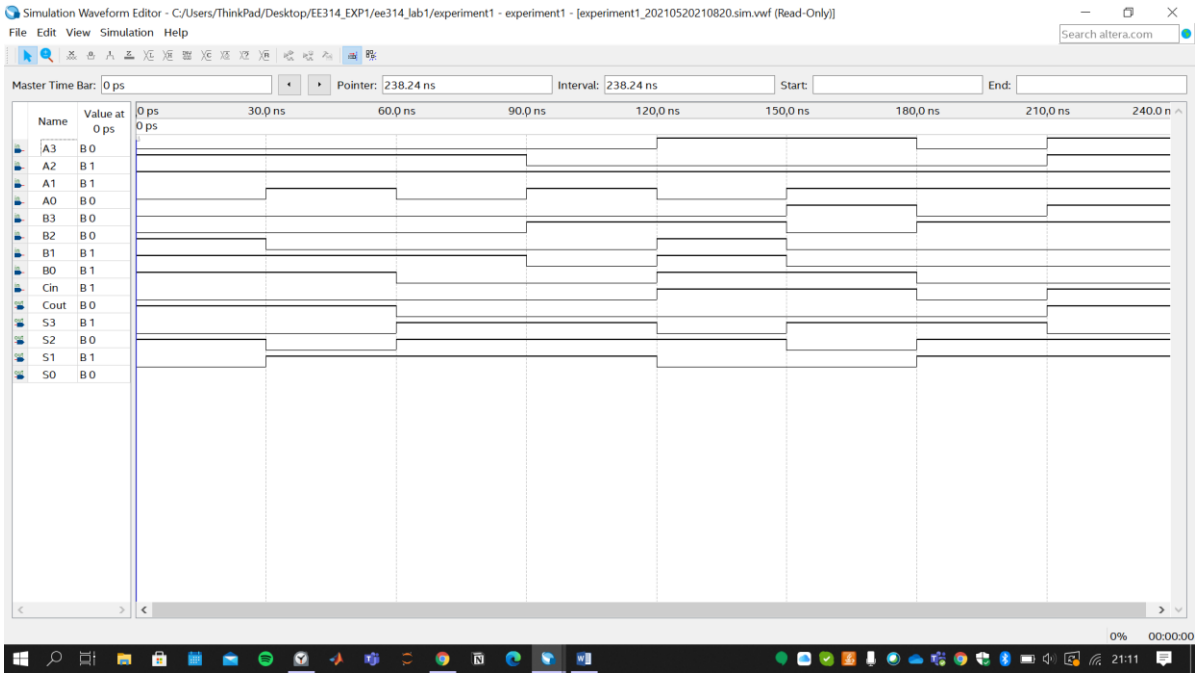


B. Implementation of the 4-bit Binary Adder

B1) Construct 4-bit binary adder by using full adder symbols and other necessary components and proper wiring as you did in preliminary work part 4. Take a screenshot of the schematic from Quartus II.

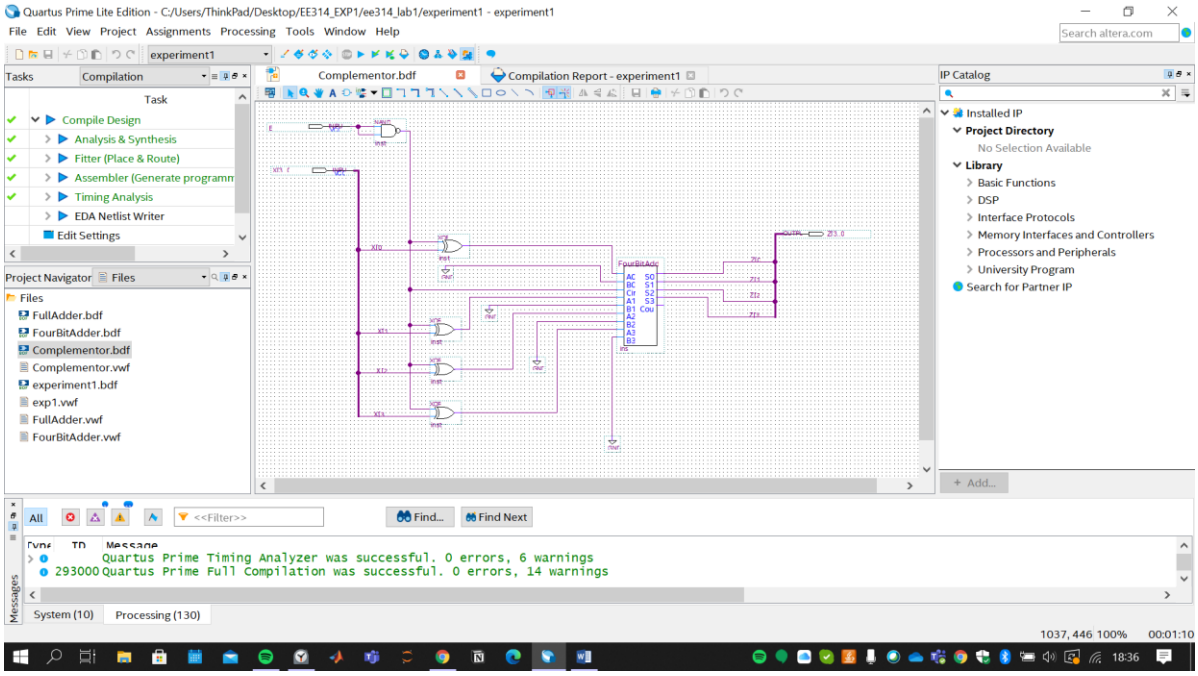


B2) Draw the proper input test waveforms, run the functional simulation to verify the operation of your circuit. Then, take the screenshot of the simulation from Quartus II.

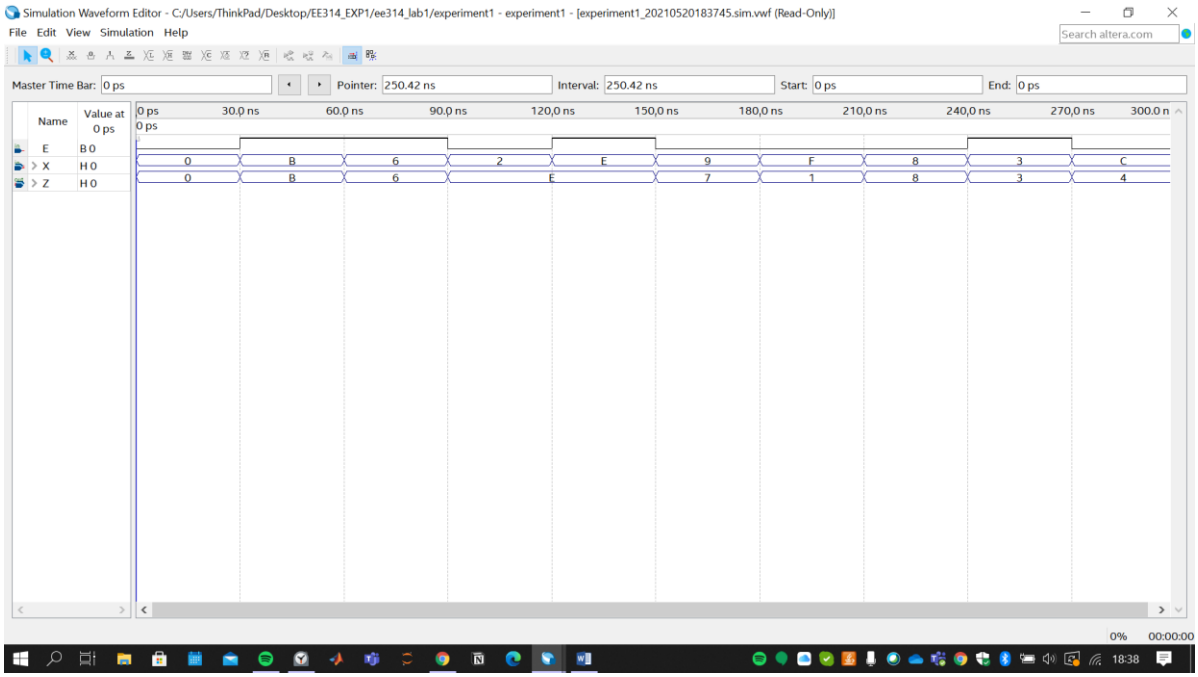


C. Implementation of the Complementor

C1) Based on the logic circuit design in your Preliminary work part 5, create the 4-bit 2's complementor (Your schematic should include the fourbitadder symbol and bus structure). Take a screenshot of the schematic from Quartus II.

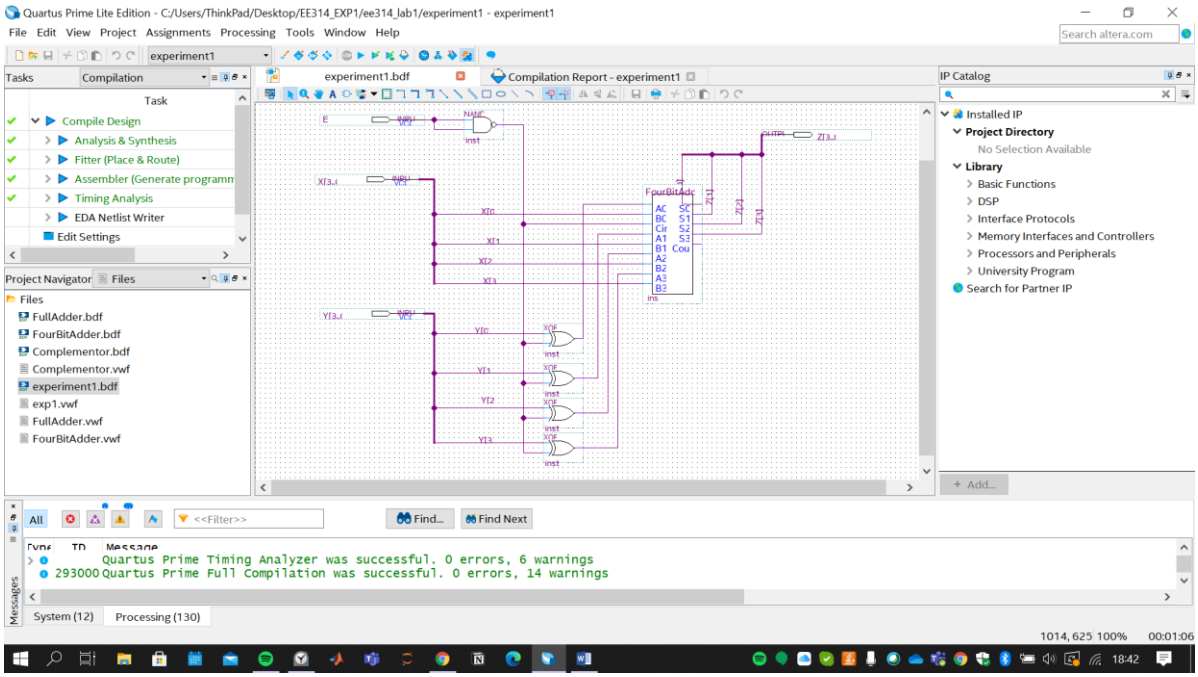


C2) Draw the proper input test waveforms, run the functional simulation by using the input test vectors as given in Table 1.5 to verify the operation of your circuit. Then, take the screenshot of the simulation from Quartus II.

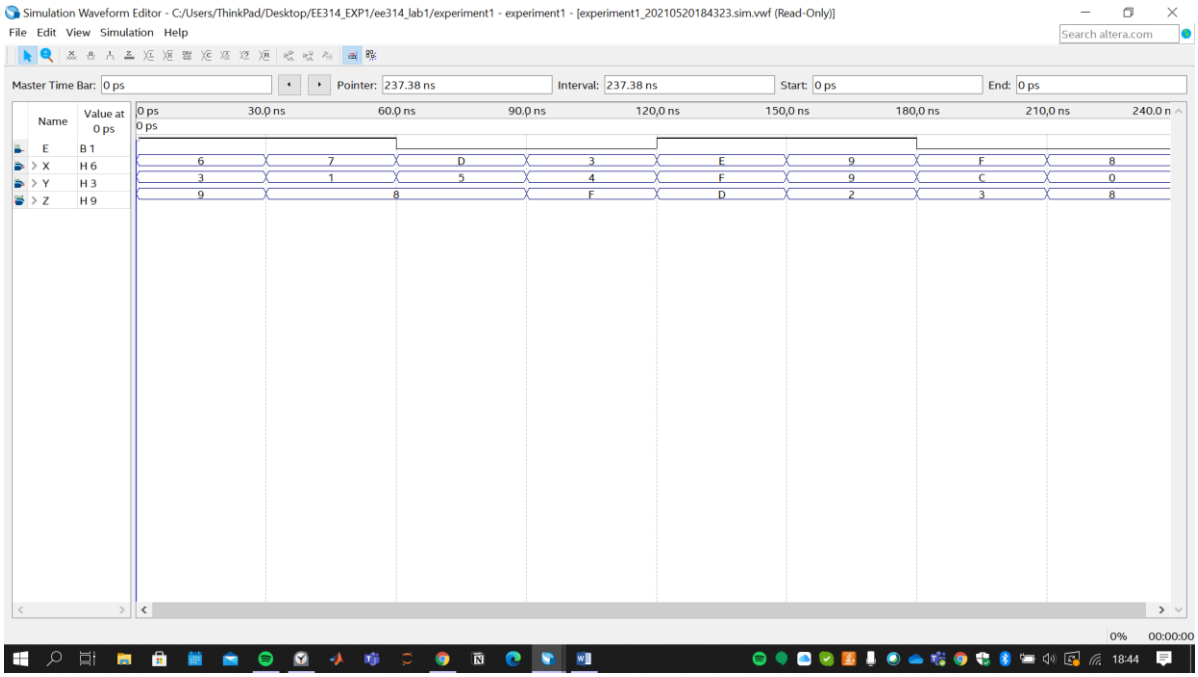


D. Implementation of the Adder/Subtractor

D1) Based on your design in preliminary work part 6, implement your adder/subtractor design. Note that inputs and output of your design should be included by bus structures. Take a screenshot of the schematic from Quartus II.

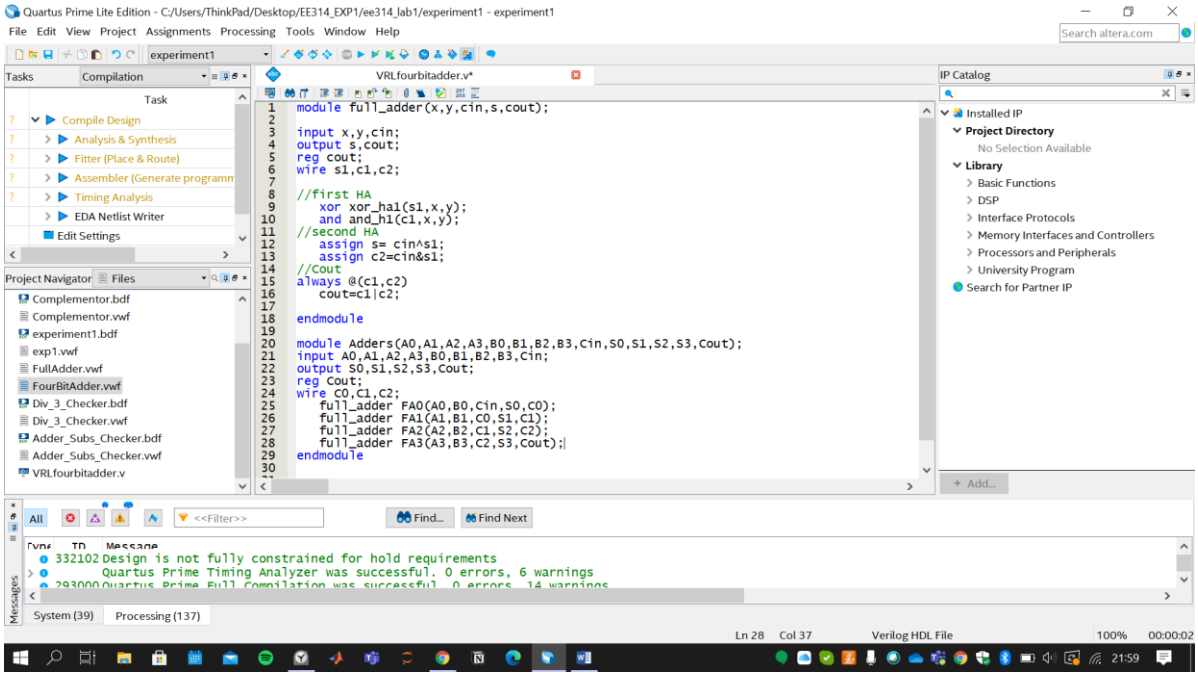


D2) Draw the proper input test waveforms, run the functional simulation by using the input test vectors as given in Table 1.6 to verify the operation of your circuit. Then, take the screenshot of the simulation from Quartus II.



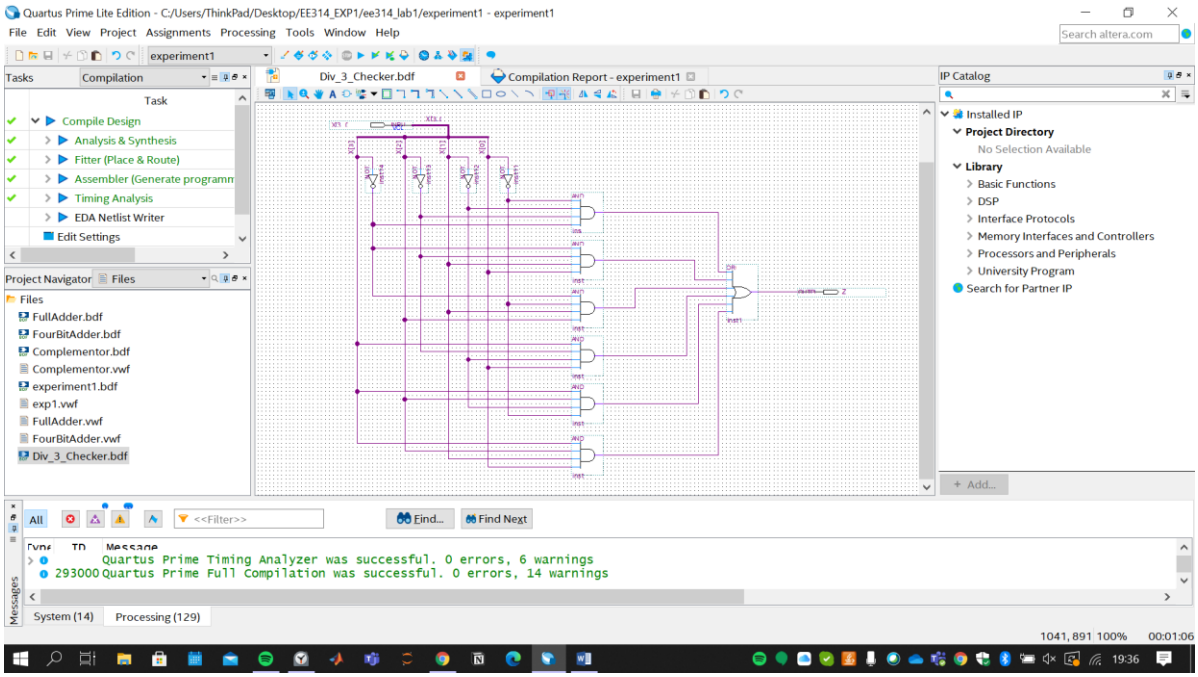
E. Verilog Implementation

Implement the 4-bit binary adder that you designed in preliminary work in Verilog HDL. You should use hierarchical design technique. Take a screenshot of your code.

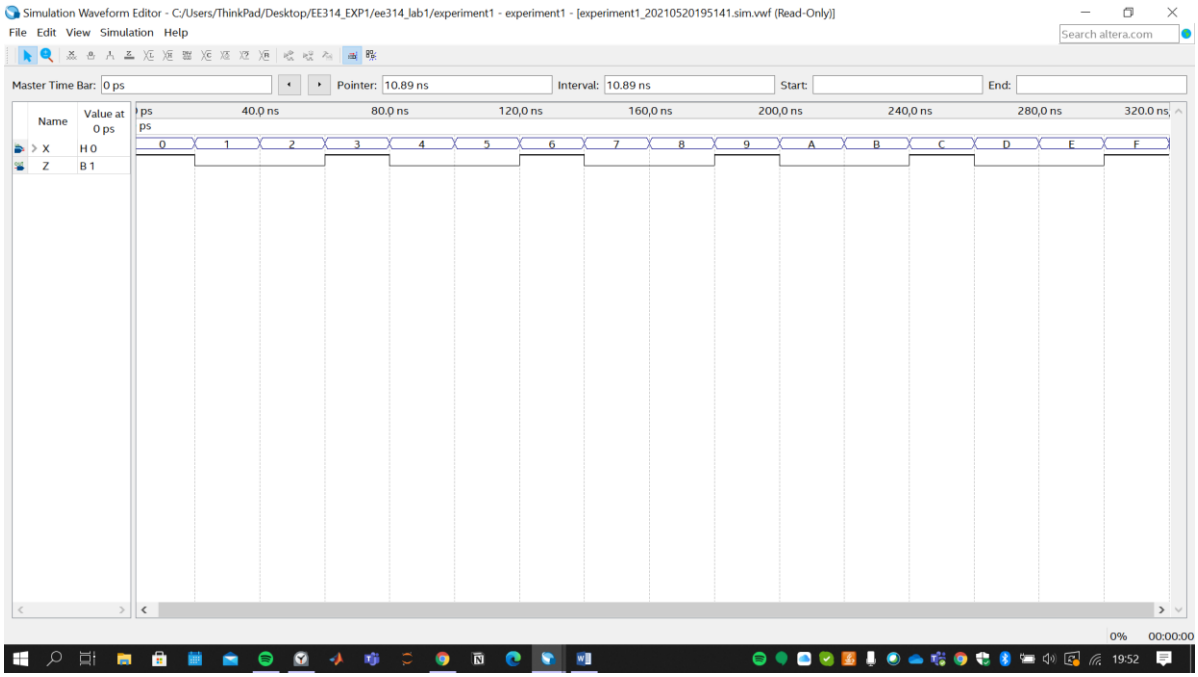


F. Implementation of the Design Question

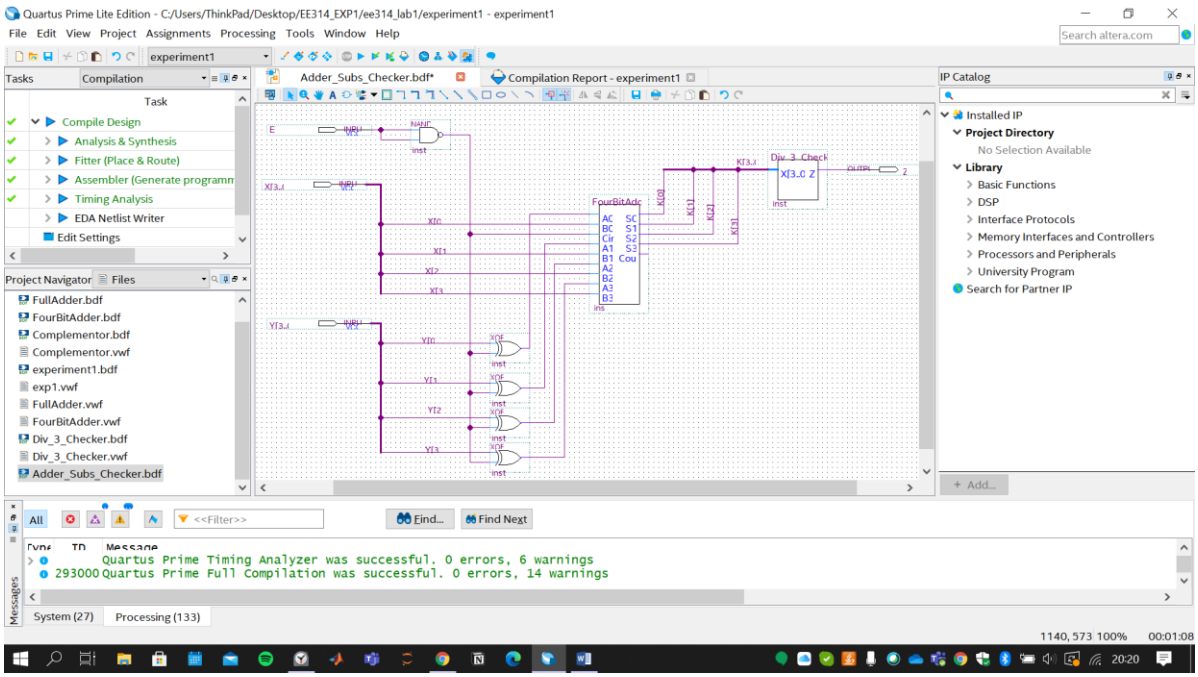
F1) Based on the circuit in Experiment 1 Take-Home Design Q2, implement the number checker design. Note that input of your design should be included by bus structure. Take a screenshot of the schematic from Quartus II.



F2) Draw the proper input test waveforms, run the functional simulation by using all 16 input combinations to verify the operation of your circuit. Then, take the screenshot of the simulation from Quartus II.



F3) Insert your number checker to the output of your adder/subtractor design. Note that the symbol must be used for the number checker. Take a screenshot of the schematic from Quartus II.



F4) Draw the proper input test waveforms, run the functional simulation by using the input test vectors as given in Table 1.6 to verify the operation of your circuit. Then, take the screenshot of the simulation from Quartus II.