KOCAELİ UNIVERSITY

FACULTY OF ENGINEERING

ELECTRONICS AND COMMUNICATION ENGINEERING

VLSI DESIGN TERM PROJECT

4-BIT BINARY ADDER/ SUBTRACTOR
4X16 DECODER LAYOUT DESIGN

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FIGURES AND TABLES

1. 4 - BIT BINARY ADDER/SUBTRACTOR

1.1. S-EDIT DESIGN

Firstly, the require components are EXOR and Full Adder circuits. S- EDIT designs of EXOR and Full Adder circuits are shown in below figure.

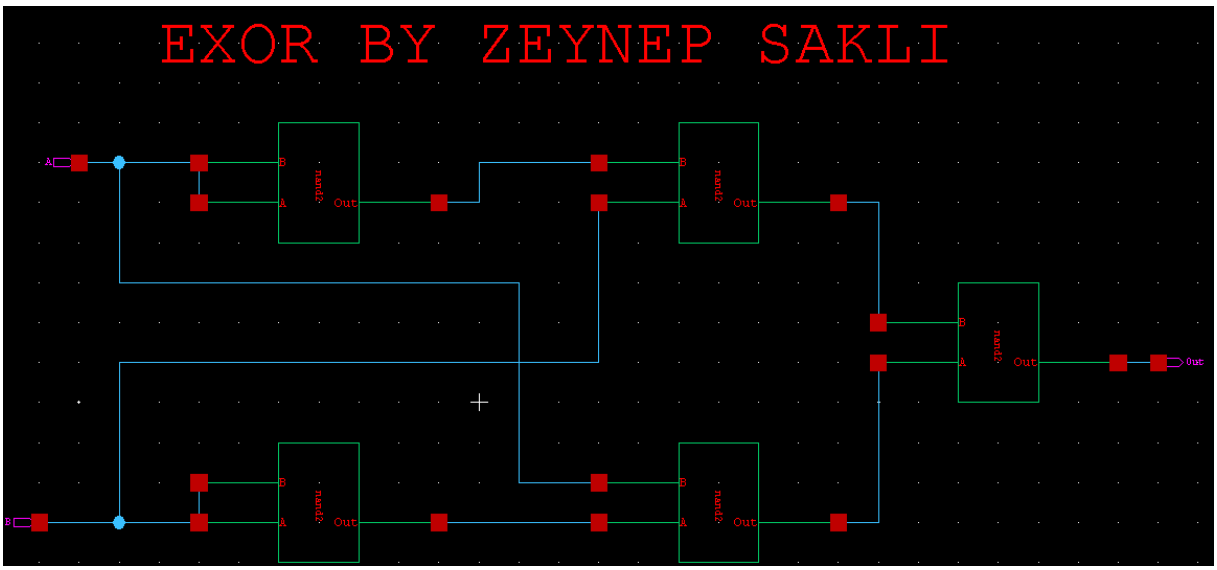

Figure 1. 1: EXOR S-EDIT Design

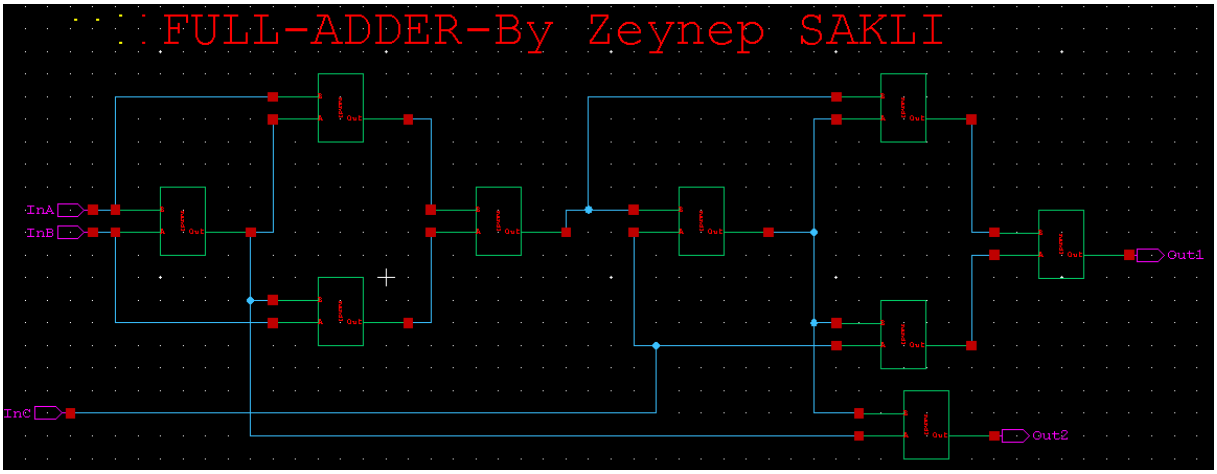

Figure 1. 2: Full Adder S-EDIT Design

The Full Adder Design is designed with 9 NAND Gates. In the other senario, the Full Adder circuit can be designed with AND, EXOR and OR Gates.

According to all information, 4- BIT Adder/ Subtractor Design is shown in below.

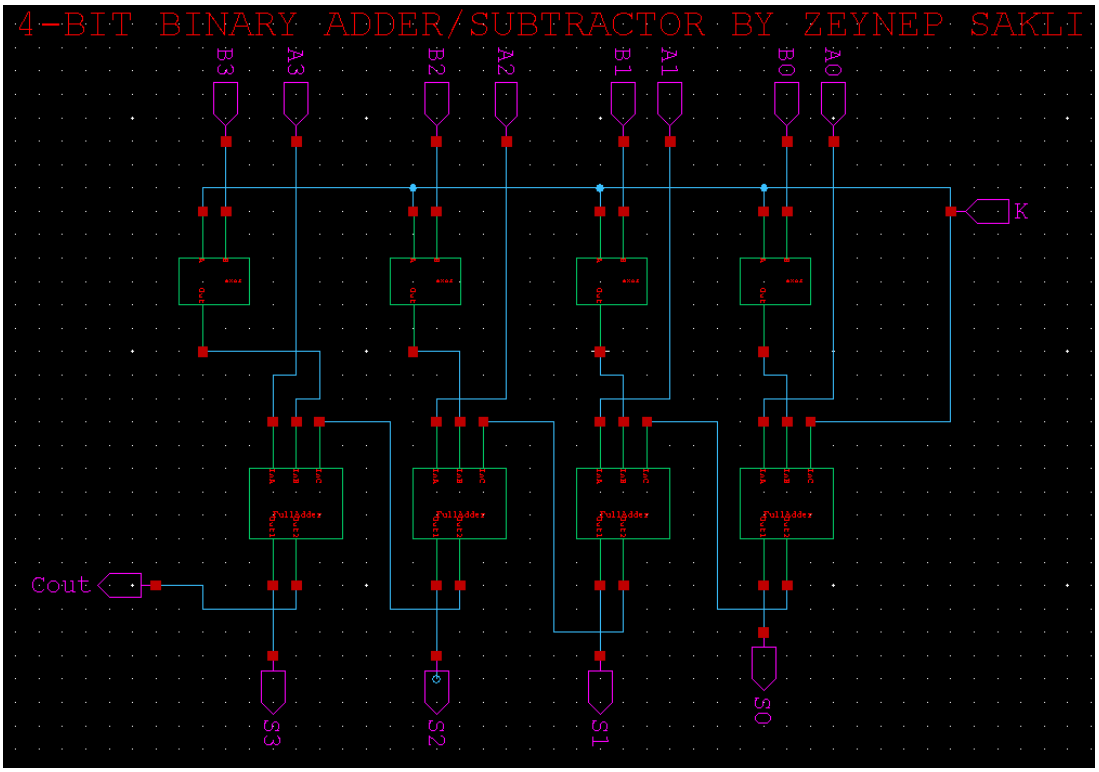

Figure 1. 3: 4- BIT Adder/Subtractor S-EDIT Design

When K=1, the circuit is a subtractor and K=0, the circuit is an adder.

```
********* Simulation Settings - Additional SPICE commands *********
VZeynepp Vdd Gnd 5V

VK K Gnd dc 0 BIT   ({0101010101010101} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n  delay=0) AC 0 0 ROUND=0

VA3 A3 Gnd dc 0 BIT ({0000000011111111} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n  delay=0) AC 0 0 ROUND=0
VA2 A2 Gnd dc 0 BIT ({0000111100001111} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n  delay=0) AC 0 0 ROUND=0
VA1 A1 Gnd dc 0 BIT ({0011001100110011} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n  delay=0) AC 0 0 ROUND=0
VA0 A0 Gnd dc 0 BIT ({0101010101010101} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n  delay=0) AC 0 0 ROUND=0

VB3 B3 Gnd dc 0 BIT ({0000000011111111} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n  delay=0) AC 0 0 ROUND=0
VB2 B2 Gnd dc 0 BIT ({0000111100001111} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n  delay=0) AC 0 0 ROUND=0
VB1 B1 Gnd dc 0 BIT ({0011001100110011} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n  delay=0) AC 0 0 ROUND=0
VB0 B0 Gnd dc 0 BIT ({0101010101010101} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n  delay=0) AC 0 0 ROUND=0

.tran 160p 160n start=0
.print tran v(S3) v(S2) v(S1) v(S0) v(Cout)
.include "C:\Users\Zeynep\Desktop\VLSI_TASARIM_DERSLER\VLSI_tech_files\SCN_0.25u_CMOS.md"

.END
```

Figure 1. 4: 4- BIT Adder/Subtractor T-Spice Code

According to the T- Spice code, addition and subtraction in order. W- Edit output is shown in below.

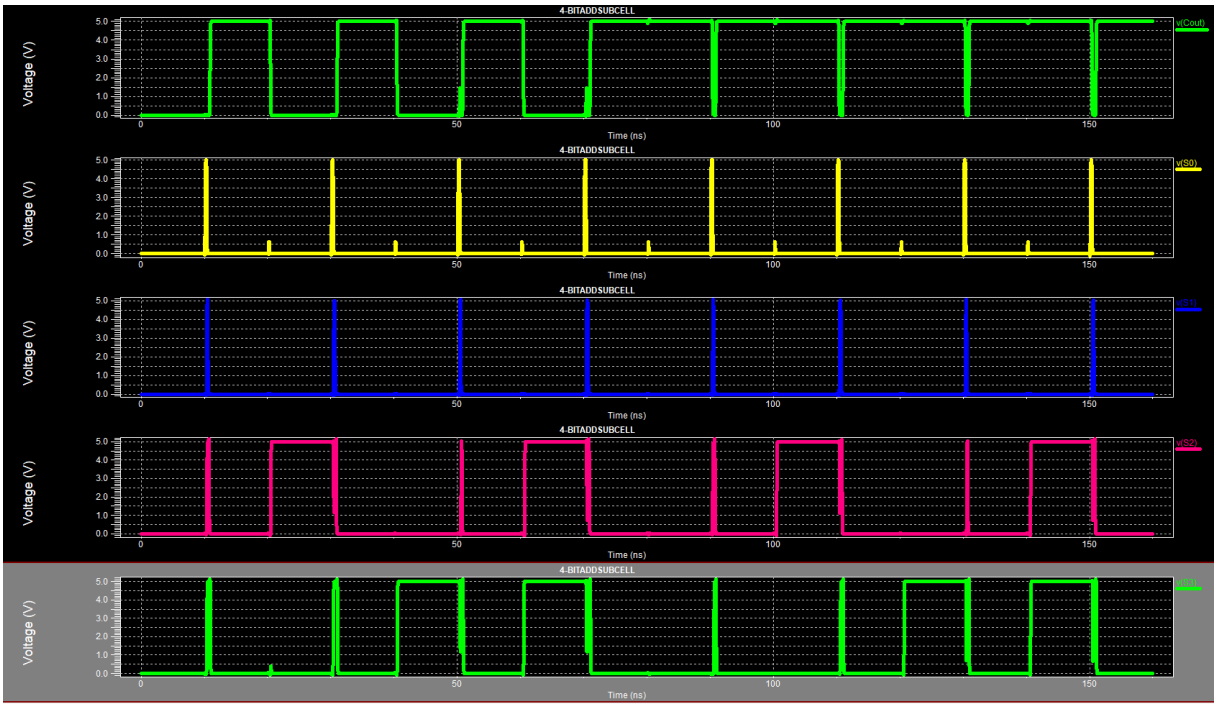

Figure 1. 5: 4- BIT Adder/Subtractor W-EDIT Simulation

W-EDIT output shows that the circuit works correctly.

1.2. L-EDIT DESIGN

According to S-Edit design, the circuit was designed using cell hierarchy. As cell hieararchy XOR Gate, Fulladder L-Edit design and full circuit 4- Bit Binary Adder/ Subtractor L-Edit design are shown in below.

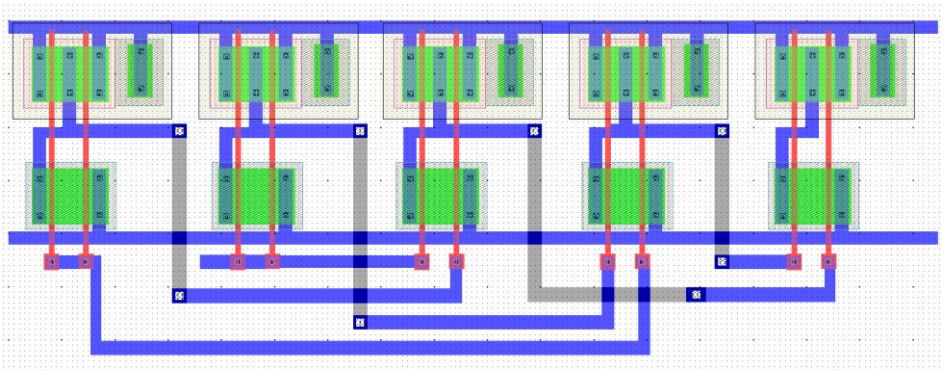

Figure 1. 6: 2 Input XOR Gate Layout

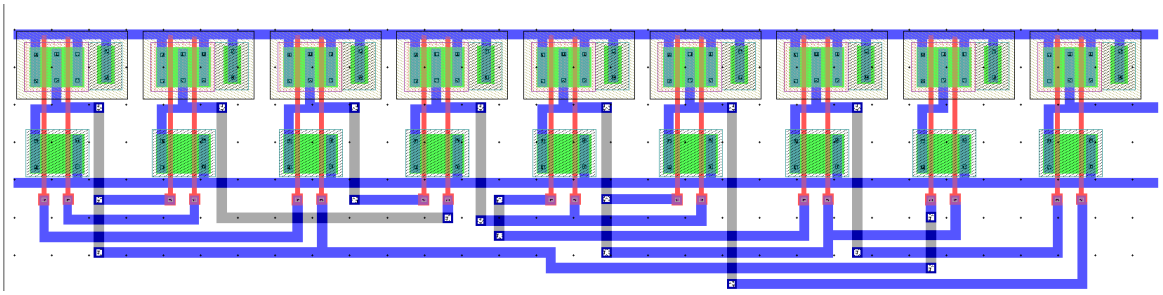

Figure 1. 7: 2 Input Full Adder Circuit Layout

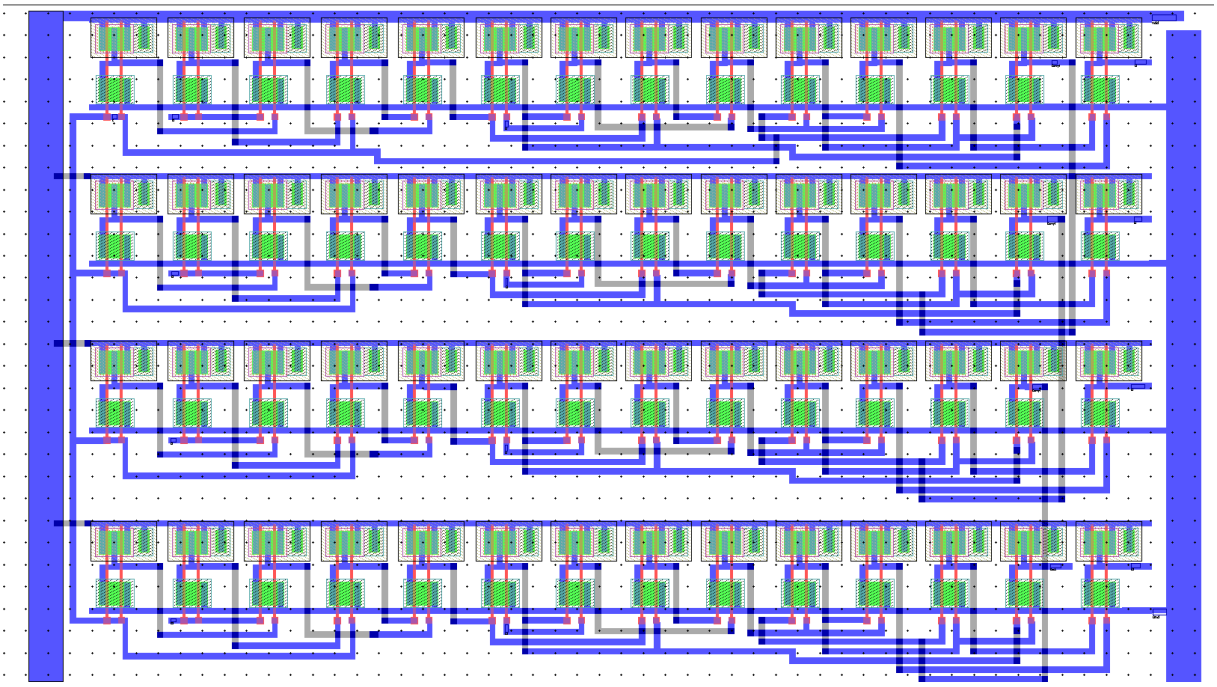

Figure 1. 8: 4-Bit Binary Adder/Subtractor L-Edit Design

```
* Total Nodes: 124
* Total Elements: 224
* Total Number of Shorted Elements not written to the SPICE file: 0
* Output Generation Elapsed Time: 0.012 sec
* Total Extract Elapsed Time: 4.380 sec
VZeynepp Vdd Gnd 5V

VK K Gnd dc 0 BIT   ({0101010101010101} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n  delay=0) AC 0 0 ROUND=0

VA3 A3 Gnd dc 0 BIT ({0000000011111111} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n  delay=0) AC 0 0 ROUND=0
VA2 A2 Gnd dc 0 BIT ({0000111100001111} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n  delay=0) AC 0 0 ROUND=0
VA1 A1 Gnd dc 0 BIT ({0011001100110011} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n  delay=0) AC 0 0 ROUND=0
VA0 A0 Gnd dc 0 BIT ({0101010101010101} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n  delay=0) AC 0 0 ROUND=0

VB3 B3 Gnd dc 0 BIT ({0000000011111111} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n  delay=0) AC 0 0 ROUND=0
VB2 B2 Gnd dc 0 BIT ({0000111100001111} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n  delay=0) AC 0 0 ROUND=0
VB1 B1 Gnd dc 0 BIT ({0011001100110011} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n  delay=0) AC 0 0 ROUND=0
VB0 B0 Gnd dc 0 BIT ({0101010101010101} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n  delay=0) AC 0 0 ROUND=0

.tran 160p 160n start=0
.print tran v(S3) v(S2) v(S1) v(S0) v(Cout)
*.print tran p(VZeynepp)
*.power VZeynepp 0n 160n

.include "C:\Users\Zeynep\Desktop\VLSI_TASARIM_DERSLER\VLSI_tech_files\SCN_0.25u_CMOS.md"
```

Figure 1. 9: Extract to T-Spice

W- Edit simulation output is shown in below.

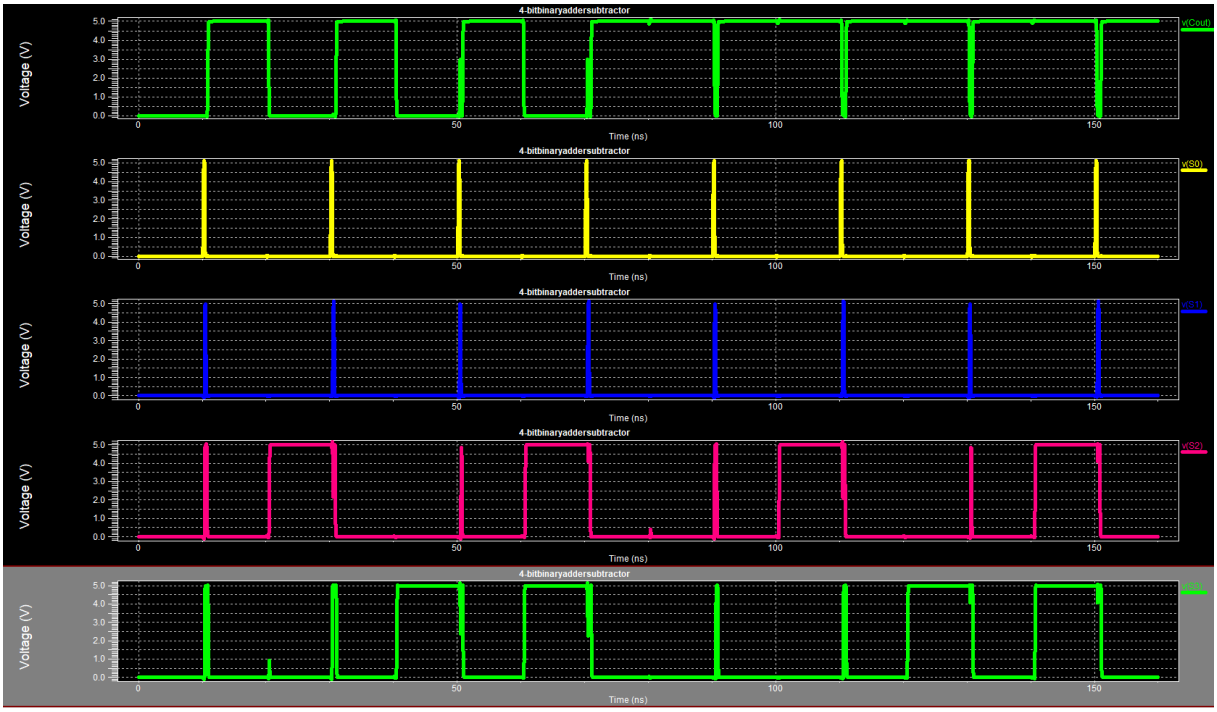

Figure 1. 10: 4-Bit Binary Add/Sub L-Edit Design W-Edit Output

To find out, how much power it consumed, ".print tran p(VZeynepp)" code can be written. Power consumption is shown in below. In CMOS technology, there is no power consumption where it is in logic 0 and logic 1.

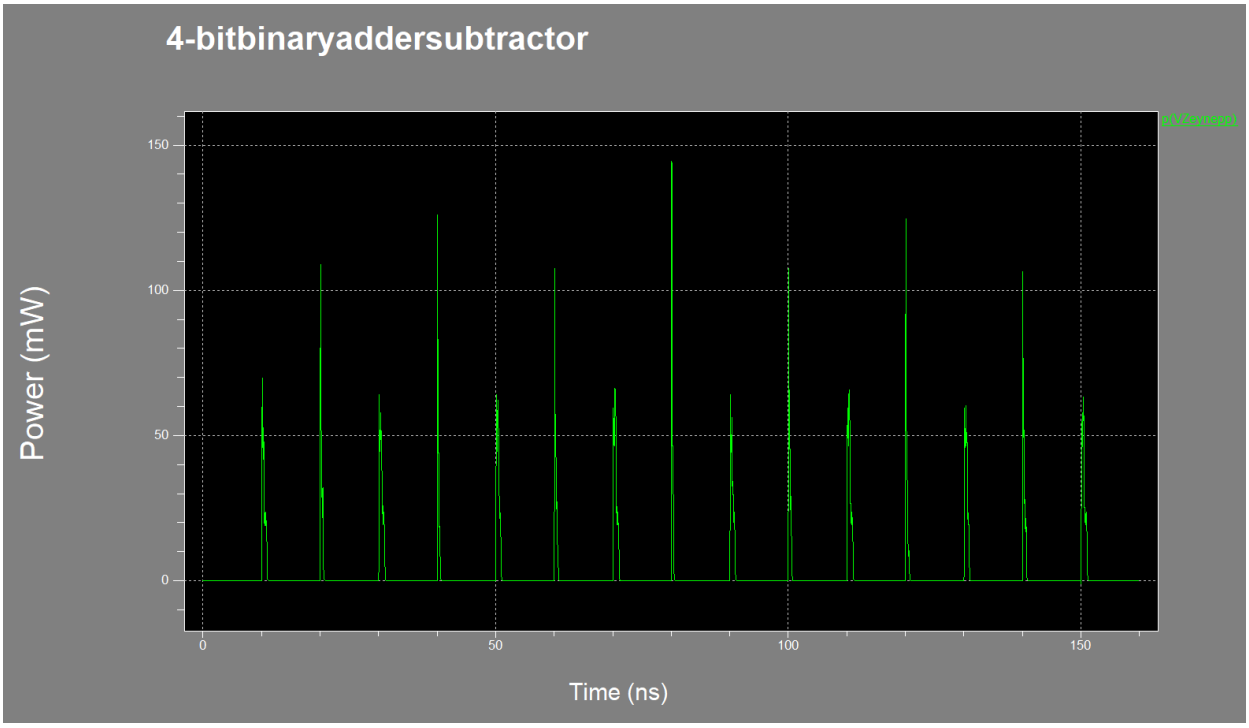

Figure 1. 11: 4-Bit Binary Add/Sub Power Consumption

To find out average power consumed, ".power VZeynepp 0n 160n" code can be written. ".Out" file's output is shown in below.

```
Power Results
VZeynepp from time 0 to 1.6e-007
Average power consumed -> 2.862761e-003 watts
Max power 1.443479e-001 at time 8.0086e-008
Min power 3.924939e-007 at time 9.42e-009
```

Figure 1. 12: 4-Bit Binary Add/Sub Average Power Result

2. 4x16 DECODER DESIGN

2.1. 2 TO 4 DECODER

2x4 Decoder S-EDIT Design circuit is shown in below.

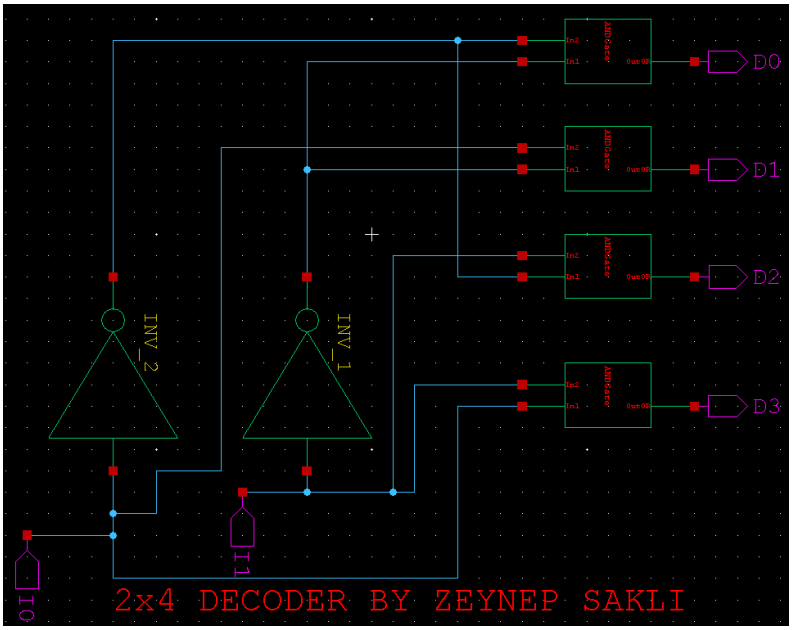

Figure 2. 1: 2 to 4 Decoder S-EDIT Design

```
VZeynepp Vdd Gnd 5V

VI1 I1 Gnd dc 0 BIT ({0011} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n  delay=0) AC 0 0 ROUND=0

VI0 I0 Gnd dc 0 BIT ({0101} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n  delay=0) AC 0 0 ROUND=0

.tran 40p 40n start=0
.print tran v(D3) v(D2) v(D1) v(D0)
.include "C:\Users\Zeynep\Desktop\VLSI_TASARIM_DERSLER\VLSI_tech_files\SCN_0.25u_CMOS.md"
.END
```

Figure 2. 2: 2 to 4 Decoder T-Spice Code

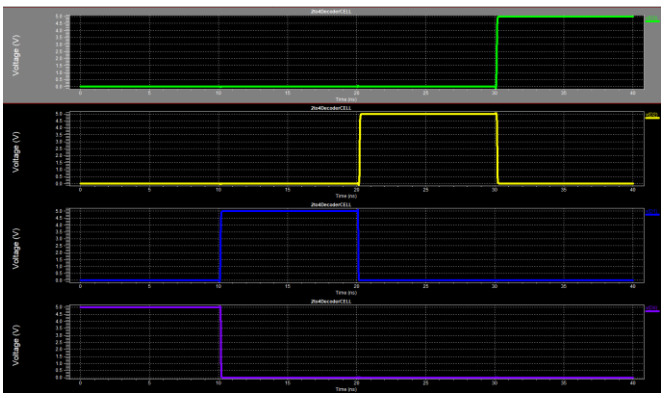

Figure 2. 3: 2 to 4 Decoder D0 to D3 W-Edit Simulation Output

2.2. 4 TO 16 DECODER

2.2.1. S-EDIT DESIGN

S- EDIT designs of 4x16 Decoder circuit is shown in below figure.

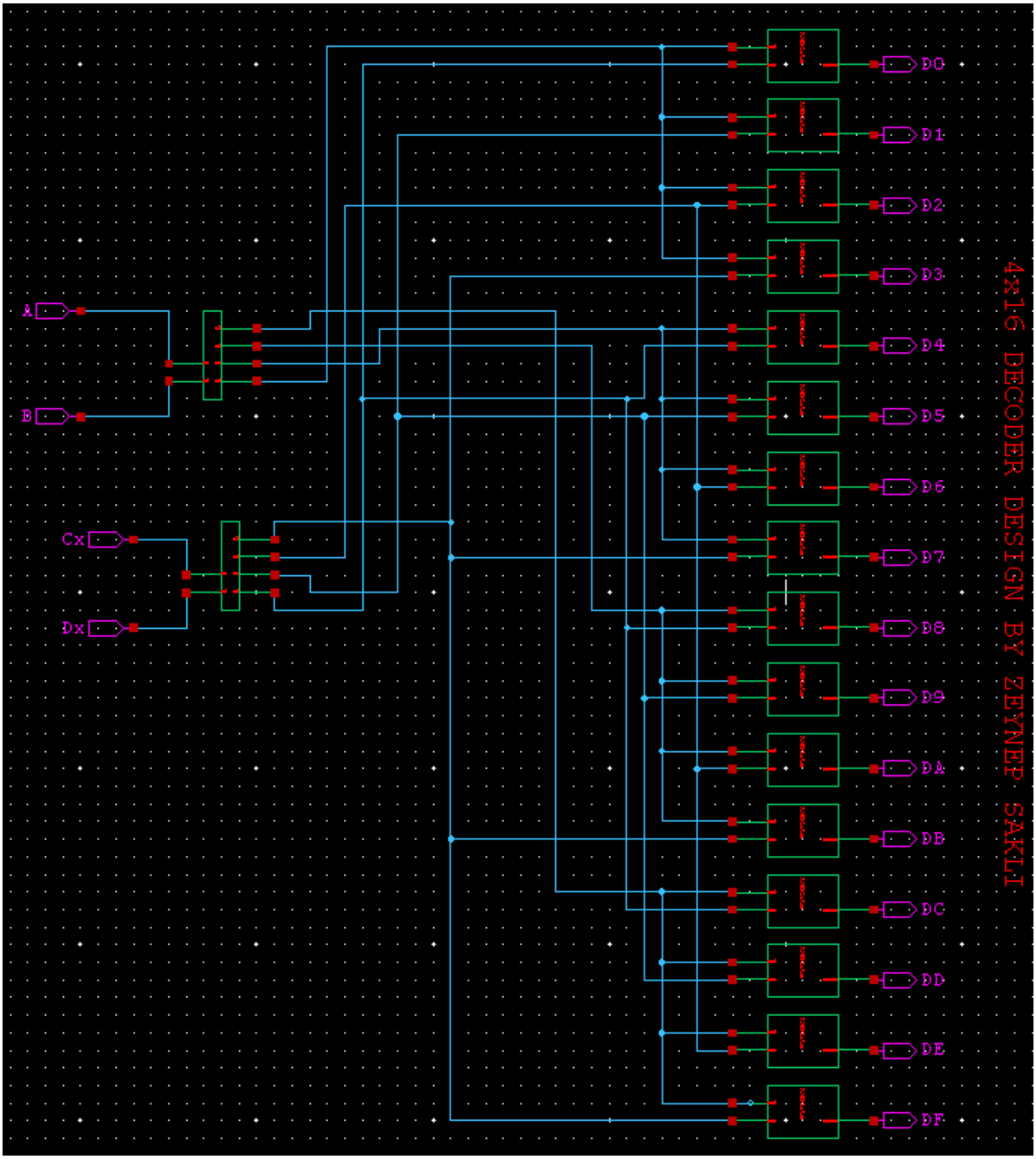

Figure 2. 4: 4 to 16 Decoder S-EDIT Design

```
********* Simulation Settings - Additional SPICE commands *********
VZeynepp Vdd Gnd 5V

VA A Gnd dc 0 BIT   ({0000000011111111} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n  delay=0) AC 0 0 ROUND=0
VB B Gnd dc 0 BIT   ({0000111100001111} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n  delay=0) AC 0 0 ROUND=0
VCx Cx Gnd dc 0 BIT ({0011001100110011} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n  delay=0) AC 0 0 ROUND=0
VDx Dx Gnd dc 0 BIT ({0101010101010101} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n  delay=0) AC 0 0 ROUND=0


.tran 160p 160n start=0
.print tran v(D0) v(D1) v(D2) v(D3) v(D4) v(D5)
.include "C:\Users\Zeynep\Desktop\VLSI_TASARIM_DERSLER\VLSI_tech_files\SCN_0.25u_CMOS.md"


.end
```

Figure 2. 5: 4 to 16 T-Spice Code

In the T-Spice code, just 5 steps are shown as output in the W-EDIT program.

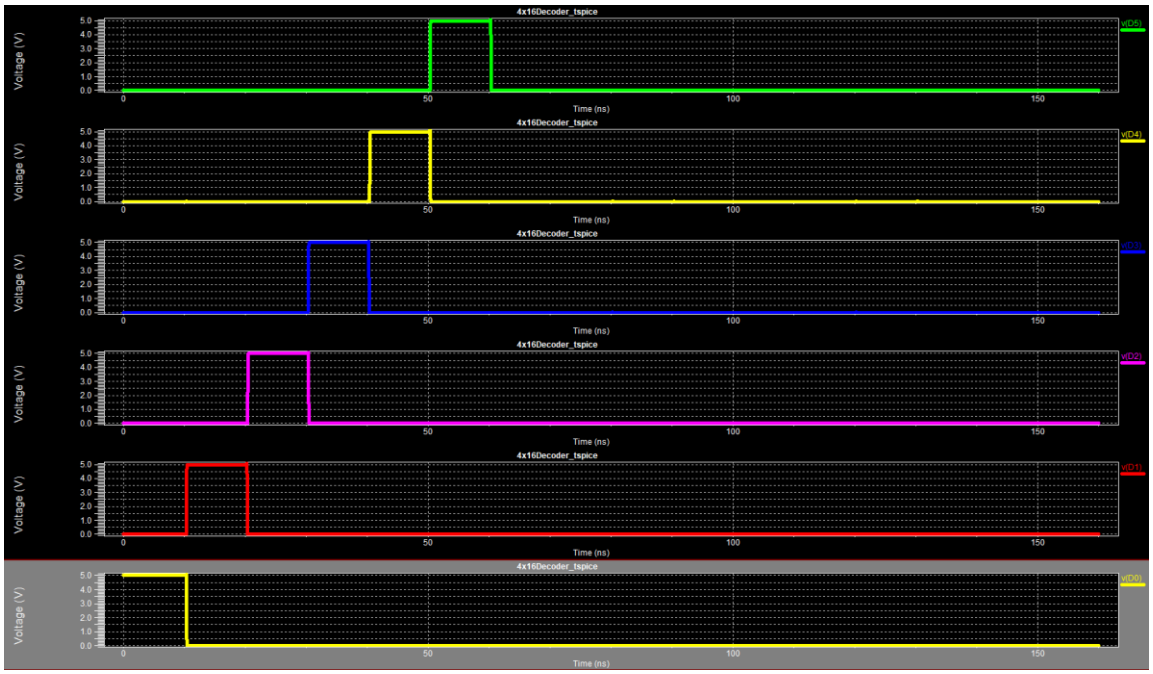

Figure 2. 6: 4 to 16 Decoder D0 to D5 W-EDIT Simulation

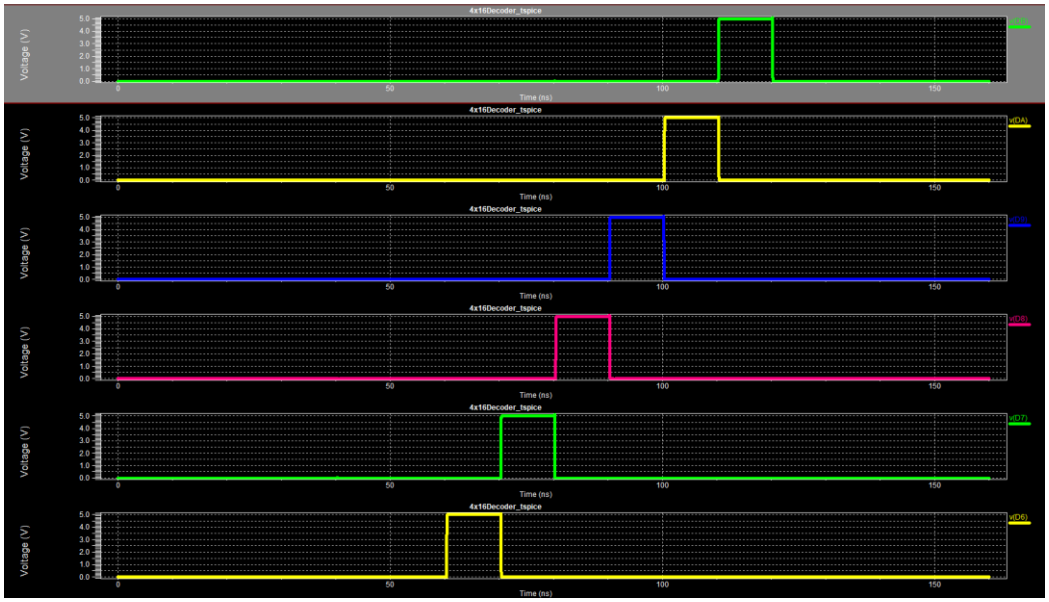

Figure 2. 7: 4 to 16 Decoder D6 to DB W-EDIT Simulation

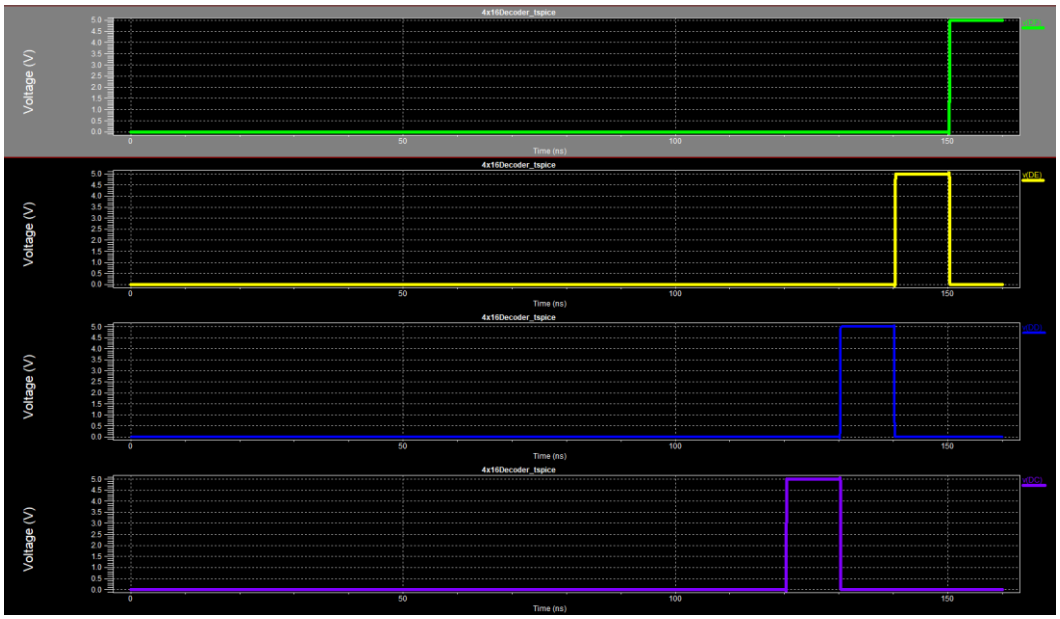

Figure 2. 8: 4 to 16 Decoder DC to DF W-EDIT Simulation

2.2.2. L-EDIT DESIGN

According to S-Edit design, the circuit was designed using cell hierarchy. Firstly using NAND gates and INVERTER as cell, 2 to 4 decoder was designed. Then 2 to 4 decoder was used as different cell.

AND Gate using NAND Gate cell hierarchy circuit is shown in below.

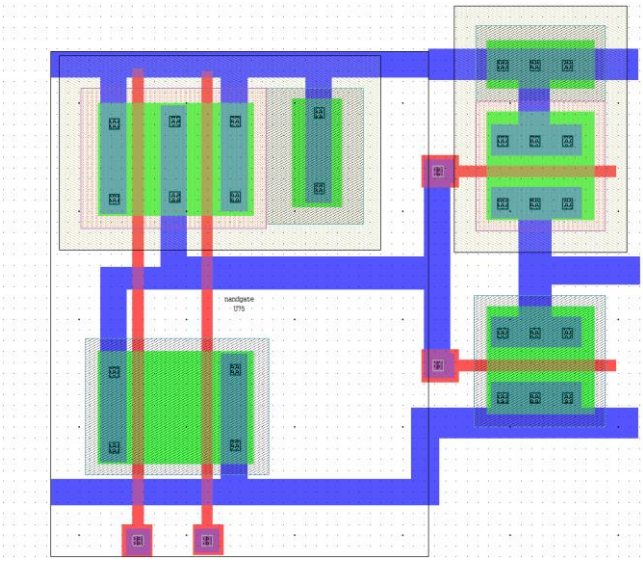

Figure 2. 9: ANG Gate Using NAND Gate Cell Hierarchy

2x4 Decoder S-EDIT Design circuit is shown in below.

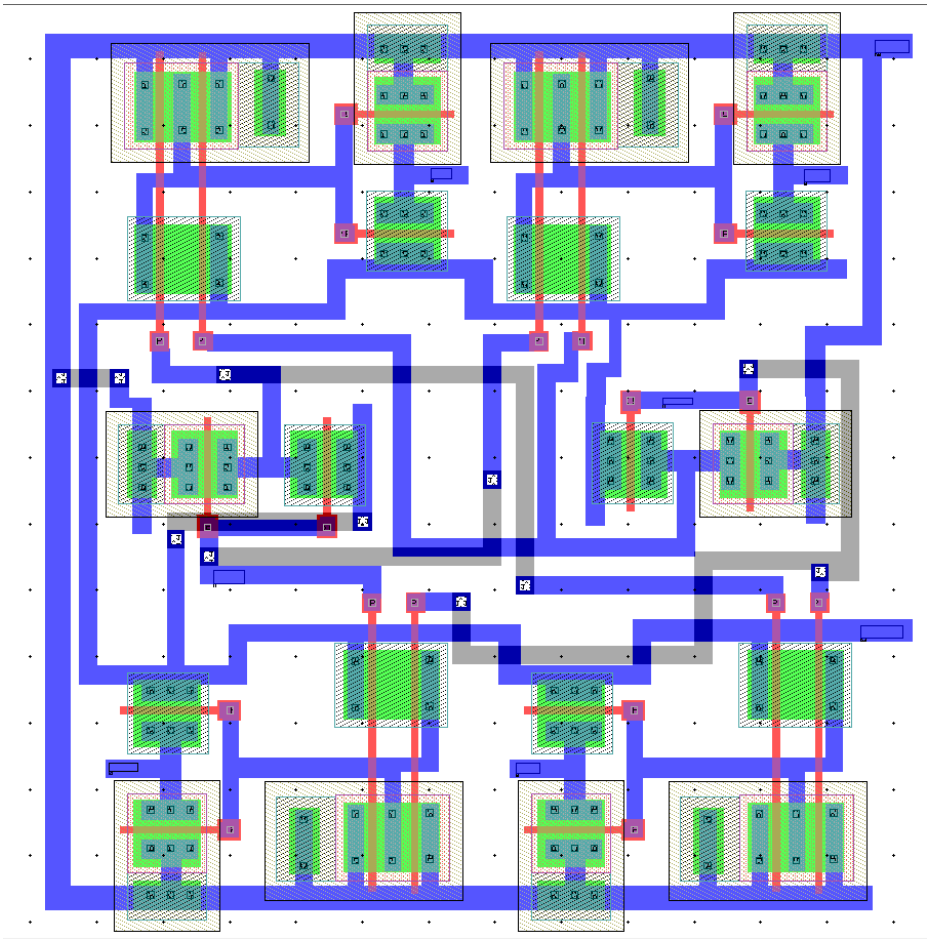

Figure 2. 10: 2x4 Decoder L-edit Using AND Gate Cell Hierarchy

According to S-Edit design, Using 2 2x4 Decoder and 16 AND gates, 4x16 Decoder was designed using cell hierarchy.

4x16 Decoder L-EDIT Design circuit is shown in below.

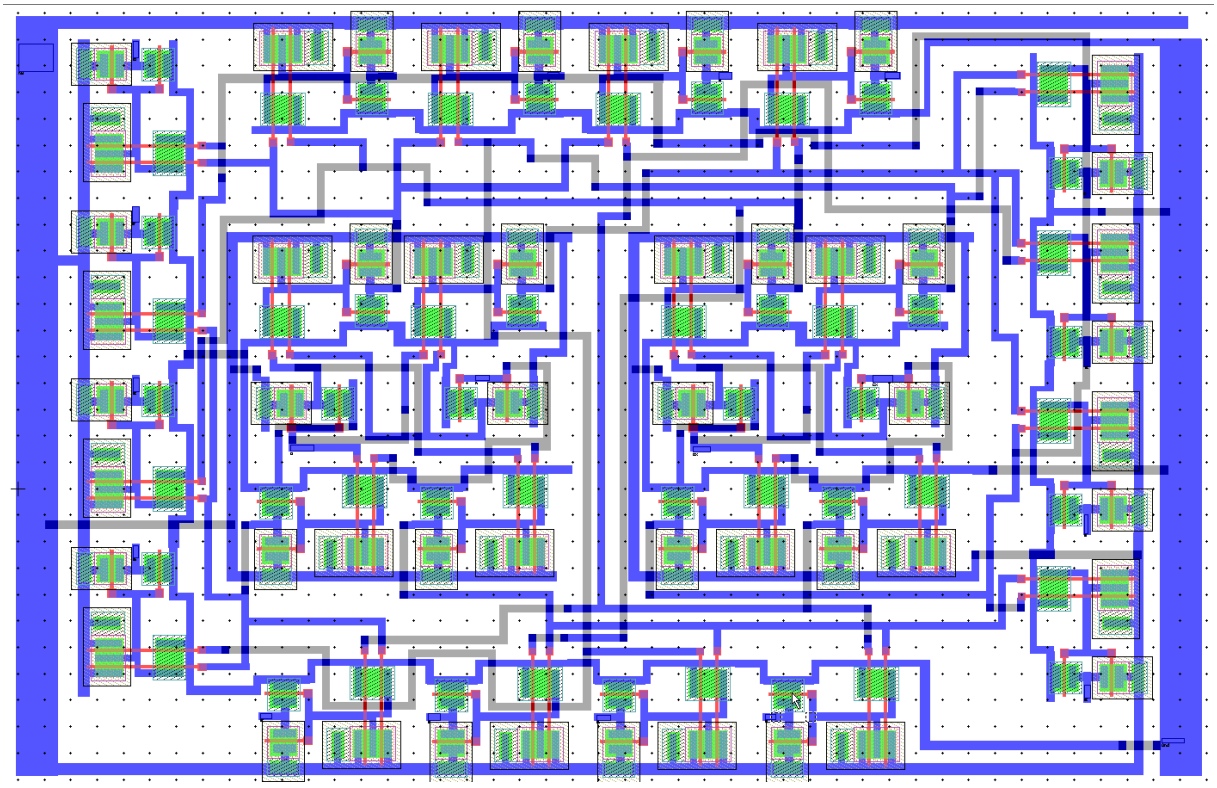

Figure 2. 11: 4x16 Decoder L-Edit Design Using Cell Hierarchy

4x16 Decoder T-Spice code is shown in below.

```
* Total Nodes: 83
* Total Elements: 152
* Total Number of Shorted Elements not written to the SPICE file: 0
* Output Generation Elapsed Time: 0.012 sec
* Total Extract Elapsed Time: 5.191 sec
VZeynepp Vdd Gnd 5V

VA A Gnd dc 0 BIT   ({0000000011111111} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n  delay=0) AC 0 0 ROUND=0
VB B Gnd dc 0 BIT   ({0000111100001111} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n  delay=0) AC 0 0 ROUND=0
VCx Cx Gnd dc 0 BIT ({0011001100110011} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n  delay=0) AC 0 0 ROUND=0
VDx Dx Gnd dc 0 BIT ({0101010101010101} pw=10n lt=10n ht=10n on=5 off=0 rt=0.1n ft=0.1n  delay=0) AC 0 0 ROUND=0


.tran 160p 160n start=0
*.print tran v(MA) v(MB) v(MC) v(MD) v(ME) v(MF)
*.print tran p(VZeynepp)
.power vZeynepp 0n 160n
.include "C:\Users\Zeynep\Desktop\VLSI_TASARIM_DERSLER\VLSI_tech_files\SCN_0.25u_CMOS.md"

.END
```

Figure 2. 12: 4x16 Decoder L-Edit Design T-Spice Code

Just 10 steps are shown as output in the W-EDIT program.

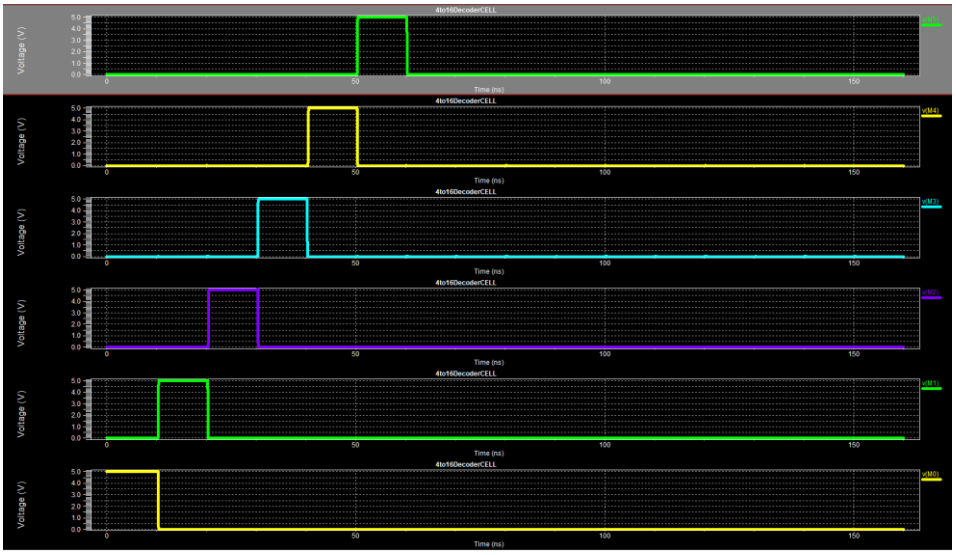

Figure 2. 13: M(0) to M(5) W-Edit Output Simulation

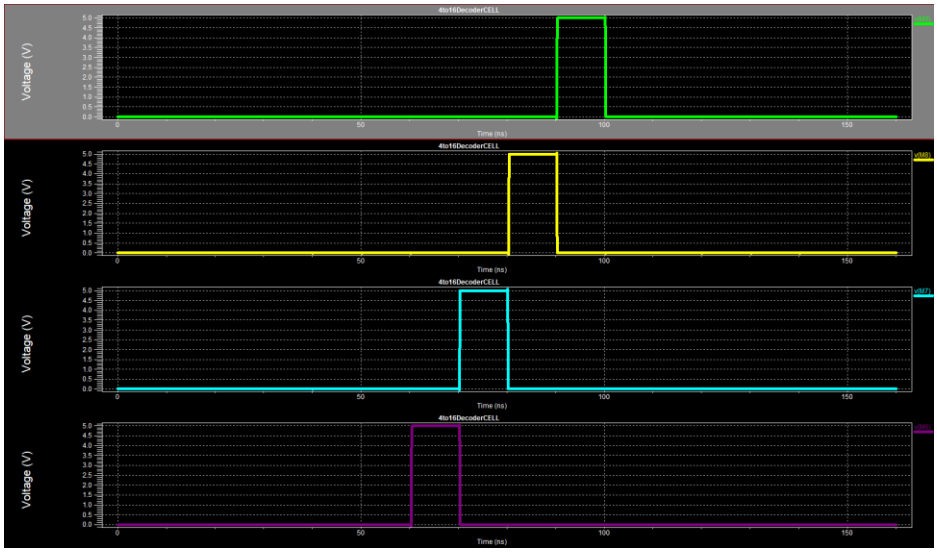

Figure 2. 14: M(6) to M(9) W-Edit Output Simulation

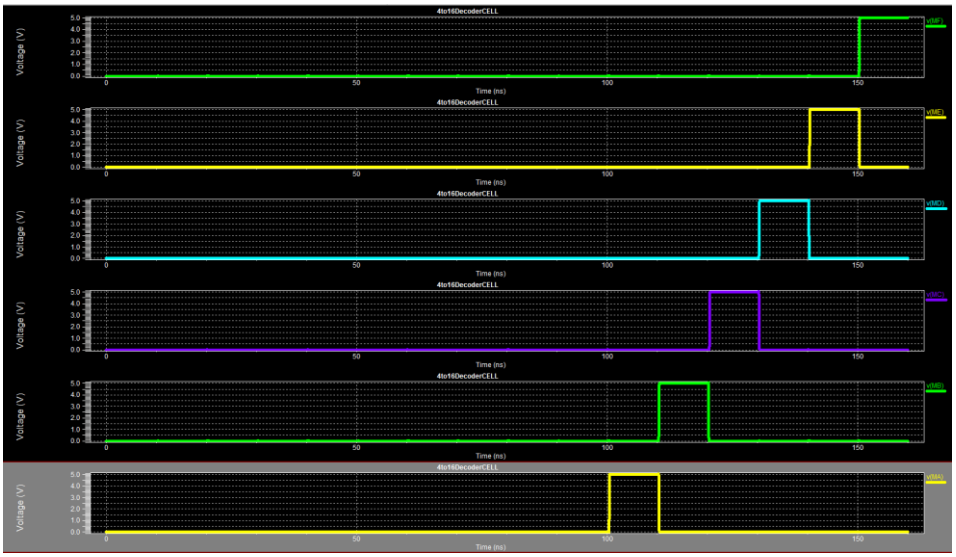

Figure 2. 15: M(A) to M(F) W-Edit Output Simulation

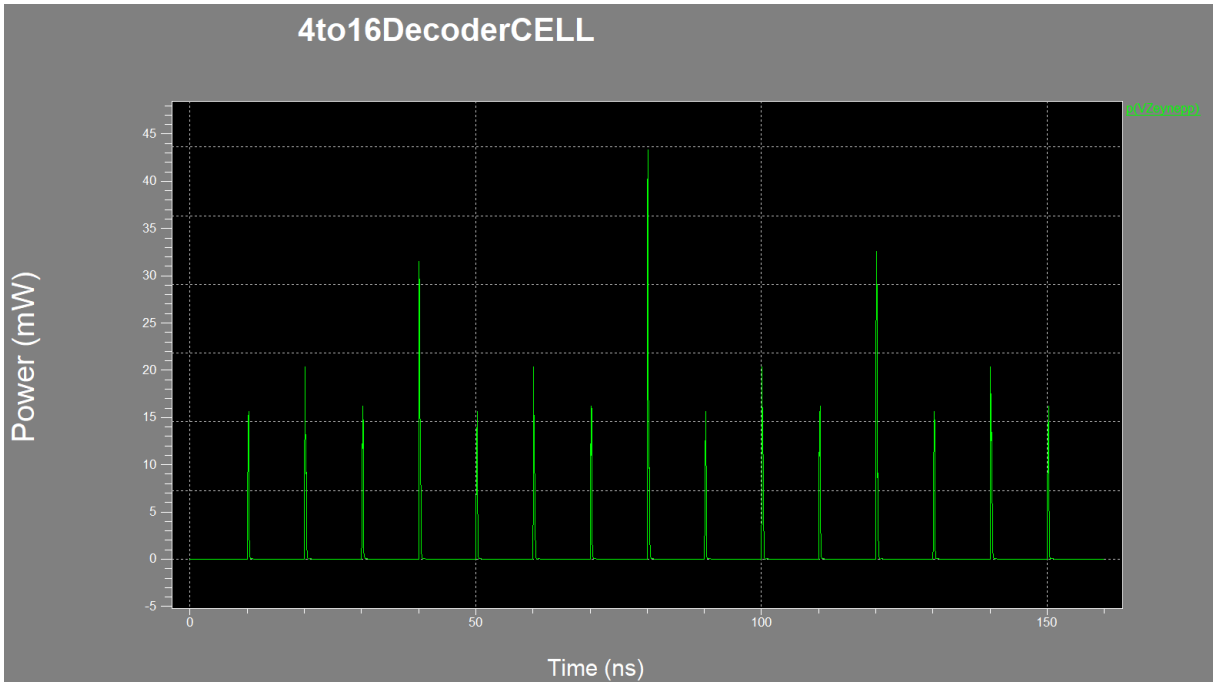

Figure 2. 16: 4x16 Decoder Design Power Consumption

To find out average power consumed, ".power VZeynepp 0n 160n" code can be written. ".Out" file's output is shown in below.

```
Power Results
vZeynepp from time 0 to 1.6e-007
Average power consumed -> 6.303199e-004 watts
Max power 5.953448e-002 at time 8.01e-008
Min power 2.221012e-007 at time 9.42e-009
```

Figure 2. 17: 4x16 Decoder Design Average Power Results