Course Code: CS-223

Course Name: Digital Design and Computer Architecture

Section: 03

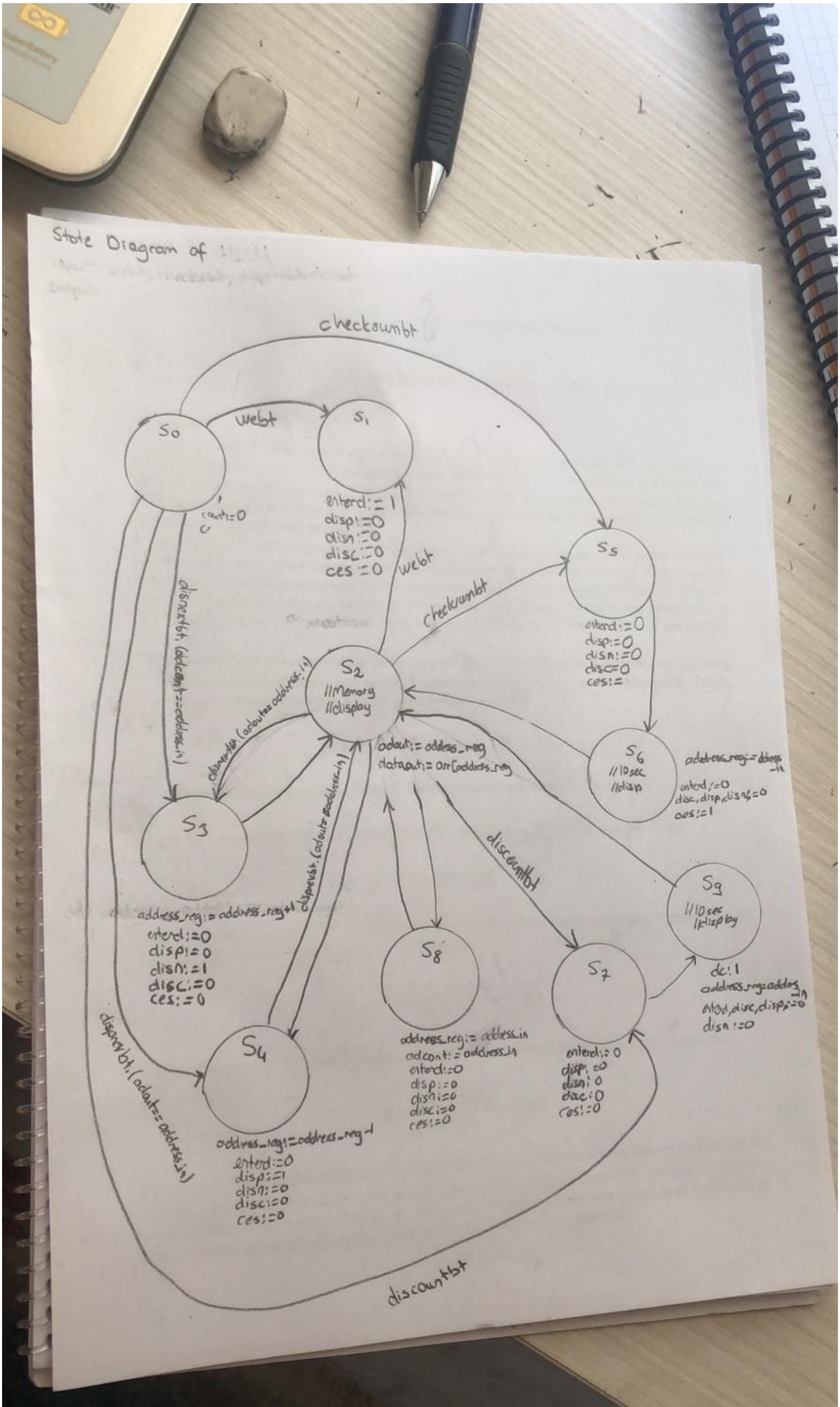
FINAL PROJECT

Name & Surname:Zeynep Büşra Ziyagil

Student ID: 21802646

Date: 18.05.2020

S0: Beginning state of FSM. Inputs fwill be passed to the address_reg and adcont.
S1: Inputs by using 8 switches passed to the address given by 4 switches input. Next state is made S2.
S2: The display state of the FSM. Next and previous address and its value is displayed in the seven segment displayer, . If switches changes it is shown in the S2 state. The previous or next buttons' values change and switches are same next states is S4 and S3 .
S3:Next value of the data is in the displayer.
S4:Previous value of the data is in the displayer.
S5: Calculate checksum and give value n to wait ten seconds, nextstate is S6 .
S6: Checksum value is displayed for ten seconds, address_reg is updated therefore,switch input will be displayed in S2.
S7:Counter value is used. Nextstate is S9 which waits ten seconds.
S8:Conditions of switches,incase they change current values of address and data passes to these switches. Nextstate S2.
S9: Counter value is displayed ten seconds, address_reg is updated therefore,switch input will be displayed in S2.


State Diagram of
checksumbt
webt
S0
S1
countt:=0
enterd:=1
disp:=0
disn:=0
disc:=0
ces:=0
webt
S5
checksumbt
enterd:=0
disp:=0
disn:=0
disc=0
ces:=
S2
//Memory
//display
adout:=address_reg
dataout:=arr[address_reg]
S6
//10sec
//disp
disnextbt.(adcount:=address_in)
S3
address_reg:=address_reg+1
enterd:=0
disp:=0
disn:=1
disc:=0
ces:=0
disprevbt.(adout:=address_in)
discountbt
S9
//10sec
//display
S8
S7
S4
address_reg:=address_in
adcont:=address_in
enterd:=0
disp:=0
disn:=0
disc:=0
ces:=0
enterd:=0
ces:=0
address_reg:=address_reg-1
enterd:=0
disp:=1
disn:=0
disc:=0
ces:=0
discountbt