Prof. Hanson
ECE 302H: Introduction to Electrical Engineering Honors
10/23/2025
100 pts

Mid-Term Exam 2

Name: _____

UT EID: _____

Instructor: _____

Please answer ALL questions. 100 points total.

PLEASE ATTEMPT ALL PROBLEMS AND SHOW ALL WORK!

WRITE ALL EXAM SOLUTIONS IN THE SPACES PROVIDED ON THE EXAM SHEETS.
YOU MAY USE THE BACK OF EACH PAGE FOR SCRATCH, BUT ONLY THE FRONT SIDES WILL BE SCANNED AND GRADED.

No class notes, books, homework assignments, or other materials are allowed. You may use a calculator for the exam. Any calculator that does not have phone/communication/photo capability is allowed. Your calculator's memory should not contain any disallowed information or programs. You have **120 minutes** from the start of the exam to complete the exam.

NOTES: Unless otherwise stated, you may assume all numerical quantities given in the exam problems are known to 3 significant figures, and calculate your answers accordingly. You must show all of your work to receive credit. If you need to make an assumption to answer a question, state it explicitly.

Instructions for turning in your exam:

1) After completing your exam, you may turn on your phones.
2) Please write your EID on the top of **every page** of the exam.
3) Log in to Gradescope and find **MT2** or **Midterm 2**.
4) For each problem, please finish your response within the space for the answer. Scan *all* pages of this exam booklet including the first page and any blank pages in the correct order. Gradescope will automatically assign your answers to each question according to the template.
5) **DOUBLE CHECK YOUR SUBMISSION. YOU SHOULD HAVE ALL PAGES INCLUDING THE COVER PAGE AND THE PAGES YOU LEFT EMPTY.**
6) Turn in your paper exam to the proctor (this will be used as a reference).

Question 1. (30 pts) The op-amp circuit below has 2 op-amps (A_1 and A_2) connected in series.

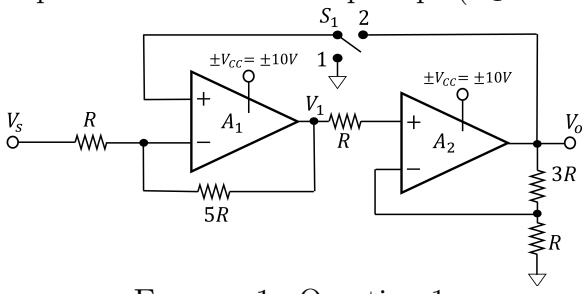


FIGURE 1. Question 1.

For (a)-(e) The switch S_1 is in position 1 (connected to ground).
(a) (2 pts). What is the voltage ($V_{n,1}$) at the inverting input of A_1?
(b) (4 pts) Determine the gain of the first stage of the circuit $G_1 = V_1/V_s$, for linear regime operation.
(c) (3 pts) Determine the gain of the second op-amp circuit $G_2 = V_o/V_1$, for linear regime operation.
(d) (4 pts) What is the total op-amp circuit gain $G = V_o/V_s$ for linear regime operation **and** is the total circuit inverting or non-inverting?
(e) (4 pts) If the input voltage to A_1 is $V_s = 1\,\mathrm{V}$, determine the voltages V_1 and V_o.

For (f)-(h) The switch S_1 is placed in position 2 (connected to V_o).
(f) (2 pts). What is the voltage ($V_{n,1}$) at the inverting input of A_1?
(g) (7 pts) What is the gain $G = V_o/V_s$ of the op-amp circuit? Is the op-amp circuit inverting or non-inverting?
(h) (4 pts) For what range of input voltages V_s is the op-amp circuit operating in the linear regime?

(a) (iv) 0, $V_{n1} = V_{p1} = 0$
(b) $G_1 = -5$
(c) $G_2 = V_o/V_1 = 4$
(d) $G = -20$. The total circuit is **inverting**.
(e) $V_o = -10V$
(f) (i) V_o
(g) $G = \frac{20}{23} = 0.87$, the circuit is **non-inverting**.
(h) $-11.5V \leq V_s \leq +11.5V$

Question 2. (25 pts) On-chip resistors are sometimes formed of the same material that is used to interconnect MOSFETs, namely polysilicon ("poly" simply indicates that the crystal structure is not pure, and can be ignored). Consider a poly-Si resistor that is $w = 180\,\text{nm}$ wide and $t = 180\,\text{nm}$ tall. It is doped with donors at a density of $N_D = 3.45 \times 10^{18}\ \text{cm}^{-3}$. Assume that the intrinsic free electron density in poly-Si is $n_i = 10^{10}\ \text{cm}^{-3}$ and the electron mobility in poly-Si is $\mu_e = 1000\,\text{cm}^2/(\text{V}\cdot\text{s})$.

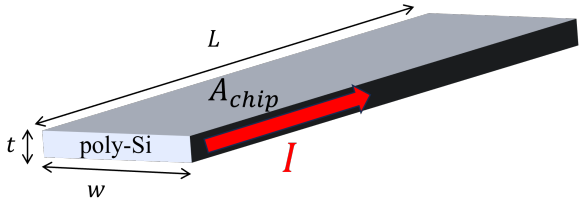


FIGURE 2. Question 2.

(a) (5 pts) Without considering holes, what is the conductivity of the poly-Si in S/cm?
(b) (5 pts) Is it reasonable to not consider the holes? Justify your answer.
(c) (5 pts) You need a 100 kΩ resistor such that 1 V across it results in 10 μA of current through the cross-sectional area $t \times w$ as indicated in the diagram. How much *chip area* ($A_{chip} = L \times w$) would you need to use in μm^2?
(d) (4 pts) By contrast, consider using a MOSFET as a resistor. For small v_{ds}, the MOSFET current is approximately linear with v_{ds}, thus approximating the behavior of a resistor. Use the derivative of $i(v_{ds})$ at $v_{ds} \approx 0$ to show that the equivalent resistance of a MOSFET in this condition is

$$R_{eq} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{gs} - V_T)}$$

(e) (4 pts) Assuming $\mu_n = 1000\,\text{cm}^2/(\text{V}\cdot\text{s})$, $C_{ox} = 0.38\,\mu\text{F/cm}^2$, $W_{FET} = L_{FET} = 180\,\text{nm}$, and $V_T = 0.7\,\text{V}$, and assuming the MOSFET is indeed in the linear region with small v_{ds}, what voltage V_{gs} is required for the MOSFET to behave as a 100 kΩ resistor?
(f) (2 pts) Compare the area of the MOSFET channel ($L_{FET} \times W_{FET}$) to the footprint area of the polysilicon resistor (A_{chip}) – how many times larger is the "real" resistor compared to the MOSFET?

(a) $\sigma = 553 \quad S/cm$
(b) Yes. $p = 29 \quad cm^{-3} \ll n$
(c) $A_{chip} = 32.3\,\mu\text{m}^2$

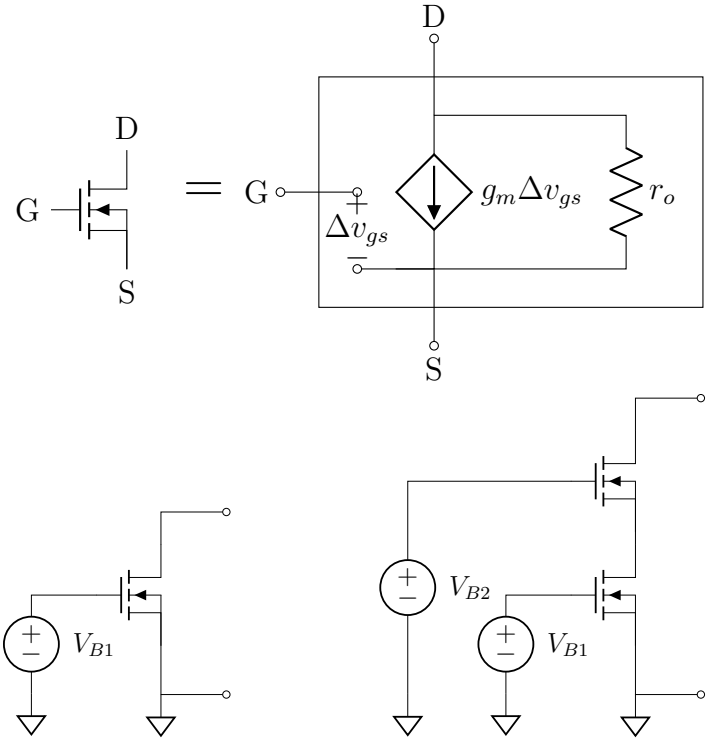
(d) $R = \frac{1}{C_{ox}\mu_n \frac{W_{FET}}{L_{FET}}(V_{GS} - V_T)}$

(e) $V_{GS} = 0.726\,\text{V}$
(f) The real (poly-Si) resistor is 993.8× or almost 1000× larger.

Question 3. (25 pts)
(a) (6 pts) A square parallel-plate capacitor uses SiO_2 with relative permittivity $\varepsilon_r = 3.9$ and oxide thickness $t_{ox} = 60\,\text{nm}$. Each plate is $120\,\mu\text{m} \times 120\,\mu\text{m}$. Compute the *total capacitance* C.
(b) (6 pts) An MIS capacitor uses SiO_2 of thickness $t_{ox} = 40\,\text{nm}$ ($\varepsilon_r = 3.9$) on p-type Si. The (given) threshold is $V_T = 0.50\,\text{V}$. For a *gate voltage* $V_G = 1.80\,\text{V}$, compute the *electron sheet density at the interface* n_s (in cm^{-2}).
(c) (6 pts) Let the *voltage across the oxide* be V_{ox} and the *oxide electric field (magnitude)* be $E_{ox} = |V_{ox}|/t_{ox}$. A reliability guideline specifies $|E_{ox}| \le 5\,\text{MV cm}^{-1}$. For $t_{ox} = 40\,\text{nm}$, find the *largest allowable* $|V_{ox}|$ (in volts) that satisfies the limit.
(d) (7 pts) You require a *capacitance per unit area* of $C/A = 4.0\,\mu\text{F cm}^{-2}$ while the applied *oxide voltage* is $V_{ox} = 1.8\,\text{V}$ and the *oxide-field limit* is $|E_{ox}| \le 6\,\text{MV cm}^{-1}$. Determine the *minimum relative permittivity* ε_r that satisfies *both* requirements.

(a) $C \approx 8.28\,\text{pF}$
(b) $n_s = 7.01 \times 10^{15}\ \text{m}^{-2} = 7.01 \times 10^{11}\ \text{cm}^{-2}$
(c) $|V_{ox,max}| = 20.0\,\text{V}$
(d) $\varepsilon_{r,min} = 13.6$.

Question 4. (20 pts)



(a) (7 pts) A more accurate model for the current through an NMOS device in saturation is

$$i = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(v_{gs} - V_T)^2(1 + \lambda v_{ds})$$

Show that the small-signal model for the MOSFET is given by

$$\Delta i = \left[\mu_n C_{ox}\frac{W}{L}(V_{gs} - V_T)(1 + \lambda V_{ds})\right] \times \Delta v_{gs} + \left[\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs} - V_T)^2\lambda\right] \times \Delta v_{ds}$$

where capital letters represent constant operating point values and Δx values represent small signal perturbations from the operating point. When you cancel or zero-out terms, explicitly indicate why.
Plug in $x = X + \Delta x$ for v_{ds}, v_{gs}, and i. Cancel operating point terms. Let nonlinear terms ($\Delta x \Delta y$ or smaller) be zero.

(b) (6 pts) Explain why the small signal model can be represented by a dependent current source $g_m \Delta v_{gs}$ in parallel with a resistor r_o as shown in the first circuit diagram. What are g_m and r_o in terms of the known parameters? (Not completing this will *not* prevent you from doing the next parts)
Recognize KCL expression to give circuit topology. Recognize v_{gs} term as dependent current source with coefficient g_m. Recognize v_{ds} term as resistor with inverse coefficient r_o.

(c) (4 pts) A current source with a saturated MOSFET with constant gate bias is shown in the second circuit diagram. A perfect current source would have Thevenin reistance $R_{TH} = \infty$. What is the small-signal R_{TH} of this circuit? Again, if it helps, attach a test source to the terminals. You may use g_m and r_o in your answer as known quantities. (Not completing this will *not* prevent you from doing the next parts)
r_0

(d) (8 pts) One way to make a current source with higher R_{TH} is to stack a second MOSFET in series, the so-called "cascode" shown in the last circuit diagram. Consider the MOSFETs to be saturated with the same g_m and r_o and constant gate biases, and use the small signal model to calculate R_{TH} for this circuit. Again, if it helps, attach a test source to the terminals.
$(2 + g_m r_o) \times r_o$, much bigger than r_o