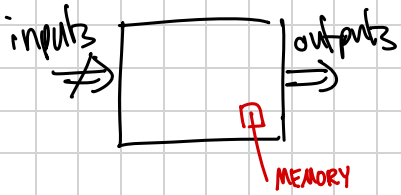
Combinational Logic Circuits

System

- Requirements ⇒ Design Solution



① TT inputs outputs

② Logic expressions

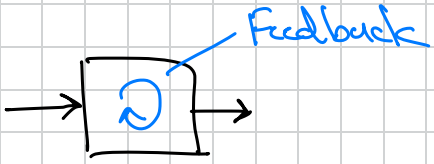
PLA

⇓ simplify

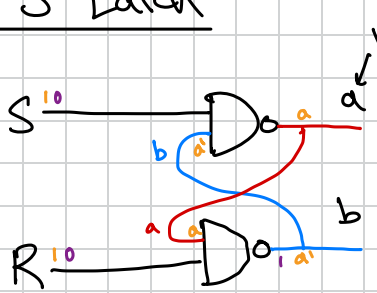
⇓

③ Circuit! ☆

1-bit Storage

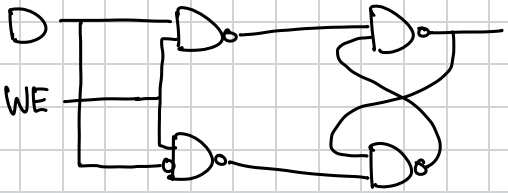


R-S Latch



S	R	a
1	1	holds
0	1	1 latches
1	0	0 latches
0	0	Invalid

D-Latch: Avoids invalid state of an R-S latch by design



D	WE	
%	0	S=1 R=1 Holds
0	1	S=1 R=0 Latches 0
1	1	S=0 R=1 Latches 1

D	WE	Q
	0	Holds
D	1	D

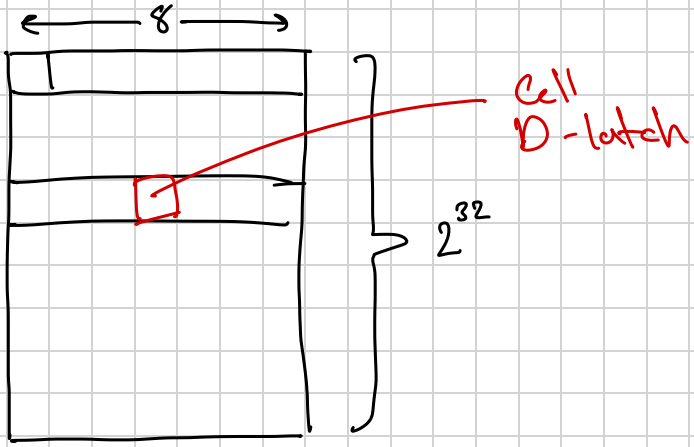
Memory is multi bit storage

4 GiB → Byte 8-bits

Gi - Gibi

2^{30}

$4 \cdot 2^{30} = 2^{32}$



4x3 memory