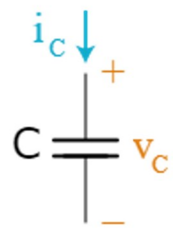
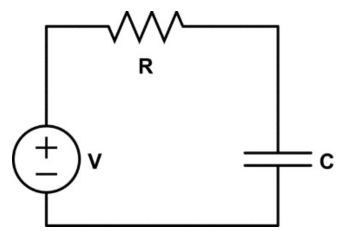
Homework 7 **ECE 302H: Introduction to Electrical Engineering**

Problem 7.1 – Capacitors in circuits (1h)

In class, we mainly learned about capacitors in terms of the charge-voltage relationship, $Q=CV$. This becomes a new circuit component for us. In the circuits context, as usual, we focus on it's current-voltage relationship, $i=C\,dV/dt$.





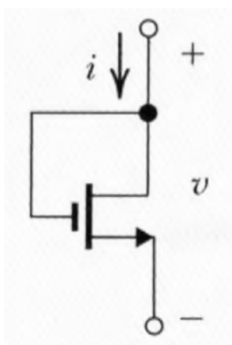
While we're not yet prepared to tackle every circuit with any number of capacitors, with basic calculus we can do some classes of problems. Consider the so-called RC circuit in the Figure above, where we would like to solve for the voltage across the capacitor.

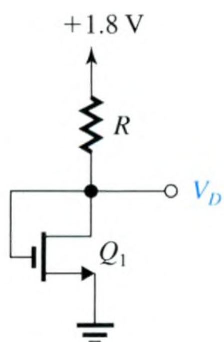
a) Write the KVL, KCL, and component law equations that define how this circuit works (as usual)
b) Combine the equations into a single equation in which v_c is the only unknown (as usual)
c) Your equation will be a differential equation, which is different from the algebraic equations we've seen so far. Let $V=0$ and solve the differential equation assuming that the capacitor's voltage starts at V_{ic}. Write a phrase/sentence stating how the capacitor's **initial condition** enters into the calculation.
d) Your solution will rely on the product $R\times C$. What are the units of RC? What is the significance of this number, known as the **time constant** of the system?
e) Create a table with the percent of the overall transition that the capacitor voltage has completed after N time constants, where N = 1,2,3,4,5.
f) Use Thevenin's Theorem to demonstrate that a system with a single capacitor (plus any number of resistors and sources) will result in the same solution as above and therefore will be characterized by a single time constant. Do the sources affect the time constant?
g) Use LTSpice to simulate the RC circuit with V = 0V, R = 10Ω, C=3μF. Label the node below the capacitor as ground and the node above the capacitor as "vc." Place a "spice directive" anywhere on the schematic that says ".ic V(vc)=5" to set the initial condition on the capacitor. Use a transient simulation and make sure to simulate for a long enough time to see the whole transition but not so long of a time that you can't see the transition. Include a screenshot of the schematic and the capacitor voltage as your solution to this part.

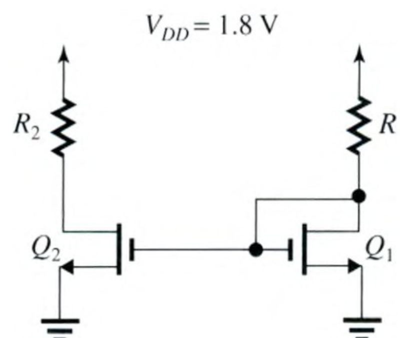
Problem 7.2 – Diode-Connected Device (1h)

Sometimes NMOS transistors have their gates shorted to their drains as shown in the Figure. This is known as a diode connected device.

a) Will the transistor operate in the cutoff, linear, or saturation region?
b) Assume the MOSFET parameters and geometry (μ_n, C_{ox}, V_t W, L) are known and ignore channel length modulation ($\lambda = 0$). Calculate the I-V characteristic of this two-terminal device when v is positive and when v is negative. In what way is this characteristic similar to the exponential behavior of a diode and in what way is it not similar?
c) The NMOS transistor in the second Figure have $V_t = 0.5\,V$, $\mu_n C_{ox} = 400\,\mu A/V^2$, $\lambda = 0$, $W = 0.72\,\mu m$, and $L = 0.18\,\mu m$. Find the value of R that results in $V_D = 0.7\,V$.
d) The third Figure is obtained by augmenting the second Figure with a transistor Q_2 identical to Q_1 but with $W = 2.16\,\mu m$. As long as Q_2 is in the saturation region, what will I_{D2} be? Does it matter what value R_2 is?
e) What value of R_2 results in Q_2 being at the edge of saturation? Should R_2 be bigger or smaller than this value to keep Q_2 in saturation?







Problem 7.3 – MIS capacitors (0.5h)

An MIS capacitor is composed of an SiO_2 (relative permittivity = 3.9) dielectric of thickness 40 nm on top of p-type silicon with doping level $N_A = 10^{17}/cm^3$. Assume the threshold voltage is 0.5 V and a voltage of 1.8 V is applied to the capacitor.

a) Calculate the induced surface charge density (charge per unit area) in the metal electrode. Are these charges positive or negative, mobile or stationary?
b) What must the induced charge density be at the semiconductor surface?
c) How much of the induced charge density at the semiconductor surface is due to stationary charges vs mobile charges?

Problem 7.4 – An MOS FET (0.5h)

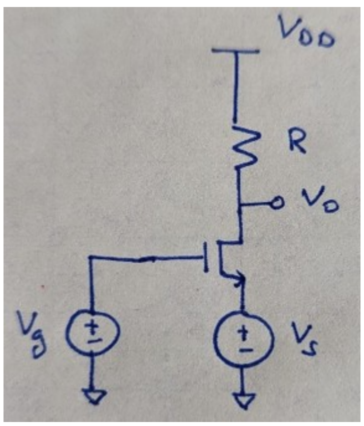
A MOSFET is made with a dielectric composed of SiO_2 (relative permittivity 3.9) and thickness 40 nm. The channel length is 180 nm and the channel width is 3 μm. The applied gate voltage is 3V, the source voltage is 0 V, and the drain voltage is 0.5 V. The threshold voltage is 0.5 V. Assume the mobility of electrons to be 1000 cm^2/Vs.

a) Calculate the drain current
b) Calculate the equivalent resistance of the MOSFET assuming that its drain current rises linearly with its voltage up to the operating point in the problem.
c) All else equal, if the drain voltage is gradually increased, at what value of drain voltage will the drain current saturate to a constant value? What will that constant value be?

Problem 7.5 – Small Signal Modeling (1h)

Consider the so-called "common-gate" amplifier below. For all parts, assume the following:

$\mu_n C_{ox} = 200\ \mu A/V^2$ $\mu_p C_{ox} = 100\ \mu A/V^2$
$V_T = 0.4\,V$ for NMOS devices $V_T = -0.4\,V$ for PMOS devices
W/L = 10



a) An amplifier is made with an NMOS transistor as shown in the figure. $R = 2k$ and $V_{DD} = 2V$. The DC value of the gate voltage (V_G) is 0 V. Calculate the value of the input, V_S, that will result in the FET being at the edge of saturation.
b) Calculate the small signal transconductance g_m for the MOSFET in (a).
c) $v_s(t)$ has a dc value V_S calculated in (a) as well as small perturbation such that $v_s(t) = V_S + \tilde{v}_s$. Draw the small signal model of the amplifier and calculate the small signal voltage gain $\tilde{v}_o / \tilde{v}_s$. Let your answer be symbolic, i.e., a function of g_m and R rather than a number.
d) At the output port, calculate the Thevenin equivalent of the small-signal model of the circuit as a function of g_m and R.

e) At the input port (i.e., across v_s), calculate the Thevenin input impedance of the small signal model of the circuit as a function of g_m and R, assuming that the output is open circuited.