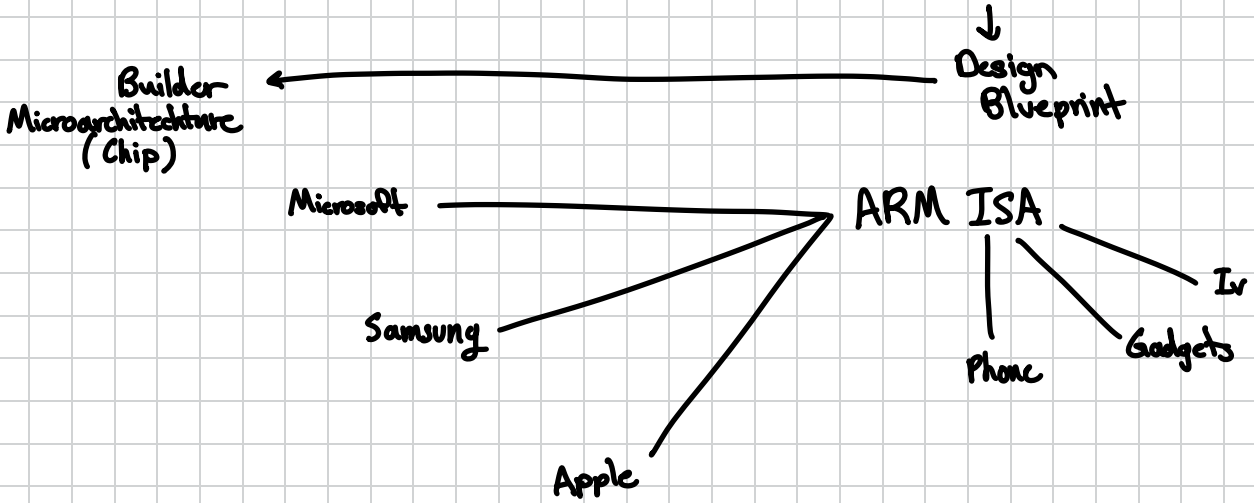
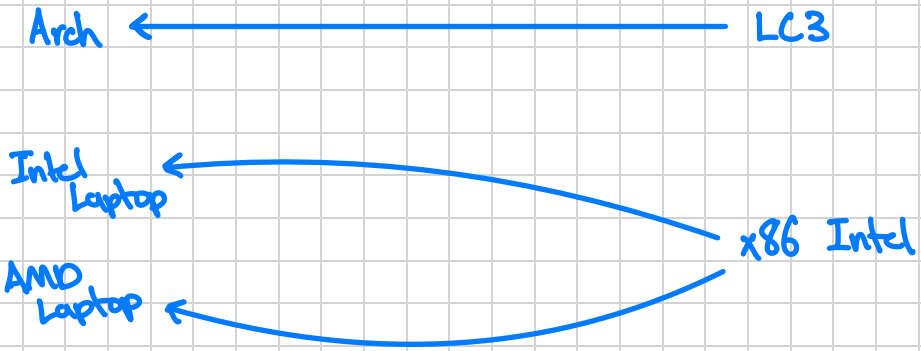
Instruction Set Architecture

Von Neumann Model

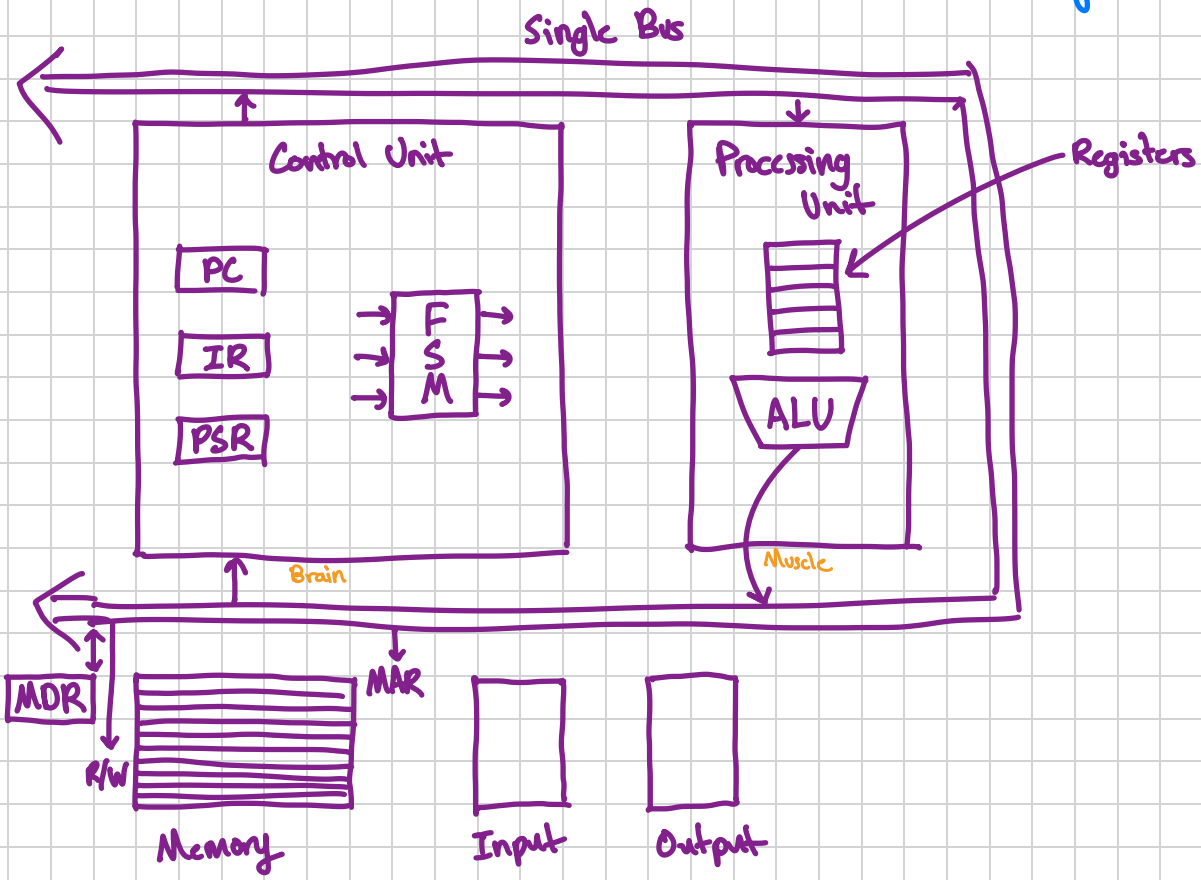
LCS ISA





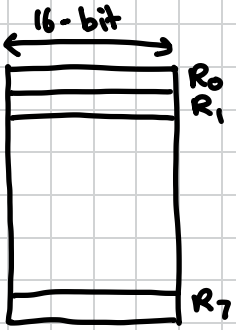
LC3 ISA → Arch

Von Neumann Model
Single Bus



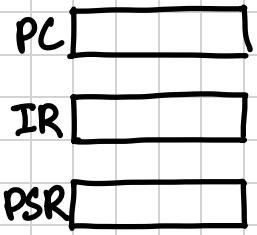
LC3 ISA

① Registers



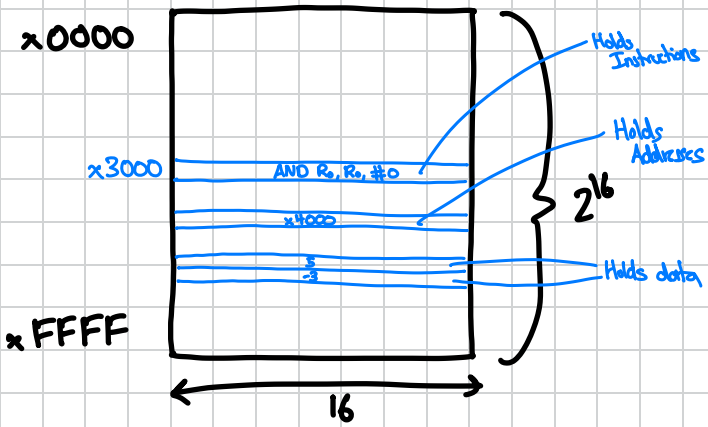
General Purpose Registers
Hold Data/Address

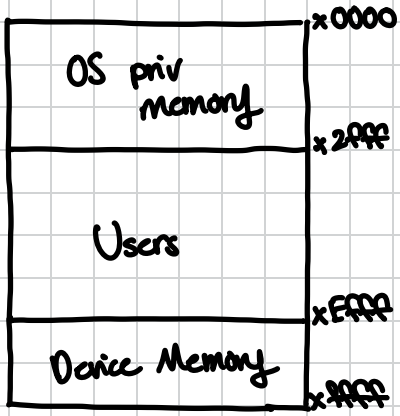
Special



Holds address of the NEXT instruction to exec
Holds the instruction currently being executed
Holds the status of the program

② Memory





③ Instruction Set

- Arithmetic Logic Instruction

  ADD NOT AND

- Data movement (load/share)

  LD ST
  LDR STR
  LDI STI

- Control Instructions

  BR JMP JSR TRAP

  RTI