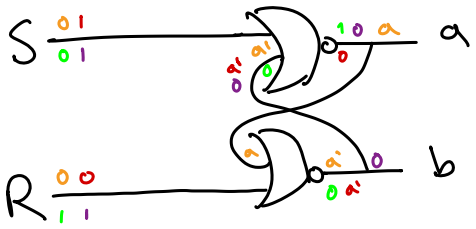
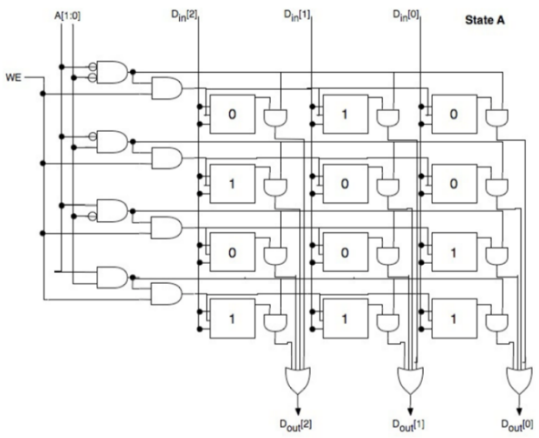
(1)

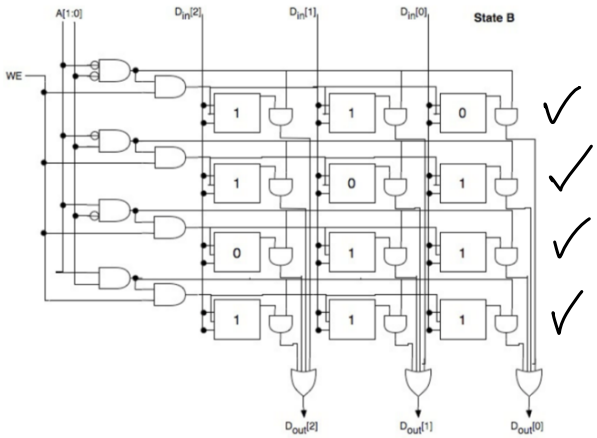


S	R	a
0	0	holds
0	1	1 latches
1	0	0 latches
1	1	invalid

(2)

2. (10 pts) After five clock cycles memory goes from state A to state B (shown below). The table below shows values of the 2-bit address(A[1:0]), 1-bit Write-Enable and 3-bit D_{in} signals. For each cycle, fill in the missing bits (represented by dashes)



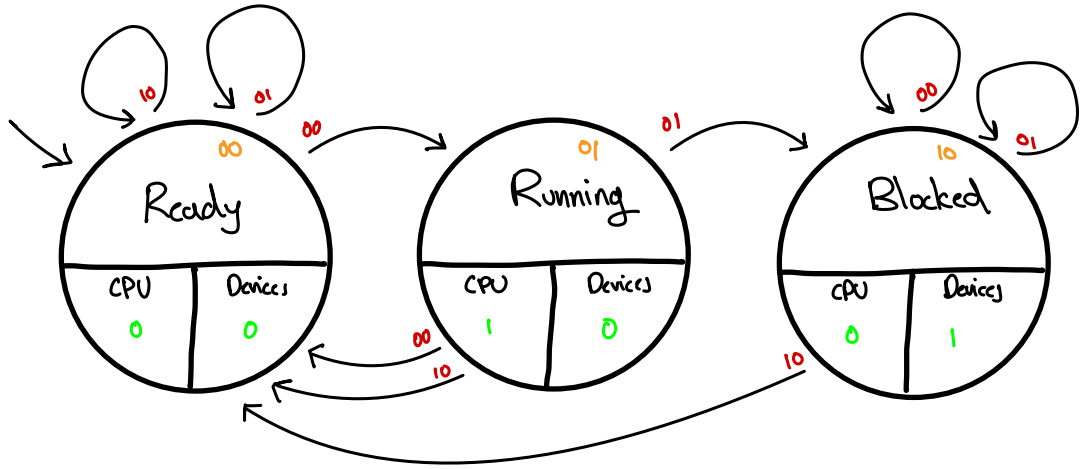


	A[1:0]	WE	D_{in}[2:0]
Cycle 1	1 0	1	0 1 1
Cycle 2	1 1	0/1	1 1 1
Cycle 3	0 0	1	0 0 0
Cycle 4	0 0	1	1 1 0
Cycle 5	0 1	1	1 0 1

3

- Input is the scheduler which can pick one of 3 states, 00, 01, 10.

a.



b.

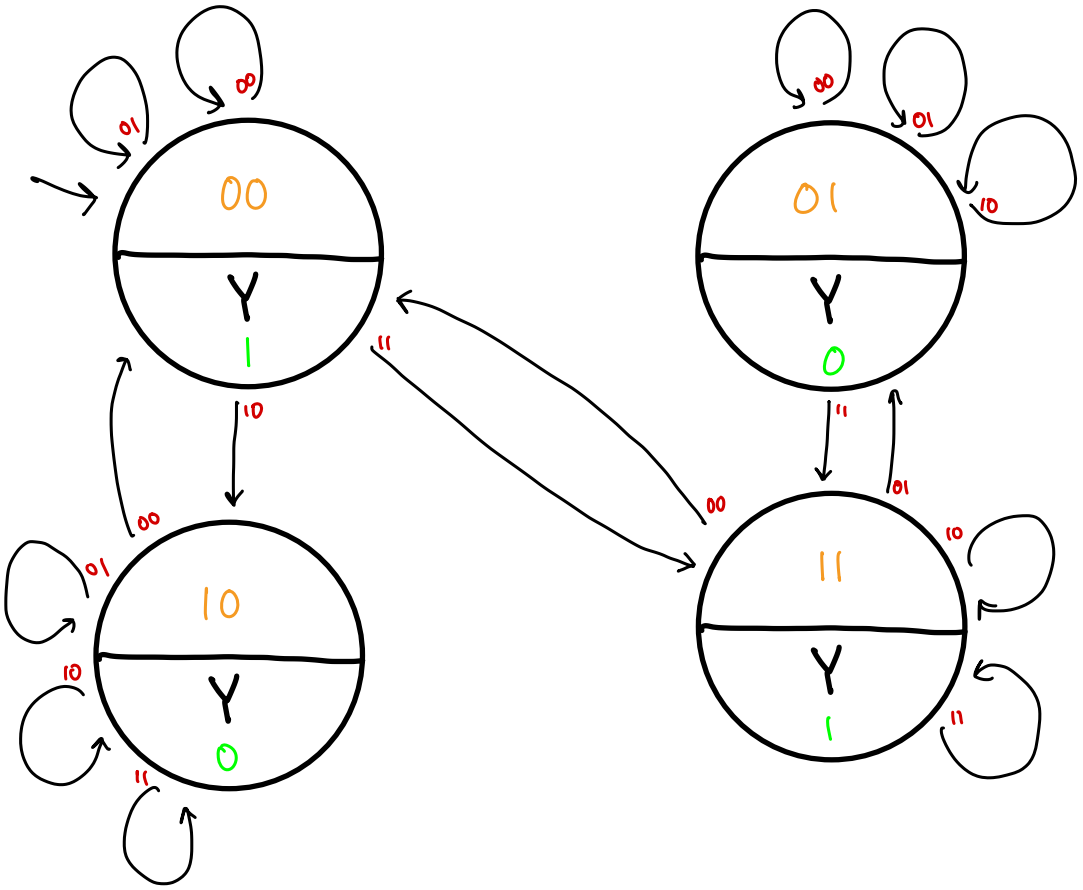
C.S.	I	N.S.
0 0	0 0	0 1
0 0	0 1	0 0
0 0	1 0	0 0
0 1	0 0	0 0
0 1	0 1	1 0
0 1	1 0	0 0
1 0	0 0	1 0
1 0	0 1	1 0
1 0	1 0	0 0

c.

C.S.	CPU	Dev
0 0	0	0
0 1	1	0
1 0	0	1

4

a.



b. $2^4 = 16$

You would need a $4 \rightarrow 16$ decoder

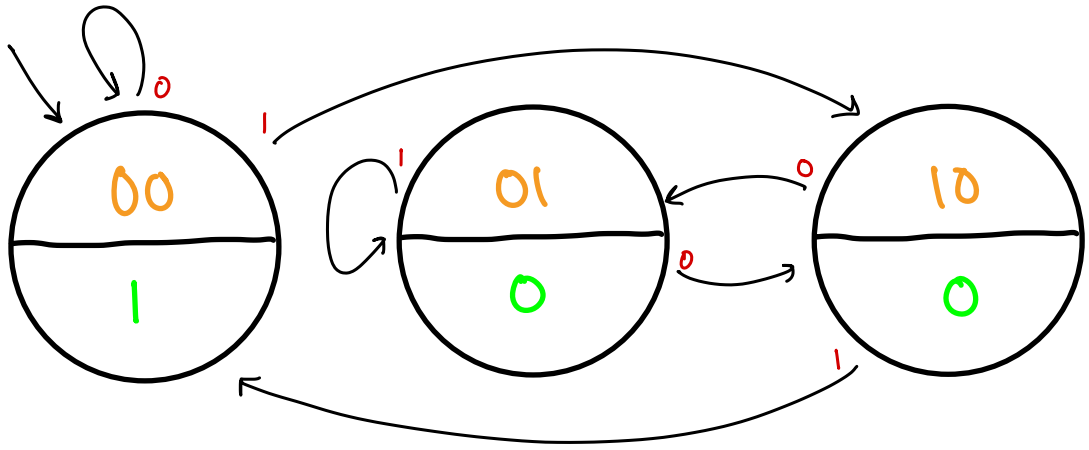
c. $S_1' S_0' + S_1 S_0 = XNOR(S_1, S_0)$

5

a.

CS_1 CS_0 C.S.	I	NS_1 NS_0 N.S.	X
0 0	0	0 0	1
0 0	1	1 0	1
0 1	0	1 0	0
0 1	1	0 1	0
1 0	0	0 1	0
1 0	1	0 0	0

b.

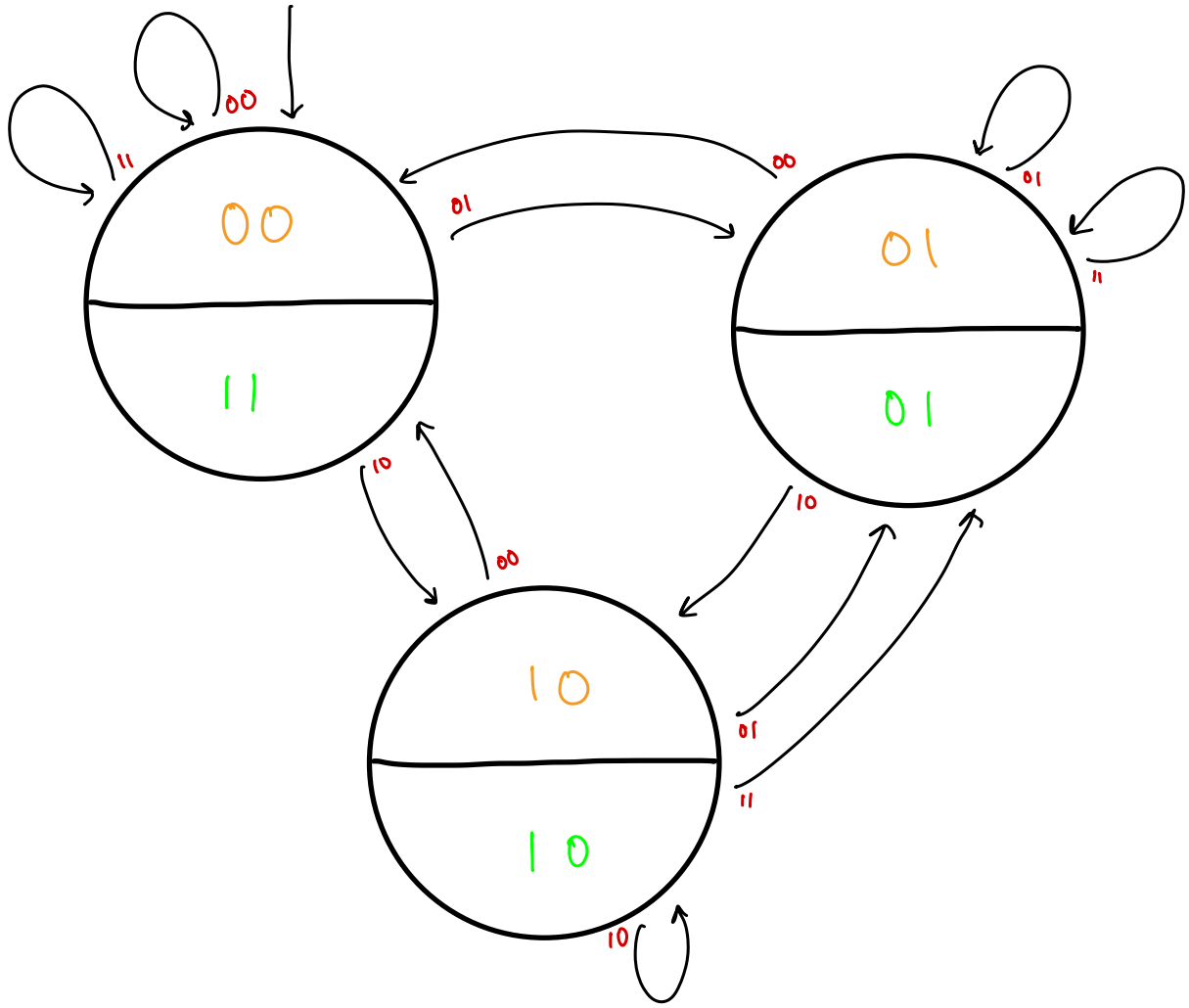


6

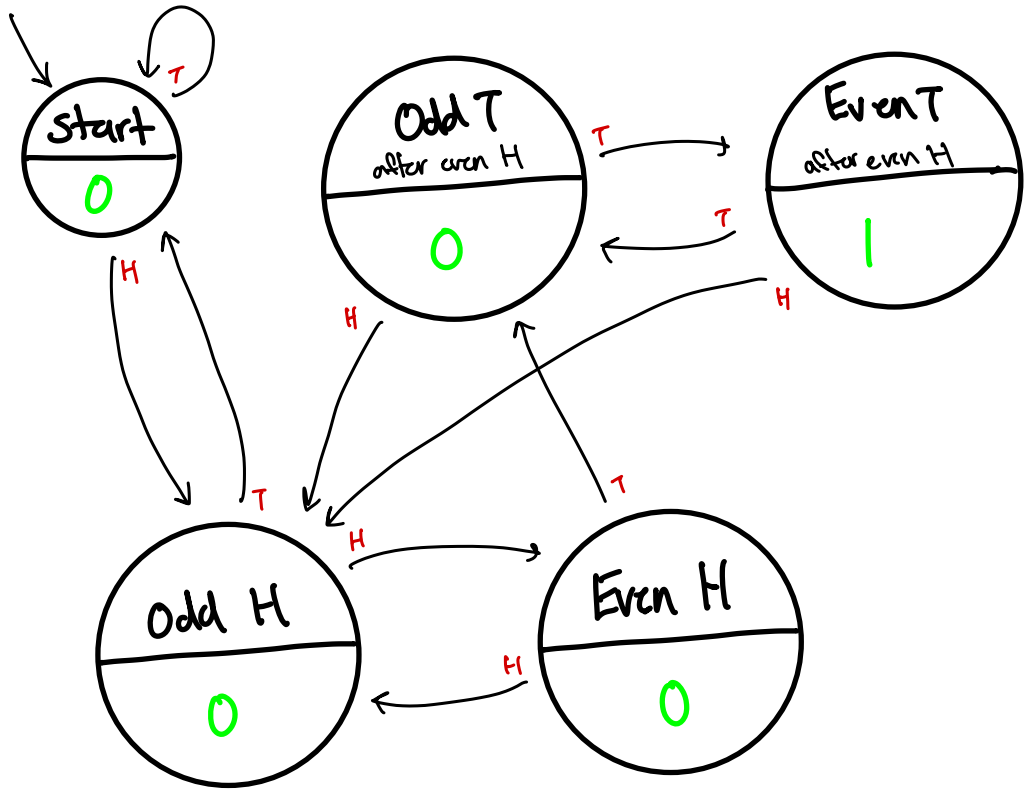
a.

C.S.	Out
0 0	1 1
0 1	0 1
1 0	1 0

b.



7


Start
0
T
Odd T
after even H
0
T
T
Even T
after even H
1
H
H
H
T
T
T
H
Odd H
0
Even H
0
H

What if not restricted to even T after even H