

# Introduction to Computing: Homework 3

Fall 2025

Dr. Ramesh Yerraballi

The University of Texas at Austin

Due: Tuesday 9/23 11:59pm

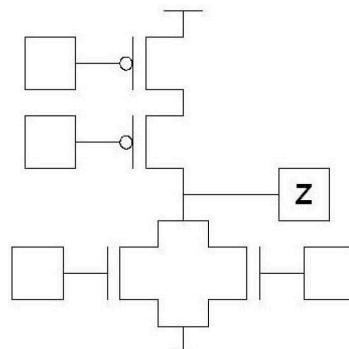
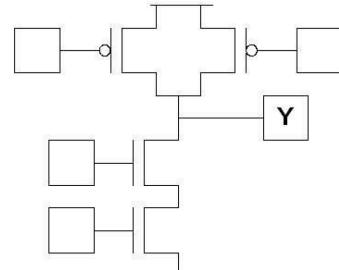
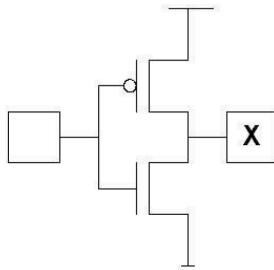
Instructions:

You may discuss the problem set solutions with your fellow classmates but the write up must be your own. Please use the TAs and the Instructor for help before you seek out a friend or classmate. Show your work. You may handwrite or type-write your answers.

1. (16 pts) Label the inputs of each single circuit of transistors to achieve the equation:

$$\text{OUT} = \text{NOT(A AND (B OR C))}$$

Using the circuits below, label all inputs (square boxes) to achieve the above equation. The output signal Out is one of X, Y, or Z. Note that the output of one circuit can be the input of another, and only A, B, C, X, Y and Z can be used as inputs.



2. (8 pts)

- Fill in the truth table for the logic equation:

$$\text{OUT} = \text{NOT(NOT(A) AND NOT(B) AND NOT(C))}$$

- What single (3-input) logic gate has this same truth table?
- What property of logic operations does this equation illustrate?

3. (16 pts)

- How many output lines will a five-input decoder have?
- How many output lines will an  $n$ -input decoder have? ( $n$  can be any number)
- How many select lines will a 9-to-1 MUX have?
- How many select lines will an  $n$ -to-1 MUX have? ( $n$  can be any number)

4. (10 pts) Suppose we wanted to build a 4-input AND gate, but we only had 2-input AND gates available. Since AND is an associative logical operator,

$$Z = A \text{ AND } B \text{ AND } C \text{ AND } D$$

could be computed as

$$Z = ((A \text{ AND } B) \text{ AND } C) \text{ AND } D$$

as shown below in figure below:



It turns out that XOR is also an associative logical operator, and a 4-input XOR gate can be constructed using 2-input XOR gates in the same manner.



- Complete a truth table for the gate-level logic circuit shown in figure above.
- What do you notice about the input combinations that give an output value of 1?
- What do you notice about the input combinations that give an output value of 0?

5. (15 pts) We wish to implement two logic functions  $Y(a,b,c)$  and  $Z(a,b)$ .  $Y$  is 1 in exactly those cases where an odd number of  $a$ ,  $b$ , and  $c$  equal 1.  $Z$  is the exclusive-OR of  $a$  and  $b$ .

- Construct the truth tables for  $Y$  and  $Z$ .
- Implement the two logic functions  $Y$  and  $Z$  described above using ONLY the logic circuits provided below: a 3-to-8 decoder and two OR gates. That is, draw the wires from the outputs of the decoder to the inputs of the OR gates as necessary to do the job. You can assume you have as many inputs to each OR gate as you find necessary.

6. (10 pts) Write down the truth table for a 2:1 MUX with 3 inputs  $S$ ,  $A$  and  $B$  and one output  $X$ . Note that  $S$  is the select line of the MUX, if  $S = 0$  then  $X = A$  and if  $S = 1$  then  $X = B$ . Write the expression for  $X$  based on the truth table and reduce the expression using the Boolean algebra rules discussed in class.

7. (10 pts) You may recall the 4-bit Adder circuit which does addition or subtraction based on the select value  $S$  (0:Add;1:Subtract). Rework the circuit so that the generated output is:

- Addition:  $A+B$  if Select S:00
- Increment A:  $A+1$  if Select S:01
- Decrement A:  $A-1$  if Select S:10
- Subtract:  $A-B$  if Select S:11

8. (15 pts)

- a) Implement a 4-to-1 Mux using only 2-to-1 Muxes making sure to properly connect all of the terminals. Remember that you will have 4 inputs ( $A$ ,  $B$ ,  $C$ , and  $D$  in that order from left to right), 2 control signals ( $S_1$  and  $S_0$ ), and 1 output (OUT).

- b) Implement the following logic function using two 2-to-1 Muxes:

$$A \text{ XOR } B$$

Inverters are not allowed. You are allowed to feed a constant 0 or 1 into your Muxes.