

Von Neumann Model

Builder
Microarchitecture
(Chip)

LCS ISA

Design Blueprint

Microsoft

Samsung

Apple

ARM ISA

Phone

Iv

Gadgets

Arch

LC3

Intel
Laptop

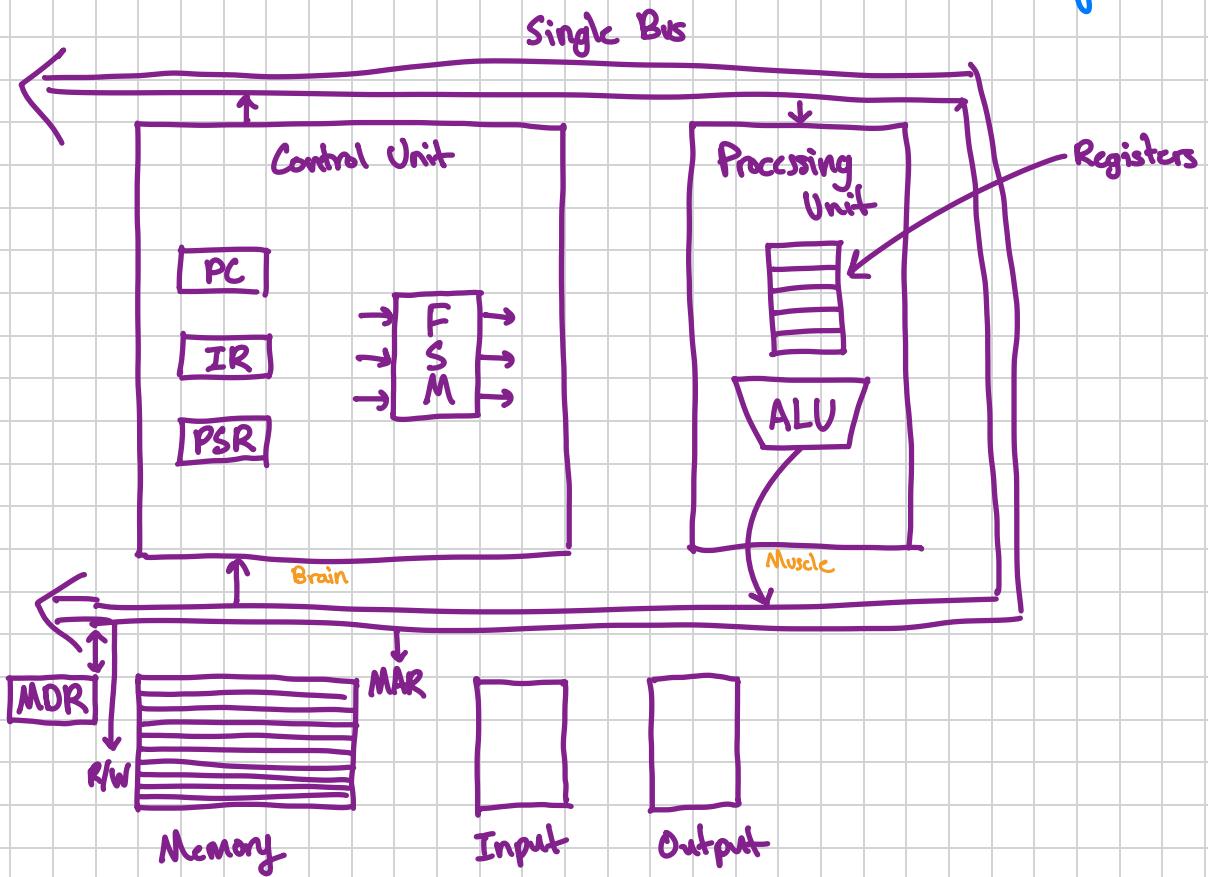
AMD
Laptop

x86 Intel

LC3 ISA

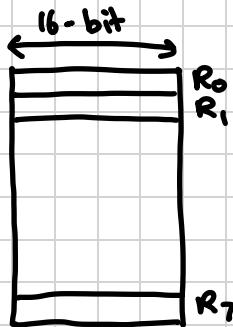
→ Arch

Von Neumann Model
Single Bus



LC3 ISA

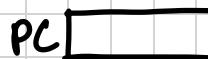
① Registers



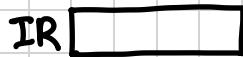
General Purpose Registers

Holds Data/Address

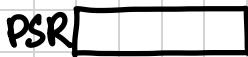
Special



Holds address of the NEXT instruction to execute

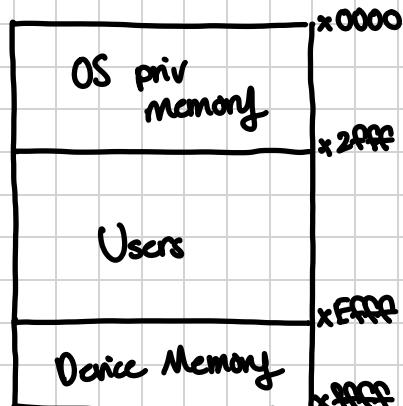
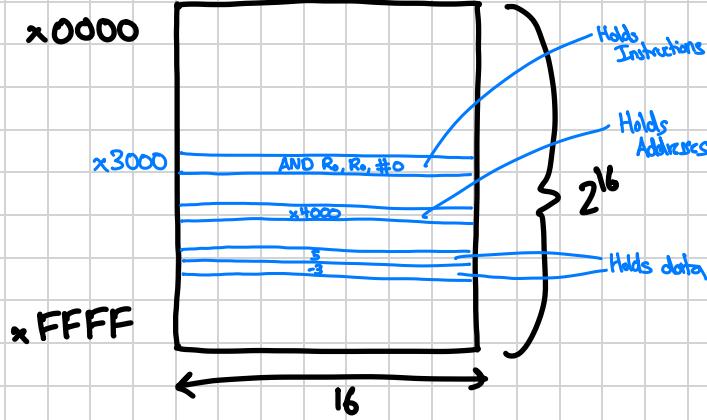


Holds the instruction currently being executed



Holds the status of the program

② Memory



③ Instruction Set

- Arithmetic Logic Instruction

ADD NOT AND

- Data movement (load/share)

LD ST
LDR STR
LDI STI



- Control Instructions

BR JMP JSR TRAP

RTI

