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UNIVERSITY OF TEXAS AT AUSTIN
ELECTRICAL ENGINEERING DEPARTMENT

EE 306, Introduction to Computing, Fall 2019
Exam 1
Oct, 2019

Directions There are 7 problems worth a total of 100 points. The number of points for each question is indicated. Make sure that you show all work since partial credit will be given. This exam is closed book, closed notes, and **no calculators are allowed**. You may not communicate in any way with anyone other than exam proctors during the exam time. Don't forget to put your name and UTEID on ALL pages. You may use the back of the sheets if you need extra space to do scratch work.

You have **75+5 mins** to finish the exam

Name: Sol

	Points possible	Score
Problem 1	20	
Problem 2	12	
Problem 3	12	
Problem 4	10	
Problem 5	10	
Problem 6	20	
Problem 7	16	
Total	100	

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1. (20 points) Answer the following

(a) (5 points) What decimal values does the binary sequence 10101010 represent as a unsigned number and a Signed number in 2's complement representation?

```
10101010 - Unsigned number : 2+8+16+64 = 90

10101010 - Signed number : 2+8+16-64 = -38
```

(b) (5 points) A signed number in 2's complement representation is expressed in hexadecimal as x1A. What decimal value does it represent?

```
x1A - 00011010 : Is a positive number

Value: 16+8+2 = 26
```

(c) (5 points) Given the 6-bit logic sequence 011001, you are to clear the least-significant bit and set the most-significant bit without changing any of the other bits. What two consecutive operations (with masks) will accomplish this? (show your work)

```
011001

To clear LSB:
 AND with mask 111110
     011001
AND
     111110
-----------
     011000
```

```
To clear the MSB:
  OR with mas 100000
        011001
OR
        100000
------------
        111001
```

(d) (5 points) Assuming unsigned addition, the result of adding the octal number $(324)_8$ and another unknown octal number $(X)_8$ is $(430)_8$. What is X?

$$(324)_8 + X_8 = (430)_8$$

```
   3 2 4
+
   X Y Z
========
   4 3 0
```

You can do this in octal or convert to binary and do it

```
4+Z=8 which is 10 in octal
=> Z must have been 4 and 1 carried
1(carry)+2+Y=3
=> Y must have been 0 and 0 carried
0(carry)+3+X=4
=> Z must be 1
X = XYZ = 104
```

2. (12 points) Given a 13-bit floating-point representation, with 7 bits for the fraction. Answer the following:

   (a) (6 points) What does 1100011001110 represent (you can leave the answer as a fraction or reduce it to decimal and fractional part)?

```
1 10001 1001110

   Fraction is 5 bits => Bias = 2^(5-1) - 1 =  15

   = (-1)* 1.100111 * 2^(17-15)
   = (-1)* 1.100111 * 2^2 = -110.0111
   = -(6 + 1/4+1/8+1/16) = -6 7/16
```

   (b) (6 points) Using the same format, what is the floating point representation for the real number 3 7/8?

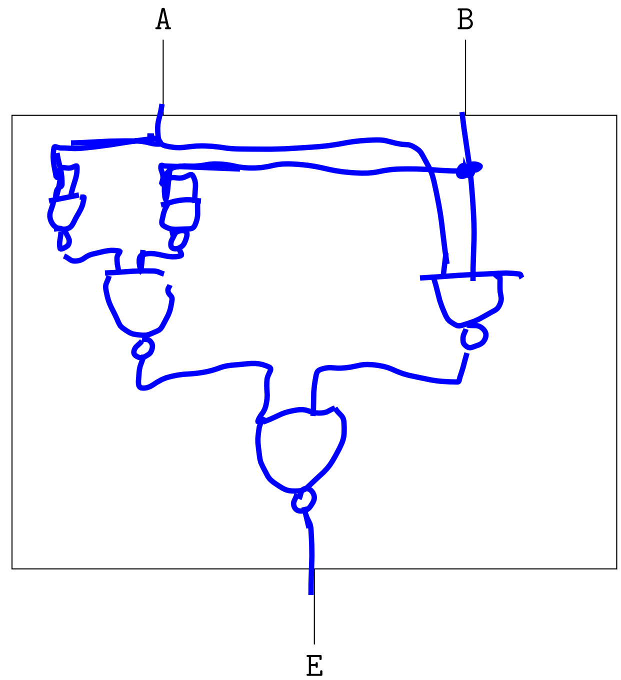
```
3 7/8

   = 11.111
   = 1.1111 * 2^1
   = 1.1111 * 2^(16-15)
FP Format:

     0 10000 1111000
```

3. (12 points) Answer the following circuit questions:

   (a) (8 points) Design a 1-bit equality logic circuit with input bits A and B, and output E. The output E indicates whether the bits are not equal (E = 0) or equal (E = 1. Give the logic circuit diagram for it using only NAND gates.

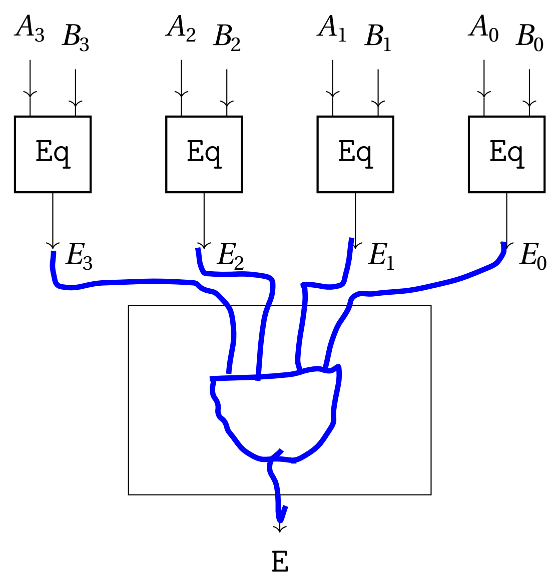


TT

A	B	E
0	0	1
0	1	0
1	0	0
1	1	1

$E = A'B' + AB$

   (b) (4 points) Now, design a 4-bit equality logic circuit using as many of the 1-bit equality (Eq) circuits (from above) as needed and, one additional logic gate of your choice. The output E is 1 only when both 4-bit numbers are equal, 0 otherwise.



4. (10 points) A series of read and write operations are performed on the memory. You have been given the initial state of the memory, the final state of the memory after all operations have been performed, and, a table with the read/write memory operations. However, some of the entries are missing.

   Fill in the missing entries.

Initial State			
Memory Address	Contents		
00	1	1	1
01	0	1	0
10	0	1	0
11	0	0	0

Final State			
Memory Address	Contents		
00	0	1	0
01	1	1	0
10	0	0	1
11	1	1	0

Read/Write Operations		
MAR	R/W	MDR
00	0	_ _ _
_ _	0	0 0 0
_ _	1	1 1 0
1 1	_	0 0 1
1 0	_	0 0 1
_	_	_ _ _
11	_	_ _ _

5. (10 points) Give a truth-table for a User(U) vs. Computer(C) game of *Rock-Paper Scissors.*
Rules:

   (a) Both the User and the Computer make one (and only one) of the three choices.

   (b) Rock beats Scissors; Scissors beats Paper; Paper beats Rock.

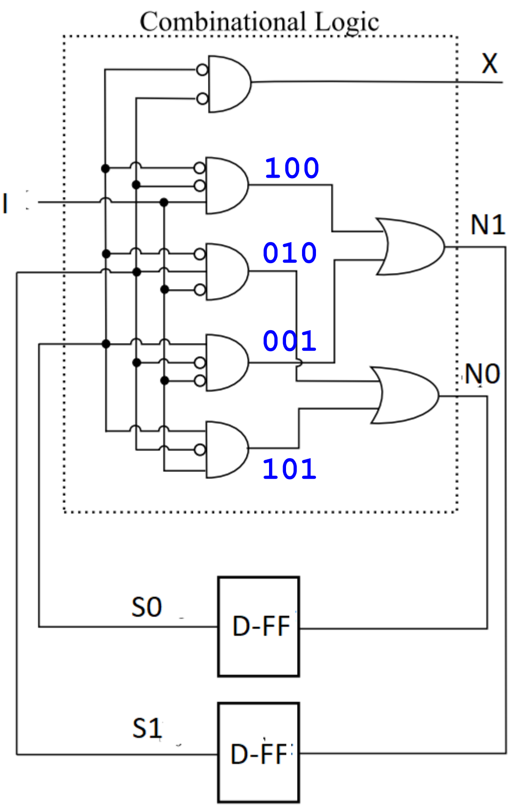
   (c) The outcome of the game is a win by either the User or the Computer, or a tie.

   (d) Invalid input combinations can be left out of the truth-table

   Clearly Identify (with labels) the inputs and outputs and give the truth table. Remember, only 0's and 1's are allowed in a truth-table.
   Notes:
   1. There are more lines provided in the table below than needed;
   2. Use simple labels like `UW` for *User Wins* and provide a legend for your labels on the right side

Inputs (Labels below)						Outputs (Labels below)		
UR	UP	US	CR	CP	CS	UW	CW	T
0	0	1	0	0	1	0	0	1
0	1	0	0	1	0	0	0	1
1	0	0	1	0	0	0	0	1
1	0	0	0	0	1	1	0	0
0	1	0	1	0	0	1	0	0
0	0	1	0	1	0	1	0	0
0	0	1	1	0	0	0	1	0
1	0	0	0	1	0	0	1	0
0	1	0	0	0	1	0	1	0

6. (20 points) Shown below is the logic circuit implementation of a Finite State Machine.



X = S0'.S1'

N1 = S0'.S1'.I + S0.S1'.I'

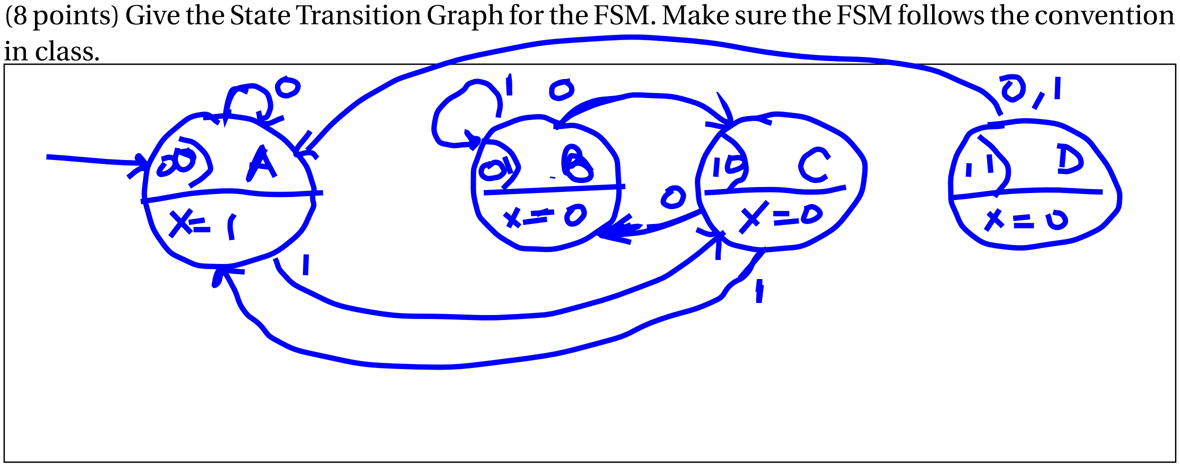
N0 = S0'.S1.I' + S0.S1'.I

(a) (12 points) Give the *State Transition* and *Output Determination* Truth Tables that this circuit is designed from?

I	S1	S0	N1	N0
0	0	0	0	0
0	0	1	1	0
0	1	0	0	1
0	1	1	0	0
1	0	0	1	0
1	0	1	0	1
1	1	0	0	0
1	1	1	0	0

S1	S0	X
0	0	1
0	1	0
1	0	0
1	1	0

(b) (8 points) Give the State Transition Graph for the FSM. Make sure the FSM follows the convention used in class.



7. (16 points) Answer the following:

(a) (4 points) Given a memory module with N-bit MAR and M-bit MDR. What is the total memory in bytes?

```
Total Memory in bits  = M x 2^N
             in bytes = (M x 2^N)/8
```

(b) (4 points) Fill in the blanks so the following boolean equations are valid:

i. `1 NOR X = _0__`

ii. `_0_ XOR X = X`

iii. `_X_ AND 1 = X`

iv. `X NAND _0_ = 1`

(c) (2 points) There are 200 students in a class. How many bits are needed, to assign each student a unique binary id?

```
200 students => ceiling(log2(200)) =  8
OR
200 falls between 128 (2^7) and 256 (2^8) => 8 bits needed
```

(d) (2 points) Which of these are logically complete gates?

i. OR gate
ii. NAND gate
iii. NOR gate
iv. AND gate
v. None of the above

(e) (1 points) The number of storage elements needed in a FSM implementation is dependent (not equal) solely on the number of states. [True/~~False~~]

(f) (1 points) If the exclusive-OR of A, B is a 0 then A and B must be equal. [True/~~False~~]

(g) (1 points) If a NAND gate output is a 1 then at least one of its inputs must be a 1. [~~True~~/False]

(h) (1 points) A NOT gate is made of one n-type and one p-type transistor. [True/~~False~~]