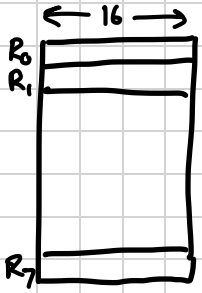
ISA

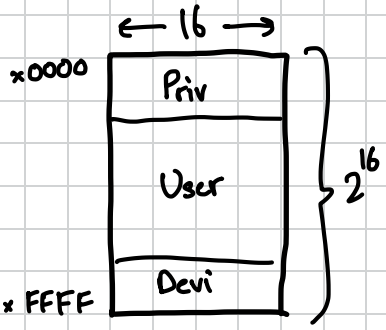
① Registers



Reg
100

Special PC, IR, PSR

② Memory



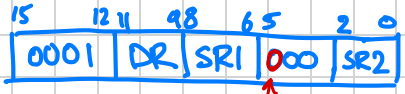
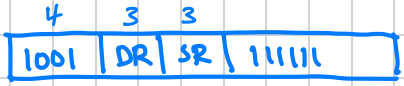
③ Instruction Set

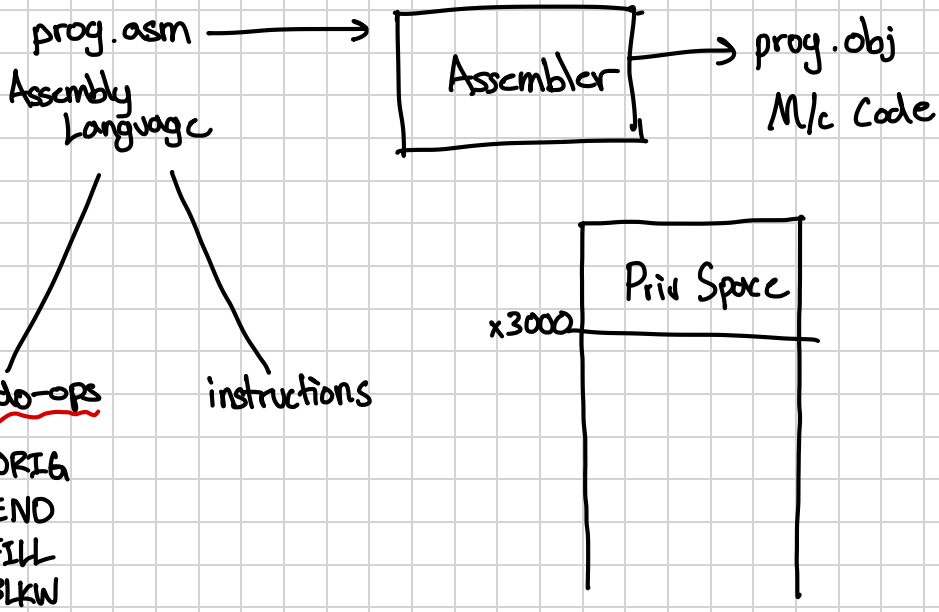
- Arithmetic Logic ADD NOT AND
- Data Movement LD, ST
- Control Operation BR, TRAP

④ Addressing Modes : How do operands form?

⑤ Data Types :

INSTRUCTIONS

	format syntax	meaning semantics	M/c code
ADD	DR, SR1, SR2	DR ← SR1 + SR2	
ADD	DR, SR1, #imm5 (signed 5-bit [-16,15])	DR ← SR1 + SEXT(imm5)	
AND	DR, SR1, SR2	DR ← SR1 AND SR2	
AND	DR, SR, #imm5	DR ← SR AND SEXT(imm5)	
NOT	DR, SR	DR ← NOT(SR)	



Address	Contents
x3000	LD, R0 ✓
	x3001 + F = x3010
x3010	X -5
x3011	Y 3
x3012	Z -8

```
; comment
    .ORIG x3000                 PC's
    LD  R0, xOF          1
    LD  R1, xOF          2
    NOT R1, R1           3
    ADD R1, R1, #1       4
    ADD R2, R0, R1       5
    ST  R2, xOC          6
    HALT  ------------------> TRAP x25
```

$$\begin{array}{r} 3012 \\ -\ 3006 \\ \hline 000C \end{array}$$

LD R0, x3010 (crossed out: "PC offset")

4	3	9
0010	000	