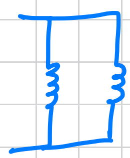
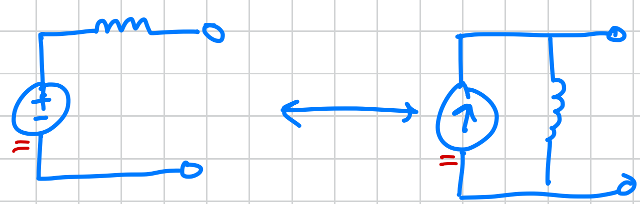
DUALITY

KVL $\Sigma v = 0$

KCL $\Sigma i = 0$

★ exchanging the roles of voltage and current

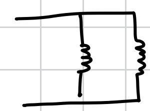




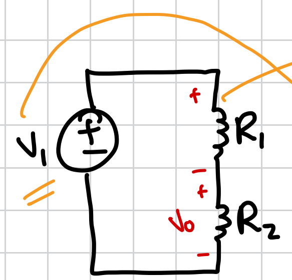
Duality

If two components share current by virtue of KCL ⇒ series.

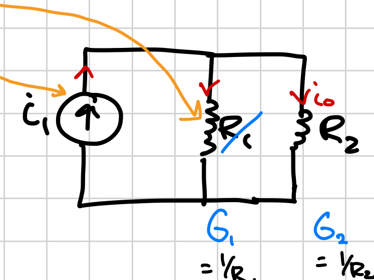
If two components share voltage by virtue of KVL ⇒ parallel



Voltage ⟷	Current
Across ⟷	Through
Short ⟷	Open
Parallel ⟷	Series
KVL → loops ⟷	KCL → nodes
Outer loop ⟷	Ground Node
Resistor ⟷	Conductance



⇒



A voltage divider has a voltage source in series with two resistors. The output is the voltage across the 2nd resistor.

A current divider has a current source in parallel with two resistors. The output is the current through the 2nd resistor.

$$\boxed{V_o = \frac{R_2}{R_1+R_2} V_1}$$

$$\boxed{i_o} = \frac{V}{R_2} = \left(\frac{R_1R_2}{R_1+R_2} i_1\right)\frac{1}{R_2} = \boxed{\frac{R_1}{R_1+R_2} i_1}$$

some error

R

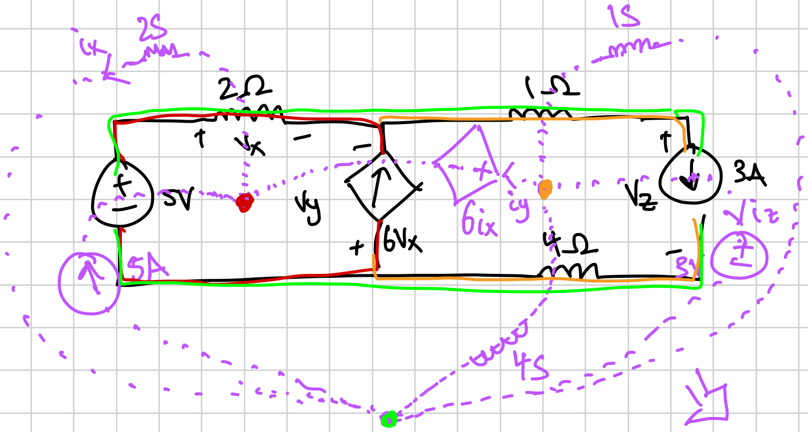
A resistor is a linear voltage-current relationship when $v = i \times \text{const}$ $[\text{const}] = \frac{\text{volts}}{\text{amps}}$ (ohms Ω)

A conductance is a linear current-voltage relationship when $i = v \times \text{const}$ $[\text{const}]$ $\frac{\text{amps}}{\text{volts}}$ (siemens S)

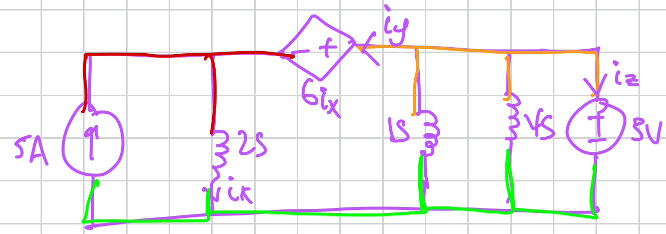
conductance

G

In one circuit, $R = \frac{1}{G}$



Draw node for each mesh
Draw node outside for outer loop



Label voltage across each component

If v counts as (+) when KVL clockwise, then the dual i is into dual node

If PSE in original, PSE applies