CA2015 Midterm

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1 Specification Document

This report details the functionality of a bike light. The light takes a button as an input and outputs a signal to an LED. The frequency of the output signal affects the brightness of the light. There are four output modes for the light: off, bright, dim and blink. When the button is pressed, the state of the bike light changes, in the order shown in Figure **??** on page ??.

In the bright state, the light will be powered by a signal with a frequency of 256HZ. Each individual pulse is 1 clock cycle long ($\frac{1}{32,768}$s) and this pulse repeats 256 times every second. The dim setting is done similarly, with the frequency being 128HZ.

In the Blinking State, the light flashes bright once for 0.125 seconds, then dim 3 times, each for 0.125 seconds. In between each flash the light is off for 0.125 seconds. This cycle repeats once a second.

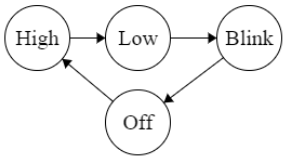

Figure 1: Diagram of Bike Light Modes

2 Block Diagram

The schematic for this system is broken up into many subunits, described in the next section. A high level block diagram of the system can be seen in Figure 2. The one piece not placed into a subunit is the LED signal processing at the end of the circuit. This creates one clock cycle wide pulses at the desired frequency and sends them to the LED.

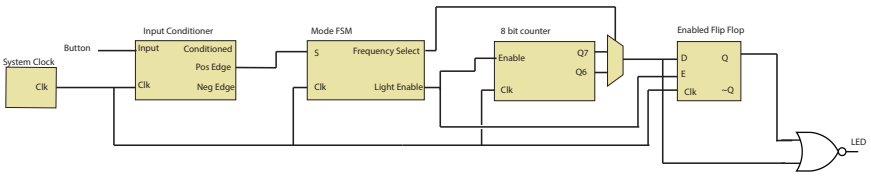

Figure 2: Block Diagram of Bike Light System

3 Schematic

3.1 Up Counter

The Up Counter is a binary counter which increments with every clock cycle for 2^N cycles, where N is the number of bits in the counter, after which it resets to 0. The counter takes Clk and enable as inputs and outputs $Q_0, Q_1, Q2...Q_N$, which encode the binary representation of the output with Q_0 being the least significant bit. The circuit for this unit can be seen in Figure 3 and the cost estimation can be seen in Table 1.

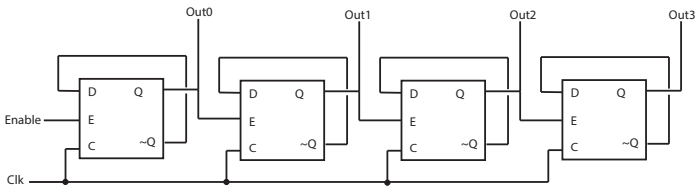

Figure 3: Schematic of an Up Counter

Gate	Cost Per Unit	Number Used	Total
Enabled Edge Triggered D Flip Flop	20	N	20N
			20N

Table 1: Cost Estimation of an Up Counter

3.2 Input Conditioner

The input conditioner changes the input signal from the button to remove noise and ensure the rest of the system is receiving a clear signal. It debounces the button signal and adds flags for the positive and negative edges of the input signal, which are each high for one clock cycle when they detect the appropriate edge. The input is the output of the button and the outputs are the conditioned signal, the positive edge flag and the negative edge flag. The wait time of the conditioner is the time it waits in order to debounce the signal. In this circuit, the wait time is 32 clock cycles, but this parameter can be changed by increasing the size of the up counter. The circuit schematic can be seen in Figure 4 on the following page.

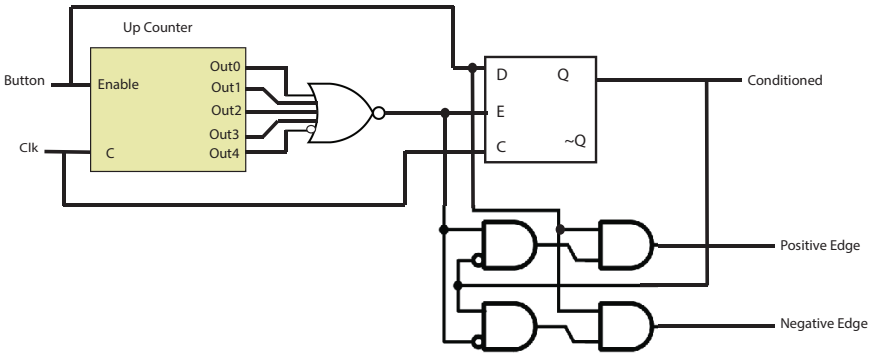

Figure 4: Schematic of an input conditioner

Gate	Cost Per Unit	Number Used	Total
5-Input `NOR`	5	1	5
`AND`	3	4	12
Inverter	1	2	2
5-Bit Up Counter	(5)20	1	100
			117

Table 2: Cost Estimation of an Input Conditioner

3.3 Modes FSM

This unit responds to the press of the input button and changes its state and the parameters accordingly. It cycles through four stages: off, bright, dim and blink. During blink, the light cycles through 8 states, shown in Figure **??** on page ??. Its inputs are a conditioned button signal and the clock signal and its outputs are frequency select and light enable. The circuit for the FSM can be seen in Figure 5 on the following page and the cost estimate can be seen in Table 3 on the next page. A diagram of the states can be seen in Figure ?? on page ??.

Gate	Cost Per Unit	Number Used	Total
2-Input `OR`	3	1	3
Enabled Edge Triggered D Flip Flop	20	2	40
4-Input MUX	19	2	38
12-Bit Up Counter	(12)20	1	240
			321

Table 3: Cost Estimation of an FSM

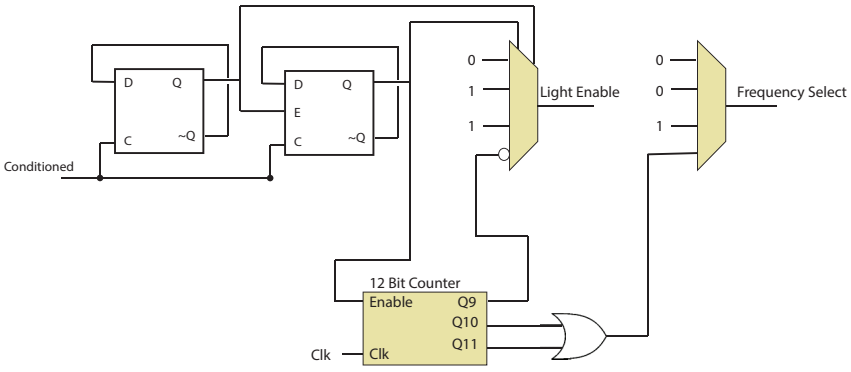

Figure 5: Schematic of an FSM

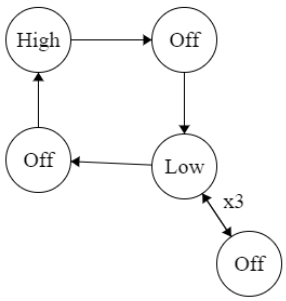

Figure 6: Diagram of States of Blink

4 Cost Estimation

Component	Cost
System Clock	2
Input Conditioner	117
FSM	321
8-Bit Up Counter	160
Enabled Flip Flop	20
2-Input MUX	7
2-Input `NOR`	2
	629

Table 4: Caption