Embedded Neural Recording With TinyOS-Based Wireless-Enabled Processor Modules

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***Abstract*—To create a wireless neural recording system that can benefit from the continuous advancements being made in embedded microcontroller and communications technologies, an embedded-system-based architecture for wireless neural recording has been designed, fabricated, and tested. The system consists of commercial-off-the-shelf wireless-enabled processor modules (motes) for communicating the neural signals, and a back-end database server and client application for archiving and browsing the neural signals. A neural-signal-acquisition application has been developed to enable the mote to either acquire neural signals at a rate of 4000 12-bit samples per second, or detect and transmit spike heights and widths sampled at a rate of 16670 12-bit samples per second on a single channel. The motes acquire neural signals via a custom low-noise neural-signal amplifier with adjustable gain and high-pass corner frequency that has been designed, and fabricated in a 1.5-μm CMOS process. In addition to browsing acquired neural data, the client application enables the user to remotely toggle modes of operation (real-time or spike-only), as well as amplifier gain and high-pass corner frequency.**

***Index Terms*—Biomedical electronics, embedded sensor, low-power circuit design, neural amplifier, unit detection.**

I. Introduction

NEUROSCIENTISTS typically acquire neural signals from implanted depth electrodes interfaced with a recording apparatus via a bundle of fine wires. However, in many cases it is preferable to acquire these signals when the test subjects are untethered, freely behaving, and even interacting. Existing wireless neural-recording systems range from fully integrated analog transmitters [1], [2], to analog transmitters with threshold-based spike detection [3]–[5] to digital application-specific integrated circuits (ASICs) [6], to microcontroller-based embedded systems [7], to commercial-off-the-shelf (COTS) PC-based systems [8]. Fully integrated transmitters and ASICs benefit from being very small (several mm^2) and low-power (several mWs), thus enabling them to be implanted with the electrode and inductively powered. However, fully integrated approaches provide limited user-configurability while requiring considerable re-engineering for incorporating minor design or algorithmic changes. Microcontroller-based embedded systems are larger (several cm^2), and consume more power (tens of mWs), to the point where their lifetime is limited when using small batteries. However, these systems require less engineering to develop and to provide users with a higher degree of signal-processing flexibility. COTS PC-based systems are large and heavy (greater than 0.1 kg), while providing nearly the level of signal processing and communications that is available to a PC-class device. In the interest of increasing channel count and sampling rate while maintaining reasonable battery life, some groups have demonstrated solutions with some on-board signal-processing capability, such as thresholding as demonstrated in [3] and [4]. Unfortunately, these threshold-based systems typically cannot differentiate spikes from artifacts, and require circuit redesign for modifying the detection algorithms. The limited adoption of existing wireless neural recording systems by the neuroscientific community may be an indicator that users could benefit from a greater degree of flexibility in terms of methods for spike detection. An attractive solution would leverage advances in an underlying, commercial architecture, in a manner similar to PCs, but without the upfront power penalty associated with the platform (as seen in [8]). Researchers have developed a wireless platform for small, low-power, and low-cost embedded sensors using COTS microcontrollers and transceivers. This effort led to the development of nesC [9], an extension to the C programming language designed to embody the structuring concepts and execution model of TinyOS [10]. TinyOS is an event-driven operating system designed for sensor-network nodes that have limited memory and computational resources (e.g., 8 kB of program memory, 512 B of RAM). TinyOS enables developers to access low-level hardware resources at the application level, thus resulting in a level of data-acquisition and communications flexibility that is unavailable to other existing mainstream wireless communications technologies. This inherent flexibility enables TinyOS developers to realize high-frequency real-time peer-to-peer communications systems (e.g., one node streaming neural signals captured at over 10 kHz to another node), as well as low-duty-cycle mesh networks.

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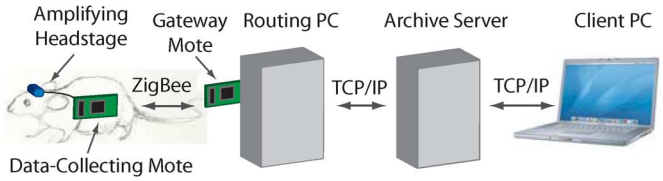

Fig. 1. Top-level system architecture.

TinyOS is available open-source and wireless-enabled processor modules (motes) that operate with it are commercially available.

II. System Architecture

Our modular neural-recording system can benefit from advances in embedded microcontroller technologies and enable the user to implement custom filtering algorithms without re-implementing the entire application. Hardware and software has been designed to enable motes to acquire, process (in a programmable and modular fashion), and transmit neural signals. Specifically, we have developed 1) a neural-signal amplifier chip that can be interfaced directly to a microcontroller ADC for the selective acquisition of spikes and field potentials, 2) an application based upon a dynamically tunable signal-acquisition, filtering, and transmission framework [11] for spike detection, and 3) a back-end system architecture for receiving, archiving, hosting, and browsing the neural signals (Fig. 1).

A. Hardware

The type of mote used in this work is the TelosB mote produced by Crossbow Technology Inc. (San Jose, CA) and Moteiv (El Cerrito, CA). Data is processed by a microprocessor (MSP430, Texas Instruments, Dallas, TX). The TI MSP430 has 8 analog input channels that are time-multiplexed onto a single analog-to-digital converter (ADC). Data transmission is handled by a ZigBee-compliant (IEEE 802.15.4) 2.4-GHz transceiver (CC2420, Chipcon, Oslo, Norway). An antenna embedded on the printed-circuit board is used for wireless communication.

The mote is interfaced with neural tissue via a custom monolithic low-noise neural-signal amplifier with adjustable gain and bandwidth [12]. The novel amplifier is capable of many things. Specifically, it can 1) reject the dc offset that occurs at the tissue-electrode interface, 2) amplify the neural-signal potential from the order of μVs to volts for acquiring the signal with the best possible fidelity given the 12-bit resolution provided by the microcontroller ADC, 3) dc-reference the neural signal (which oscillates above and below the animal ground) to half the battery supply voltage, to operate from the single supply used by the mote to avoid requiring additional batteries that add mass and volume to the system, 4) provide the current necessary to drive an off-chip load (i.e., the microcontroller ADC), 5) provide adjustable high-pass-filtering and gain so that LFP or spikes can be acquired selectively, 6) have low input-referred noise to acquire the neural signals with satisfactory signal-to-noise ratio, and 7) be monolithic to enable its integration with a recording headstage, as well as the opportunity to integrate it onto the same silicon as that of a future-generation single-chip mote.

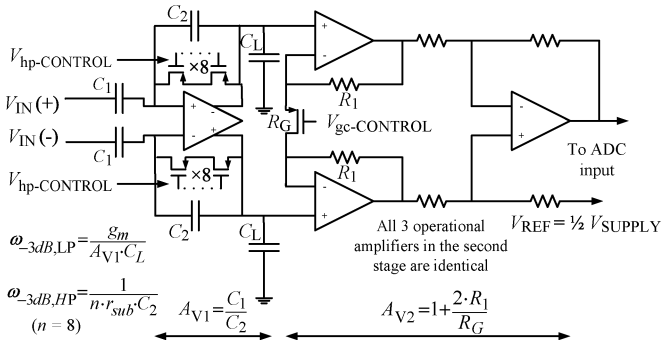

Fig. 2. Top-level schematic of the neural-signal-amplifier circuit.

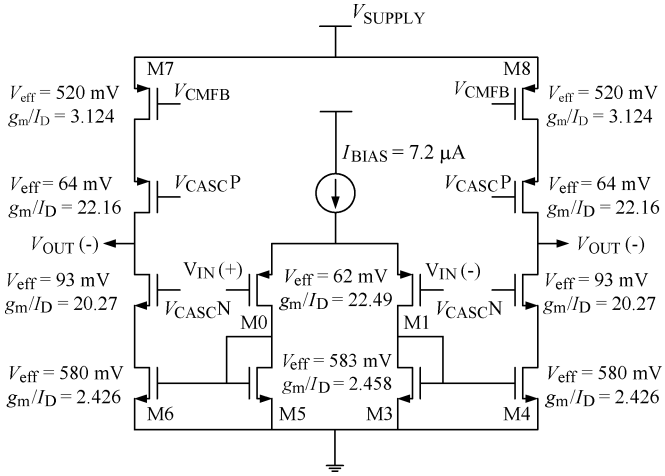

Fig. 3. First-stage OTA with bias voltages and currents.

A major challenge in realizing a single-chip amplifier that meets the above criteria is realizing the large passive elements necessary to achieve a high-pass filter in the near-dc range (to avoid filtering the slow-moving LFP) on silicon [13]. One approach is to use a metal–oxide–semiconductor (MOS) transistor biased in subthreshold (referred to as a subthreshold MOS resistor from here on), to achieve a very large resistance, although other groups have explored alternative techniques [14]. However, this approach limits the achievable gain in a single stage due to the small voltage drop the subthreshold MOS resistor can sustain before its resistance drops. High-pass corner-frequency adjustability is realized by modifying the gate voltage of the subthreshold-MOS resistors. To achieve high gain, the current necessary to drive an off-chip microcontroller, as well as dc referencing (to set the dc signal level to the middle of the ADC input range), a low-power instrumentation amplifier has been designed, with the addition of gain adjustability via a triode MOS transistor.

A top-level schematic of the neural-signal amplifier circuit is depicted in Fig. 2. The first stage is a high-pass adjustable, low-noise operational transconductance amplifier (OTA), shown in Fig. 3; which is a fully differential version of the amplifier introduced in [15] that operates on a single 3-V supply, rather than dual, 2.5-V supplies. The high-pass corner frequency of this stage is

$$f_{(-3\text{ dB,hp})} = \frac{1}{8 \cdot r_{\text{ds}} \cdot C_2} \tag{1}$$

where r_{ds} is the resistance of the subthreshold MOS resistors. The resistance of a subthreshold MOS resistor is governed by

$$R = \left(\frac{W}{L} \cdot \mu \cdot C \cdot \frac{V_{\mathrm{T}}}{n} \cdot e^{\left(\frac{V_{\mathrm{GS}}}{n \cdot V_{\mathrm{T}}} + \frac{\phi_0}{V_{\mathrm{T}}} \right)} \cdot e^{-\left(\frac{V_{\mathrm{DS}}}{n \cdot V_{\mathrm{T}}} \right)} \right)^{-1} \quad (2)$$

where W, L, μ, n, and C are the device width, length, carrier mobility, subthreshold-slope factor, and gate capacitance, respectively [16]. In addition, V_{T} is the thermal voltage, V_{GS} is the gate-source voltage (controllable by the 12-bit mote DAC), V_{DS} is the drain-source voltage, and ϕ_0 is the carrier Fermi energy [17]. Although the resistance can vary exponentially with a linear change in the applied gate voltage, since the purpose of the filtering action is to isolate spikes from LFPs, it is only necessary for the resistor to be set at a value to yield a high-pass corner frequency on the order of 100 Hz, rather than a precise resistor value. The gain of this stage is limited to 100 by the ratio of the input and feedback capacitors (C_1 and C_2, respectively), since the subthreshold MOS resistors can only sustain a small voltage (e.g., on the order of tens of milivolts) before their resistance drops exponentially. The input-referred thermal noise power of this OTA can be described by

$$\overline{v_{\mathrm{ni,thermal}}^2} = \frac{16 \cdot \mathrm{k} \cdot T}{3 \cdot g_{\mathrm{m1}}} \cdot \left(1 + 2 \cdot \frac{g_{\mathrm{m3}}}{g_{\mathrm{m1}}} + \frac{g_{\mathrm{m7}}}{g_{\mathrm{m1}}} \right) \cdot \Delta f$$

where g_{m3} and g_{m7} are the transconductances of the PMOS and NMOS current-mirror devices, respectively, g_{m1} is the transconductance of the input devices, k is Boltzmann's constant, T is temperature, and f is frequency. The input-referred noise power of the OTA is proportional to the ratio of the transconductance of the current-mirror devices (M3, M4, M5, and M6) to the transconductance of the input devices (M0 and M1). Low noise is achieved by biasing the input devices in the subthreshold region of operation (where they exhibit a high transconductance-to-drain-current ratio), and all other devices in strong inversion (where they exhibit a low transconductance-to-drain-current ratio). The input devices are biased in subthreshold by sizing them with a large gate area (approx 6400 $\mu\mathrm{m}^2$) and sinking a small drain current (approximately 8 μA) through them. The current-mirror devices are biased in strong inversion by sizing them with small W/L ratios. The cascade devices are biased with a Sooch bias circuit [18]. The dc level of the output nodes is set by a continuous-time common-mode feedback circuit [19], which senses the voltage of the output nodes and modifies the gate voltage of the p-channel current-source devices (M7 and M8) to maintain a dc voltage of 1.5 V (half the 3-V supply voltage) at the output.

The second stage is a gain-adjustable instrumentation amplifier circuit, composed of three identical compensated two-stage OTAs. The gain of this stage is

$$A_{\mathrm{V2}} = 1 + \frac{2 \cdot R_1}{R_{\mathrm{G}}} \quad (3)$$

where R_{G} is the resistance of a voltage-controlled triode MOS resistor, which is also controlled by the 12-bit mote DAC. This stage also provides differential-to-single-ended conversion, with dc referencing to half the supply voltage. Individual transistor sizes, as well as other more detailed information on this circuit can be found in [20]. Two circuit boards have been designed for mounting the recording system to the test subject. One circuit board, carrying the neural-signal amplifier chip, is mounted to the headstage carrying the electrodes. A second circuit board carries a coin-cell battery and voltage buffer for creating the reference voltage (half the battery supply), which is provided to the headstage-mounted neural-signal-amplifier chip and is also used to bias the test subject. Leads from the headstage connect the output of the neural-signal amplifier circuit to the ADC input of the mote, as well as the mote DAC0 and DAC1 outputs to the high-pass-filtering control, and gain-control nodes of the neural-signal amplifier chip, respectively.

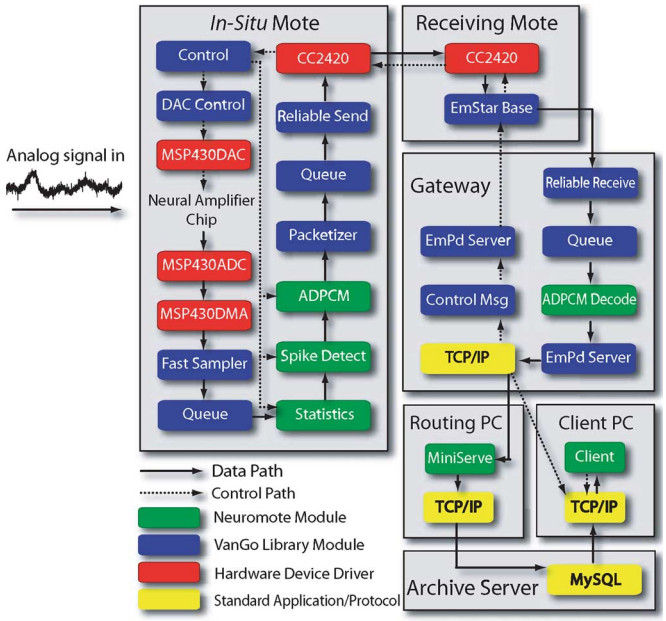

Fig. 4. Data and control flow through the Neuromote application.

B. Software

To create a system that can be easily reconfigured to the needs of the investigator, a dynamically-tunable, high-rate data acquisition, filtering, and transmission framework called VanGo [11] was used as a basis for the application. VanGo is a fast (i.e., 10s of kHz) and low-jitter data-acquisition system for resource-constrained motes, which provides an interface to activate and control mote-side and gateway-side processing of signals. VanGo is used to realize high-throughput applications with dynamically configurable filter chains, which are a series of software modules for filtering data (i.e., extracting useful information from raw analog signals). The VanGo software stack can be viewed as a filter chain that spans across a mote and a gateway device (Fig. 4). The gateway device consists of a PC-class device running Emstar [21] interfaced with a TelosB mote via USB. On the mote side, a driver has been written to acquire data from the direct memory access (DMA) controller packaged with the MSP430 microcontroller (Texas Instruments, Dallas, TX). Using the DMA allows data to be sampled without having to interrupt the processor for each sampled data point, which was a major factor that limited the performance of the MICA2-based

system described in [22]. In contrast, the DMA generates an interrupt each time a RAM buffer is filled with data.

Neuromote, a VanGo-based neural-signal acquisition, filtering, compression, and communication application has been designed (see [11] for a complete description of its design and operation). Neuromote can be configured to 1) acquire and transmit a single channel of neural signals in real time at a rate of 4000 12-bit samples per second or 2) send summary spike information (i.e., spike time of occurrence, peak-to-trough time and peak-to-trough height) with data acquired at 16670 12-bit samples per second. Eliminating the processor overhead required to packetize and transmit neural signals in real time enables the mote to sample data at the higher speed achieved in the summary mode of operation.

In the real-time mode of operation, the neural signals are acquired via the DMA and stored in a sample set consisting of 168 12-bit samples. In the spike-acquisition mode of operation, an adaptive absolute threshold is used to identify the occurrence of spikes. The rationale behind this choice of spike-acquisition algorithm is that its computational requirements allow it to be implemented on this hardware-constrained platform, and it has been identified as a very efficient method to acquire spikes in comparison to other known spike-detection algorithms when taking required memory, computations, missed-spike frequency, and false-positives frequency into account [23]. When a spike is detected, peak-trough height and peak-trough width are recorded in a new sample set and marked for transmission over the radio, while the original sample set is marked for deletion. Specifically, the user must define two thresholds (i.e., peak height and trough depth) as multiples of root-mean-square of the background noise level. Spike data is processed in the form of 1024-point sample sets. When the absolute value of the signal crosses the peak threshold, the algorithm pauses the mean and standard-deviation calculation, waits for a zero crossing followed by a trough-threshold crossing within a user-specified amount of time (typically 500 μs). If a trough crossing is detected subsequent to a zero crossing, the time of the peak-threshold crossing, the peak-to-trough time, and peak-to-trough height are recorded in a buffer. If a zero-crossing followed by a trough crossing is not detected within the user-defined period of time, the crossing is regarded as noise and discarded. Signal mean and standard deviation is subsequently resumed until the algorithm comes across another peak-threshold crossing. When 10 spikes are detected (a user-adjustable value), a packet is generated and transmitted over the radio to the gateway device.

III. Bench Testing

Hardware and software sub-systems were initially tested on a bench to assess their specific performance parameters.

A. Neural-Signal Amplifier Chip

The integrated circuit was fabricated in a dual-metal, dual-poly 1.5-μm CMOS process (Fig. 5). Bench testing was performed with a fully-differential signal source created by applying a sinusoid from a signal generator (Agilent 33120A, Palo Alto, CA) to the input of a discrete unity-gain inverting amplifier circuit. The output of the signal generator was connected

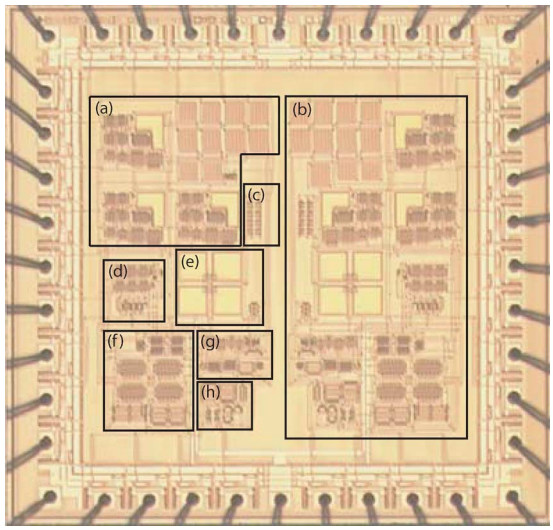

Fig. 5. Die micrograph of the $2.2 \times 2.2\ \mathrm{mm}^2$ neural-signal-amplifier chip. (a) Gain-adjustable instrumentation-amplifier circuit. (b) Replica of the complete amplifier with fixed gain and high-pass corner frequency. (c) Outlines the MOS subthreshold resistors. (d) Wide-swing constant-g_m bias circuit for biasing the current-source loads. Section (e) outlines the input capacitors. (f) High-pass adjustable, fully-differential, low-noise input stage. (g) Sooch bias circuit for biasing the cascode loads of the first amplifier stage. (h) Outlines the common-mode-feedback circuit.

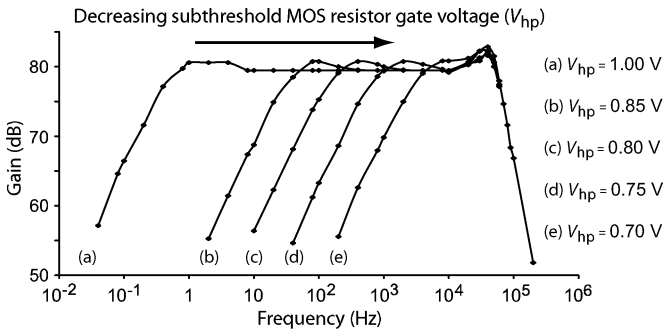

Fig. 6. Bode plots of the amplifier circuit with varying high-pass-filtering control voltages (V_hp).

to the non-inverting input of the neural-signal amplifier via a 10000:1 voltage-divider circuit (100 kΩ and 10 Ω). The output of the inverting amplifier was connected to the inverting input of the neural-signal amplifier via a similar voltage-divider circuit. The reference voltage of the circuit was tied to half the supply voltage.

The ac-magnitude response of the amplifier for several high-pass-filtering control settings at the maximum gain setting of 80 dB ($V_\mathrm{gc} = 251\ \mathrm{mV}$) have been plotted in Fig. 6. Fig. 6 reveals that there is an exponential increase in high-pass-corner frequency for a linear drop in V_hp

$$r_\mathrm{ds} = k \cdot e^{29.272 \cdot V_\mathrm{hp}}. \tag{4}$$

By comparing (2) with (4), a subthreshold slope factor of 0.761 can be derived, which verifies that the devices are in the subthreshold region throughout the high-pass control range.

Amplifier gain was measured as a function of gain-control voltage (V_gc), which was applied at the gate of the triode MOSFET resistor in the instrumentation amplifier circuit.

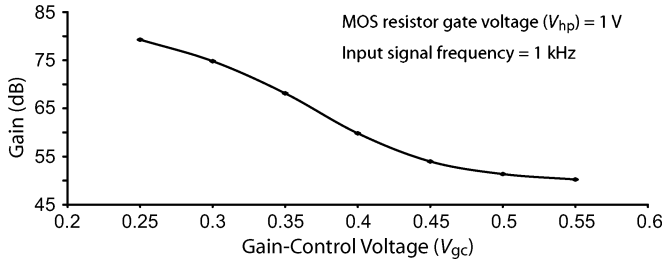

Fig. 7. Amplifier gain as a function of gain-control voltage ($V_{\rm gc}$). A 1-kHz, 100-μV peak-to-peak sinusoid was applied at the input of the amplifier with $V_{\rm hp}$ set at 1 V for a high-pass corner frequency near 0.5 Hz.

TABLE I
COMPARISON OF THE NEURAL-SIGNAL AMPLIFIER CIRCUIT WITH SEVERAL RECENTLY-REPORTED CIRCUITS

Reference	This Work	[3]	[5]	[13]	[16]	[24]
Supply Voltage [V]	3 V	± 1.5	5	0.8 - 1.5	± 1.65	2.8
Current/Channel [μA]	100	22.6	12.8	0.33	75	2.7
High Cutoff [Hz]	0.5 - 1.0	near DC	300	0.003	0.026	45
Low Cutoff [kHz]	10	9.9	5	0.245	10	5.32
CMRR [dB]	80	-	-	61 - 64	-	66
PSRR [dB]	61	50.5	-	62 - 63	-	75
Amplification [dB]	80	38.9	60	40.2	34	41
Noise [μV_{rms}]	3.12	9.2	5.1	2.7	3	3.06
NEF [-]	13.8	-	4	3.8	-	2.67

Amplifier gain as a function of $V_{\rm gc}$ has been depicted in Fig. 7. Common-mode rejection is beyond 80 dB, and power-supply rejection is measured at 61 dB. The input-referred offset (primarily due to the second stage) is approximately 18 μV. Total harmonic distortion is less than 1%. Amplifier noise was measured with a spectrum analyzer (Agilent 35670A, Palo Alto, CA), with the amplifier high-pass corner frequency set to 0.5 Hz and gain set to 80 dB. Noise power was measured with the inputs of the spectrum analyzer floating (to measure the instrument noise), and with the input to the spectrum analyzer attached to the amplifier chip, from which the amplifier noise referred to the input was calculated. The inputs of the amplifier chip were shorted together for this test. To improve resolution at lower frequencies, one FFT (10 000 points averaged over 100 measurements) was taken from 250 mHz to 400 Hz, and another was taken from 400 Hz to 51.2 kHz for each test configuration. Integrating the input-referred noise of the amplifier from 0.5 Hz to 50 kHz yields an integrated input-referred noise power of 3.12 $\mu V_{\rm rms}$. To compare the input-referred thermal noise against that of several recently-reported low-noise neural-signal amplifier circuits, we use the following noise-efficiency-factor (NEF) figure of merit introduced in [23]

$$\mathrm{NEF} = V_{\rm ni,rms}\sqrt{\frac{2\cdot I_{\rm total}}{4\cdot\pi\cdot V_{\rm T}\cdot k\cdot T\cdot BW}} \tag{5}$$

where $I_{\rm total}$ is the total current consumed by the amplifier circuit, $V_{\rm T}$ is the thermal voltage, k is Boltzmann's constant, T is absolute temperature, and BW is the amplifier bandwidth. Given that a single bipolar-junction transistor will have an NEF of 1, the NEF of any practical amplifier circuit will be more than 1. The NEF of this amplifier is measured at 13.8.

A performance summary of this amplifier relative to several other recently-reported neural-signal amplifier circuits [24], is outlined in Table I.

B. Neuromote Application

The data throughput capability of the TelosB's Chipcon CC2420 radio (Oslo, Norway) limits real-time data transmission to 4000 12-bit samples per second after ADPCM compression. Likewise, the mote on the receiving end can only receive real-time neural signals (at a rate of 4000 12-bit ADPCM-compressed bits per second), also due to bandwidth limitation. This limits the receiver to communicating with only a single mote operating in real-time signal-acquisition mode. However, operating the motes in spike-detection mode enables data to be acquired at 16700 12-bit samples per second, and several motes to communicate simultaneously with a single gateway module. The percentage of received packets as a function of spike firing rate (which affects data throughput) for one to four motes communicating with a single gateway module has been measured. It has been observed that packet loss begins to occur at spike rates over 20 spikes/s/mote with 4 or more motes communicating with a single gateway device (a more in-depth analysis can be found in [20]). The number of spikes that can be detected per second is limited to 50. Exceeding this rate of spike acquisition results in the sensors attempting to resend data that was not successfully sent previously due to network congestion (when there are more than two motes communicating with a single gateway device) while acquiring data from the ADCs, which eventually fills up the mote memory and causes the mote to cease sampling data. The measured power consumption with a single 3-V 160-mAh photo cell (CR-1/3N, Energizer, St. Louis, MO) for real-time and spike-detection was measured. In the real-time mode of operation, the mote consumes 48.46 mW of power. In the spike detection mode of operation, the mote consumes 4.62, 3.87, 3.16, 2.13, and 1.25 mW when detecting spikes at a rate of 50, 40, 30, 20, and 10 spikes per second, respectively.

IV. BIOLOGICAL TESTING

To validate the spike-acquisition and filtering capabilities of Neuromote, the multiunit activity acquired by the neural-signal amplifier was saved and applied to the mote in an EmStar mote-simulation environment [21].

The positive and negative thresholds were set to $+6$ and -2 standard deviations from the calculated baseline noise, respectively. The measured parameters of the detected spikes indicate the presence of three general classes of spikes in the 1-s dataset (more information on these results can be found in [20]). The performance was tested against a popular threshold-based spike-detection algorithm; Powernap [25], by setting the threshold to the same level. The detected spikes were then analyzed by the PowerNAP Pricipal Component tool for classification. Among five cluster-group choices, three spike clusters provided the most pronounced clusters.

The neural-recording system was initially tested by obtaining neural signals from a 350-μm-thick coronal hippocampal slice preparation from an adult C57/B16 mouse. The brain slice was induced to exhibit neural-spike activity through the application of 8 mM KCl. The sample bath was biased at half the 3-V

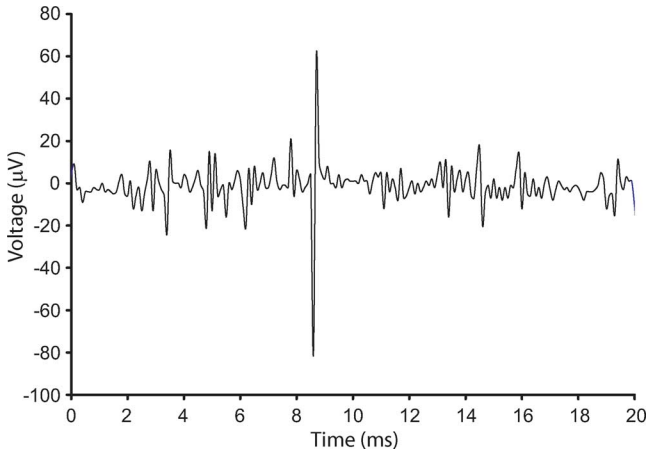

Fig. 8. Action potentials acquired from a 350-μm-thick coronal slice preparation (adult C57/B16 mouse) with 8 mmol KCl applied to depolarize the slice and evoke action potentials.

Fig. 9. Custom Java-based neural-signal browser application depicting neural signals acquired by the system *in vivo*. The user can select a portion of the waveform from the bottom panel to be displayed with adjustable resolution in the top panel. The top slider adjusts the zoom level, while the bottom slider scrolls through the dataset. The user can save zoom states, which are listed in the left-hand panel, as well as step back and fourth through zoom states.

supply and was used as the reference voltage. The neural signals were acquired differentially by a bipolar stainless steel differential electrode (PlasticsOne, Roanoke, VA), with the gain of the neural-signal amplifier set to 80 dB, and its high-pass corner frequency set to 1 kHz. Since the sampling rate of our signal-acquisition equipment was limited to 20 kHz, the output of the amplifier was applied to an eight-pole low-pass Butterworth filter with its corner frequency set at 10 kHz. A considerable amount of 60-Hz noise was coupled into the system due to the need for long wires to attach the electrodes to the prototype neural-signal amplifier chip. However, setting the high-pass corner frequency to 1 kHz lowered the 60-Hz interference to an acceptable level. A recorded spike is depicted in Fig. 8.

The system was also tested in-vivo on a living mouse. An adult C57/B16 mouse was anesthetized with 100 mg/kg ketamine, 5.2 mg kg-1 xylazine, and 1.0 mg kg-1 acepromazine according to a protocol approved by the UCLA Chancellor's Animal Research Committee. A hippocampal depth electrode (Plastics One, Roanoke, VA) was placed 2.2 mm posterior to the bregma and 1.7 mm lateral to the midline at a depth of 2.9 mm. The electrode was fixed to the skull using dental cement and the mouse was allowed to recover for 48 h. Recordings were started 10 min before an intraperitoneal injection of 15 mg kg-1 kainic acid. The amplifier chip was packaged in a 16-pin SOIC package and mounted upon a 2.5×1.2 cm^2 circuit board and mounted directly upon an implanted depth electrode (PlasticsOne, Roanoke, VA). The amplifier board was connected via copper wires to the 23-g TelosB mote running the Neuromote application, was powered by two AA batteries and placed near the anesthetized mouse. The neural signals were obtained differentially, with the animal tied to the reference voltage (half the 3-V supply) via a clip on its back. Field potentials were acquired with the amplifier gain set to 60 dB and the high-pass corner frequency set to 500 Hz. A screen shot of the Java application depicting the acquired neural signals stored on the archive server is depicted in Fig. 9.

V. Conclusion

In conclusion, an embedded neural recording system has been designed and tested. The animal-mounted sensor is a COTS wireless-enabled processor module that has been interfaced with neural tissue via a custom neural-signal amplifier chip. The custom neural-signal amplifier chip provides an adjustable gain between 50 and 80 dB, and an adjustable high-pass corner frequency from 500 mHz to 1 kHz, while consuming 0.1 mA of current per channel from a single 3-V supply to drive the off-chip ADC. The sensor operates on a modular signal-acquisition, filtering, and communication framework upon which an application for real-time neural-signal compression and absolute-threshold-based spike-detection application has been developed. Furthermore, a gateway device, archive server, and client application has been designed to acquire the analog signals and control the sensor mode of operation (i.e., real-time or spike detection), and tune amplifier parameters (i.e., gain and high-pass corner frequency).

The system is capable of transmitting a single channel of real-time spike signals at a rate of 4000 12-bit samples/s, or a single channel of spike information (peak-trough height, peak-trough depth, and time of occurrence) sampled at 16.7 kHz. A single sensor can communicate with a single gateway device in real-time, but three sensors can communicate with a single gateway device while communicating up to 40 spikes/s/mote in spike-detection mode. Power consumption ranges from 48.46 mW in the real-time mode of operation, and 1.25 mW to 4.62 mW in spike detection mode with spike detection rates ranging from 10 spikes/s to 50 spikes/s. The increased power consumption for increased detection rates results from transmitting the data assocated with the spike heights, widths, and times of occurence. A quick comparison reveals the higher power dissipation and noise associated with the amplifier introduced in this paper, since it has been designed to drive on off-chip ADC, and has hence been over-specified to be used on other/future generations of embedded sensors.

Although a major limitation of this system is its limited channel count, the biological interface circuit (if redesigned for driving a known on-chip load rather than an uncertain off-chip load), the Neuromote application, and the Vango framework, can scale up to hundreds of channels. Scaling up the system requires a TinyOS-based wireless-enabled processor module with the computational and communications ability to acquire, process, and transmit multiple channels of data. It has been predicted that motes will follow Moore's law from the perspective of performance, size, and power efficiency [26], which would inevitably lead to a chip-scale mote that could handle many channels. However, the market made cost and performance the priority, which has delayed the availability of advanced, chip-scale, high-performance motes that could yield systems, when augmented with the software and hardware described in this paper, with a performance comparable to the custom-integrated alternatives.

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