

A large, abstract graphic on the left side of the image consists of numerous thin, yellowish-gold lines that curve and overlap, creating a sense of depth and motion. These lines form a shape that tapers towards the bottom right.

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Chiplet Design Exchange

Jawad Nasrullah, zGlue Inc
Alex Wright, Ayar Labs

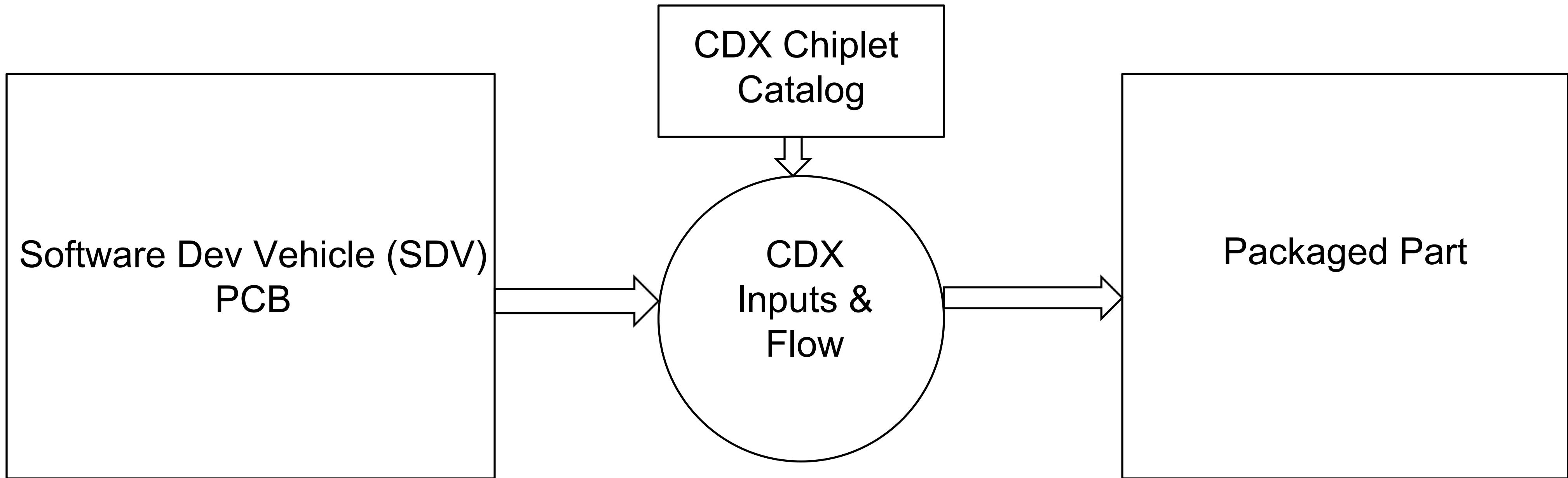


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CDX Subgroup Charter

- 1- Chiplet Machine Readable Description Standard Generation
- 2- Chiplet Catalog
- 3- Pchiplet-based SDV to Chiplet-based package conversion flow



Outline

Background: The Case for Chiplet Design Exchange (CDX)

Survey Results

Proposed CDX Spec/Whitepaper Overview

ZEF Extension

How to Participate.

Call to Action

Background

Chiplet Selection

Designer need a number of design collaterals to make a choice of components for a given application and to complete a design. These include at minimum;

- Product Briefs
- Data Sheets
- PCB/Substrate Design Resources

With complicated chips, traditional PCB type design flows are limiting and will not easily scale. Also there are too many ways to describe chiplets.

Chiplet Design Data Exchange

There is no one standard way to express basic information: A standard format should be simple and usable across different tools

- Design Entry tools
- Layout tools
- Simulators (PI/SI, Thermal, Behavioral)
- Test

BUT There is a question of what info people are willing to share. Hence we did a survey.

Survey Question Overview

1. I can share what my chiplet's function is (i.e. a high-level description of what the chip does):
2. I can share the number and value of voltage rails:
3. I can share pin-by-pin functional information (i.e. EC table / AbsMax):
4. I can share the size (X and Y dimensions) of my chiplet:
5. I can share bump physicals (pitch, location, thickness, and tolerances) of my chiplet:
6. I can share height (Z dimension) of my chiplet:
7. I can share a heat map of my chiplet:
8. I can share what mechanisms I provide to test for chip functionality prior to assembly:
9. I can share what mechanisms I provide to test for chip functionality post assembly:
10. I can share my business model (wafer with known good die map vs. individual die or other):

- a) As public information
- b) Through a tool with a standard agreement in place
- c) Directly with an interested company with a two-way NDA in place
- d) I cannot share this information

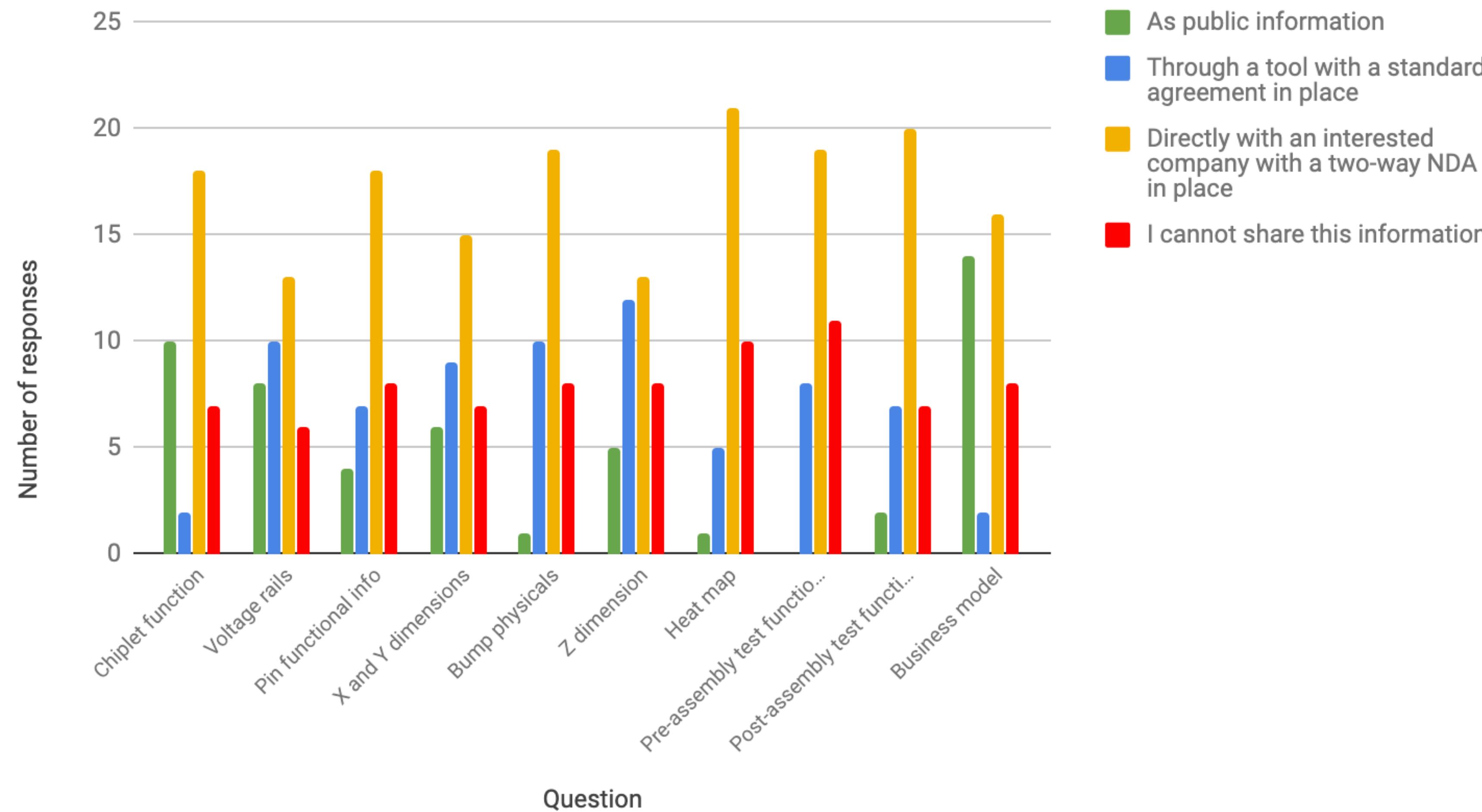
Survey Respondents: An Overview

- 25 responses
- 20 familiar with ODSA or chiplets, 4 familiar with chips, 1 not familiar
- 11 chiplet vendors
- 9 chiplet purchasers
- Job functions:



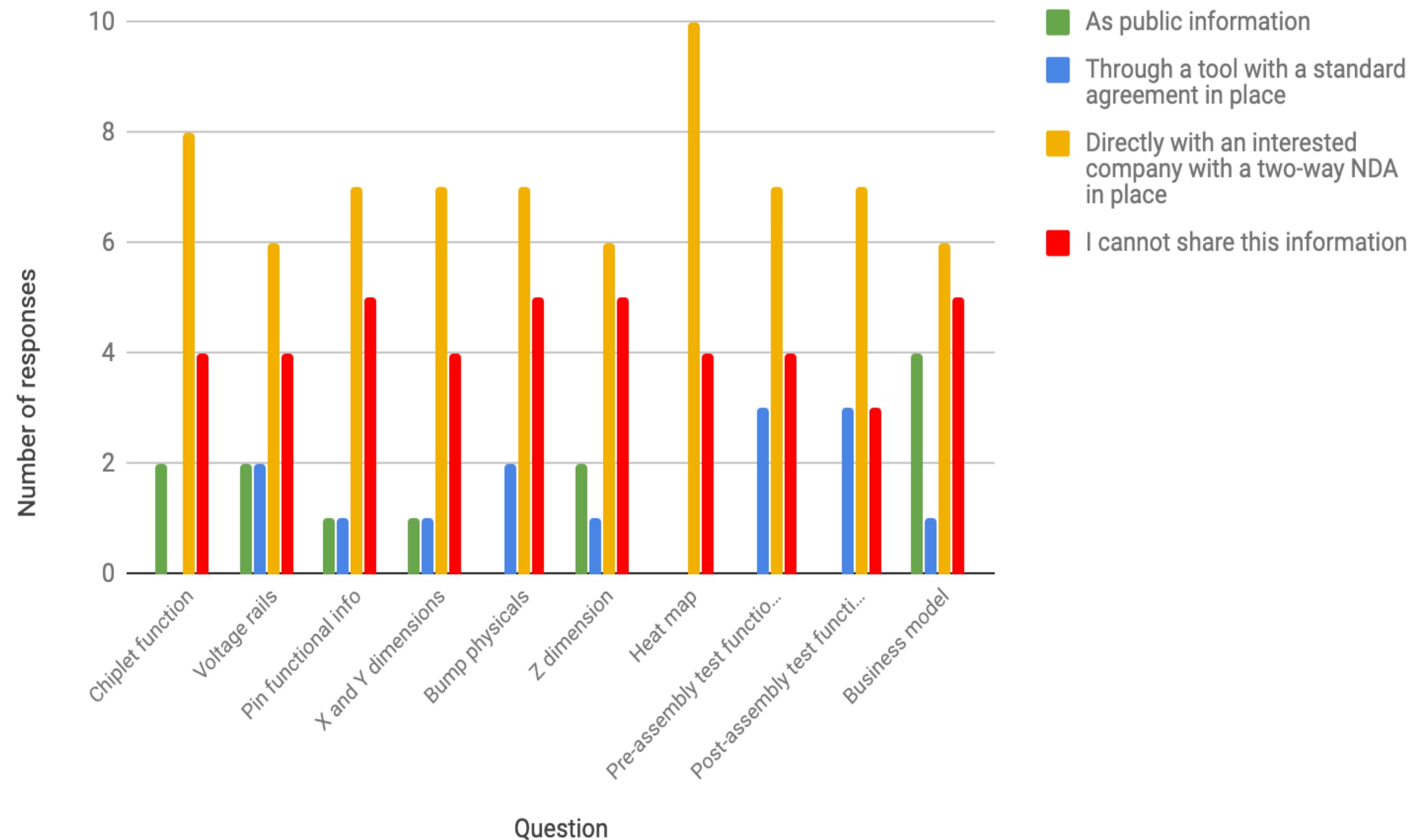
Survey Results: An Overview

ODSA Survey Response Overview



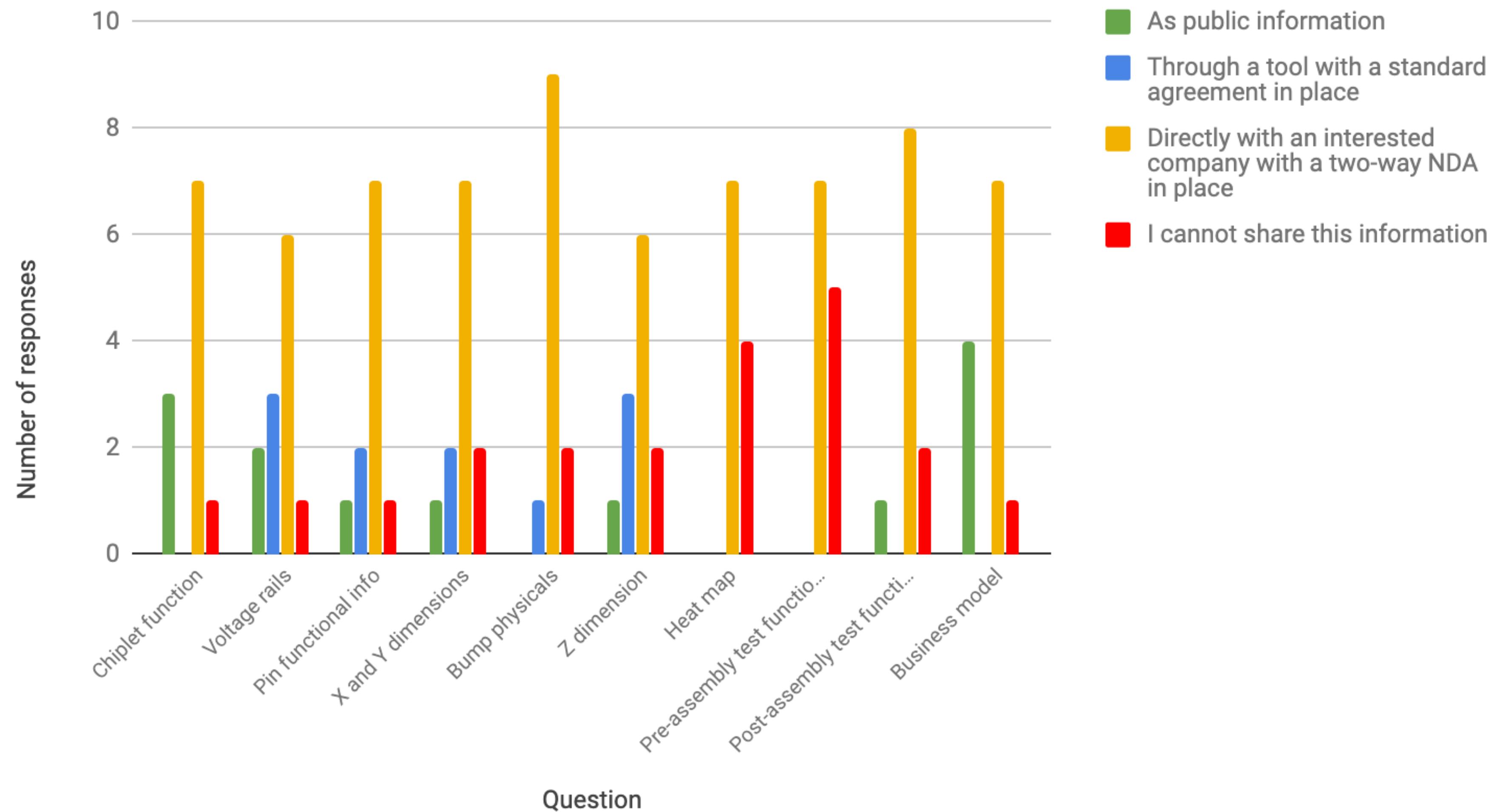
Survey Results: Engineers

ODSA Survey Responses - from Engineers



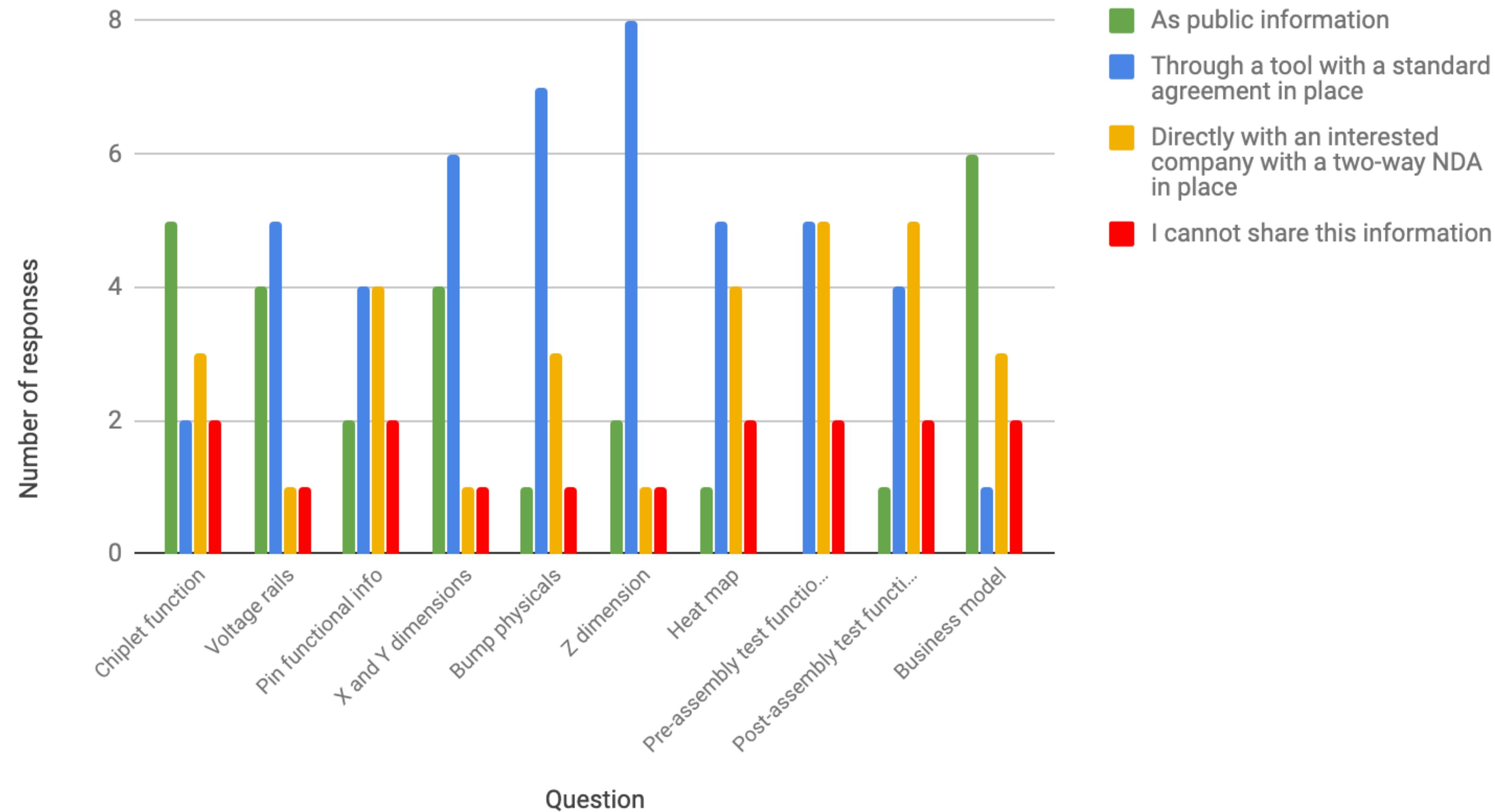
Survey Results: Architects

ODSA Survey Responses - from Architects



Survey Results: Execs, BD &

ODSA Survey Responses - from Execs, BD & Marketing



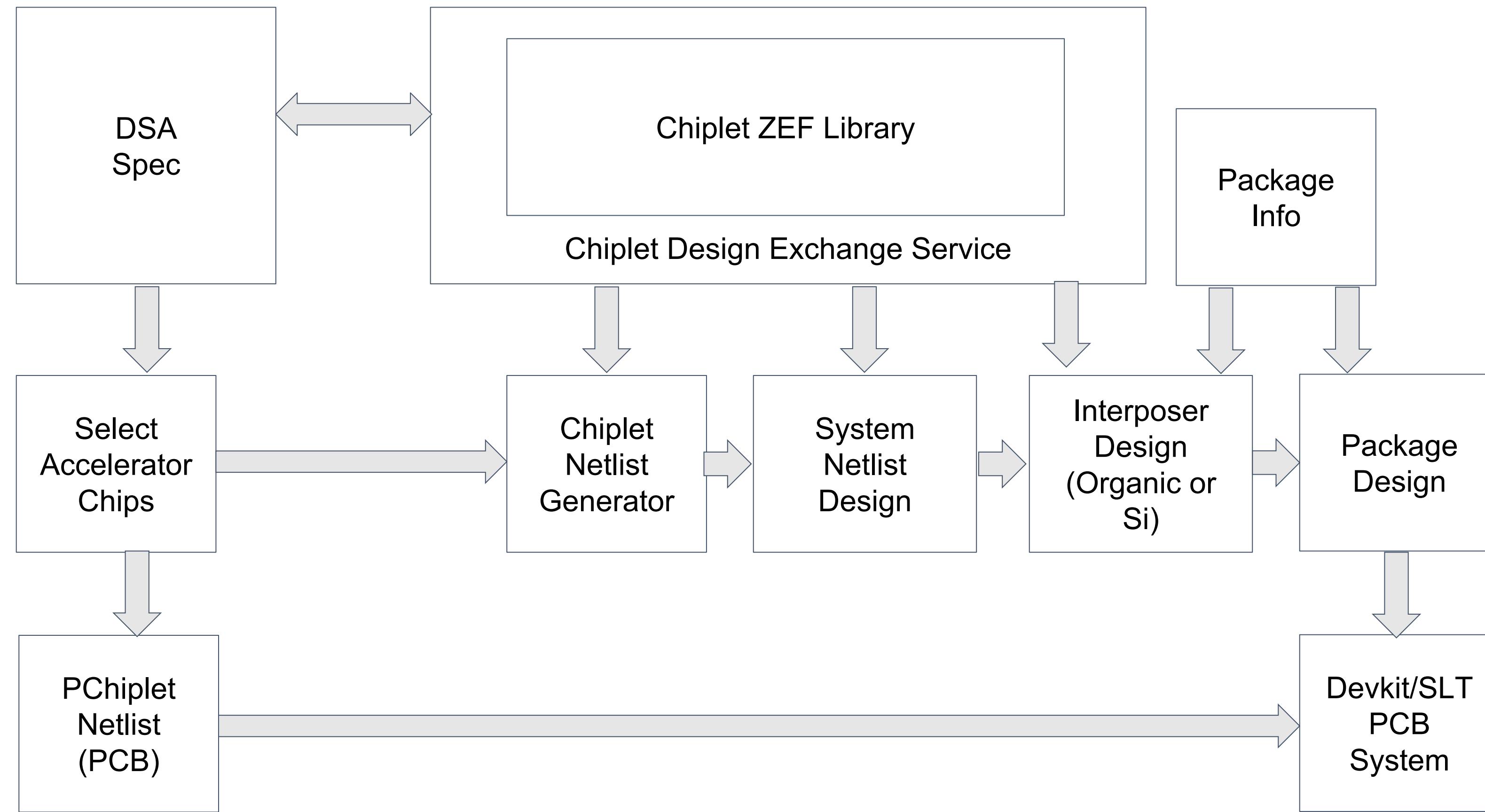
Conclusions from the Survey

Executives and Business Developers indicate the need for Chiplet sharing mechanism.

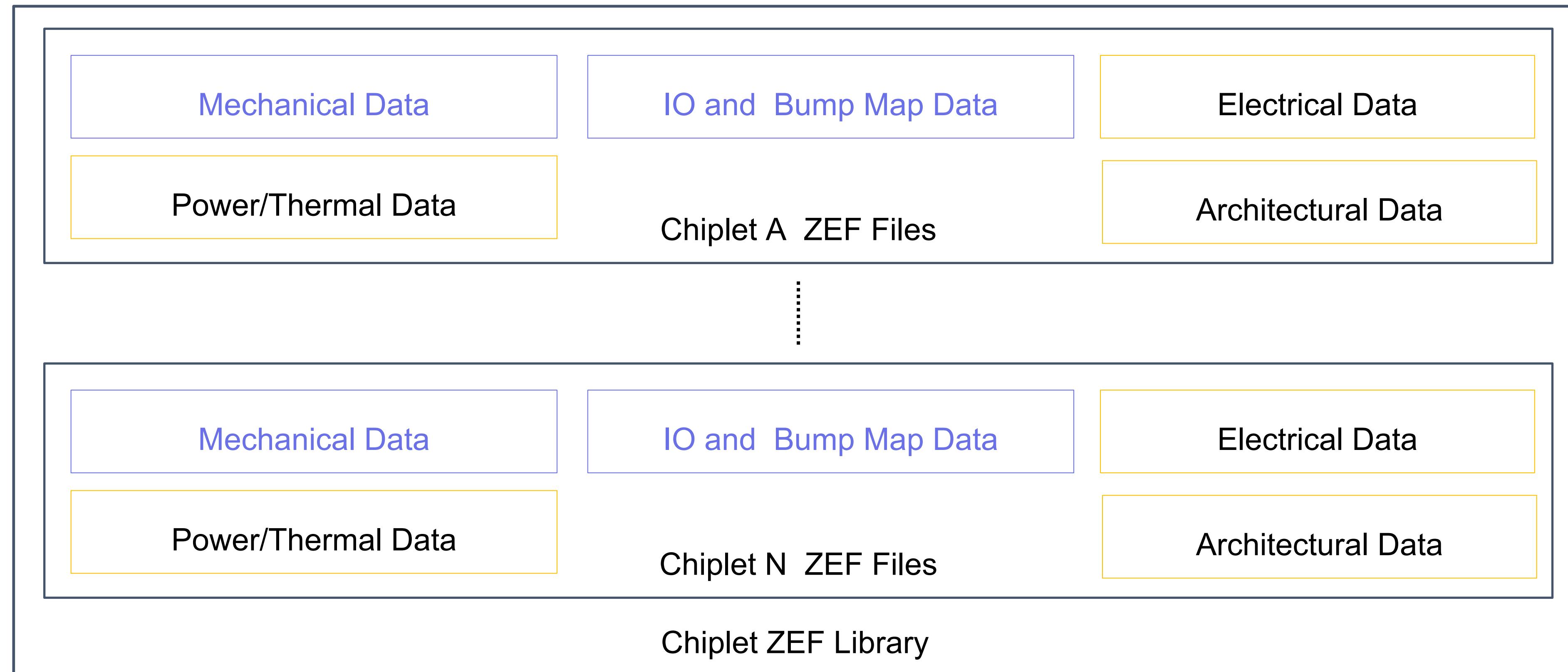
Architects are willing to share information under NDAs.

We believe the the opinion of the segment coded in red will transition to blue or green as business thinking develops and business need arises. CDX effort will help with that transition.

Chiplet Design Exchange Design Process



Chiplet Data Exchange Service



■ Through a tool with a standard agreement in place

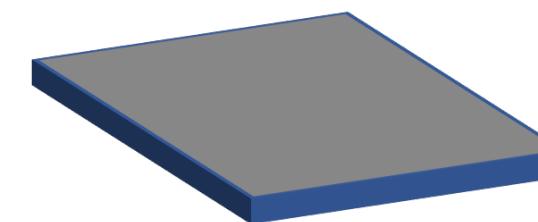
■ Directly with an interested company with a two-way NDA in place

ZEF – Mechanical Format

The Data to be provided in a CSV format with a number of standardized variable names;

For Example Try Reading the following Chiplet

x	y	z
1280	1790	520



A More Complete Mechanical :

Reference, Part_value, MPN, Order_Number, Container, Pieces_per_unit, Name, Pkg_type, Pkg_IPC_code, SMT_compatible, Width_x, Width_tolerance, Length_y, Length_tolerance, Thickness_z, Thickness_tolerance, Count_IO, Bump_pitch, Bump_pitch_tol, Bump_dia, Bump_dia_tol, Bump_thickness, Bump_thickness_tol, Bump_material, Mold Material, Reflow Profile

[More details at https://github.com/zglue/ZEF](https://github.com/zglue/ZEF)

Status for Chiplet Design Exchange

- A specification and white paper for CDX effort is being worked on.
- Draft 0.1 has been published to the group member.
- Trying to ratify access control mechanism for data sharing
- Once a week online meeting of participants
- Current participants include zGlue, Ayar Labs, Sarcina, Cadence, AveraSemi, ASE, Netronome

Looking for Volunteers

Send an email to jawad@zglue.com for participation

<https://www.opencompute.org/wiki/Server/ODSA>



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Next Steps and Call to Action

- Join Us. Looking for EDA, OSAT, Design Service, Chiplet Vendor, Distributor participation.
- Define a flow for PCB to Package conversion
- Setup a CDX service of your own
- List your Chiplets
- Share your requirements and wishlist for Chiplets

Looking for Volunteers

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Backup



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OCP Regional Summit
26–27, September, 2019

