CENG 2034 - Operating Systems

Week 9: Synchronization Tools

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Outline

Background

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  - May be interrupted at any time, partially completing execution
- Concurrent access to shared data may result in data inconsistency
- Maintaining data consistency requires mechanisms to ensure the orderly execution of cooperating processes

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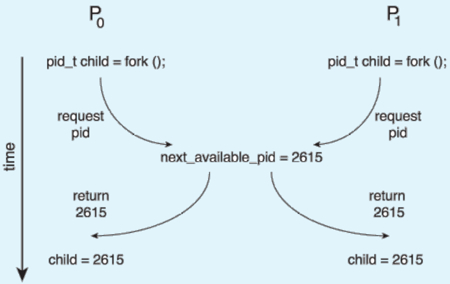
- Race condition on kernel variable `next_available_pid` which represents the next available process identifier (`pid`)



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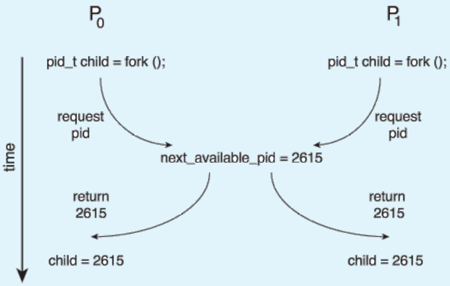

- Unless there is a mechanism to prevent P_0 and P_1 from accessing the variable `next_available_pid` the same `pid` could be assigned to two different processes!

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  - Process may be changing common variables, updating table, writing file, etc.
  - When one process in critical section, no other may be in its critical section
- Critical section problem is to design protocol to solve this
- Each process must ask permission to enter critical section in entry section, may follow critical section with exit section, then remainder section

Critical Section

General structure of process P_i

```
while (true)
{
    enrty section

    /* critical section */

    exit section

    /* reminder section */
}
```

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3. Bounded Waiting - A bound must exist on the number of times that other processes are allowed to enter their critical sections after a process has made a request to enter its critical section and before that request is granted
    - Assume that each process executes at a nonzero speed
    - No assumption concerning relative speed of the n processes

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  - What if there are two CPUs?

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  `int turn`
- The variable turn indicates whose turn it is to enter the critical section
- initially, the value of `turn` is set to `i`

Algorithm for Process P_i

```
while (true)
{
  while (turn == j);

  /* critical section */

  turn = j

  /* reminder section */
}
```

Correctness of the Software Solution

- Mutual exclusion is preserved

$\boxed{P_i \text{ enters critical section } \texttt{turn = i} \text{ and } \texttt{turn} \text{ cannot be both } \texttt{i} \text{ and } \texttt{j} \text{ at the same time}}$

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Correctness of the Software Solution

- Mutual exclusion is preserved

  P_i enters critical section `turn = i` and `turn` cannot be both `i` and `j` at the same time

- What about the Progress requirement?
- What about the Bounded-waiting requirement?

Outline

Peterson's Solution

- Two process solution
- Assume that the load and store machine-language instructions are atomic; that is, cannot be interrupted
- The two processes share two variables:

```
int turn;
boolean flag[2];
```

- The variable turn indicates whose turn it is to enter the critical section
- The flag array is used to indicate if a process is ready to enter the critical section.

`flag[i] = true` implies that process P_i is ready!

Algorithm for Process P_i

```
while (true)
{
  flag[i] = true;
  turn = j;
  while (flag[j] && turn == j);

  /* critical section */

  flag[i] = false

  /* reminder section */
}
```

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  - To improve performance, processors and/or compilers may reorder operations with no dependencies
- Understanding why it will not work is useful for better understanding race conditions
- For single-threaded this is fine as the result will always be the same
- For multithreaded the reordering may produce inconsistent or unexpected results

Example (Modern Architecture)

- Two threads share the data:

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bool flag = false;
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x = 100;
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```

- Q: What is the expected output?
  A: 100

Example (Modern Architecture (cont'd))

- However, since the variables flag and x are independent of each other, the instructions:

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Example (Modern Architecture (cont'd))

- However, since the variables flag and x are independent of each other, the instructions:

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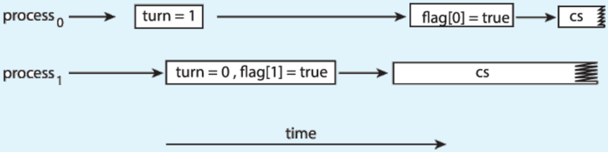
  for Tread 2 may be reordered
- If this occurs, the output may be 0

Peterson's Solution Revisited

- The effects of instruction reordering in Peterson's Solution



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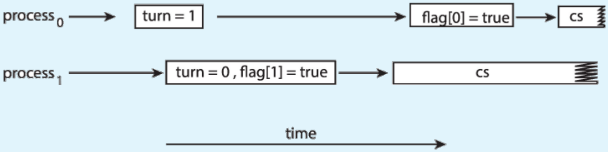

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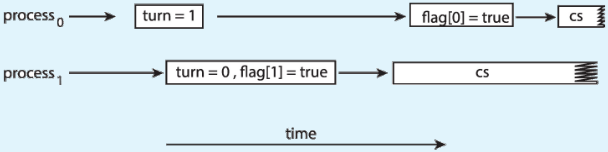

- This allows both processes to be in their critical section at the same time
- To ensure that Peterson's solution will work correctly on modern computer architecture we must use Memory Barrier

Outline

Memory Barrier

- Memory model – memory guarantees by computer architecture

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Memory Barrier

- Memory model – memory guarantees by computer architecture
- Memory models may be either:
  - Strongly ordered – where a memory modification of one processor is immediately visible to all other processors
  - Weakly ordered – where a memory modification of one processor may not be immediately visible to all other processors
- A memory barrier is an instruction that forces any change in memory to be propagated (made visible) to all other processors

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- When a memory barrier instruction is performed, the system ensures that all loads and stores are completed before any subsequent load or store operations are performed
- Therefore, even if instructions were reordered, the memory barrier ensures that the store operations are completed in memory and visible to other processors before future load or store operations are performed

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x = 100;
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- For Thread 1 we are guaranteed that the value of `flag` is loaded before the value of `x`.
- For Thread 2 we ensure that the assignment to `x` occurs before the assignment `flag`.

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  Operating systems using this not broadly scalable
- We will look at Hardware instructions

Hardware Instructions

Special hardware instructions that allow us to either test-and-modify the content of a word, or to swap the contents of two words atomically (uninterruptedly.)

- Test-and-Set instruction
- Compare-and-Swap instruction

The `test_and_set` Instruction

- Definition

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bool test_and_set (bool *target)
{
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  *target = true;
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    - Set the new value of passed parameter to true

Solution Using `test_and_set`

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```
do {
    while (test_and_set(&lock)); /* do nothing */

    /* critical section */

    lock = false;

    /* remainder section */

} while (true);
```

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- Does it solve the critical-section problem?

The compare_and_swap Instruction

- Definition

```
int compare_and_swap(int *value, int expected, int new_value)
{
        int temp = *value;
        if (*value == expected)
          *value = new_value;
        return temp;
}
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- Properties
  - Executed atomically
  - Returns the original value of passed parameter value
  - Set the variable `value` the value of the passed parameter `new_value` but only if `*value == expected` is true. That is, the swap takes place only under this condition.

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```
while (true)
{
  while (compare_and_swap(&lock, 0, 1) != 0); /* do nothing */

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  lock = 0;

  /* remainder section */
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Bounded-waiting with compare_and_swap

```
while (true)
{
    waiting[i] = true;
    key = 1;

    while (waiting[i] && key == 1)
        key = compare_and_swap(&lock,0,1);

    waiting[i] = false;

    /* critical section */

    j = (i + 1) % n;
    while ((j != i) && !waiting[j])
        j = (j + 1) % n;

    if (j == i)
        lock = 0;
    else
        waiting[j] = false;

    /* remainder section */
}
```

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  - Usually implemented via hardware atomic instructions such as compare-and-swap.
- But this solution requires busy waiting
- This lock therefore called a spinlock

Solution to CS Problem Using Mutex Locks

```
while (true)
{
  acquire lock

  /* critical section */

  release lock

  /* reminder section */
}
```

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  S = S - 1;
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{
  while (S <= 0); // busy wait
  S = S - 1;
}
```

- Definition of the `signal()` operation

```
signal(S)
{
  S = S + 1;
}
```

Semaphore (cont'd)

- Counting semaphore – integer value can range over an unrestricted domain

Semaphore (cont’d)

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- With semaphores we can solve various synchronization problems

Example (Semaphore Usage)

- Solution to the CS Problem

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  - Create a semaphore "`mutex`" initialized to 1

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  - Create a semaphore "mutex" initialized to 1

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wait(mutex);
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signal(mutex);
```

- Consider P_1 and P_2 that with two statements S_1 and S_2 and the requirement that S_1 to happen before S_2
  - Create a semaphore "synch" initialized to 0

```
P1:
  S1;
  signal(synch);
P2:
  wait(synch);
  S2;
```

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- These – and others – are examples of what can occur when semaphores and other synchronization tools are used incorrectly.

Outline

Monitors

- A high-level abstraction that provides a convenient and effective mechanism for process synchronization

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- Abstract data type, internal variables only accessible by code within the procedure
- Only one process may be active within the monitor at a time
- Pseudocode syntax of a monitor:

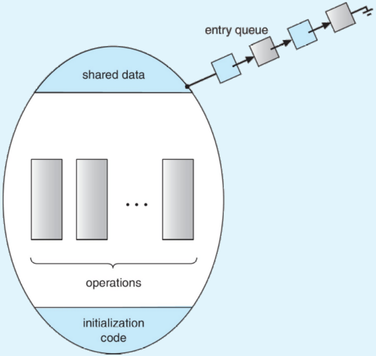
```
monitor monitor-name
{
  // shared variable declarations
  procedure P1 (...) { ... }

  procedure P2 (...) { ... }

  procedure Pn (...) { ... }

  initialization code (...) { ... }
}
```

Schematic view of a Monitor



Monitor Implementation Using Semaphores

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- Mutual exclusion within a monitor is ensured

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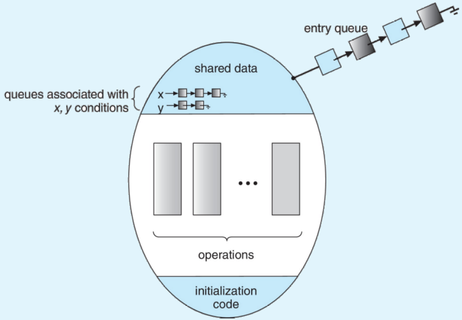
  - `x.signal()` – resumes one of processes (if any) that invoked `x.wait()`

Monitor with Condition Variables



Monitor Implementation Using Semaphores

- Variables

```
semaphore mutex;  // (initially  = 1)
semaphore next;   // (initially  = 0)
int next_count = 0; // number of processes waiting inside the monitor
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Monitor Implementation Using Semaphores

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- Each function *P* will be replaced by

```
wait(mutex);
  ...
  body of P;
  ...
if (next_count > 0)
  signal(next)
else
  signal(mutex);
```

Implementation (Condition Variables)

- For each condition variable x, we have:

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- Waiting indefinitely violates the progress and bounded-waiting criteria discussed at the beginning of this chapter.
- Liveness refers to a set of properties that a system must satisfy to ensure processes make progress.
- Indefinite waiting is an example of a liveness failure.

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- However, P_1 is waiting until P_0 execute `signal(S)`.
- Since these `signal()` operations will never be executed, P_0 and P_1 are deadlocked.

Liveness

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Liveness

- Other forms of deadlock:
- Starvation – indefinite blocking
  - A process may never be removed from the semaphore queue in which it is suspended

Thanks! & Questions?