CENG 2034 - Operating Systems

Week 13: Main Memory

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Outline

Protection

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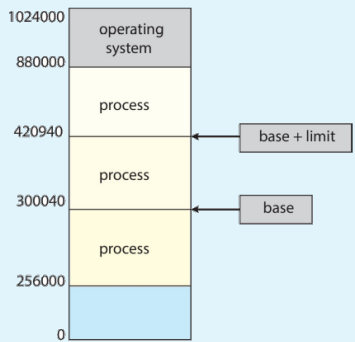
- Need to ensure that a process can access only those addresses in its address space.
- We can provide this protection by using a pair of base and limit registers define the logical address space of a process



Hardware Address Protection

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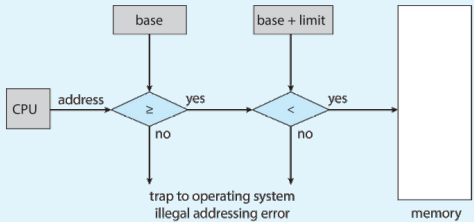

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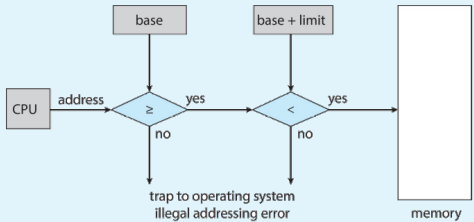

- the instructions to loading the base and limit registers are privileged

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  - Each binding maps one address space to another

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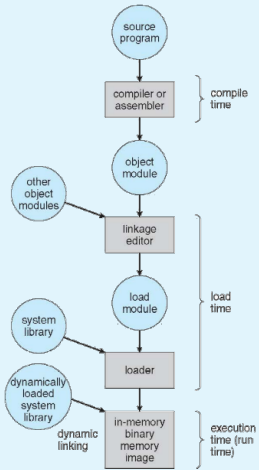
  - Need hardware support for address maps (e.g., base and limit registers)

Multistep Processing of a User Program



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- Physical address space is the set of all physical addresses corresponding to these logical addresses

Memory-Management Unit (MMU)

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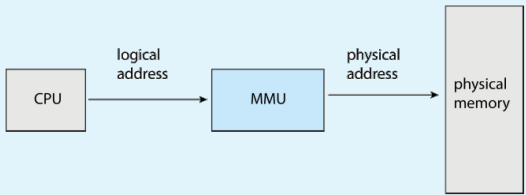

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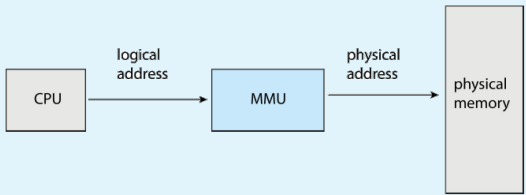

- Many methods possible, covered in the rest of this chapter

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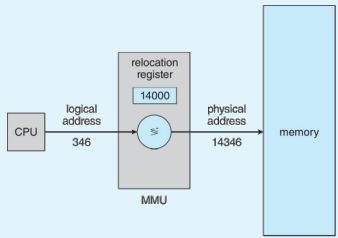

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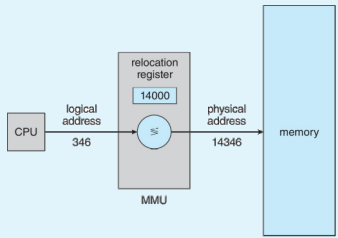

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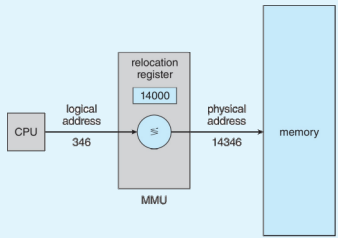

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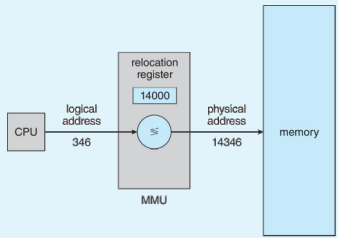

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  - Logical address bound to physical addresses

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  - OS can help by providing libraries to implement dynamic loading

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- Dynamic linking is particularly useful for libraries

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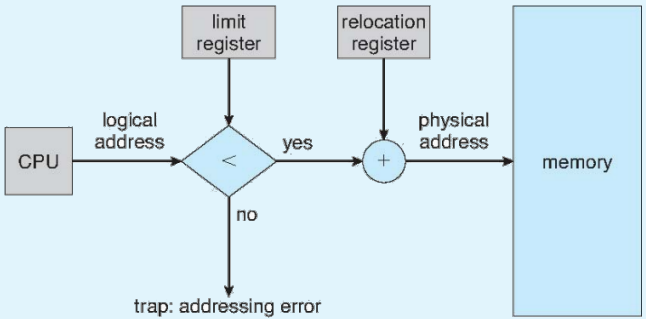
Hardware Support for Relocation and Limit Registers



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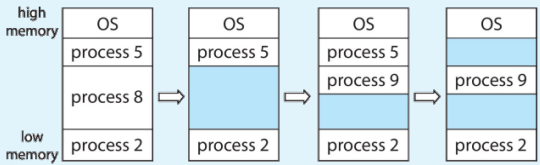
- Operating system maintains information about: a) allocated partitions b) free partitions (hole)



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  - 1/3 may be unusable → 50-percent rule

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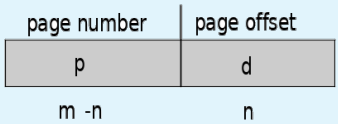

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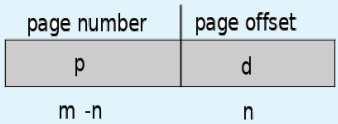

- For given logical address space 2^m and page size 2^n

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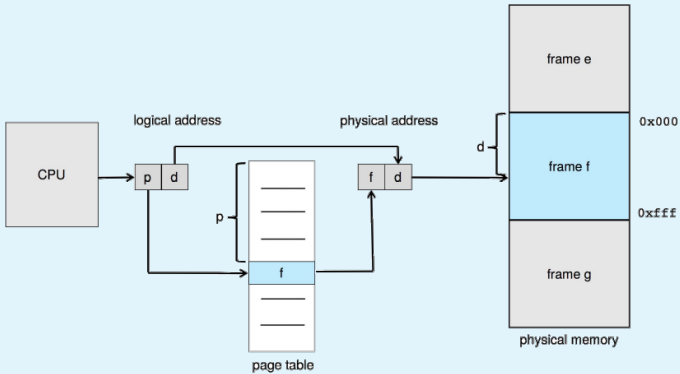
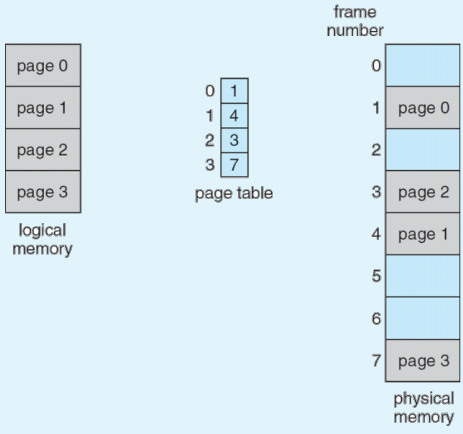


Paging Model of Logical and Physical Memory



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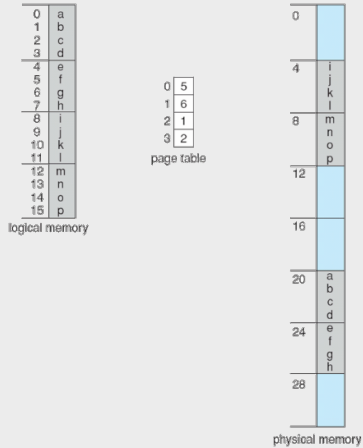

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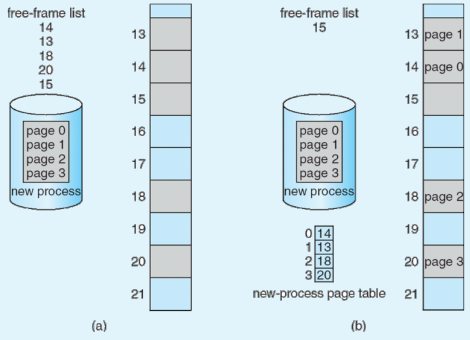

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- The two-memory access problem can be solved by the use of a special fast-lookup hardware cache called translation look-aside buffers (TLBs) (also called associative memory).

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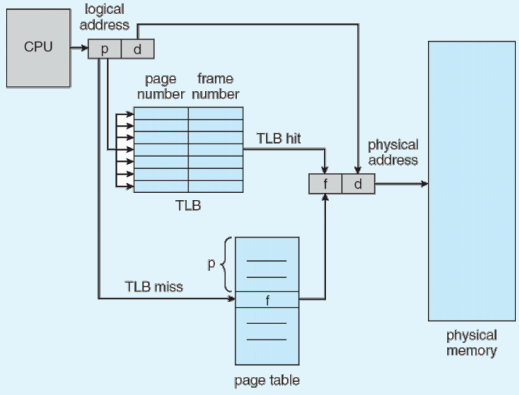
Paging Hardware With TLB



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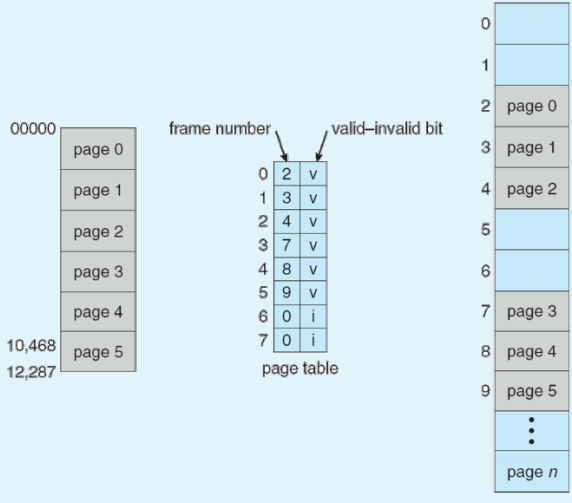

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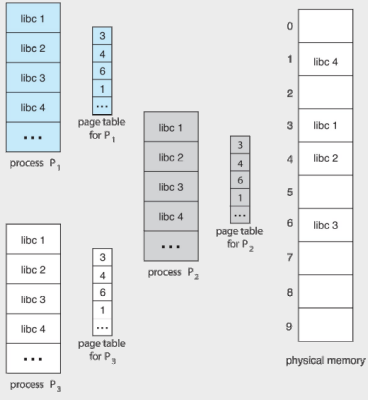

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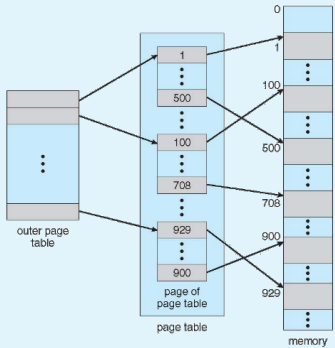

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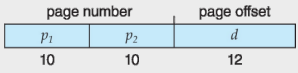

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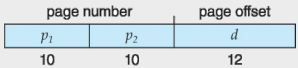

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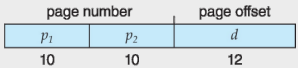
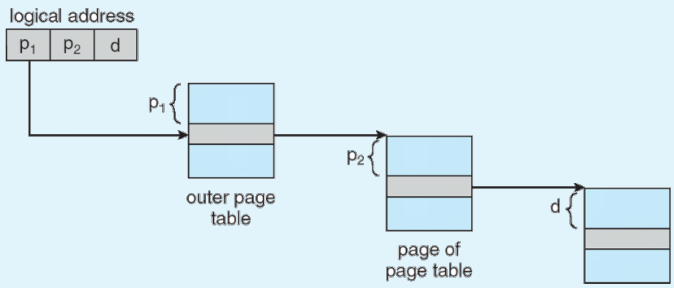


- where p_1 is an index into the outer page table, and p_2 is the displacement within the page of the inner page table
- Known as forward-mapped page table

Address Translation Scheme



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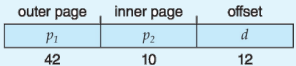

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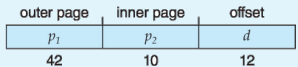

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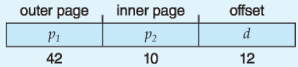

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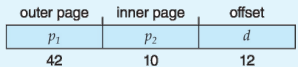

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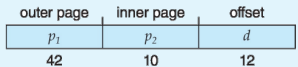

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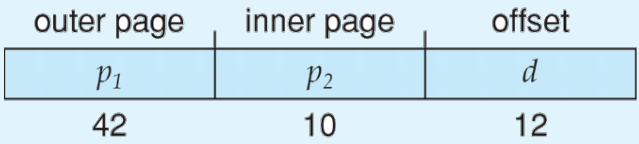
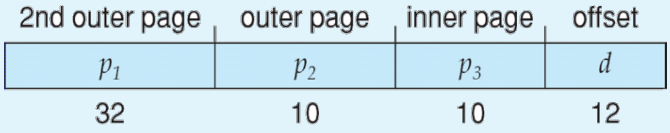
  - And possibly 4 memory access to get to one physical memory location

Three-level Paging Scheme





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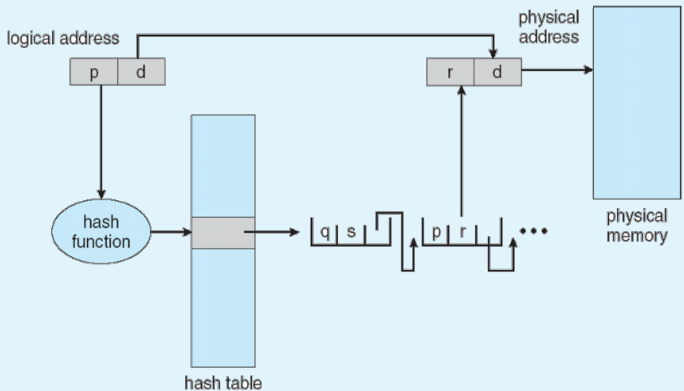

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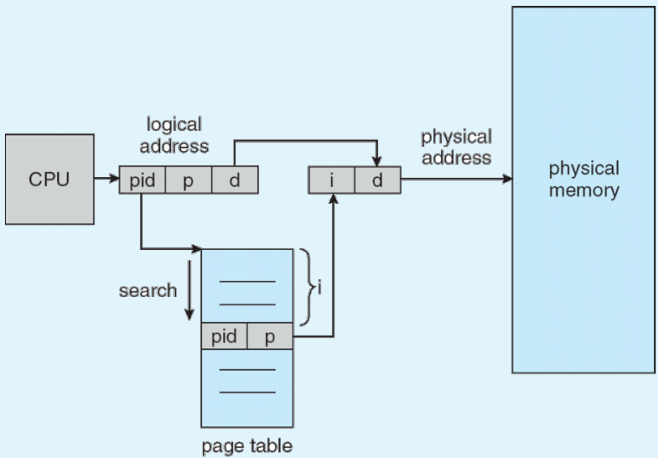
Inverted Page Table Architecture



Outline

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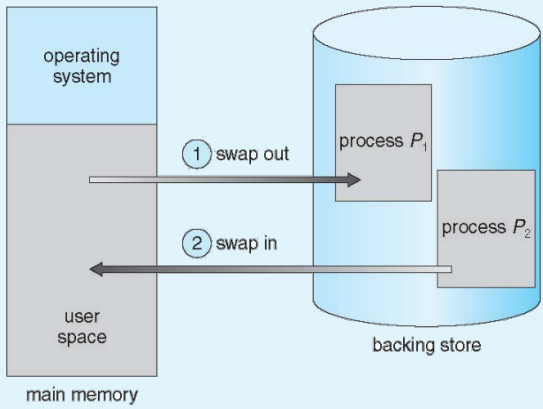
Schematic View of Swapping



Thanks! & Questions?