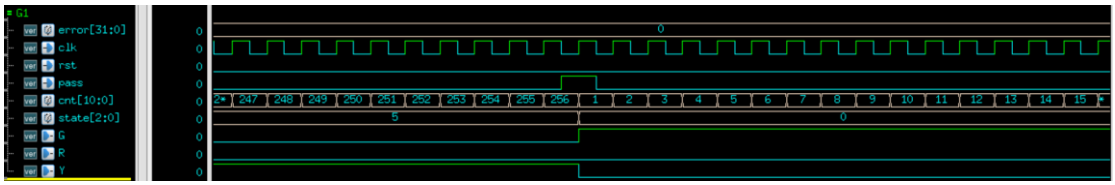
實驗結果圖：

（波形圖及模擬完成截圖）



（波形圖）

```
cd sw;
cd /home/caid011/HW2_P110775004/build; \
cp /home/caid011/HW2_P110775004/sim/ans.txt .;
cd /home/caid011/HW2_P110775004/build; \
ncverilog /home/caid011/HW2_P110775004/sim/traffic_light_tb.v /home/caid011/HW2_P110775004/src/traffic_light.v \
+incdir+/home/caid011/HW2_P110775004/src \
+nc64bit \
+access+r
ncverilog(64): 15.20-s084: (c) Copyright 1995-2020 Cadence Design Systems, Inc.
Loading snapshot worklib.traffic_light_tb:v ..... Done
*Verdi* Loading libsscore_ius152.so
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
FSDB Dumper for IUS, Release Verdi_O-2018.09, Linux x86_64/64bit, 08/30/2018
(C) 1996 - 2018 by Synopsys, Inc.
*Verdi* FSDB WARNING: The FSDB file already exists. Overwriting the FSDB file may crash the programs that are using this file.
*Verdi* : Create FSDB file 'traffic_light.fsdb'
*Verdi* : Begin traversing the scopes, layer (0).
*Verdi* : End of traversing.
*Verdi* : Begin traversing the MDAs, layer (0).
*Verdi* : Enable +mda and +packedmda dumping.
*Verdi* : End of traversing the MDAs.


       ***************************
       **                       **       /|__/|
       **  Congratulations !!   **      / 0,0  |
       **                       **    /_ .  _  |
       **  Simulation PASS!!    **   /^ ^ ^ ^ \ |
       **                       **  |^ ^ ^ ^ ^|w|
       *************** ************   \m___m__|_|


Simulation complete via $finish(1) at time 81921 NS + 0
../sim/traffic_light_tb.v:85     $finish;
ncsim> exit
```

(make rtl)

```
Operating Conditions: WCCOM   Library: fsa0m_a_generic_core_ss1p62v125c
Wire Load Model Mode: enclosed

  Startpoint: rst (input port clocked by clk)
  Endpoint: R_reg (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  traffic_light      G5K                   fsa0m_a_generic_core_ss1p62v125c

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.50       0.50
  input external delay                     5.00       5.50 r
  rst (in)                                 0.01       5.51 r
  U131/O (AO12)                            0.32       5.83 r
  U118/O (NR3)                             0.23       6.06 f
  U117/O (ND3)                             0.30       6.36 r
  U105/O (INV1S)                           0.70       7.06 f
  U62/O (AO222)                            0.57       7.64 f
  R_reg/D (QDFFN)                          0.00       7.64 f
  data arrival time                                   7.64

  clock clk (rise edge)                   10.00      10.00
  clock network delay (ideal)              0.50      10.50
  clock uncertainty                       -0.10      10.40
  R_reg/CK (QDFFN)                         0.00      10.40 r
  library setup time                      -0.13      10.27
  data required time                                 10.27
  -----------------------------------------------------------
  data required time                                 10.27
  data arrival time                                  -7.64
  -----------------------------------------------------------
  slack (MET)                                         2.64
```

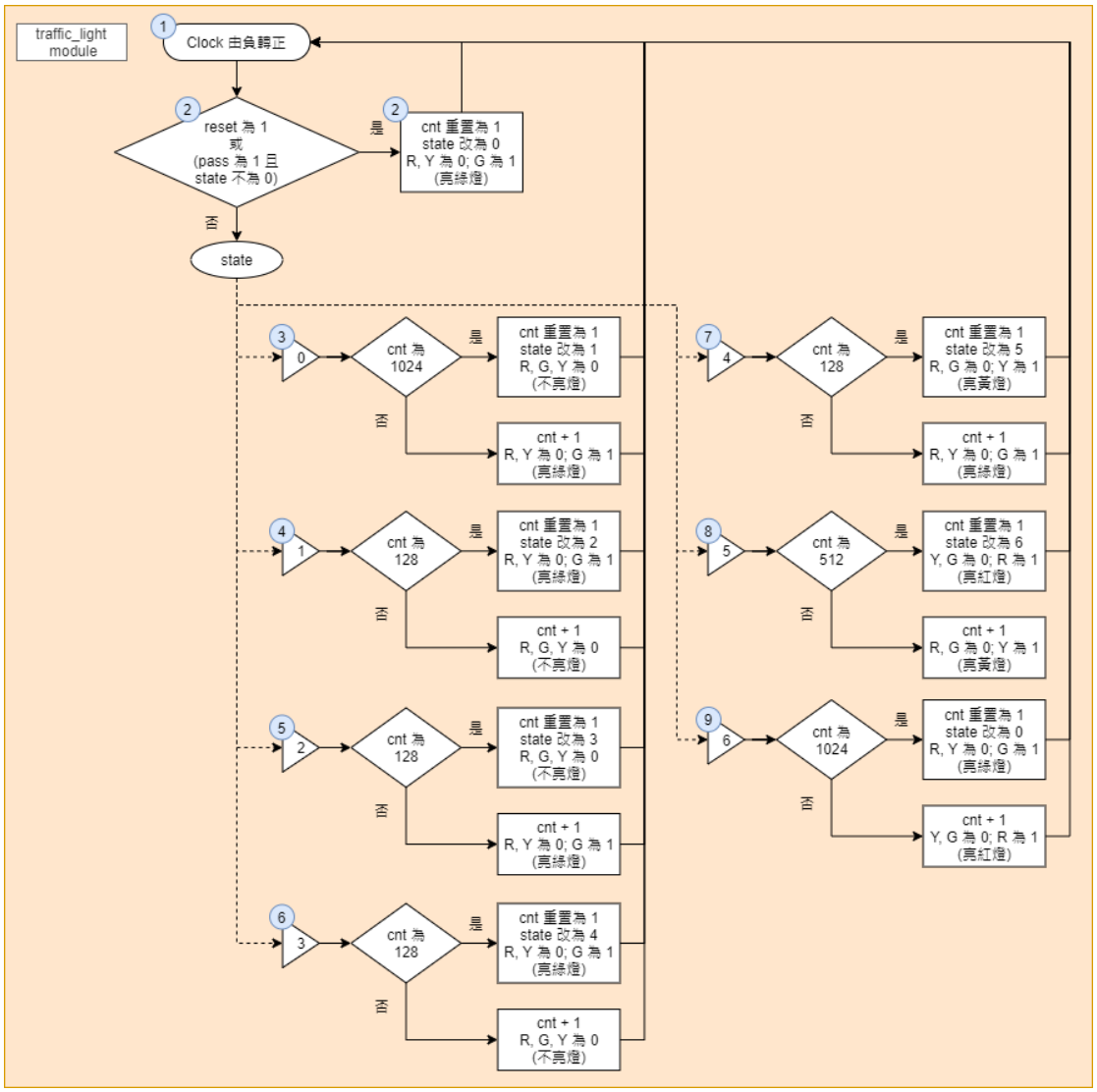
(make syn:report_timing)

```
Library(s) Used:

    fsa0m_a_generic_core_ss1p62v125c (File: /usr/cad/CBDK/CBDK018_UMC_Faraday_v1.0/CIC/SynopsysDC/db/fsa0m_a_generic_core_ss1p
62v125c.db)

Number of ports:                          160
Number of nets:                           495
Number of cells:                          276
Number of combinational cells:            252
Number of sequential cells:                17
Number of macros/black boxes:               0
Number of buf/inv:                         20
Number of references:                      25

Combinational area:            5618.390254
Buf/Inv area:                   124.991999
Noncombinational area:          921.816006
Macro/Black Box area:             0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:               6540.206260
Total area:                 undefined
```

(make syn:report_area)

程式運作流程:

(簡單說明波形變化的意義)



1. 每當 clock 由負轉正觸發後續執行
2. 若 reset 為 1 或 pass 為 1 且非狀態 0 時，cnt 重置為 1，狀態為 0，亮綠燈；若非以上情況，判斷狀態
3. 狀態 0，亮綠燈，直到 cnt 為 1024，cnt 重置為 1，轉為狀態 1，不亮燈
4. 狀態 1，不亮燈，直到 cnt 為 128，cnt 重置為 1，轉為狀態 1，亮綠燈
5. 狀態 2，亮綠燈，直到 cnt 為 128，cnt 重置為 1，轉為狀態 1，不亮燈
6. 狀態 3，不亮燈，直到 cnt 為 128，cnt 重置為 1，轉為狀態 1，亮綠燈
7. 狀態 4，亮綠燈，直到 cnt 為 128，cnt 重置為 1，轉為狀態 1，亮黃燈
8. 狀態 5，亮黃燈，直到 cnt 為 512，cnt 重置為 1，轉為狀態 1，亮紅燈
9. 狀態 6，亮紅燈，直到 cnt 為 1024，cnt 重置為 1，轉為狀態 1，亮綠燈