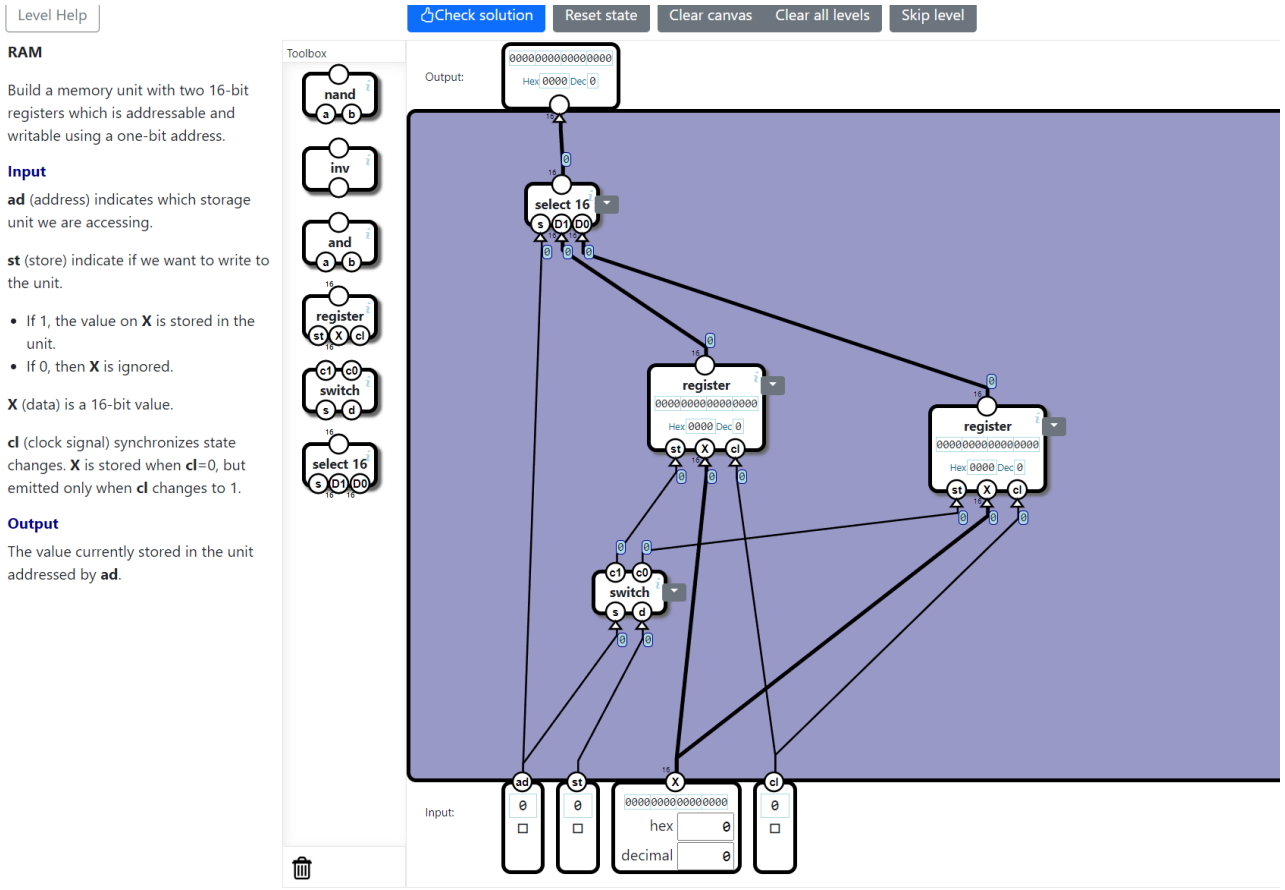
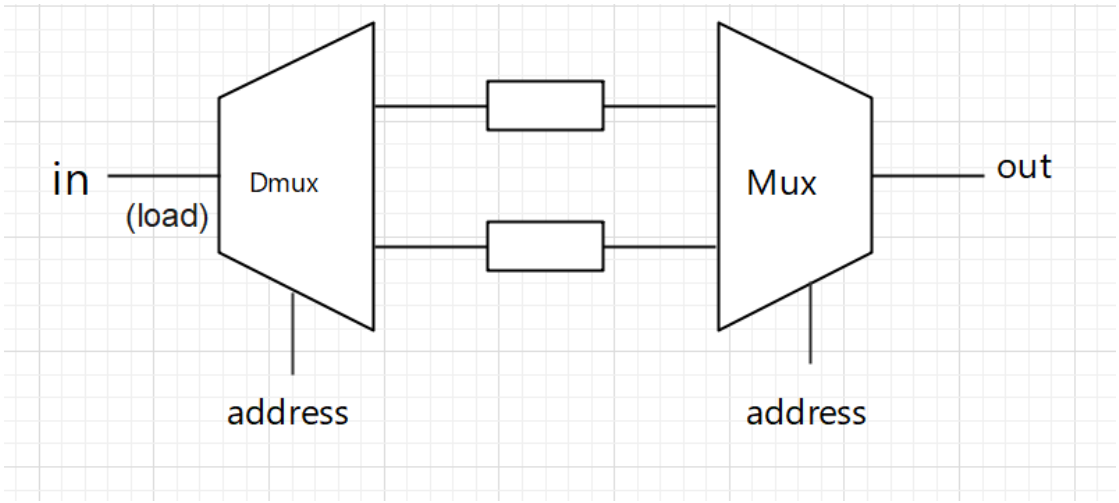
Coursework 1

Hints

Task1: RAM (Random-access memory)



RAM



Level Help

RAM

Build a memory unit with two 16-bit registers which is addressable and writable using a one-bit address.

Input

ad (address) indicates which storage unit we are accessing.

st (store) indicate if we want to write to the unit.

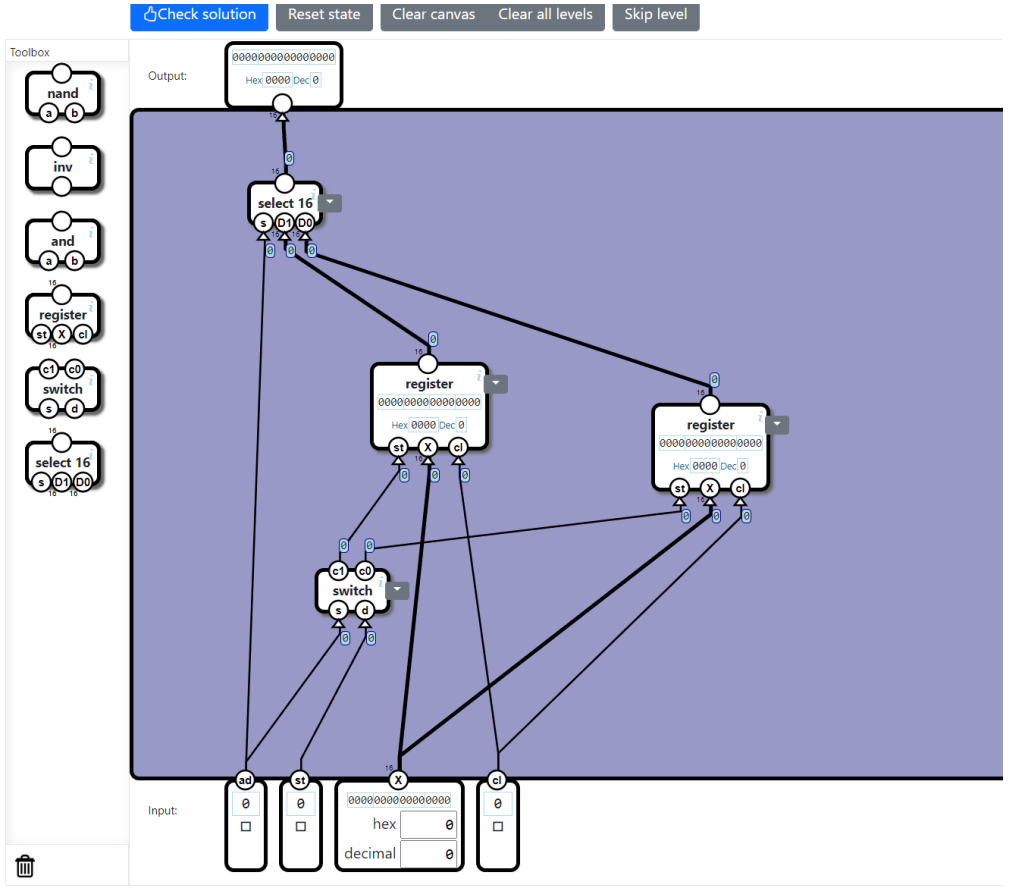
- If 1, the value on **X** is stored in the unit.
- If 0, then **X** is ignored.

X (data) is a 16-bit value.

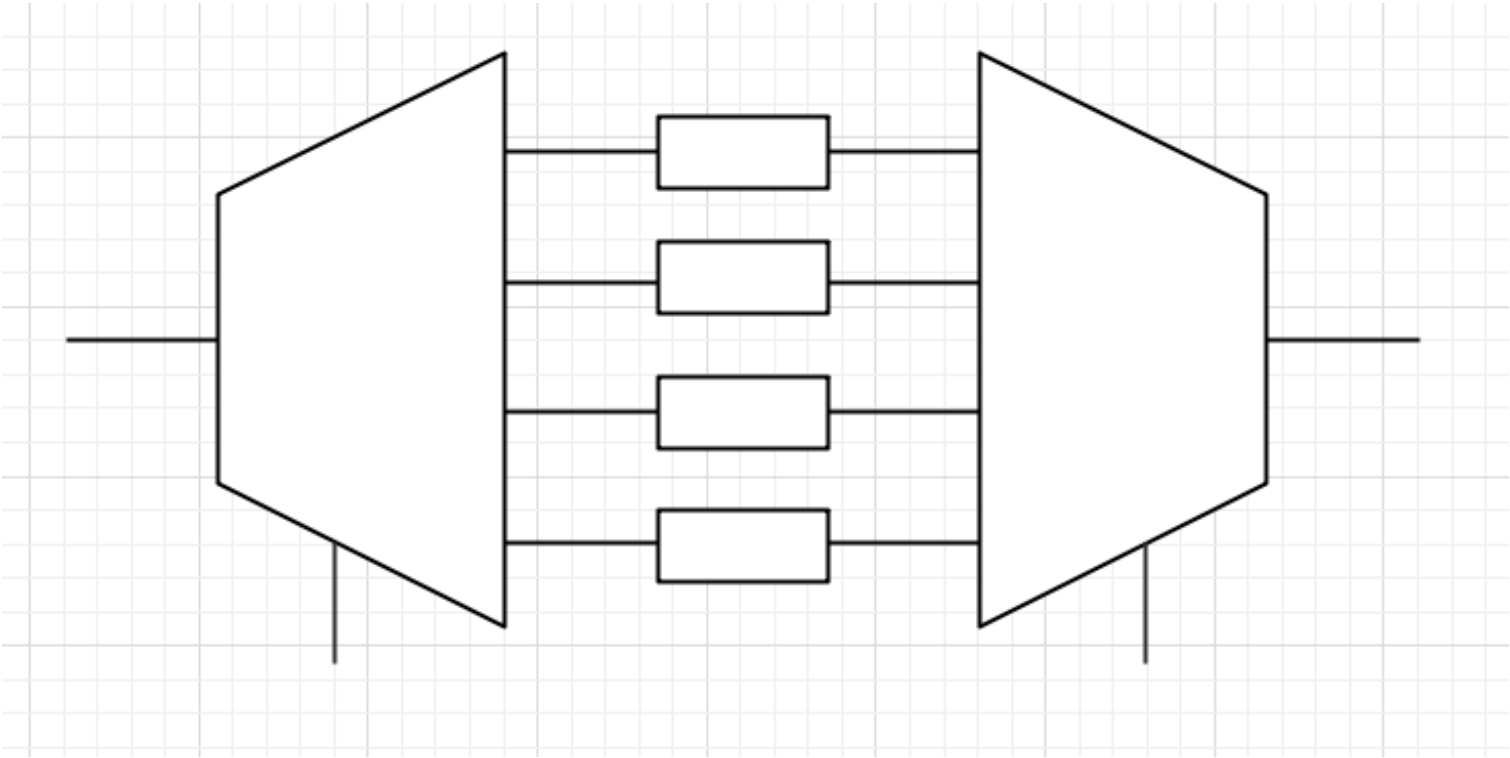
cl (clock signal) synchronizes state changes. **X** is stored when **cl**=0, but emitted only when **cl** changes to 1.

Output

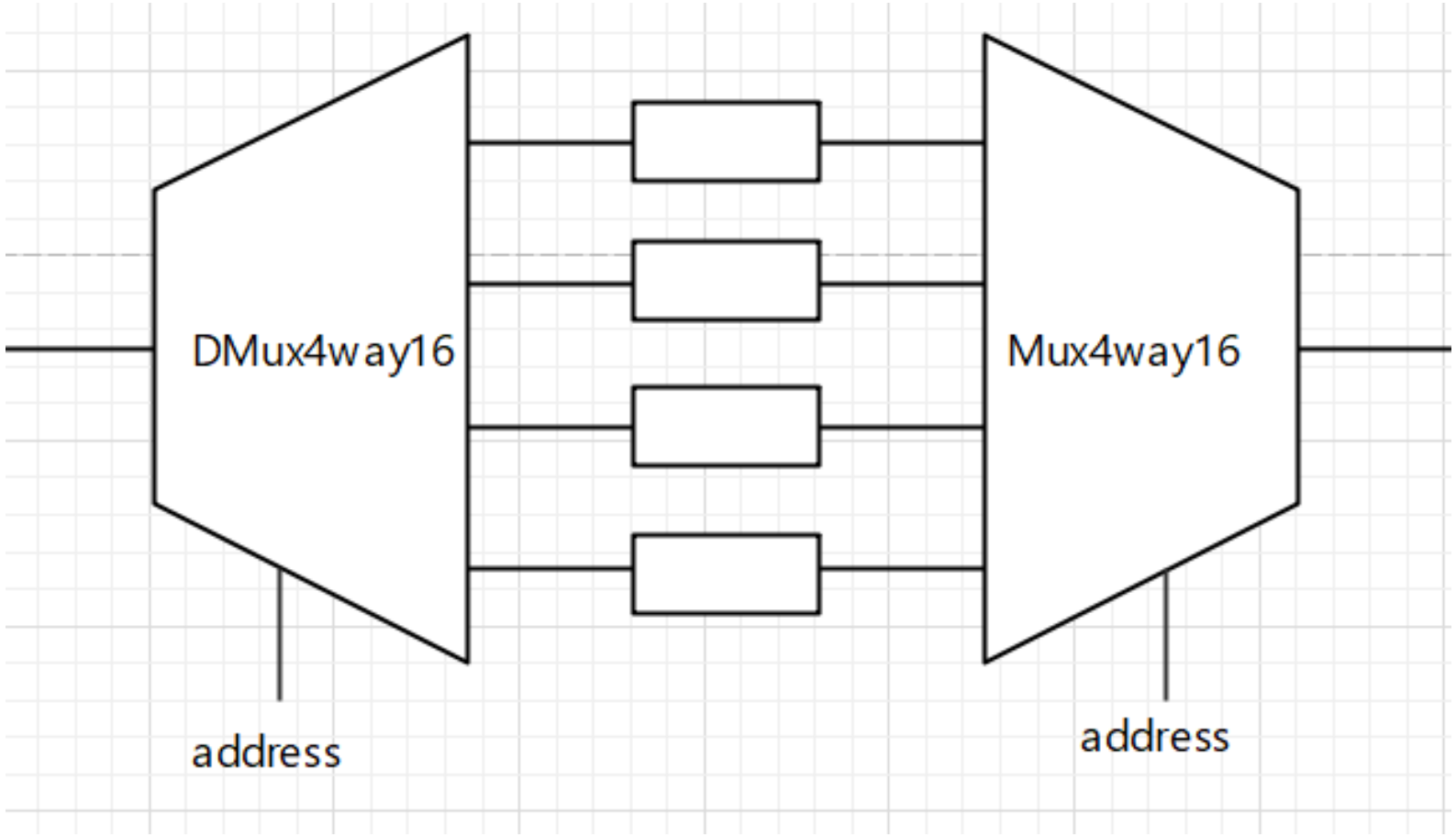
The value currently stored in the unit addressed by **ad**.



RAM

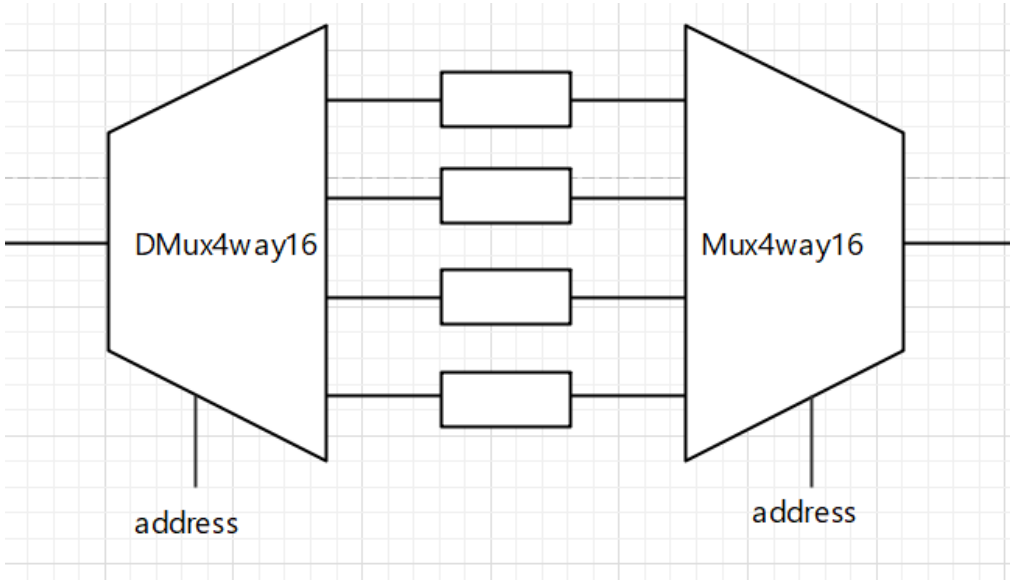


RAM



Task2: SAM (Sequential access memory)

How to create “address”



Counter

A **counter** component increments a number for each clock cycle.

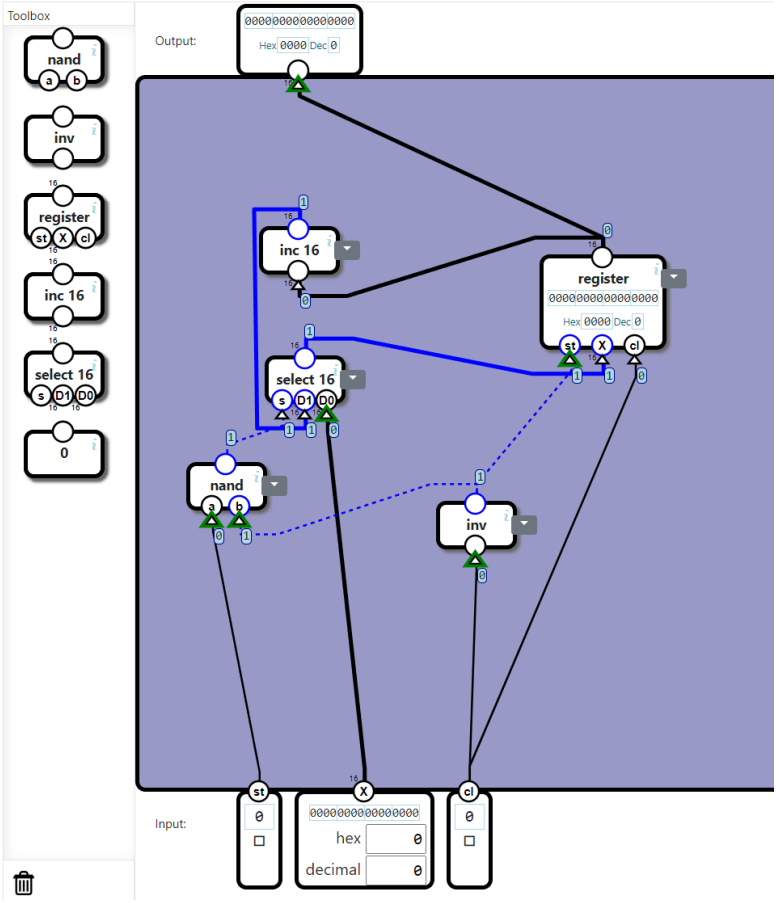
The counter output changes when **cl** (clock signal) changes to 1.

If **st** is 0, then the previous counter value is incremented with 1.

If **st** (store) is 1, then the input value **X** is used as the new counter value.

To describe this in a table requires two variables, **in** and **out**, which stores 16-bit numbers:

Input		Effect	Output
st	**cl**		
0	0	set **in** to **out** + 1	**out**
1	0	set **in** to **X**	**out**
-	1	set **out** to **in**	**out**



SUM

Full adder

Half adder

Overflow:

- consider the “carry”
- don’t worry about the sum when overflow = 1

Binary division

When dividing by multiples of two:
i.e.

8 => 1000
8 / 2 = 4 => 0100
displacement: right 1
4 / 2 = 2 => 0010
displacement: right 1

8 => 1000
8 / 4 = 2 => 0010
displacement: right 2

Notice:
Task 4 has no negative numbers, no division by 0, and no possible overflow.

Task5 may have some difficult test cases
You will get 1 mark if you can pass any one of the test cases, but if you want to get full mark you must pass all of them.
Any cases may appear in task 5.

Consider displacement
consider about how to calculate multiplication

CSF GTA office hour

- What we can help:
  - Solve your doubts about coursework
  - Help with doubts about the concepts
  - Tell you what makes your code fail

- What we can not help:
  - Debug directly
  - Tell you how to finish cw directly

Chip name doesn’t match HDL name

XX is not a pin in XX

Chip XX is not found in the working and built in folders

X(1) and X(16) has different bus widths

Loading chip …….

CHIP XX{

```
    IN a , b;
    OUT out;

    PARTS:
    XX(a=a, b=b, out=out);  // Loading chip …….
    X(a = a,b= b ,out = out); // Chip XX is not found in the working and built in folders
    AND(a=a, b=b, out=out); //Chip name doesn’t match HDL name
    AND(in=a, b=b, out=out); //XX is not a pin in XX
    And16(a=a, b=b, out=out); //X(1) and X(16) has different bus widths
```

}