Datasheet for Telink

BLE Multi-Standard Wireless SoC

TLSR8271

DS-TLSR8271-E1

Version 0.1.0

2019-12-26

Key Words:

BLE; BLE Mesh; 2.4GHz; Features; Typical Applications; Ordering Info;

Brief:

This datasheet is dedicated for Telink BLE multi-standard SoC TLSR8271 (VID: 0x00). In this datasheet, key features, working mode, main modules, electrical specification and application of TLSR8271 are introduced.

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1. Overview

The TLSR8271 is Telink-developed Bluetooth LE wireless SoC solution with internal Flash and audio support, which combines the features and functions needed for all 2.4GHz IoT standards into a single SoC. It's completely RoHS-compliant and 100% lead (Pb)-free.

The TLSR8271 combines the radio frequency (RF), digital processing, protocols stack software and profiles for multiple standards into a single SoC. The chip supports standards and industrial alliance specifications including Bluetooth Low Energy (up to Bluetooth 5.1), BLE Mesh, ANT and 2.4GHz proprietary standard. The TLSR8271's embedded FLASH enables dynamic stack and profile configuration, and the final end product functionality is configurable via software, providing ultimate flexibility. The TLSR8271 also has hardware OTA upgrades support and multiple boot switching, allowing convenient product feature roll outs and upgrades.

The TLSR8271 supports concurrent multi-standards. For some use cases, the TLSR8271 can "concurrently" run two standards, for example, stacks such as BLE and 2.4G can run concurrently with one application state but dual radio communication channels for interacting with different devices. The end product working in this mode can maintain active Bluetooth Smart connections to smart phones or other BLE devices while control and communicate with other 2.4GHz devices at the same time. In this case, it's compatible with Bluetooth standard, supports BLE specification up to Bluetooth 5.1, allows easy connectivity with Bluetooth Smart Ready mobile phones, tablets, laptops, which supports BLE slave and master mode operation, including broadcast, encryption, connection updates, and channel map updates. At the same time, it also supports 2.4G standard, and is perfect for creating interoperable solution for use within the home combined with leading 2.4G software stack. This feature enables products to bridge the smartphone and home automation world with a single chip and no requirement for an external hub.

The TLSR8271 integrates hardware acceleration to support the complicated security operations required by Bluetooth, up to and including 5.0 standard, without the requirement for an external DSP, thereby significantly reducing the product eBOM.

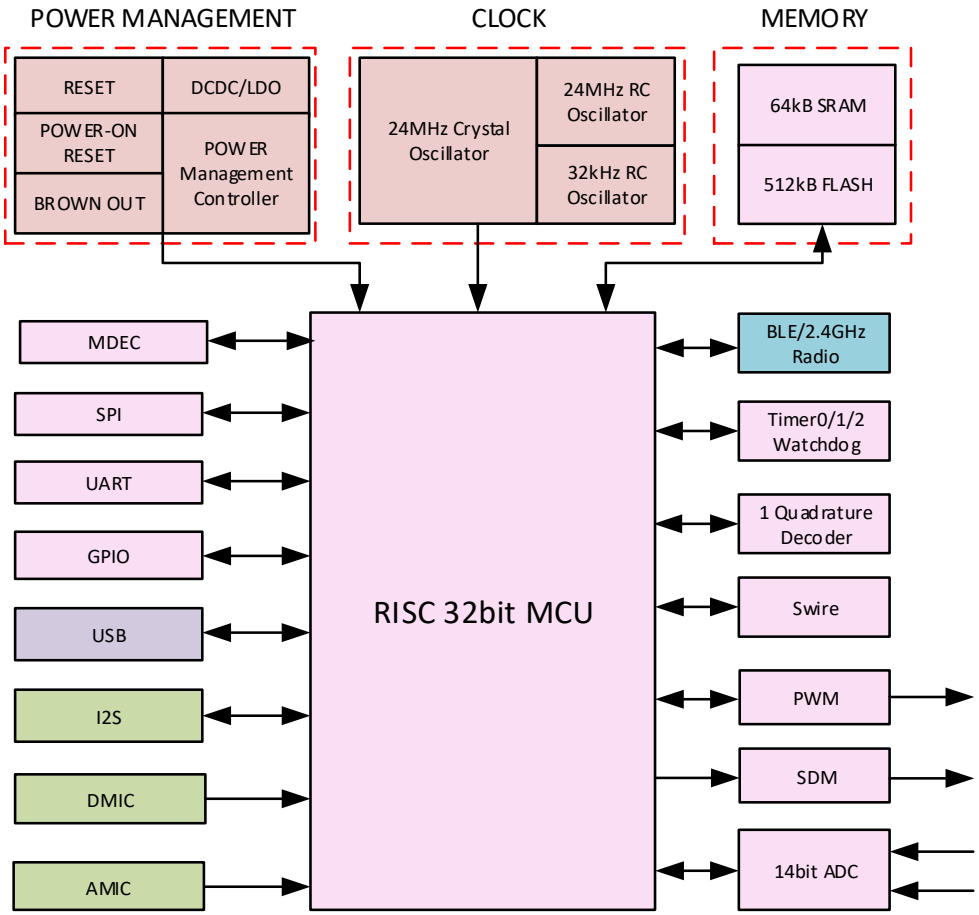
The TLSR8271 supports single-channel analog microphone or dual-channel digital microphone, and stereo audio output with enhanced voice performance for voice search and other such applications. The TLSR8271 also includes a full range of on-chip peripherals for interfacing with external components such as LEDs, sensors, touch controllers, keyboards, and motors. This makes it an ideal single-chip solution for IoT (Internet of Things) and HID (Human Interface Devices) application such as wearable devices, smart lighting, smart home devices, advanced remote controls, and wireless toys.

The TLSR8271 series have passed ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US) and ARIB STD-T66 (Japan) certification.

1.1 Block Diagram

The TLSR8271 is designed to offer high integration, ultra-low power application capabilities. The system's block diagram is as shown in Figure 1-1.

Figure 1-1 Block Diagram of the System



Note:

- *Modules marked with different colors belong to different power domains. Power state of each power domain can be controlled independent of other power domains, for example, the audio module (including I2S, DMIC, AMIC) can be independently powered on or powered down irrespective of other modules such as power management module, clock, and etc.*
- *The BLE/802.15.4/2.4GHz Radio, USB and Audio (I2S, DMIC, AMIC) are powered down by default.*
- *The power management module and clock should be always powered on, even in deep sleep.*
- *In deep sleep, except for the power management and clock, all other modules should be powered down.*

The TLSR8271 integrates a power-balanced 32-bit MCU, BLE/2.4GHz Radio, 64kB (16k+16k+32k) SRAM, 512kB internal Flash, single-channel analog microphone input, dual-channel digital microphone input, stereo audio output, 6-channel PWM (1-channel IR/IR FIFO/IR DMA FIFO), one quadrature decoder (QDEC), abundant and flexible GPIO interfaces, and nearly all the peripherals needed for IoT (Internet of Things) and HID (Human Interface Devices) application development (e.g. Bluetooth Low Energy). The TLSR8271 also includes multi-stage power management design allowing ultra-low power operation and making it the ideal candidate for wearable and power-constraint applications.

With the high integration level of TLSR8271, few external components are needed to satisfy customers' ultra-low cost requirements.

1.2 Key Features

1.2.1 General Features

General features are as follows:

1. 4-byte Chip UID (Unique ID).
2. Embedded 32-bit proprietary microcontroller.
   - ✧ Better power-balanced performance than ARM M0
   - ✧ Instruction cache controller
   - ✧ Maximum running speed up to 48MHz
3. Program memory: internal 512kB Flash.
4. Data memory: 64kB on-chip SRAM
   - ✧ Up to 32kB SRAM with retention in deep sleep
   - ✧ One 32kB SRAM without retention in deep sleep.
5. RTC and other timers:
   - ✧ Clock source of 24MHz and 32kHz/24MHz embedded RC oscillator
   - ✧ Three general 32-bit timers with four selectable modes in active mode
   - ✧ Watchdog timer
   - ✧ A low-frequency 32kHz timer available in low power mode
6. A rich set of I/Os:
   - ✧ Up to 14 GPIOs. All digital IOs can be used as GPIOS.
   - ✧ Dual-channel DMIC (Digital Mic).
   - ✧ Single-channel AMIC (Analog Mic).
   - ✧ I2S.
   - ✧ Stereo Audio output.
   - ✧ SPI.
   - ✧ UART with hardware flow control and 7816 protocol support.
   - ✧ USB.
   - ✧ Swire debug Interface.
   - ✧ Manchester decoder interface selectable as wakeup source
7. Up to 6 channels of differential PWM:
   - ✧ PWM1~PWM5: 5-channel normal PWM output.
   - ✧ PWM0: 1 channel with normal mode as well as additional IR/IR FIFO/IR DMA FIFO mode for IR generation.
8. Sensor:
   - ✧ 14bit 10-channel (only GPIO input) SAR ADC
   - ✧ Temperature sensor
9. One quadrature decoder.
10. Embedded hardware AES and AES-CCM.
11. Embedded hardware acceleration for Elliptical curve cryptography (ECC), supports Bluetooth standard up to and including BLE5.0.
12. Embedded low power comparator.
13. Embedded TRNG (True Random Number Generator).
14. Operating temperature range:
    - ✧ ET version: -40℃~+85℃

- ✧ AT version: -40℃~+125℃

15. Supports all 2.4GHz IoT standards into a single SoC, including BLE, BLE Mesh, ANT, and 2.4GHz proprietary technologies without the requirement for an external DSP.

1.2.2 RF Features

RF features include:

1. BLE/2.4GHz RF transceiver embedded, working in worldwide 2.4GHz ISM band.
2. Bluetooth 5.1 Compliant, 1Mbps, 2Mbps, Long Range 125kbps and 500kbps.
3. 2.4GHz proprietary 1Mbps/2Mbps/250kbps/500kbps mode with Adaptive Frequency Hopping feature support.
   - ✧ Support flexible GFSK/FSK modulation index configuration
   - ✧ Support 1-N receiver capability
4. Automatic Rate Detection mode
   - ✧ 2.4GHz 250kbps standard mode with packet format
   - ✧ High data rate modes up to 2Mbps, e.g. 500kbps, 1Mbps, 2Mbps, with the same packet header
5. ANT mode.
6. Rx Sensitivity: -96.5dBm@BLE 1Mbps(estimated), -100dBm@ IEEE802.15.4 250kbps(estimated), -94dBm @ BLE 2Mbps mode(estimated), -99dBm @ BLE 500kbps mode(estimated), -101dBm @ BLE 125kbps mode(estimated).
7. Tx output power: up to +10dBm.
8. Single-pin antenna interface.
9. RSSI monitoring with +/-1dB resolution.
10. Auto acknowledgment, retransmission and flow control.
11. Support full-function BLE AoA and AoD location features.
12. Integrated load inductor.
13. PTA interface with 2/3/4-wire support.

1.2.3 Features of Power Management Module

Features of power management module include:

1. Embedded LDO and DCDC.
   - ✧ DCDC for 1.8V flash with bypass LDO
   - ✧ DCDC for chip with bypass LDO
   - ✧ USB LDO with power supply of 4.5V~5.5V
2. Battery monitor: Supports low battery detection.
3. Power supply: 1.8V~3.6V. USB 4.5V ~ 5.5V
4. Multiple stage power management to minimize power consumption.
5. Low power consumption:
   - ✧ Whole Chip RX mode: 5.3mA with DCDC, 10mA with LDO
   - ✧ Whole Chip TX mode @ 0dBm: 4.8mA with DCDC, 9.5mA with LDO

- ✧ Deep sleep with external wakeup (without SRAM retention): 0.4uA
- ✧ Deep sleep with SRAM retention: 1uA (with 16kB SRAM retention), 1.4uA (with 32kB SRAM retention)

1.2.4 USB Features

USB features include:

1. Compatible with USB2.0 Full speed mode.
2. Supports 9 endpoints including control endpoint 0 and 8 configurable data endpoints.
3. Independent power domain.
4. Supports ISP (In-System Programming) via USB port.

1.2.5 Flash Features

The TLSR8271 embeds Flash with features below:

1. Total 512kB (4Mbits).
2. Flexible architecture: 4kB per Sector, 64kB/32kB per block.
3. Up to 256 Bytes per programmable page.
4. Write protect all or portions of memory.
5. Sector erase (4kB).
6. Block erase (32kB/64kB).
7. Cycle Endurance: 100,000 program/erases.
8. Data Retention: typical 20-year retention.
9. Multi firmware encryption methods for anti-cloning protection.

1.2.6 BLE Features

1. Fully compliant with Bluetooth 5.1
2. Bluetooth SIG Mesh support
3. Telink proprietary Mesh support
4. BLE AoA/AoD location and up to 8-antenna indoor positioning support
5. Telink extended profile with audio support for voice command based searches

1.2.7 BLE Mesh Features

BLE Mesh features include:

1. Compatible with Bluetooth SIG Mesh specification 1.0, with additional features from Telink enhanced design.
2. Support flexible mesh control, e.g. N-to-1 and N-to-M.
3. Supports switch control for over 200 nodes without delay.
4. Supports real time status update for over 200 nodes.
5. Secure and safe control and scalable identification within network.

6. 8/16 groups can be controlled at the same time.
7. 128/256 nodes within mesh network.
8. Configurable to more or fewer hops (e.g. 4 hops) within mesh network, single hop delay less than 15ms.
9. Flexible RF channel usage with both BLE advertising channels and data channels for good anti-interference performance.

1.2.8 Concurrent Mode Feature

In concurrent mode, the chip supports multiple standard working concurrently.

Typical combination is BLE and 2.4G based stacks can run concurrently with one application state but dual radio communication channels for interacting with different devices.

1.3 Typical Applications

The TLSR8271 can be applied to IoT (Internet of Things) and HID (Human Interface Devices) applications, such as BLE smart devices, BLE mesh devices, and 2.4GHz. Its typical applications include, but are not limited to the following:

- ✧ Smartphone and tablet accessories;
- ✧ RF Remote Control;
- ✧ Sports and fitness tracking;
- ✧ Wearable devices;
- ✧ Wireless toys;
- ✧ Smart Lighting, Smart Home devices;
- ✧ Building Automation;
- ✧ Smart Grid;
- ✧ Intelligent Logistics/Transportation/City;
- ✧ Consumer Electronics；
- ✧ Industrial Control;
- ✧ Health Care.

1.4 Ordering Information

Table 1-1 Ordering Information of the TLSR8271

Product Series	Package Type	Temperature Range	Product Part No.	Packing Method	Minimum Order Quantity
TLSR8271F512	32-pin TQFN 5x5x0.75mm	-40℃~+85℃	TLSR8271F512ET32	TR	3000

Product Series	Package Type	Temperature Range	Product Part No.	Packing Method	Minimum Order Quantity
	24-pin TQFN 4x4x0.75mm	-40℃~+85℃	TLSR8271F512ET24	TR	3000

Note：

- *1: MSL (Moisture Sensitivity Level): The 8271 series is applicable to MSL3 (Based on JEDEC Standard J-STD-020).*
  - ✧ *After the packing opened, the product shall be stored at <30℃/ <60%RH and the product shall be used within 168 hours.*
  - ✧ *When the color of the indicator in the packing changed, the product shall be baked before soldering.*
  - ✧ *If baking is required, please refer to IPC/JEDEC J-STD-033 for baking procedure.*
- *2: Packing method "TR" means tape and reel. The tape and reel material DO NOT support baking under high temperature.*

1.5 Package

Package dimension of TLSR8271F512ET32 is shown below.

Figure 1-2 Package of TLSR8271F512ET32

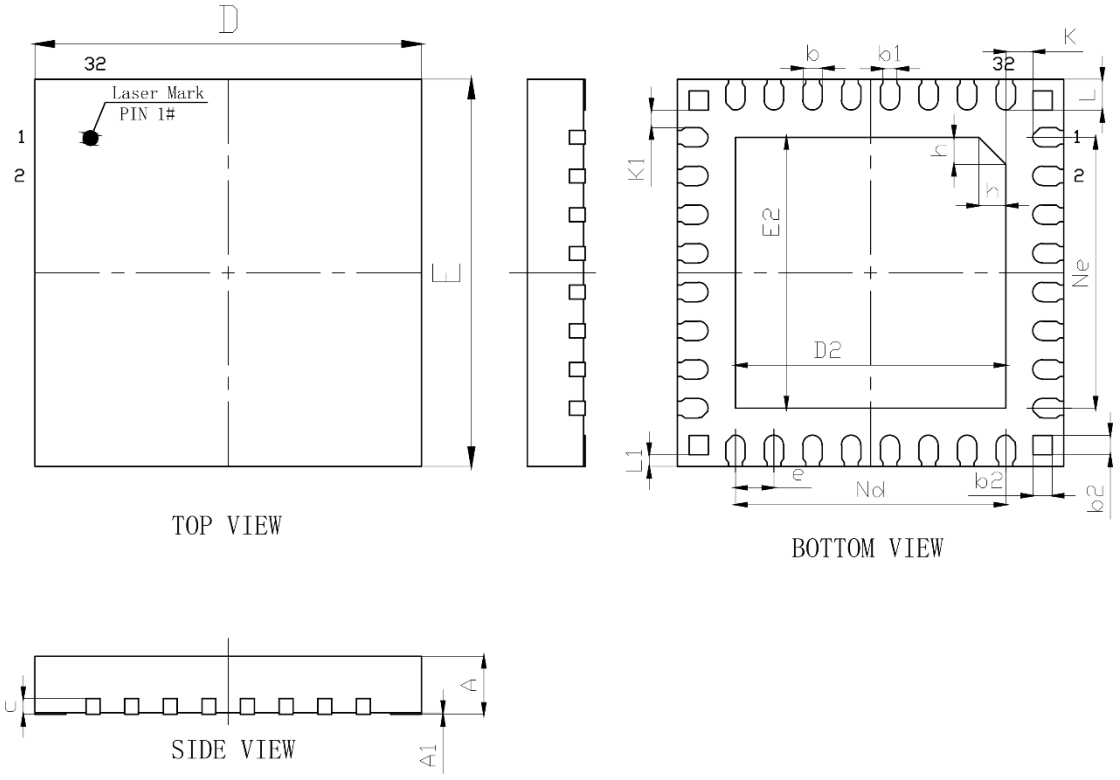


Table 1-2 Mechanical Dimension of TLSR8271F512ET32

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0. 70	0.75	0. 80
A1	0. 00	0.02	0. 05
b	0. 20	0. 25	0. 30
b1	0. 18REF		
b2	0. 20	0. 25	0. 30
c	0. 203REF		
D	4. 90	5. 00	5. 10
D2	3. 40	3. 50	3. 60
e	0. 50BSC		
Nd	3. 50BSC		
Ne	3. 50BSC		
E	4. 90	5. 00	5. 10
E2	3. 40	3. 50	3. 60
L	0. 35	0.40	0. 45
L1	0.15REF		
h	0.30	0.35	0.40
K	0.30	0.35	0.40
K1	0.225REF		

Package dimension of TLSR8271F512ET24 is shown below.

Figure 1-3 Package of TLSR8271F512ET24

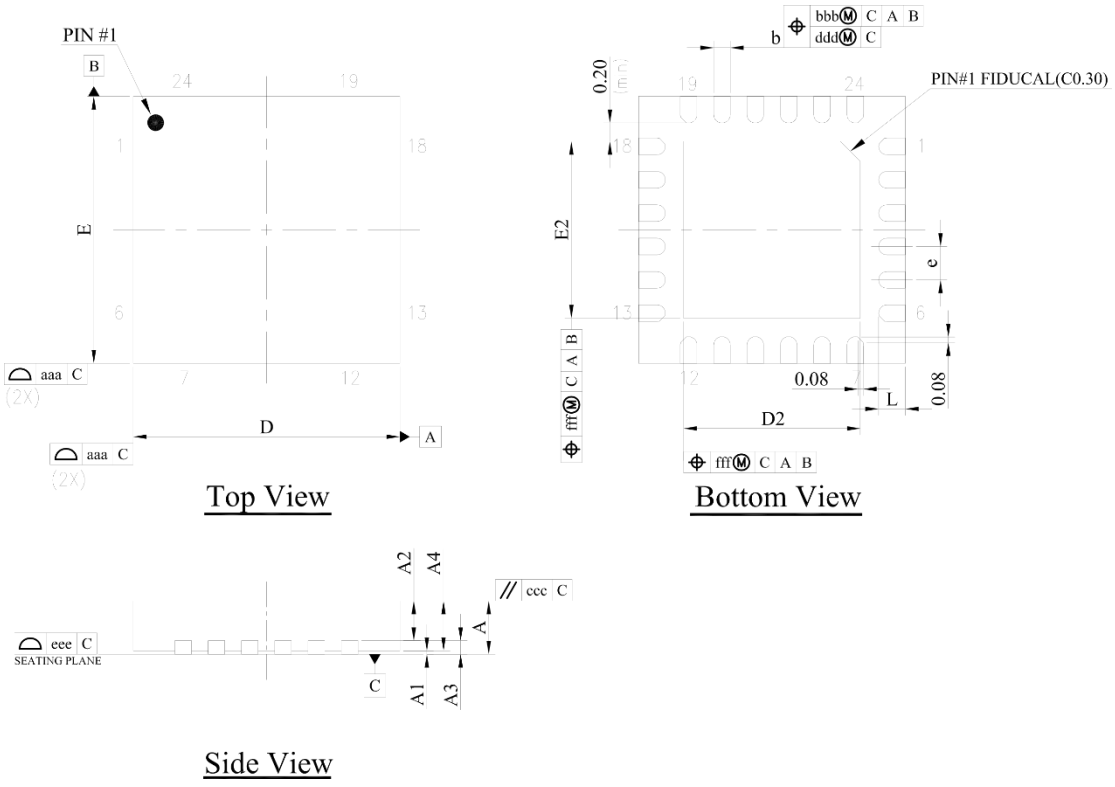


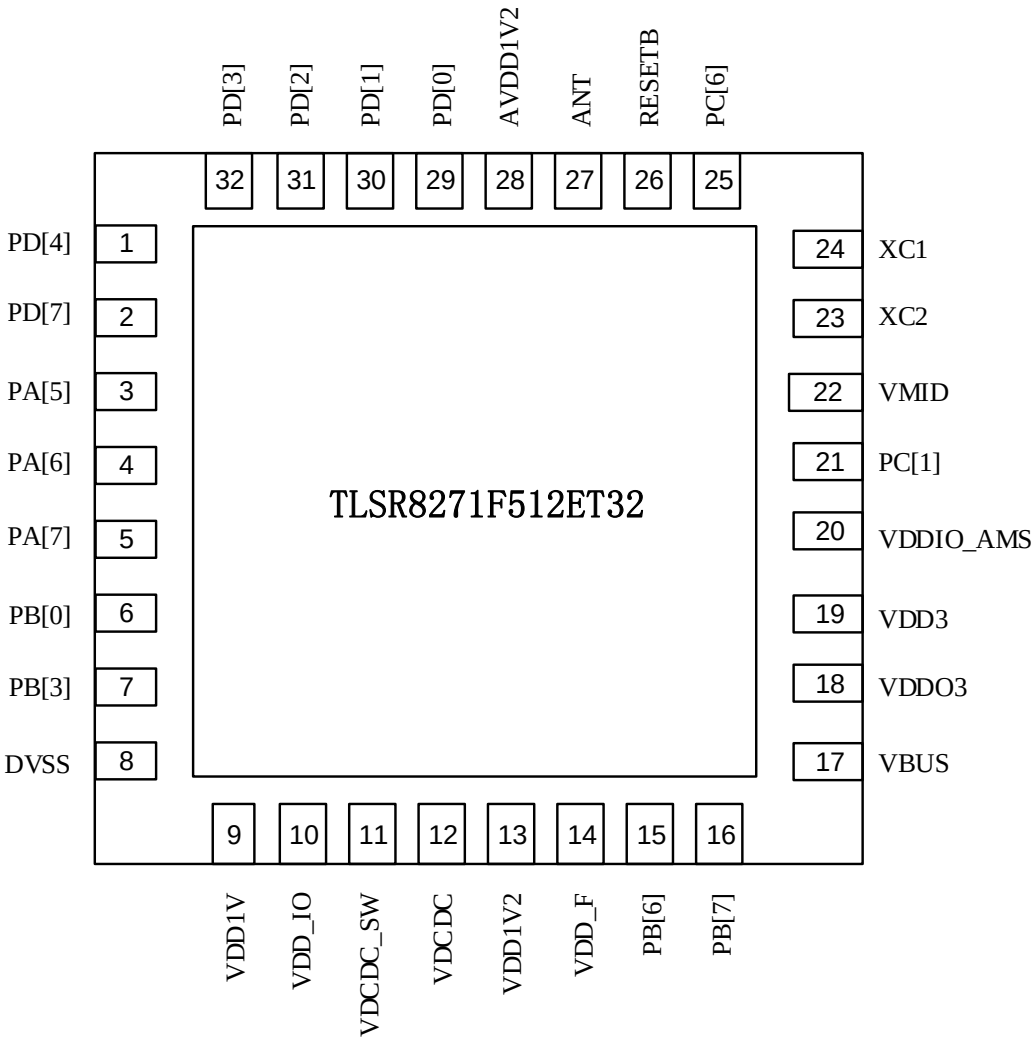
Table 1-3 Mechanical Dimension of TLSR8271F512ET24

ITEM		Symbol	DIMENSION(mm)		
			MIN.	NOM.	MAX.
Total height		A	0.70	0.75	0.80
Stand off		A1	0	0.02	0.05
Mold thickness		A2	0.53	0.55	0.56
Leadframe thickness		A3	---	0.20REF	---
Mold+Leadframe thickness+Mold gap		A4	0.70	0.73	0.80
Lead width		b	0.18	0.25	0.30
Package size	X	D	3.90	4.00	4.10
	Y	E	3.90	4.00	4.10
E-PAD Size	X	D2	2.55	2.65	2.75
	Y	E2	2.55	2.65	2.75
Lead length		L	0.35	0.40	0.45
Lead pitch		e	---	0.50BSC	---
Package profile of a surface		aaa	0.15		
Lead position		bbb	0.10		
Paralleliam		ccc	0.10		
Lead position		ddd	0.05		
Package profile of a surface		eee	0.08		
Epad position		fff	0.10		

1.6 Pin Layout

Pin assignment for TLSR8271F512ET32 is shown below.

Figure 1-4 Pin Assignment for TLSR8271F512ET32



Functions of 32 pins for TLSR8271F512ET32 are described in table below:

Table 1-4 Pin Function of TLSR8271F512ET32

No	Pin Name	Type	Description
1	PD[4]	GPIO	GPIO PD[4]
2	PD[7]	GPIO	GPIO PD[7]
3	PA[5]	GPIO	GPIO PA[5]
4	PA[6]	GPIO	GPIO PA[6]
5	PA[7]	GPIO	GPIO PA[7]
6	PB[0]	GPIO	GPIO PB[0]
7	PB[3]	GPIO	GPIO PB[3]
8	DVSS	GND	Digital LDO ground
9	VDD1V	PWR	Internal LDO generated power supply input for digital core

No	Pin Name	Type	Description
10	VDD_IO	PWR	External 3.3V power supply input for IO
11	VDCDC_SW	Analog	Connected with VDCDC via external inductor
12	VDCDC	Analog	Connected with VDCDC_SW via external inductor
13	VDD1V2	PWR	Internal DCDC generated power supply. Connect to GND via external capacitor. Route this 1.2V voltage power supply to AVDD1V2.
14	VDD_F	PWR	Internally generated power supply to flash. Connect to GND via external capacitor.
15	PB[6]	GPIO	GPIO PB[6]
16	PB[7]	GPIO	GPIO PB[7]
17	VBUS	PWR	USB 5V supply
18	VDDO3	PWR	Connect to an external 3.3V power supply
19	VDD3	PWR	Connect to an external 3.3V power supply
20	VDDIO_AMS	PWR	Connect to an external 3.3V power supply
21	PC[1]	GPIO	GPIO PC[1]
22	VMID	Analog	Audio pin connecting to external decap
23	XC2	Analog	Crystal oscillator pin
24	XC1	Analog	Crystal oscillator pin
25	PC[6]	GPIO	GPIO PC[6]
26	RESETB	Reset	Power on reset, active low
27	ANT	Analog	Pin to connect to the Antenna through the matching network
28	AVDD1V2	PWR	Supply for the radio IP
29	PD[0]	GPIO	GPIO PD[0]
30	PD[1]	GPIO	GPIO PD[1]
31	PD[2]	GPIO	GPIO PD[2]
32	PD[3]	GPIO	GPIO PD[3]

GPIO pin multi-functions of TLSR8271F512ET32 are shown below.

Table 1-5 GPIO Pin Mux of TLSR8271F512ET32

Pad	Default	Func1	Func2	Func3	Func4
PA[5]	GPIO	/	/	DM	
PA[6]	GPIO	/	/	DP(SWS)	
PA[7]	SWS	/	UART_RTS	SWS	
PB[0]	GPIO	ATSEL1	UART_RX	PWM3	lc_comp_ain<0>/sar_aio<0>
PB[3]	GPIO	TX_CYC2PA	UART_RTS	PWM0_N	lc_comp_ain<3>/sar_aio<3>

Pad	Default	Func1	Func2	Func3	Func4
PB[6]	SPI_DI	UART_RTS	SPI_DI/SDA	SDM_P1	lc_comp_ain<6>/sar_aio<6>
PB[7]	SPI_DO	UART_RX	SPI_DO	SDM_N1	lc_comp_ain<7>/sar_aio<7>/MDEC
PC[1]	GPIO	PWM0	PWM1_N	I2C_SCK	
PC[6]	GPIO	PWM4_N	ATSEL1	RX_CYC2LNA	
PD[0]	GPIO	7816_TRX/UART_TX		RX_CYC2LNA	PS_PE<1>/MDEC
PD[1]	GPIO	UART_CTS		TX_CYC2PA	PS_PE<2>
PD[2]	SPI_CN	PWM3	I2S_LR	SPI_CN	
PD[3]	GPIO	7816_TRX/UART_TX	I2S_SDI	PWM1_N	
PD[4]	GPIO	PWM2_N	I2S_SDO	SWM	
PD[7]	SPI_CK	7816_TRX/UART_TX	I2S_BCK	SPI_CK/SCL	PS_PE<3>

Descriptions of each signal are listed in Table 1-6 to Table 1-20.

Table 1-6 PWM Signal Description

Signal	Type	Description
PWM0	DO	PWM channel 0 output
PWM0_N	DO	PWM channel 0 inversion output
PWM1_N	DO	PWM channel 1 inversion output
PWM2_N	DO	PWM channel 2 inversion output
PWM3	DO	PWM channel 3 output
PWM4_N	DO	PWM channel 4 inversion output

Table 1-7 I2C Signal Description

Signal	Type	Description
I2C_SCK	DIO	I2C SCL

Table 1-8 I2S Signal Description

Signal	Type	Description
I2S_BCK	DO	I2S bit CLK

Signal	Type	Description
I2S_LR	DO	I2S left and right channel SEL
I2S_SDI	DI	I2S data IN
I2S_SDO	DO	I2S data OUT

Table 1-9 UART Signal Description

Signal	Type	Description
UART_CTS	DI	UART Clear to Send signal
UART_RTS	DO	UART Ready to Send signal
UART_RX	DI	UART RX
UART_TX	DO	UART TX

Table 1-10 Audio Output Signal Description

Signal	Type	Description
SDM_N1	DO	SDM1 diff output
SDM_P1	DO	SDM1 diff output

Table 1-11 SPI Signal Description

Signal	Type	Description
SPI_CK	DIO	SPI CLK
SPI_CN	DIO	SPI CN
SPI_DI	DIO	SPI DI
SPI_DO	DIO	SPI DO

Table 1-12 7816 Signal Description

Signal	Type	Description
7816_TRX	DIO	7816 TRX

Table 1-13 SWIRE Signal Description

Signal	Type	Description
SWM	DIO	swire master
SWS	DIO	swire slave

Table 1-14 AOA/AOD Signal Description

Signal	Type	Description
ATSEL1	DO	Antena select signal 1

Table 1-15 External Power Amplifier, Low Noise Amplifier Signal

Signal	Type	Description
RX_CYC2LNA	DO	External low noise amplifier
TX_CYC2PA	DO	External power amplifier

Table 1-16 USB Signal Description

Signal	Type	Description
DP	DIO	USB DP
DM	DIO	USB DM

Table 1-17 DECODEC Signal Description

Signal	Type	Description
MDEC	DIt	Manchester Decodec

Table 1-18 Low Current Comparator Signal Description

Signal	Type	Description
lc_comp_ain<0>	AI	low current comparator channel 0
lc_comp_ain<3>	AI	low current comparator channel 3
lc_comp_ain<6>	AI	low current comparator channel 6
lc_comp_ain<7>	AI	low current comparator channel 7

Table 1-19 SAR ADC Signal Description

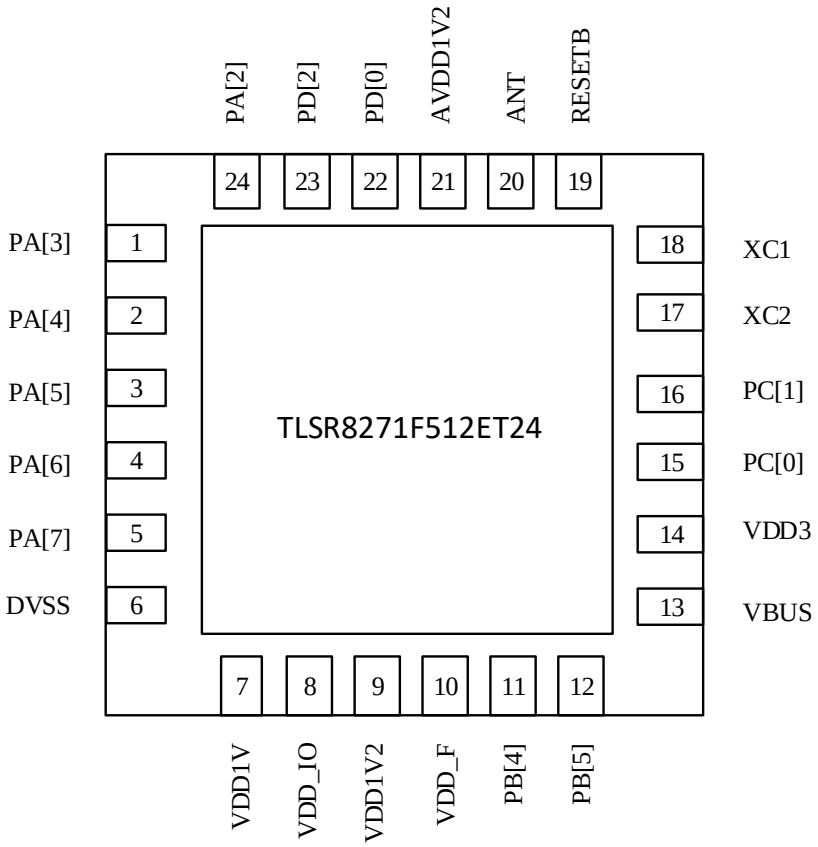
Signal	Type	Description
sar_aio<0>	AI	SAR ADC input channel 0
sar_aio<3>	AI	SAR ADC input channel 3
sar_aio<6>	AI	SAR ADC input channel 6
sar_aio<7>	AI	SAR ADC input channel 7

Table 1-20 Strong Pull Up Signal Description

Signal	Type	Description
PS_PE<1>	AO	strong pull up 1 enable
PS_PE<2>	AO	strong pull up 2 enable
PS_PE<3>	AO	strong pull up 3 enable

Pin assignment of TLSR8271F512ET24 is shown below:

Figure 1-5 Pin Assignment for TLSR8271F512ET24



Functions of 24 pins for TLSR8271F512ET24 are described in table below:

Table 1-21 Pin Function of TLSR8271F512ET24

No	Pin Name	Type	Description
1	PA[3]	GPIO	GPIO PA[3]
2	PA[4]	GPIO	GPIO PA[4]
3	PA[5]	GPIO	GPIO PA[5]
4	PA[6]	GPIO	GPIO PA[6]
5	PA[7]	GPIO	GPIO PA[7]
6	DVSS	GND	Digital LDO ground
7	VDD1V	PWR	Internal LDO generated power supply input for digital core
8	VDD_IO	PWR	External 3.3V power supply input for IO
9	VDD1V2	PWR	Internal DCDC generated power supply. Connect to GND via external capacitor. Route this 1.2V voltage power supply to AVDD1V2.
10	VDD_F	PWR	Internally generated power supply to flash. Connect to GND via external capacitor.
11	PB[4]	GPIO	GPIO PB[4]
12	PB[5]	GPIO	GPIO PB[5]

No	Pin Name	Type	Description
13	VBUS	PWR	USB 5V supply
14	VDD3	PWR	Connect to an external 3.3V power supply
15	PC[0]	GPIO	GPIO PC[0]
16	PC[1]	GPIO	GPIO PC[1]
17	XC2	Analog	Crystal oscillator pin
18	XC1	Analog	Crystal oscillator pin
19	RESETB	Reset	Power on reset, active low
20	ANT	Analog	Pin to connect to the Antenna through the matching network
21	AVDD1V2	PWR	Supply for the radio IP
22	PD[0]	GPIO	GPIO PD[0]
23	PD[2]	GPIO	GPIO PD[2]
24	PA[2]	GPIO	GPIO PA[2]

GPIO pin multi-functions of TLSR8271F512ET24 are shown below.

Table 1-22 GPIO Pin Mux of TLSR8271F512ET24

Pad	Default	Func1	Func2	Func3	Func4
PA[2]	GPIO	PWM0	UART_TX	DO	
PA[3]	GPIO	PWM1	UART_CTS	DI/SDA	
PA[4]	GPIO	PWM2	UART_RTS	CK/SCL	
PA[5]	GPIO	/	/	DM	
PA[6]	GPIO	/	/	DP(SWS)	
PA[7]	SWS	/	UART_RTS	SWS	
PB[4]	GPIO	/	PWM4	SDM_P0	lc_comp_ain<4>/sar_aio<4>
PB[5]	GPIO	/	PWM5	SDM_N0	lc_comp_ain<5>/sar_aio<5>
PC[0]	GPIO	UART_RTS	PWM4_N	I2C_SDA	
PC[1]	GPIO	PWM0	PWM1_N	I2C_SCK	
PD[0]	GPIO	7816_TRX/UART_TX	/	RX_CYC2LNA	PS_PE<1>/MDEC
PD[2]	SPI_CN	PWM3	I2S_LR	SPI_CN	

Descriptions of each signal are listed in Table 1-23 to Table 1-36.

Table 1-23 PWM Signal Description

Signal	Type	Description
PWM0	DO	PWM channel 0 output
PWM1	DO	PWM channel 1 output
PWM1_N	DO	PWM channel 1 inversion output

Signal	Type	Description
PWM2	DO	PWM channel 2 output
PWM3	DO	PWM channel 3 output
PWM4	DO	PWM channel 4 output
PWM4_N	DO	PWM channel 4 inversion output
PWM5	DO	PWM channel 5 output

Table 1-24 I2C Signal Description

Signal	Type	Description
I2C_SDA	DIO	I2C SDA
I2C_SCK	DIO	I2C SCK

Table 1-25 I2S Signal Description

Signal	Type	Description
I2S_LR	DO	I2S left and right channel SEL

Table 1-26 UART Signal Description

Signal	Type	Description
UART_CTS	DI	UART Clear to Send signal
UART_RTS	DO	UART Ready to Send signal
UART_TX	DO	UART TX

Table 1-27 Audio Output Signal Description

Signal	Type	Description
SDM_N0	DO	SDM0 diff output
SDM_P0	DO	SDM0 diff output

Table 1-28 SPI Signal Description

Signal	Type	Description
SPI_CN	DIO	SPI CN

Table 1-29 7816 Signal Description

Signal	Type	Description
7816_TRX	DIO	7816 TRX

Table 1-30 SWIRE Signal Description

Signal	Type	Description
SWS	DIO	swire slave

Table 1-31 External Power Amplifier, Low Noise Amplifier Signal

Signal	Type	Description
RX_CYC2LNA	DO	External low noise amplifier

Table 1-32 USB Signal Description

Signal	Type	Description
DP	DIO	USB DP
DM	DIO	USB DM

Table 1-33 DECODEC Signal Description

Signal	Type	Description
MDEC	DIt	Manchester Decodec

Table 1-34 Low Current Comparator Signal Description

Signal	Type	Description
lc_comp_ain<4>	AI	low current comparator channel 4
lc_comp_ain<5>	AI	low current comparator channel 5

Table 1-35 SAR ADC Signal Description

Signal	Type	Description
sar_aio<4>	AI	SAR ADC input channel 4
sar_aio<5>	AI	SAR ADC input channel 5

Table 1-36 Strong Pull Up Signal Description

Signal	Type	Description
PS_PE<1>	AO	strong pull up 1 enable

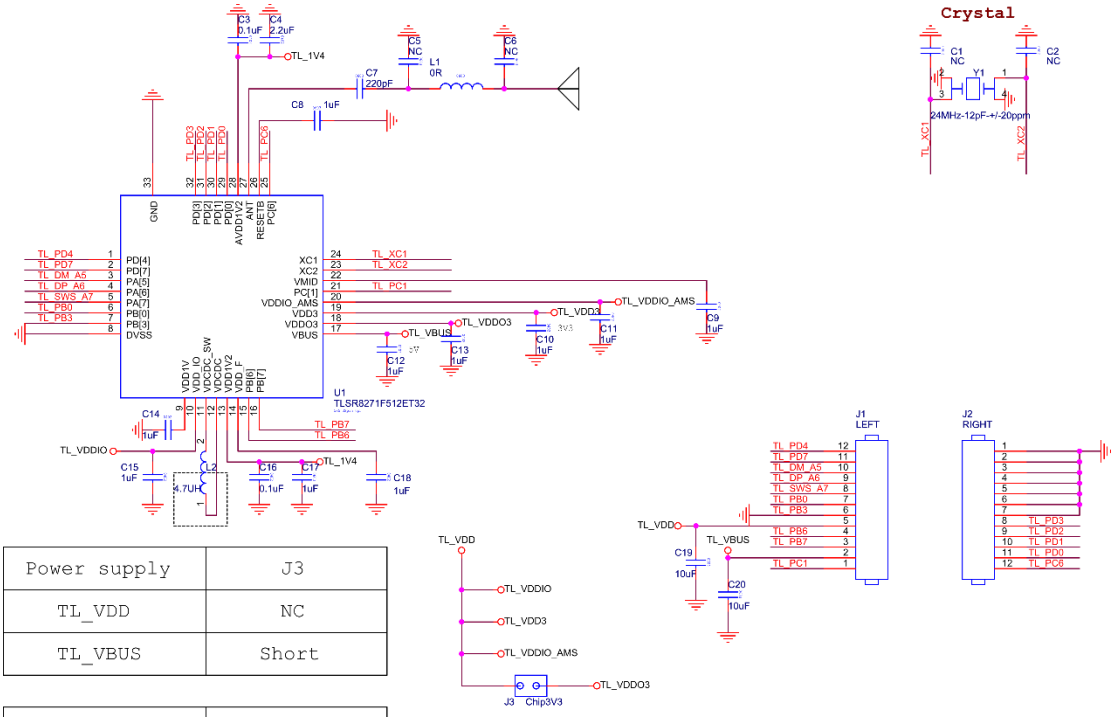
Note:

- DI: Digital input
- DO: Digital output
- DIO: Digital input/output
- AI: Analog input
- AO: Analog output
- AIO: Analog input/output

2. Reference Design

2.1 Schematic of TLSR8271F512ET32

Figure 2-1 Schematic of TLSR8271F512ET32



Power supply	J3
TL_VDD	NC
TL_VBUS	Short

DC-DC MODE	L2=4.7uH
LDO MODE	L2=NC

2.2 BOM(Bill of Material) of TLSR8271F512ET32

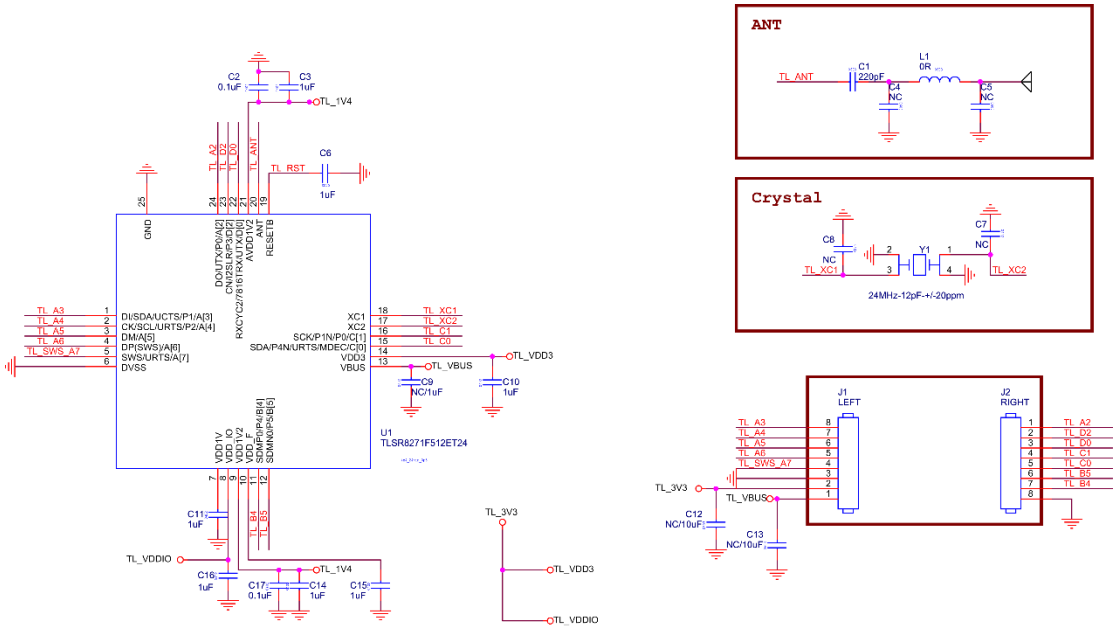
Table 2-1 BOM Table of TLSR8271F512ET32

Quantity	Reference	Value	Description	PCB Footprint
4	C1,C2,C5,C6	N.C.	Not mounted	0402
2	C3,C16	0.1uF	Capacitance,X5R,±10%	0402
1	C4	2.2uF	Capacitance,X5R,±10%	0402
1	C7	220pF	Capacitance,X7R,±10%	0402
10	C8,C9,C10,C11,C12,C13,C14,C15,C17,C18	1uF	Capacitance,X5R,±10%	0402
2	C19,C20	10uF	Capacitance,X5R,±10%	0603
1	J1	LEFT	Pin headers	hdr254f-1x12x850
1	J2	RIGHT	Pin headers	hdr254f-1x12x850
1	J3	Chip3V3	Pin headers	hdr254f-1x2x850

Quantity	Reference	Value	Description	PCB Footprint
1	L1	0R	Resistance,5%	0402
1	L2	4.7UH	High frequency chip inductor,SMD,20%	2.5x2.0x1.2mm
1	U1	TLSR8271F512ET32	BLE+2.4G RFID	QFN-32
1	Y1	24MHz	XTAL SMD 3225,24 MHz,Cl=12pF,total tol.±20ppm	XTAL_3225

2.3 Schematic of TLSR8271F512ET24

Figure 2-2 Schematic of TLSR8271F512ET24



Power supply	
TL_3V3	C9=C13=NC
TL_VBUS	C9=1uF;C13=10uF

2.4 BOM(Bill of Material) of TLSR8271F512ET24

Table 2-2 BOM Table of TLSR8271F512ET24

Quantity	Designator	Value	Description	PCB Footprint
1	C1	220pF	Capacitance,X7R,±10%	0402
2	C2,C17	0.1uF	Capacitance,X5R,±10%	0402
7	C3,C6,C10,C11, C14,C15,C16	1uF	Capacitance,X5R,±10%	0402
4	C4,C5,C7,C8	N.C.	Not mounted	0402
1	C9	N.C./1uF	Capacitance,X5R,±10%	0402

Quantity	Designator	Value	Description	PCB Footprint
2	C12,C13	N.C./10uF	Capacitance,X5R,±10%	0402
1	J1	LEFT	Pin headers	hdr254f-1x8x850
1	J2	RIGHT	Pin headers	hdr254f-1x8x850
1	L1	0R	Resistance,5%	0402
1	U1	TLSR8271F512ET24	BLE	QFN-24
1	Y1	24MHz	XTAL SMD 3225,24 MHz,Cl=12pF,total tol.±20ppm	XTAL_3225