Application Note：
TLSR8x5x Hardware Design Guide

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Brief 简介：

This document presents the checklist for hardware design based on Telink TLSR8x5x series SoCs.

本文档是基于泰凌 TLSR8x5x 系列芯片的硬件设计的检查清单。

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Revision History 修订记录

Version 版本	Major Changes 主要修订	Date 日期	Author 作者
1.0.0	Initial release 初始版本	2018/11	LX, Cynthia
1.1.0	Updated section 2.5 AMIC application pins. 更新 2.5 节 AMIC 应用管脚。	2018/12	LX, Cynthia
1.2.0	Updated section 2.9 UART pins. 更新 2.9 UART 管脚。	2019/2	LX, TJB, Cynthia

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1 Brief Introduction(简介)

This document presents the checklist for hardware design based on Telink TLSR8x5x series SoCs. For details about configurations and notes, please refer to corresponding Datasheet, SDK and Errata.

本文档是基于泰凌 TLSR8x5x 系列芯片的硬件设计的检查清单。具体配置及注意事项，请参考对应型号的 Datasheet、SDK 和 Errata。

2 Hardware Design Checklist (硬件设计检查清单)

2.1 GPIO pull-up/pull-down and wakeup (GPIO 上下拉与唤醒)

1) All GPIO pins have configurable pull-up resistor (two ranks) and pull-down resistor (one rank).

   所有 GPIO 管脚均有可配置的上拉电阻（两档）与下拉电阻（一档）。

2) All GPIO pins can be independently configured as high-level/low-level wakeup source.

   所有 GPIO 管脚均可独立配置高/低电平唤醒。

3) Actual test shows that after wakeup from deep sleep, PortC (PC0~PC7) may have about -1.4V noise for several hundred nanoseconds. Therefore, in actual applications, generally it's recommended not to use PortC (PC0~PC7) as output or control function, unless extraly using external filtering capacitor (e.g. 1uF).

   实际测试中发现，PC0~PC7 管脚在从 deep 状态醒来时存在约为-1.4V 的下拉毛刺，毛刺宽度为数百 ns。因此，应用层面不建议将 PortC（PC0~PC7）作为输出和控制使用。如果确认需要使用 PC0~PC7 作为输出和控制管脚使用，那么可以考虑外加滤波电容，例如 1uF。

2.2 PWM pins (脉宽调制模块输出管脚)

The TLSR8x5x supports up to six PWM output channels. Each PWMx (x=0~5) has its corresponding inverted output at PWMxN pin. For the convenience of PCB design, the TLSR8x5x supports multiple GPIOs with multiplexed PWM output function. Following shows the GPIO pins with multiplexed PWM function.

芯片 PWM 总共有 6 路 PWM 管脚，其中 PWMx(x=0~5)和 PWMxN 代表为互反的一对信号。为了便于 PCB 设计，TLSR8x5x 有多个管脚可以复用为 PWM 输出管脚。支持 PWM 复用功能的 GPIO 管脚如下所示：

1) PWM0 output pin: PA2, PC2; PWM0N output pin: PA0, PB3, PC4; PWM0/PWM0N multiplexed output pin: PD5

   PWM0 输出管脚：PA2，PC2；PWM0N 输出管脚：PA0，PB3，PC4；PWM0/PWM0N 共同输出管脚：PD5

2) PWM1 output pin: PA3, PC3; PWM1N output pin: PC1, PD3

   PWM1 输出管脚：PA3，PC3；PWM1N 输出管脚：PC1，PD3

3) PWM2 output pin: PA4, PC4; PWM2N output pin: PD4

   PWM2 输出管脚：PA4, PC4；PWM2N 输出管脚：PD4

4) PWM3 output pin: PB0, PD2; PWM3N output pin: PC5

   PWM3 输出管脚：PB0, PD2；PWM3N 输出管脚：PC5

5) PWM4 output pin: PB1, PB4; PWM4N output pin: PC0, PC6

   PWM4 输出管脚：PB1，PB4；PWM4N 输出管脚：PC0，PC6

6) PWM5 output pin: PB2, PB5; PWM5N output pin: PC7

   PWM5 输出管脚：PB2，PB5；PWM5N 输出管脚：PC7

2.3 IR drive pins (IR 驱动管脚)

1) PWM0 pins, including PWM0 and PWM0N, can be used as IR driver pin function.
PWM0 管脚（含 PWM0 和 PWM0N）可用于驱动 IR。

2.4 SDM output pins (SDM 输出管脚)

1) Two groups of SDMP/SDMN output pins: PB4/PB5 (SDMP0/SDMN0), PB6/PB7 (SDMP1/SDMN1)
两组 SDMP/SDMN 输出管脚：PB4/PB5（SDMP0/SDMN0），PB6/PB7（SDMP1/SDMN1）

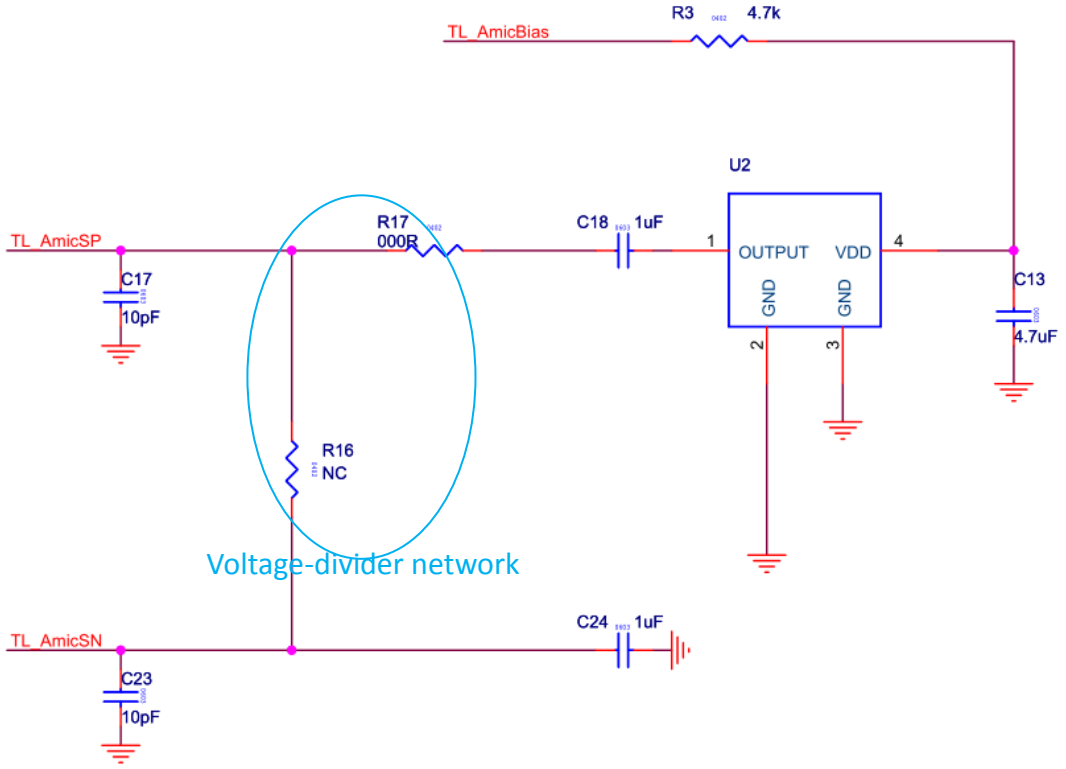
2.5 AMIC application pins (AMIC 应用管脚)

1) AMIC (Analog MIC) adopts differential input by default.
AMIC（模拟麦克风）默认采用差分输入

2) PC0~PC3 can be configured as SN/SP. Considering current reference design, PC0 and PC1 are fixed as SN and SP, and PC4 is fixed as AmicBias.
PC0~PC3 都可任意配置成 SN/SP。考虑到目前的参考设计，将 PC0、PC1 固定为 SN、SP，PC4 固定为 AmicBias。

3) AMIC serves to convert voice signal to electrical signal, and the amplitude of electrical signal is determined by its sensitivity parameter. Full amplitude of the TLSR8x5x-embedded ADC is about 40mV; therefore, when maximum AMIC sensitivity does not exceed -28dBV/Pa, or signal amplitude is equal to or less than 40mV, no voltage-divider network is needed for MIC signal channel; when maximum AMIC sensitivity exceeds -28dBV/Pa, or signal amplitude is larger than 40mV, MIC signal channel should adopt voltage-divider network, so as to avoid ADC saturation. When selecting voltage dividing ratio, it's better to ensure maximum amplitude of electrical signal from AMIC to chip is close to 40mV. Following shows the structure of voltage-divider network for reference.

AMIC用于将声音信号转换为电信号，且电信号幅度是由其灵敏度参数决定。芯片 ADC 满幅约为 40mV，因此当 AMIC 最大灵敏度不超过-28dBV/Pa 或电信号幅度小于等于 40mV 时，MIC 信号通路上不需要分压网络；当 AMIC 最大灵敏度超过-28dBV/Pa 或电信号幅度大于 40mV 时，MIC 信号通路上需要加分压网络，以避免 ADC 饱和。分压比以 AMIC 输出到芯片的最大电信号幅度接近 40mV 为佳，分压网络结构可参考下图。



2.6 DMIC pins (DMIC 管脚)

1) DMIC (Digital MIC) has one group of DMIC clock/DMIC data pins: PA1, PA0.
   DMIC（数字麦克风）有 1 组管脚：DMIC clock/DMIC data 分别对应 PA1、PA0。

2.7 I2S pins (I2S 管脚)

1) I2S has one group of Slave I2SBCK/LR/SDI/SDO pins: PD7/PD2/PD3/PD4.
   I2S 有 1 组 Slave 管脚：I2SBCK/LR/SDI/SDO 对应管脚 PD7/PD2/PD3/PD4。

2.8 ADC detect pins (ADC 检测管脚)

1) ADC supports 10 external detect pins (GPIO input channels): PB0~PB7, PC4~PC5.
   ADC 有 10 个外部检测管脚（GPIO 输入通道）：PB0~PB7，PC4~PC5。

2.9 UART pins (UART 管脚)

1) TLSR8x5x supports UART interface and 7816 UART interface. UART and 7816 UART share the same hardware. UART supports full-duplex transmission and reception, but 7816 UART only supports half-duplex as per 7816 spec.
   TLSR8x5x 芯片支持 UART 和 7816 UART 两种接口。UART 和 7816 UART 共用同一套硬件。UART 支持全双工收发，但 7816 UART 根据 7816 协议仅支持半双工。

   For the TLSR8x5x, only Baseband, AES, UART/IR support DMA. UART and IR share the same DMA channel.
   对于 TLSR8x5x，仅基带、AES 加密模块和 UART/IR 支持 DMA。其中 UART 和 IR 共用 DMA 通道。

   For the convenience of PCB design, the TLSR8x5x supports multiple GPIOs with multiplexed UART interface function.为了便于 PCB 设计，TLSR8x5x 有多个管脚可以复用为 UART 接口。

UART interface:

UART 接口：

- ✧ TX pins: PA2, PB1

  TX 管脚：PA2, PB1

- ✧ RX pins: PA0, PB0, PB7, PC3, PC5, PD6

  RX 管脚：PA0, PB0, PB7, PC3, PC5, PD6

- ✧ Test baud rate: 300/600/1200/2400/4800/19600/14400/38400/56000/57600/115200

  测试波特率：300/600/1200/2400/4800/19600/14400/38400/56000/57600/115200

- ✧ TX and RX pins can be freely combined into a group to realize data transmission reception.

  TX、RX 引脚任意进行组合都可以进行数据发送和接收。

- ✧ In actual applications, only one group can be configured as UART pins.

  实际使用时，只能有一组可以设置为 UART 管脚。

2) 7816 UART interface

   7816 UART 接口：

   - ✧ 7816 UART pins, including PD7, PC2, PD0 and PD3, can be configured as 7816 UART function or UART UTX function, but DO NOT support UART URX function.

     7816 UART 管脚 PD7、PC2、PD0、PD3 可配置为 4 组 7816 UART 口，也可配置成 UART 口的 UTX，但是不能配置为 UART 口的 URX。

*Note: Considering BQB certification, it's needed to reserve corresponding UART pins (PA0 and PA2, or PB0 and PB1). Please refer to section 2.21.

*注意：考虑到 BQB 认证，需要预留对应的 UART 管脚（PA0 与 PA2 或 PB0 与 PB1）。参见 2.21 节。

2.10 I2C pins (I2C 管脚)

For the convenience of PCB design, the TLSR8x5x supports multiple GPIOs with multiplexed I2C interface function.

为了便于 PCB 设计，TLSR8x5x 有多个管脚可以复用为 I2C 接口。

1) I2C pins: PC0/PC1 and PC2/PC3 can be configured as I2C Master/I2C Slave multiplexed pins SDA/SCK.

   I2C 管脚：PC0/PC1，PC2/PC3 可配置成 Master/Slave 共同管脚，分别对应 SDA/SCK；

2) The test result shows PA3/PA4 and PB6/PD7 can also be configured as I2C Master/Slave multiplexed pins.

   经测试，PA3/PA4、PB6/PD7 也可以配置成 I2C Master/Slave 共同管脚。

2.11 SPI pins (SPI 管脚)

For the convenience of PCB design, the TLSR8x5x supports multiple GPIOs with multiplexed SPI interface function.

为了便于 PCB 设计，TLSR8x5x 有多个管脚可以复用为 SPI 接口。

1) SPI pins: PA2/PA3/PA4/PD6 and PB7/PB6/PD7/PD2 can be configured SPI Maser/SPI Slave multiplexed pins DO/DI/CK/CN. Only one group can be configured as SPI pins.

   SPI 有两组 DO/DI/CK/CN 管脚：PA2/PA3/PA4/PD6 和 PB7/PB6/PD7/PD2。既可以作为 SPI Master 也可以作为 SPI Slave，只能有一组可以设置为 SPI 管脚。

2) I2C and SPI Usage

I2C 和 SPI 共用管脚：

- ✧ I2C and SPI cannot be used as Slave at the same time.

  不支持 SPI Slave 和 I2C Slave 共用

- ✧ I2C Slave and SPI Master can be used at the same time.

  支持 I2C Slave 和 SPI Master 共用

- ✧ I2C Master and SPI Slave can be used at the same time.

  支持 I2C Master 和 SPI Slave 共用

- ✧ I2C and SPI can be used as Master at the same time.

  支持 I2C Master 和 SPI Master 共用

2.12 External RF control pins (外部射频管脚)

1) TXCYC is used to control the PA (Power Amplifier) of external RF Front-end: PB3, PC7, PD1

TXCYC 用于控制外部射频前端的功放，共 3 路：PB3，PC7，PD1

2) RXCYC is used to control the LNA of external RF Front-end: PB2, PC6, PD0

RXCYC 用于控制外部射频前端的低噪声放大器，共 3 路：PB2，PC6，PD0

2.13 Antenna select pins (天线选择管脚)

1) Two groups of SEL<0:2>: PD6/PB0/PB1, PC5/PC6/PC7. SEL<0:2> are used to select one of up to eight external antennas connected to the antenna select component. The selected antenna channel is connected to the RF_IO pin.

8 选 1 控制信号 SEL<0:2>，共 2 组，分别对应 PD6/PB0/PB1 和 PC5/PC6/PC7，用于从外置 8 根天线中选择其一，连接至天线选择元件。选中的天线通道连接至 RF_IO 管脚。

2.14 Power supply range (供电范围)

1) Input voltage range for VDD3 pin: 1.8V~3.6V

   VDD3 管脚输入电压范围是 1.8V~3.6V

2) When power supply voltage is lower than 1.8V (e.g. single dry battery is used to supply power), external boost DCDC is needed.

   供电电压低于 1.8V 时（典型应用为单节干电池供电），需要外接升压 DC-DC。

3) When power supply voltage exceeds 3.6V (e.g. lithium battery is used to supply power), external buck DCDC or LDO is needed.

   供电电压超过 3.6V（典型应用为锂电池供电），需要外接降压 DC-DC 或 LDO。

4) When power supply voltage is 1.8V~3.6V (e.g. dual dray batteries are used to supply power), the power supply is directly connected to the chip.

   供电电压在 1.8V~3.6V 之间时（典型应用为两节干电池供电），电压直接接入芯片。

2.15 Battery voltage detect (电池电压检测)

1) When power supply voltage is lower than 1.8V (e.g. single dry battery is used to supply power), external boost DCDC is needed. Supply voltage should be sent to any ADC input channel for voltage detection.

   供电电压低于 1.8V 时（典型应用为单节干电池供电），需要外接升压 DC-DC，供电电压需要接入任一 ADC 检测口进行电压检测。

2) When power supply voltage exceeds 3.6V (e.g. lithium battery is used to supply power), external buck DCDC or LDO is needed. User should implement voltage division to the supply voltage, so that it's decreased below 3.6V. Then this voltage lower than 3.6V should be sent to any ADC input channel for voltage detection. Each ADC input pin has embedded voltage divider circuit.

   供电电压超过 3.6V（典型应用为锂电池供电），需要外接降压 DC-DC 或 LDO，供电电压需要经过分压，让电压低于 3.6V 后，接入任一 ADC 检测口进行电压检测。每个 ADC 检测口均已内置分压电路，都可用于电压检测。

3) When power supply voltage is 1.8V~3.6V (e.g. dual dray batteries are used to supply power), user does not need to directly connect the power supply to ADC input channel, but should ensure there's one ADC detect pin floating and not connected to any external signal.

   供电电压在 1.8V~3.6V 之间时（典型应用为两节干电池供电），供电电压不用直接接到 ADC 检测口，但是需要确保有一个 ADC 检测口悬空不接外界任何信号。

2.16 DCDC

1) A serial 47uH inductor should be connected between the VDCDCSW pin and DECM pin.

   VDCDCSW 和 DECM 管脚之间需要串接 47uH 电感。

2) The recommended inductance for DCDC is 47uH. Please refer to the parameters of the LB2012T470M to select inductor model.

   DCDC 电感建议选用 47uH。可参考 LB2012T470M 的参数选型。

2.17 Power structure (电源结构)

1) Internal-generated voltage (take the 8258 QFN48 for example)

   内部产生电压（以 8258 QFN48 管脚为例）

   ✧ 1.2V: PIN13, internal LDO output, supplies power for internal Core, and should be connected to GND via external capacitor. PIN18, internal DCDC output, should be connected to GND via capacitor and externally sent to AVDD1V2 (PIN39).

   1.2V：对应 PIN13/PIN18 两个管脚。PIN13 是内部 LDO 输出电压，给内部 Core 供电，需要外接电容到地；PIN18 是内部 DCDC 产生的电压，需要外面走线送到 AVDD1V2（PIN39）管脚，同时 PIN18 需接电容到地。'

- ✧ 1.8V: PIN19, 1.8V internal-generated voltage, supplies power for Flash, and should be connected with external 1uF capacitor.

  1.8V：对应 PIN19 管脚，PIN19 是内部产生的 1.8V 电压，给 Flash 供电，该管脚需要外接 1uF 电容。

2) External input voltage (take the 8258 QFN48 for example)

   外部输入电压（以 8258 QFN48 管脚为例）

   - ✧ 1.8V~3.6V: External power supplies voltage for chip via PIN15/PIN26/PIN27.

     1.8V~3.6V：外部电源通过 PIN15/PIN26/PIN27 三个管脚给芯片供电。

2.18 System crystal oscillator (系统晶振)

1) Crystal specification is 24Mhz_12pF_ +/-20ppm.

   晶体规格是 24Mhz_12pF_ +/-20ppm

2) TLSR8x5x embeds matching capacitor. Its range is 5pF~18pF, and typical value is 12pF.

   TLSR8x5x 芯片内部自带匹配电容，范围是 5pF~18pF，典型值为 12pF。

3) Currently it's recommended to adopt internal matching capacitor.

   目前推荐采用内部匹配电容。

2.19 RTC crystal oscillator (RTC 晶振)

1) PC2 and PC3 can be used to connect external 32.768kHz crystal.

   PC2 和 PC3 可以外接 32.768kHz 晶体。

2) Crystal specification is 32.768kHz _9pF_ +/-20ppm.

   晶体规格是 32.768kHz _9pF_ +/-20ppm。

2.20 Filtering capacitor (滤波电容)

Herein 8258 QFN48 is taken as an example to illustrate external capacitors required for various power pins.

此处以 8258 QFN48 封装为例，说明各个电源管脚对外接电容的要求。

	8258 QFN48	
VDD1V	PIN13	1uF
VDD_IO	PIN15	1uF
VDCDC_SW	PIN16	47uH
VDCDC	PIN17	
VDD1V2	PIN18	0.1uF+1uF
VDD_F	PIN19	1uF
VDD3	PIN26	1uF
VDDIO_AMS	PIN27	1uF
RESETB	PIN36	1uF
VANT	PIN37	18pF
AVDD1V2	PIN39	0.1uF+2.2uF

2.21 BQB certification (BQB 认证)

1) For general hardware verification, BQB firmware adopts individual BIN file and uses the PA0 and PA2 pin.

   普通硬件验证，BQB 程序都是采用单独的 BIN 文件，使用 PA0 和 PA2 管脚。

2) The 8x5x RCU SDK integrates BQB, but adopts the PB0 and PB1 pin.

   8x5x RCU SDK 中已经合入了 BQB，但是采用 PB0 和 PB1 管脚。

2.22 FCC certification (FCC 认证)

1) An external inductor should be connected between the ANT and VANT pin, so as to supply power for internal PA. Its default value is 1.3nH.

   ANT 和 VANT 管脚间需要有一颗电感，目的是给内部 PA 供电。默认为 1.3nH。

2) The VANT pin should be connected with an external filtering capacitor. Its default value is 18pF.

   VANT 管脚需要加一颗滤波电容，默认为 18pF。

3) A serial DC-blocking capacitor (default value: 220pF) is connected to the ANT pin. If the capacitor is not connected, and test instrument does not block DC signal, test may be abnormal.

   If test instrument does block DC signal, or connection test is not needed, this capacitor can be removed.

   ANT 路径上默认会串联一颗隔直电容，默认为 220pF。如果去掉，同时仪器不隔直的话，测试会异常。反之，如果仪器隔直或者不做连接测试，那么可以去掉。

4) The other capacitors and inductors are used for circuit matching during certification, the values of which are flexibly adjustable corresponding to layout.

   其余电容电感是做认证匹配所用，器件值随 layout 灵活调整。

5) Before all tests, VNA (Vector Network Analyzer) should be used to implement RX matching. Meanwhile, power on the DUT, configure the chip to enter RX mode, and then use the VNA to do RX matching.

   任何测试前一定需要借助 VNA（矢量网络分析仪）做 RX 匹配。同时，一定需要上电并配置芯片处于 RX 模式，然后再借助 VNA 进行 RX 匹配。

6) After RX test is finished, SA (Spectrum Analyzer) should be used to implement TX certification verification. If harmonics do not meet the requirements, go back to the previous step. Use the VNA to adjust component value to meet the impedance matching requirements, and then carry out TX verification.

   在 RX 测试完毕后，再用 SA（频谱分析仪）进行 TX 认证验证。如果谐波不满足需求，再回到上一步骤，借助 VNA 调整器件值同时满足阻抗匹配要求后，再进行 TX 验证。