# Application Note : Assembly And Maintenance Manual for Telink BLE 1x6 Test System 3.2

AN-18071200-E1

**Ver 1.0.0**

**2018/7/12**

**Brief:**

This document is the assembly and maintenance guide for Telink BLE 1x6 Test System 3.2, and presents DUT examples with flash or OTP.

TELINK SEMICONDUCTOR

**Published by**
**Telink Semiconductor**

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**Zhangjiang Hi-Tech Park, Shanghai, China**



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## Revision History

| Version | Major Changes | Date | Author |
|---|---|---|---|
| 1.0.0 | Initial release | 2018/7 | LWH, LX, Cynthia |

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# 1 Overall Architecture Of 1x6 Test System 3.2

Telink BLE 1x6 Test System 3.2 consists of test bench and mechanical structure. The test bench includes hardware platform and firmware folder, and it's provided by Telink; while customer needs to make the mechanical structure suitable for DUT (Device Under Test), and connect cables according to the guide in this document.

A set of Test Bench mainly contains the following hardware resources.

1) A Main Board provided by Telink. Figure 1 shows the correct direction to place the Main board.

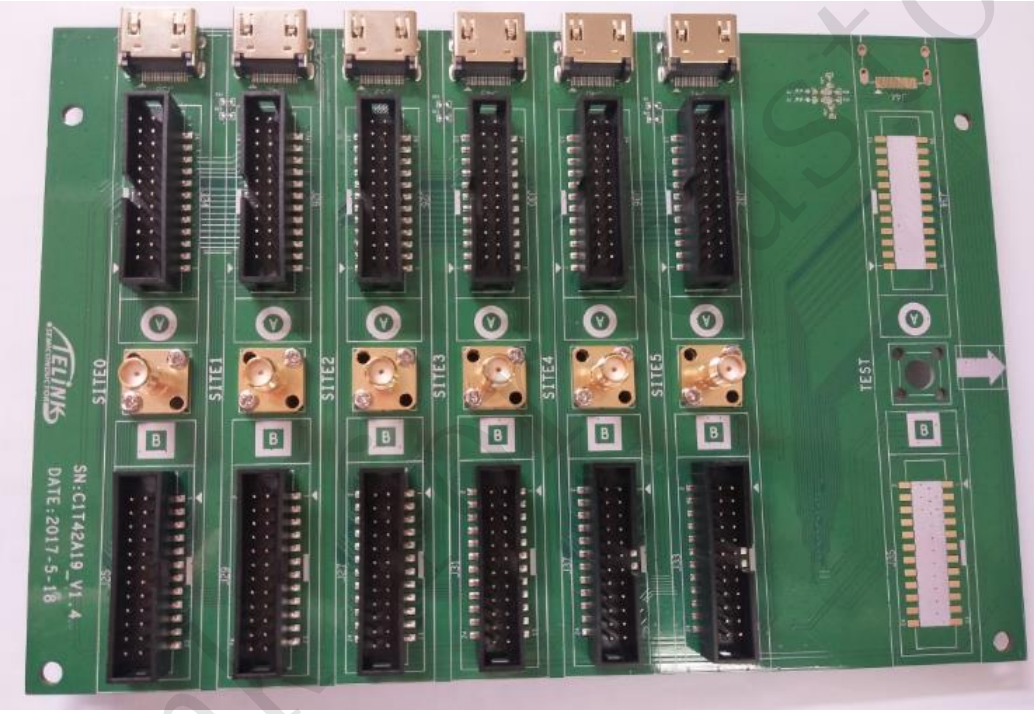



Figure 1 Top view of Main board

2) Six EVK daughter boards provided by Telink. Each should be burned with the EVK firmware for test bench.

Figure 2 EVK daughter board

3) A Power board provided by Telink. It's pin-to-pin compatible with EVK daughter board and serves to supply power for test system.

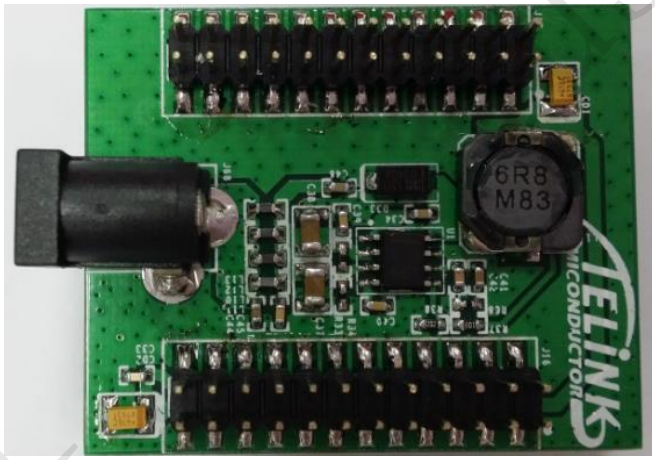
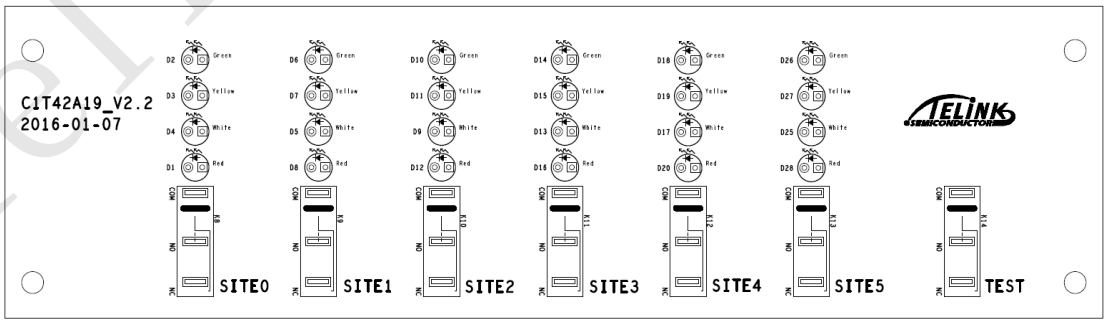
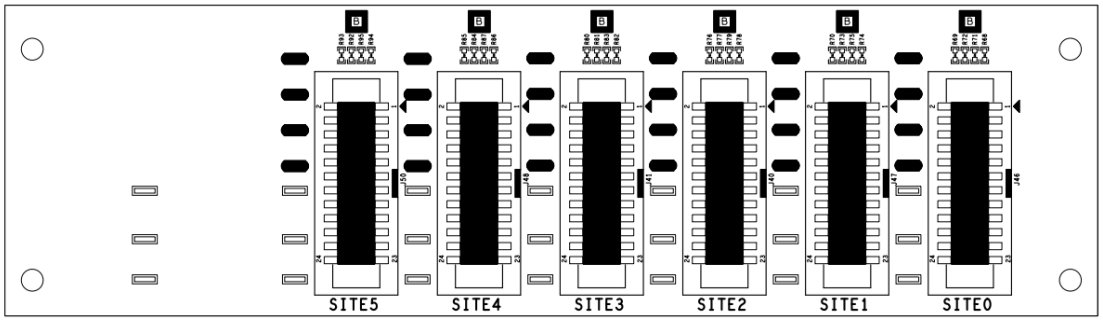



Figure 3 Power board

4) A Display board provided by Telink. Its top side contains six groups of LEDs and six independent start buttons, while the bottom side contains six connectors.




a) Top view




b) Bottom view

Figure 4 Display board

5) Six Thimble boards. Each contains a HDMI connector and soldering points, so that each test site of Main board can be connected with a DUT via a thimble board. Figure 5 shows an example of thimble board.

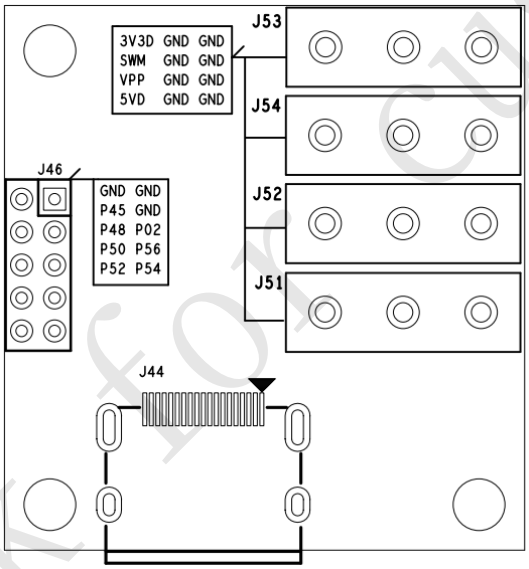



Figure 5 Thimble board

6) Six PCB Antenna boards and six RF cables provided by Telink, as shown in Figure 6.

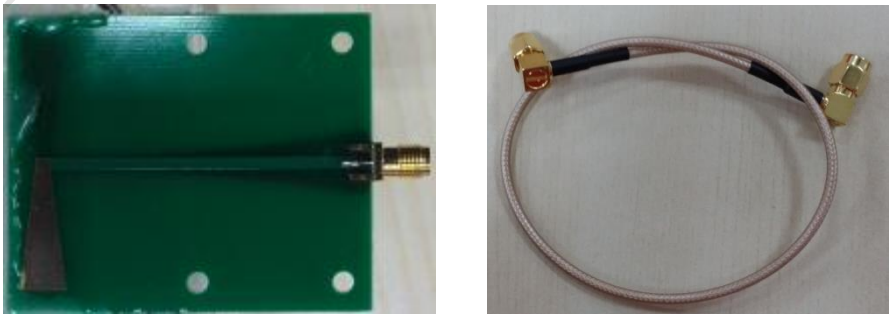


Figure 6 PCB antenna board and RF cable

7) A USB hub and six customized USB cables: The USB hub is used to connect six EVK daughter boards and PC.

8) A PC. On PC side, the EvkMonitor tool can be used to burn firmware for EVK daughter boards (refer to **Section 3**), and user can also observe test result via the EvkMonitor (refer to **Section 4**).

9) Six buzzer modules (Dimension: 50.2x16mm): Each is connected with a thimble board via a rainbow cable, thus it's connected to corresponding GPIO and Power of an EVK daughter board via HDMI interface of thimble board. The buzzer modules are used for Amic test.

   Each buzzer board should be placed as close to corresponding Amic as possible. Do not contact buzzer board with Amic directly, and there should be no obstacle between them.

   **Note:** Buzzer boards are only supplied for DUT with MIC and not contained in the hardware resources by default.

Figure 7 Buzzer module

Six EVK daughter boards and Power board are directly connected with corresponding connectors on the bottom side of the Main board (refer to **Section 2.2**).

Figure below shows the system connection chart.

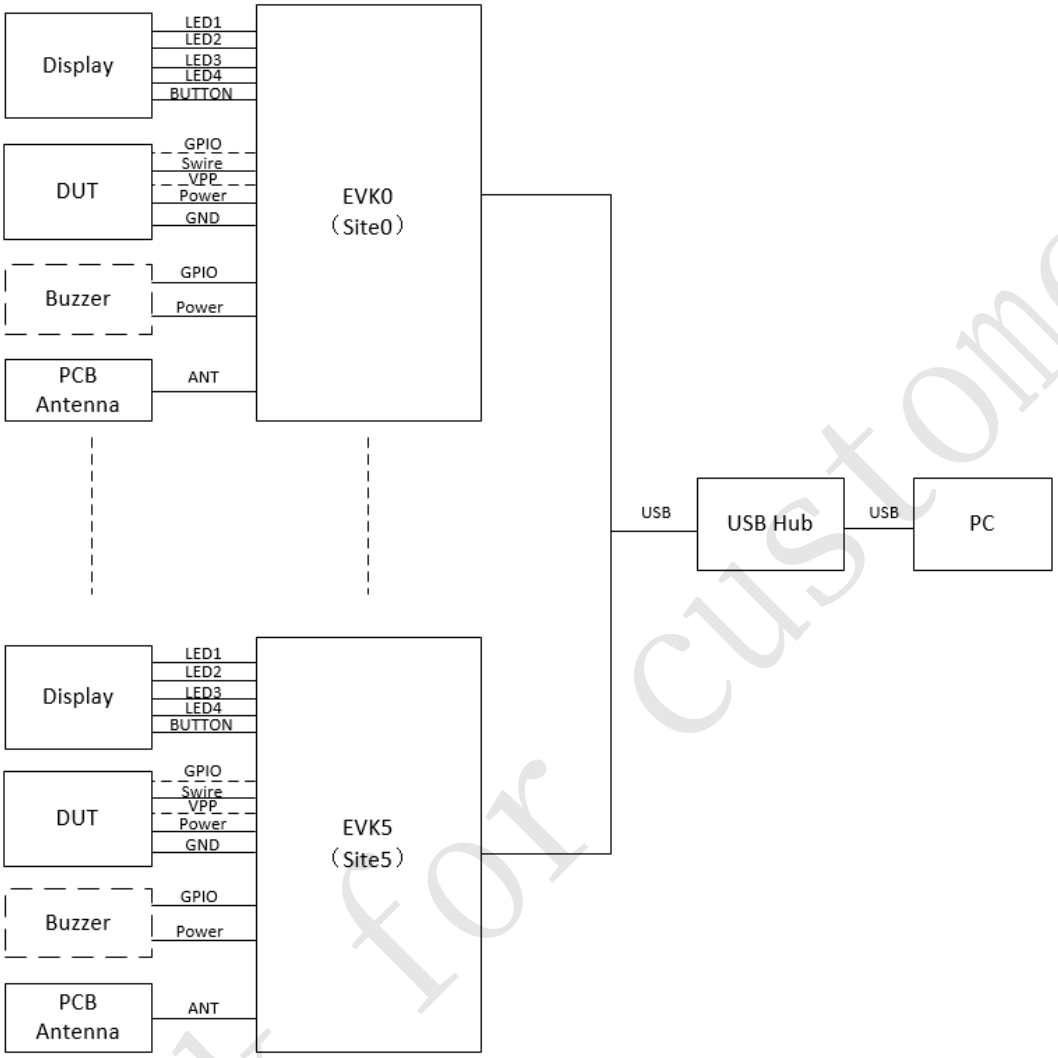



Figure 8 System connection chart

# 2 Hardware Platform Building

## 2.1 Check External Antenna

Telink test bench adopts external antennas for RF test. Customer needs to check the consistency of antennas. Figure 9 shows the PCB antenna supplied by Telink.

Figure 9 Telink PCB antenna board

Customer needs to make sliding blocks (as shown in Figure 10) which can fix the PCB antennas. The sliding blocks are used for distance debugging between the PCB antennas and PCBAs (DUTs) to guarantee test result consistency.

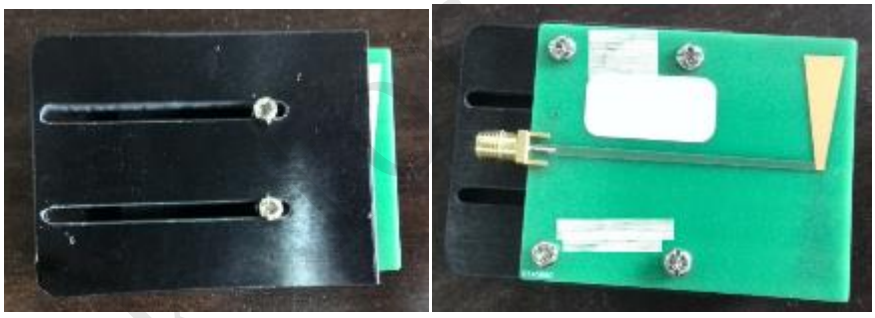


Figure 10 Sliding block to fix PCB antenna

Figure 11 shows dimensions in mm of the PCB antenna supplied by Telink.

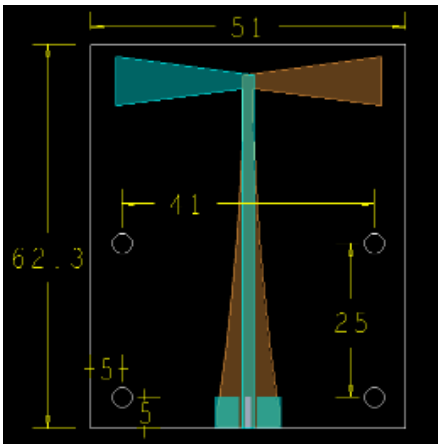



Figure 11 Telink PCB antenna dimensions

## 2.2 Hardware assembly

Connect six EVK daughter boards (EVK0~EVK5) and Power board with corresponding connector location on the bottom side of the Main board, as shown in Figure 13.

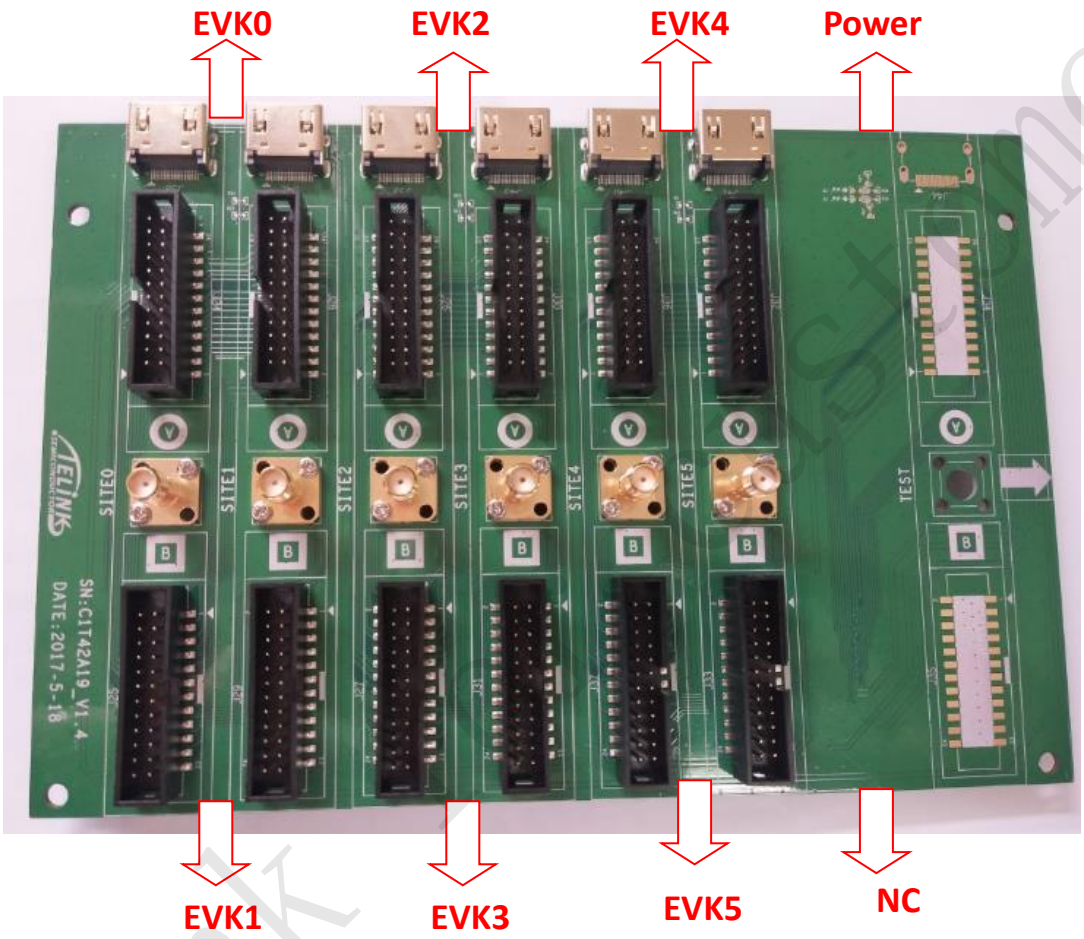



Figure 12 Top view of Main board

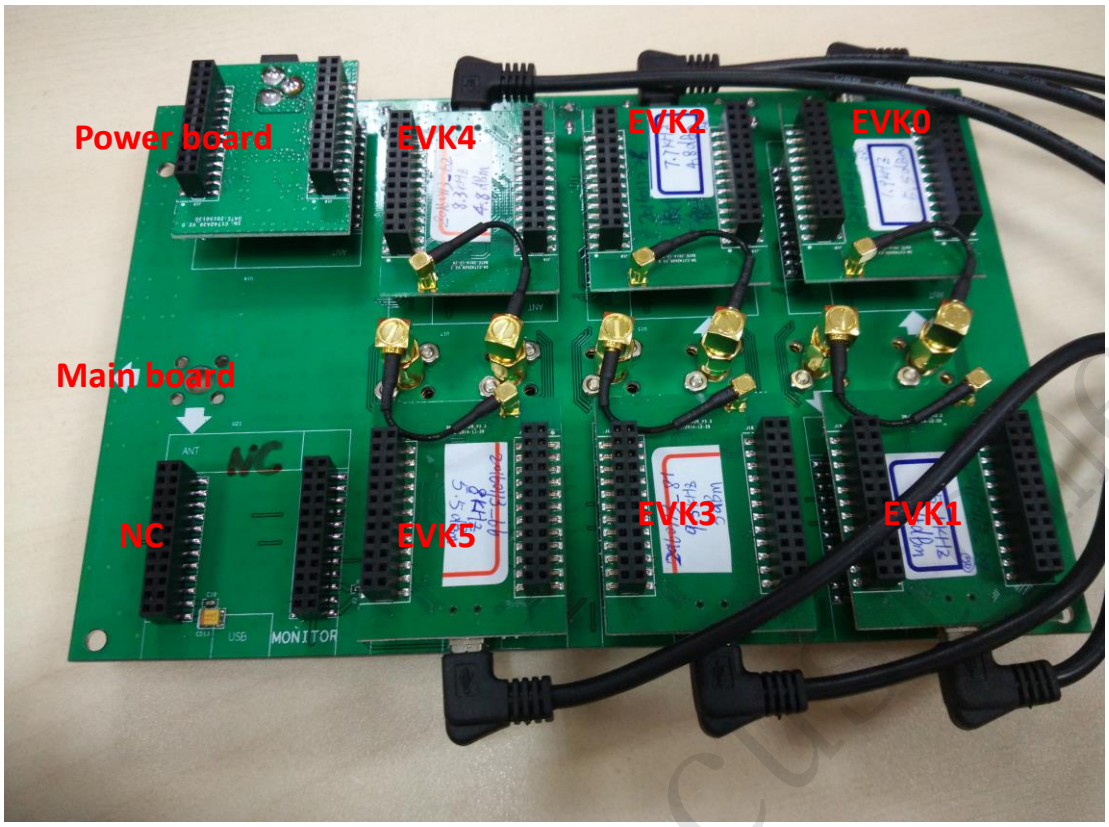



Figure 13 Assembly chart on the bottom side of Main board

Note that USB interfaces of the EVK daughter boards, as well as power interface of the Power board should be placed towards the outside direction of the Main board.

## 2.3 Cable connection

### 2.3.1 Test sites on Main board

As shown in Figure 14, the top side of the Main board contains six independent test sites (marked as Site0~Site5 from left to right). Note that the arrow should be placed towards right.

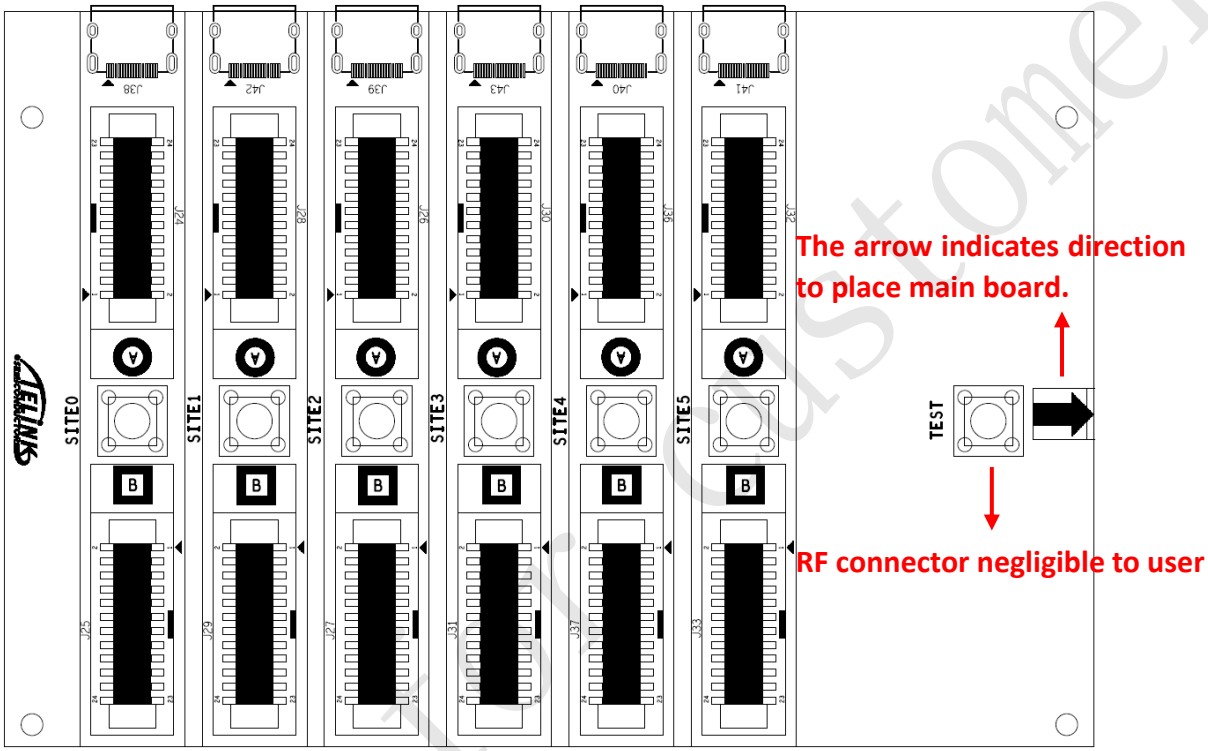



Figure 14 Top silk-screen sketch of Main board

Each Site on the Main board contains HDMI connector, connector A, flange plate and connector B from top to bottom. Connector A and B are featured with dual rows, 2.54mm spacing and 2x12pin.

Telink adopts a HDMI cable to connect a thimble board with HDMI connector on corresponding test site of the Main board, and adopts a gray flat cable to connect a Display board with corresponding connector B of the Main board.

Please refer to **Appendix 3** for illustration of test pins on the main board.

### 2.3.2 Test sites on Display board

As shown in Figure 15, the bottom side of the Display board contains six independent test sites (marked as Site5~Site0 from left to right).

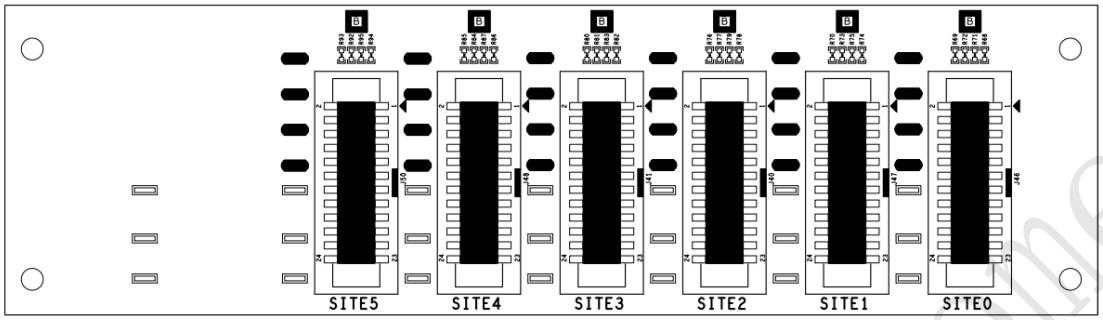



Figure 15 Bottom silk-screen of Display board

Each site (e.g. Site0 in Figure 16) on the Display board contains a mistake-proof connector (marked as B) featured with dual rows, 2.54mm spacing and 2x12pin.

In Figure 16, Site0 is taken as an example to show the mark of connection points on each test site of the Display board. G, W, R, Y and Button indicate connection point Green-LED, White-LED, Red-LED, Yellow-LED, independent start button, respectively.

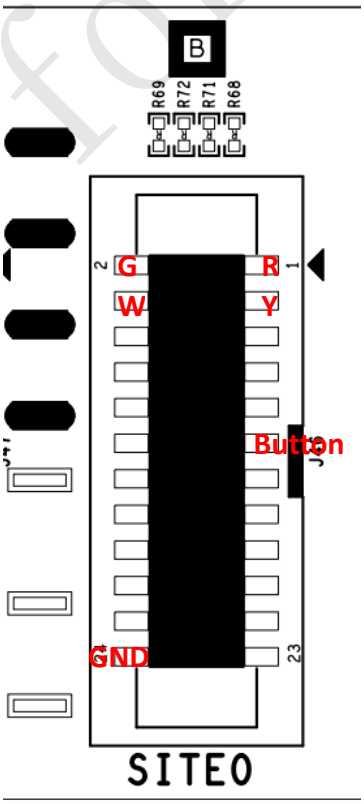



Figure 16 Connection points on test site of Display board

### 2.3.3 Cable connection between Main board and DUT thimble

Telink provides six HDMI cables. HDMI connector on each test site of the Main board should be connected with a thimble board‘s HDMI connector via a HDMI cable.

If DUT is a device board with flash, up to four cables should be connected between a thimble board and a DUT.

Table 1 Cable connection between thimble board and DUT with flash

| Connection points on thimble board | Connection points on DUT |
|---|---|
| 3V3D | BAT+ |
| GND | BAT- |
| SWM | SWS |
| P45* | Wakeup GPIO* |
| *Note: Wakeup test supports two methods including timer wakeup and GPIO wakeup.<br>1) If using timer wakeup, it’s not needed to connect P45 of thimble board with DUT’s wakeup GPIO.<br>2) If using GPIO wakeup, it’s needed to connect P45 of thimble board with DUT’s wakeup GPIO. | |

If DUT is a device board with OTP, up to five cables should be connected between a thimble board and a DUT.

Table 2 Cable connection between thimble board and DUT with OTP

| Connection points on thimble board | Connection points on DUT |
|---|---|
| 3V3D | BAT+ |
| GND | BAT- |
| SWM | SWS |
| P45* | Wakeup GPIO * |
| VPP | VPP |
| *Note: Wakeup test supports two methods including timer wakeup and GPIO wakeup.<br>1) If using timer wakeup, it’s not needed to connect P45 of thimble board with | |

DUT's wakeup GPIO.

2) If using GPIO wakeup, it's needed to connect P45 of thimble board with DUT's wakeup GPIO.

Figure 17 shows cable connection chart.

**Note:** To avoid ambient interference, all connection cables between thimble board and DUT should use STP (Shielded Twisted Pair) cable.

### 2.3.4 Cable connection between Buzzer board and Thimble board

Each thimble board (connection points: P48, 3V3D, GND) should be connected with corresponding Buzzer board (connection points: VCC, 3V3B, GND) via a 3P rainbow cable. (Rainbow cable is supplied by Telink, and user can cut it as needed.)

Figure 17 shows cable connection chart.

**Note:** Buzzer boards are only supplied for DUT with MIC and not contained in the hardware resources by default.

### 2.3.5 Cable connection between Main board and Display board

Telink provides six gray flat cables.

Connector B on each test site of the Main board (connection points: Green-LED, Red-LED, White-LED, Yellow-LED, Button (Independent start button), GND) should be connected with connector B on corresponding Site of the Display board (connection points: G, R, W, Y, Button, GND) via a gray flat cable. Figure 17 shows cable connection chart.

### 2.3.6 Cable connection between Main board and PCB antenna board

Flange plate (SMA) on each test site of the Main board should be connected with corresponding external PCB antenna board via a RF cable. Figure 17 shows cable connection chart.

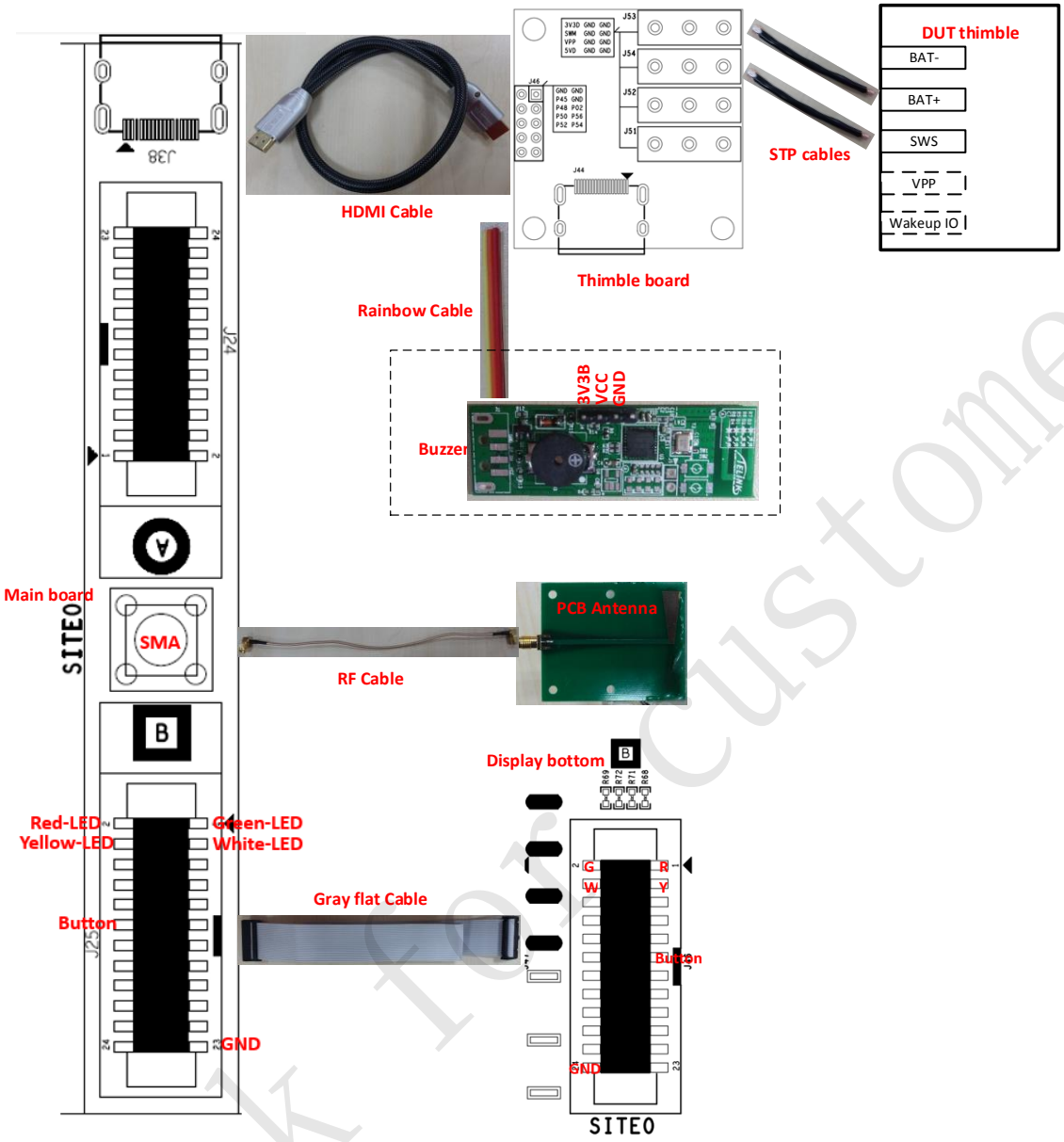



Figure 17 Cable connection chart

### 2.3.7 Other cable connection

The Power board should be connected with power to supply power for test system.

Each EVK daughter board should be connected with an USB interface of USB hub via an USB cable. The USB hub should be connected with PC via an USB cable. User can burn firmware for EVK daughter boards and observe test result via the EvkMonitor tool on PC side (refer to **Section 3 and Section 4**).

Figure 18 1x6 Test system 3.2

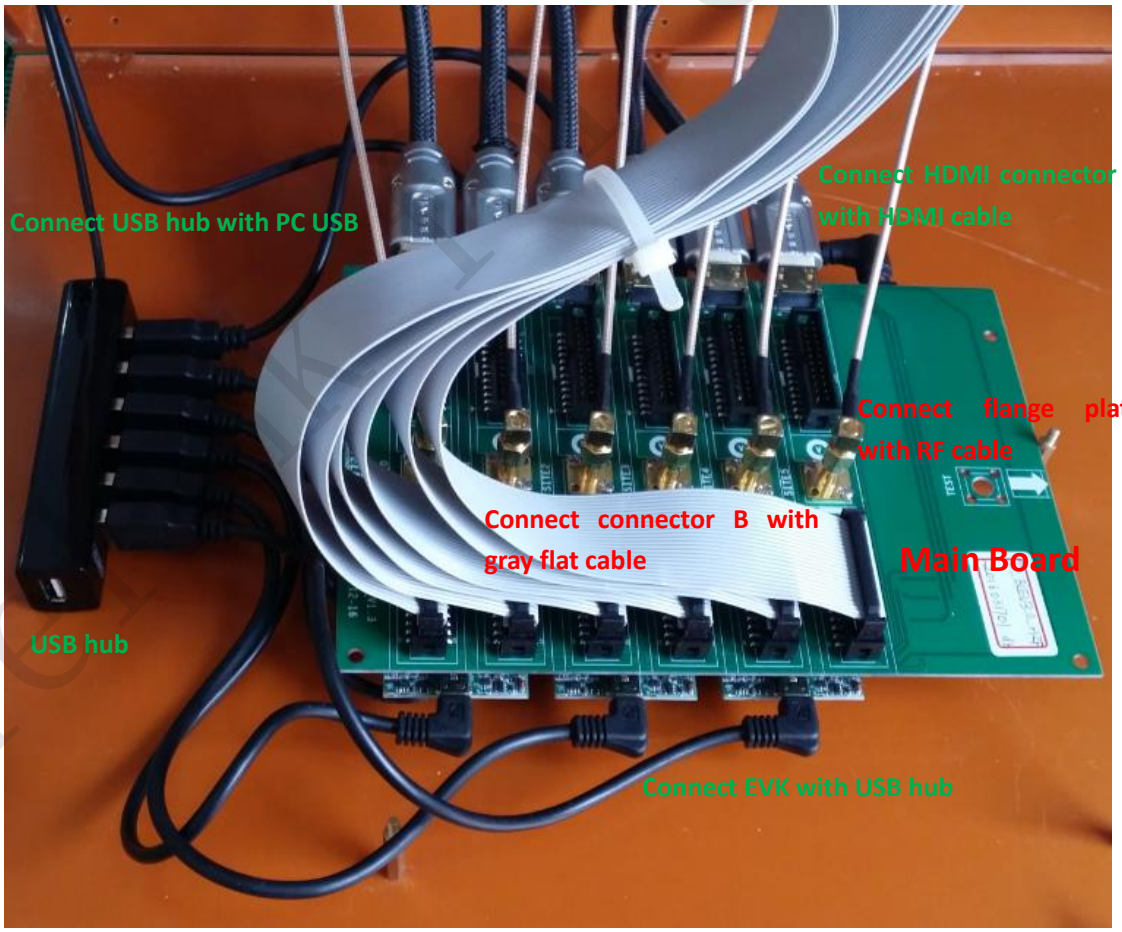



Figure 19 Cable connection sketch of Main board

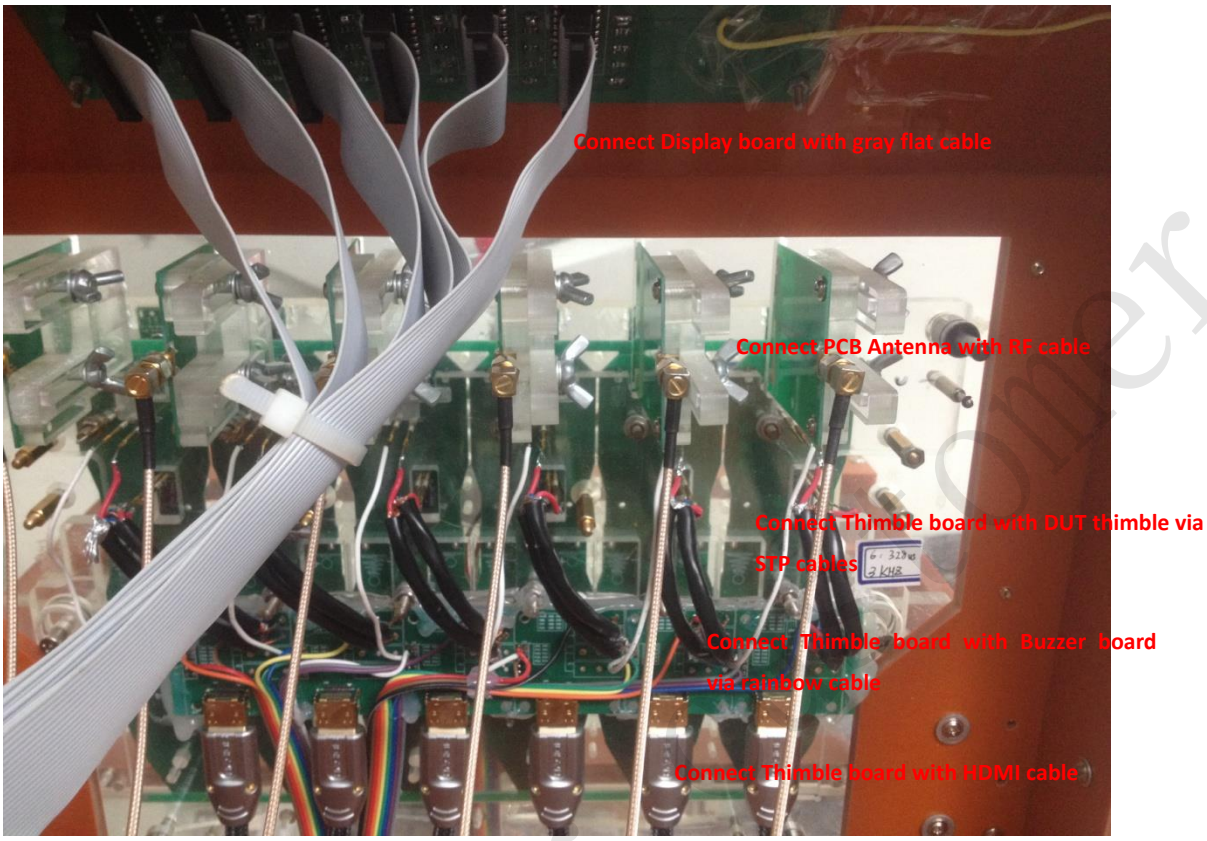



Figure 20 Cable connection of Display, Antenna, Thimble board and DUT thimble

## 2.4 Check Jig debugging

Keeping test consistency is critical for multiple sets of 1x6Jig. During debugging, it's needed to select several good products and several rejected products, then test them on each Site of each Jig; good products should pass test on each Site, and each rejected product should fail at the same test item on each Site. Take the rejected products with low RF Tx power for example, the data log is shown as follows:

| Site NO | Board NO | Channel | TX Test | Offset | RX Test | IEEE Address |
|---|---|---|---|---|---|---|
| 1 | star | 2392 | 100/-34 | 2 | | |
| | | 2495 | | 9 | | |
| | 1st ok | 2392 | 100/-26 | 6 | 92/-54 | 0x8a003a30 |
| | | 2495 | 100/-26 | 12 | 100/-54 | |
| | 2nd ok | 2392 | 100/-29 | -9 | 96/-62 | 0x8a003a36 |
| | | 2495 | 100/-27 | -4 | 100/-54 | |
| 2 | star | 2392 | 100/-29 | 1 | | |
| | | 2495 | 100/-32 | 7 | | |
| | 1st ok | 2392 | 100/-23 | 4 | 100/-53 | 0x8a1019ec |
| | | 2495 | 100/-25 | 12 | 100/-54 | |
| | 2nd ok | 2392 | 100/-23 | 1 | 100/-54 | 0x8a1019f2 |
| | | 2495 | 100/-25 | 11 | 100/-53 | |
| 3 | star | 2392 | 100/-31 | -7 | | |
| | | 2495 | 100/-32 | -1 | | |
| | 1st ok | 2392 | 100/-23 | -2 | 100/-53 | 0x8a203d21 |
| | | 2495 | 100/-25 | 4 | 100/-54 | |
| | 2nd ok | 2392 | 100/-25 | -17 | 100/-54 | 0x8a203d27 |
| | | 2495 | 100/-25 | -9 | 100/-54 | |
| 4 | star | 2392 | 100/-32 | 4 | | |
| | | 2492 | | | | |
| | 1st ok | 2392 | 100/-25 | 7 | 99/-54 | 0x8a301f13 |

| Site NO | Board NO | Channel | TX Test | Offset | RX Test | IEEE Address |
|---|---|---|---|---|---|---|
| 5 | | 2492 | 100/-25 | 11 | 100/-54 | |
| | 2nd ok | 2392 | 100/-25 | -8 | 100/-54 | 0x8a301f19 |
| | | 2492 | 100/-26 | -4 | 100/-54 | |
| | star | 2392 | 100/-32 | -3 | | |
| | | 2495 | | | | |
| | 1st ok | 2392 | 100/-25 | 2 | 100/-54 | 0x8a401fcc |
| | | 2495 | 100/-25 | 8 | 100/-54 | |
| | 2nd ok | 2392 | 100/-26 | -14 | 88/-53 | 0x8a401fd3 |
| | | 2495 | 100/-25 | -6 | 100/-54 | |
| | star | 2392 | 96/-33 | -2 | | |
| | | 2495 | | | | |
| 6 | 1st ok | 2392 | 100/-28 | 2 | 100/-56 | 0x88403d0a |
| | | 2495 | 100/-26 | 7 | 100/-54 | |
| | 2nd ok | 2392 | 100/-26 | -13 | 100/-54 | 0x88403d11 |
| | | 2495 | 100/-26 | -6 | 100/-54 | |

If the rejected products with low RF Tx power output high power on some Site, or even pass test, by tuning height of external PCB antennas, RF energy can be effectively adjusted to keep consistency of test result. To weaken RF energy, increase the distance between external PCB antenna and PCBA; to strengthen RF energy, decrease the distance between external PCB antenna and PCBA.

# 3 Firmware Burning For EVK Daughter Boards

## 3.1 Folder structure for Test Bench Firmware

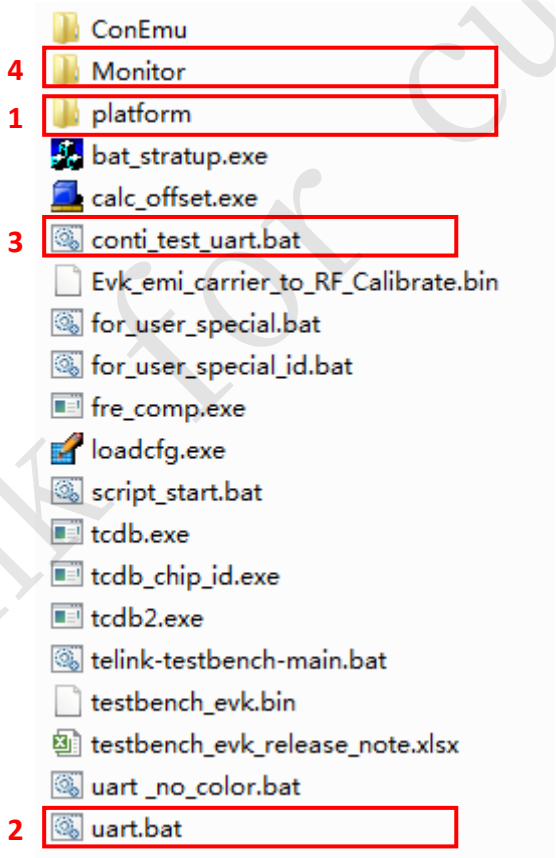
Telink test bench firmware folder is generally named as “BLE_System_V3.2_xxx”.

The structure of the “BLE_System_V3.2_xxx” folder is shown as below:


“DB”: This folder contains db files.

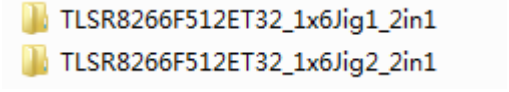
“Sch”: This folder contains schematics, cable connection illustration, and etc.

The structure of the “Script” folder is shown as below:

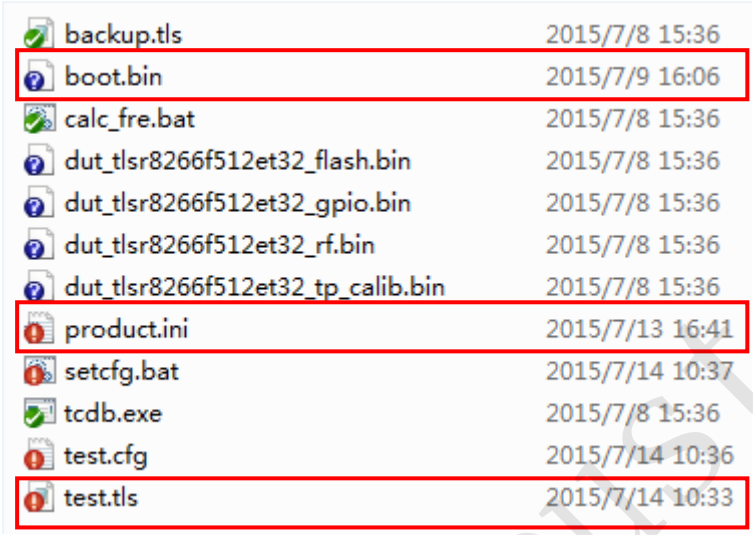



1) platform: This folder contains project files.

E.g.

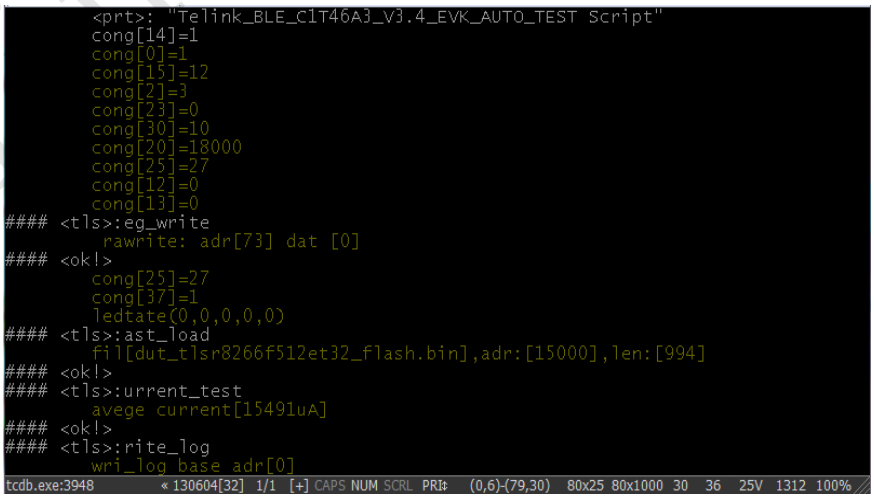



Double click “TLSR8266F512ET32_1x6Jig1_2in1” to open the following interface.

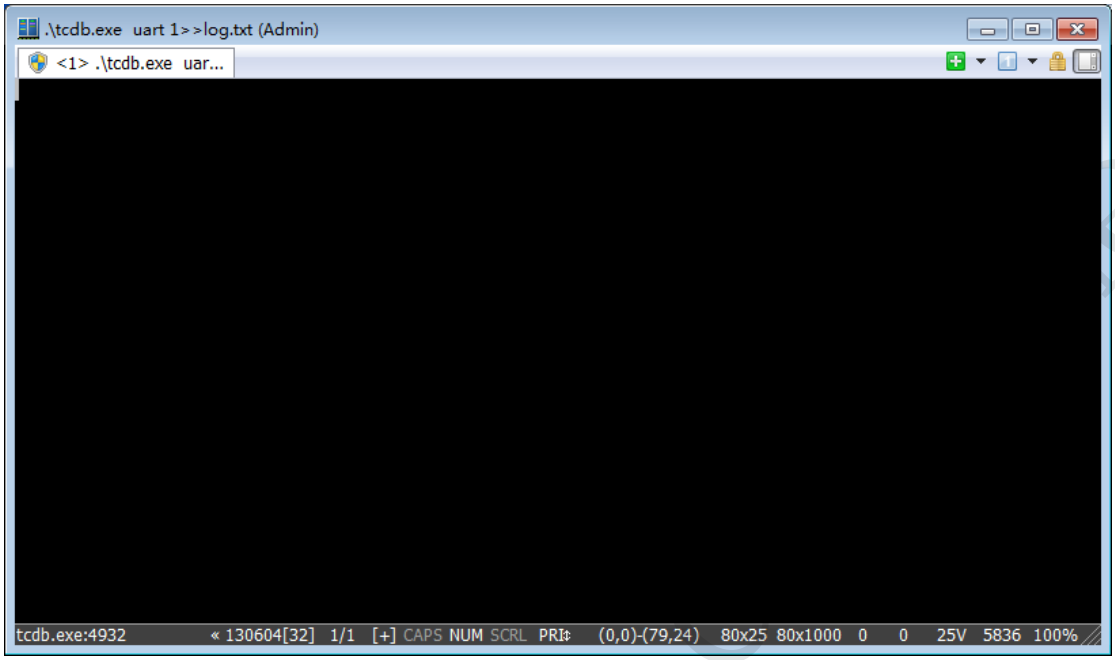



- ✧ test.tls: Jig test script to determine PCBA test items.
- ✧ product.ini: EVK product information to determine PCBA RF test frequency point and ID.
- ✧ boot.bin: Image file to download into PCBA finally.

2) uart: Double click “uart.bat” to open uart window and display real-time log for the convenience of test status check. Only one uart window is allowed at the same time.



3) conti_test_uart.bat: Double click the file, a uart window will pop up; data won't be available on the window, but only saved in "log.txt" under this directory for convenience of analysis.




4) Monitor: This folder contains the "EvkMonitor" tool on PC side.

## 3.2 Firmware burning for EVK daughter boards

Generally multiple sets of 1X6 Jig are used in factory. Note that each Site of each Jig should be burned with firmware before it's ready for use.

Each Jig has six Sites including Site0~Site5, corresponding to EVK0~EVK5.

In this section, **Jig1 Site0** (EVK0) is taken as an example to show how to burn firmware to EVK daughter board.

First connect the EVK daughter board (e.g. EVK0) with PC via an USB cable, as shown in Figure 21.

**Note:** To burn firmware for EVK daughter board, only the target board should be connected with PC, while other Sites must be disconnected from PC.

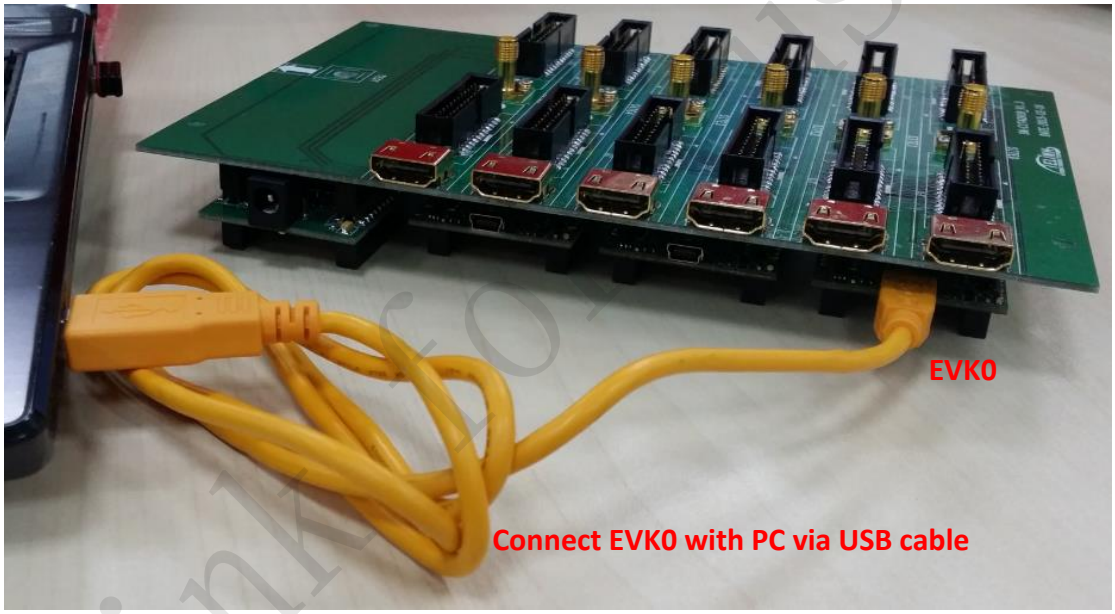
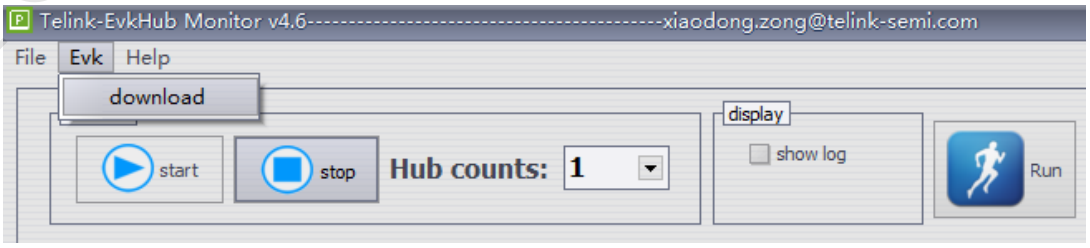



Figure 21 Connection chart between EVK daughter board and PC

Then double click the "EvkMonitor.exe" under the "BLE_System_V3.2_xxx\Script\Monitor" folder.




Click "download" under the menu "Evk" to open the burning interface.

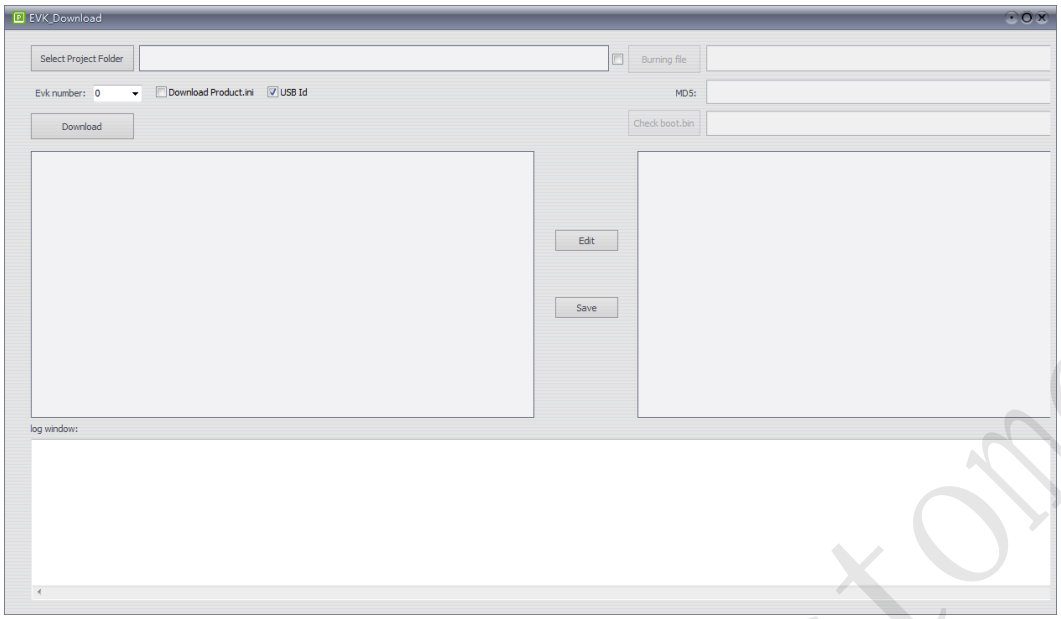



Figure 22 Firmware burning interface 1 for EVK daughter board

First click the "**Select Project Folder**" button and select the target project folder (i.e. the project under "platform") in the pop-out window. The selected project path will be available in the box next to the "Select Project Folder" button; test script and product configuration information files will be available in the "test.tls" and "product.ini" editing window, respectively.

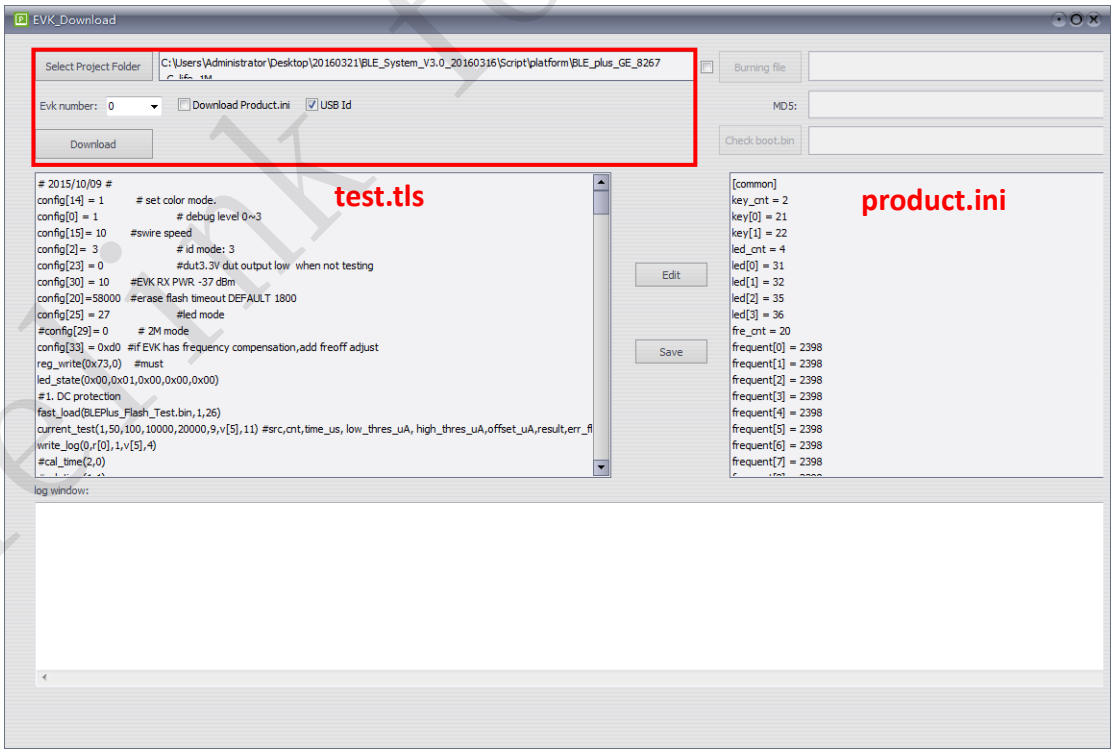
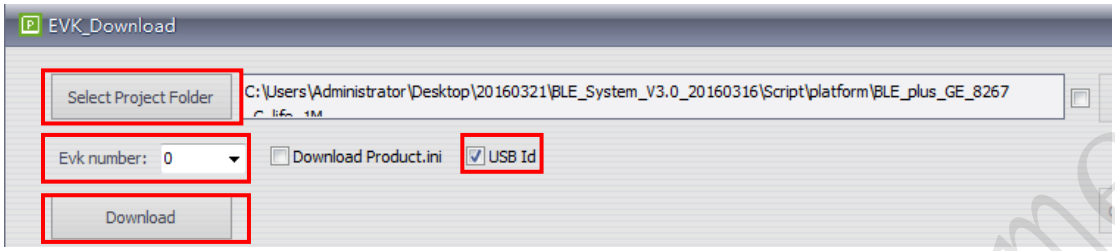
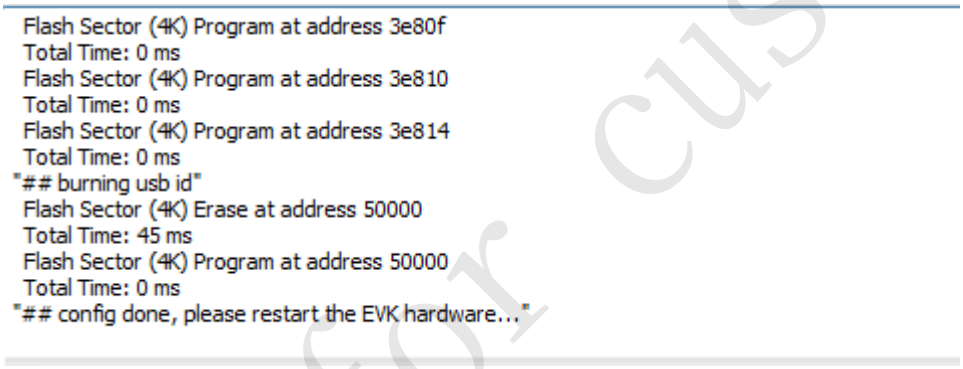



Figure 23 Firmware burning interface 2 for EVK daughter board

During first time of firmware burning, it's needed to configure product information (product.ini) for EVK daughter board. Tick the "**USB Id**" box. Set "**Evk number**" as Site number, e.g. "0" for Site0 (EVK0).




Then click the "**Download**" button to start burning. The log window keeps scrolling until it's as shown in the figure below.




Now the EVK daughter board (EVK0) is already burned with evk_testbench.bin, test.tls, product.ini, id and other bin files in the folder.

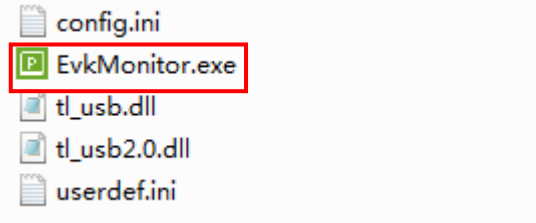
Power cycle the EVK daughter board, then it's configured as Site0 of Jig1 and ready for use.

Firmware burning steps for other Sites of Jig1 are similar, except that "Evk number" varies among 0~5.

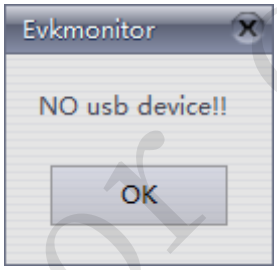
Sites of other Jigs can be burned with firmware similarly, except that project file varies correspondingly.

# 4 Observe Test Result Via PC Software EvkMonitor

Double click the “Monitor” folder under “BLE_System_V3.2_xxx\Script”.




Double click the “EvkMonitor.exe” to open the software interface. If a prompt information of “NO usb device” pops up as shown below, it indicates communication problem such as USB cable connection with EVK, hub and PC; though software interface still pops up, user must check and make sure the connection is OK, then restart the software.




After the software is started properly, the interface is shown as below:

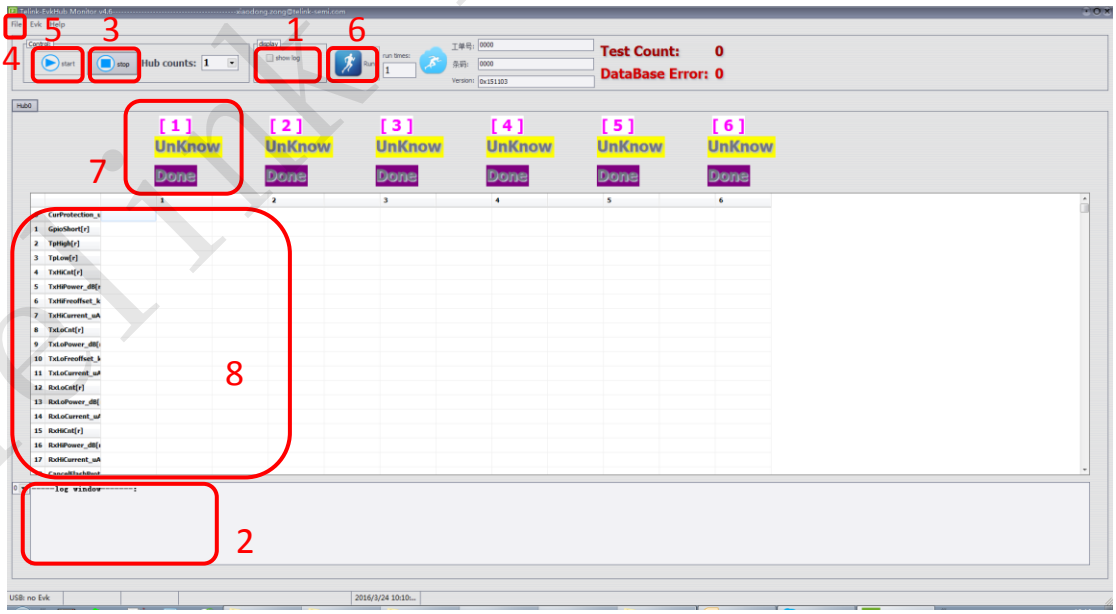
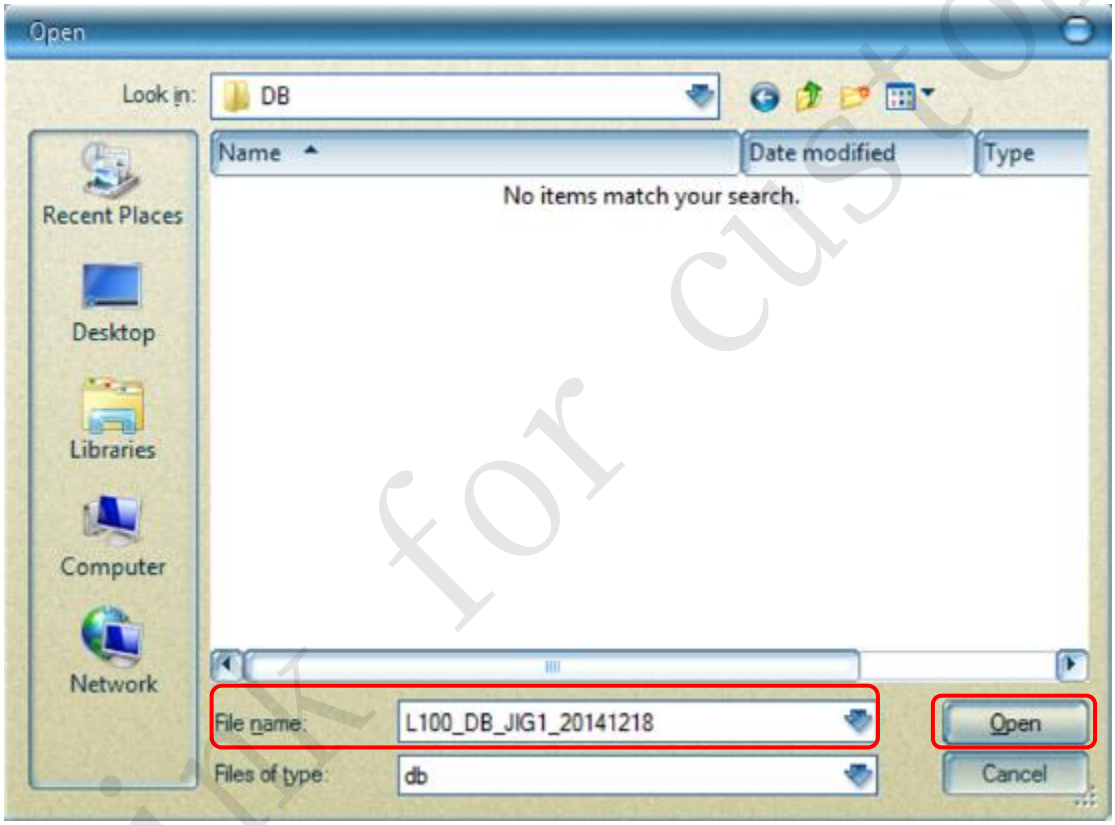



Figure 24 EvkMonitor tool interface

- ✧ show log: Tick the “show log” box (as shown in mark 1 of Figure 24) to enable the “log window” to display dynamic information.
- ✧ log window: As shown in mark 2 of Figure 24, it’s the area to display dynamic information.
- ✧ Stop: As shown in mark 3 of Figure 24, the software is in the state of stop by default.
- ✧ File: Click “open” under the “File” menu (as shown in mark 4 of Figure 24), a window to set the storage path for database files will pop up.

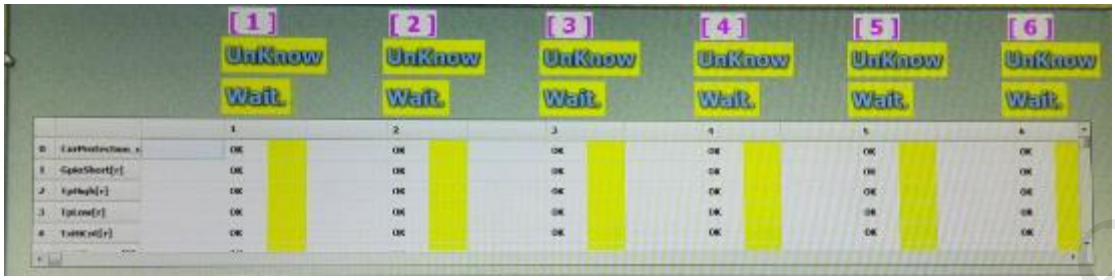



Select the storage path as needed, input file name and then click the “Open” button. Test result will be automatically stored under the directory by the software.

**Note：** Only storage path and file name in English are allowed, otherwise it will invalidate the database creation.

- ✧ start: Click the “start” icon (as shown in mark 5 of Figure 24), the software enters the state waiting for receiving the test result.
- ✧ Run: Click the “Run” icon (as shown in mark 6 of Figure 24) to start testing.

✧ status: As shown in mark 7 of Figure 24, it serves to display running state of each Site.




The figure above indicates the state of “Ongoing”.


The figure above indicates the state of “Success”.


The figure above indicates the state of “Failure”.

For convenience of subsequent maintenance, it’s highly recommended to mark the error items and classify them.

✧ data: As shown in mark 8 of Figure 24, it serves to display test result.

Please refer to **Appendix 1** Test Item List On PC Software “EvkMonitor” for details about test items and corresponding maintenance suggestions.

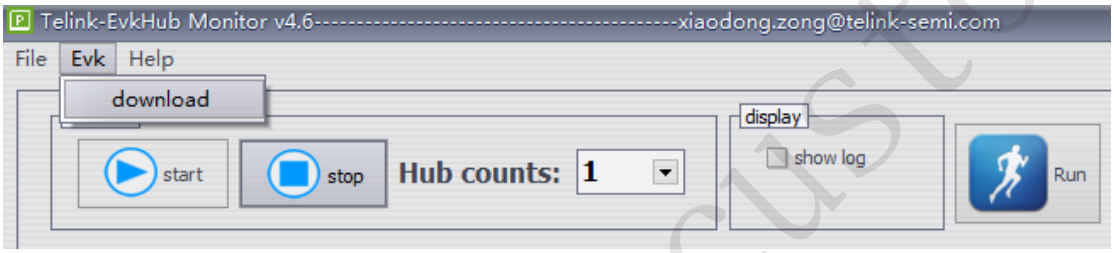
# 5 Update PCBA (DUT) Firmware

In this section, Jig2 Site0 is taken as an example to introduce how to update PCBA firmware when needed.

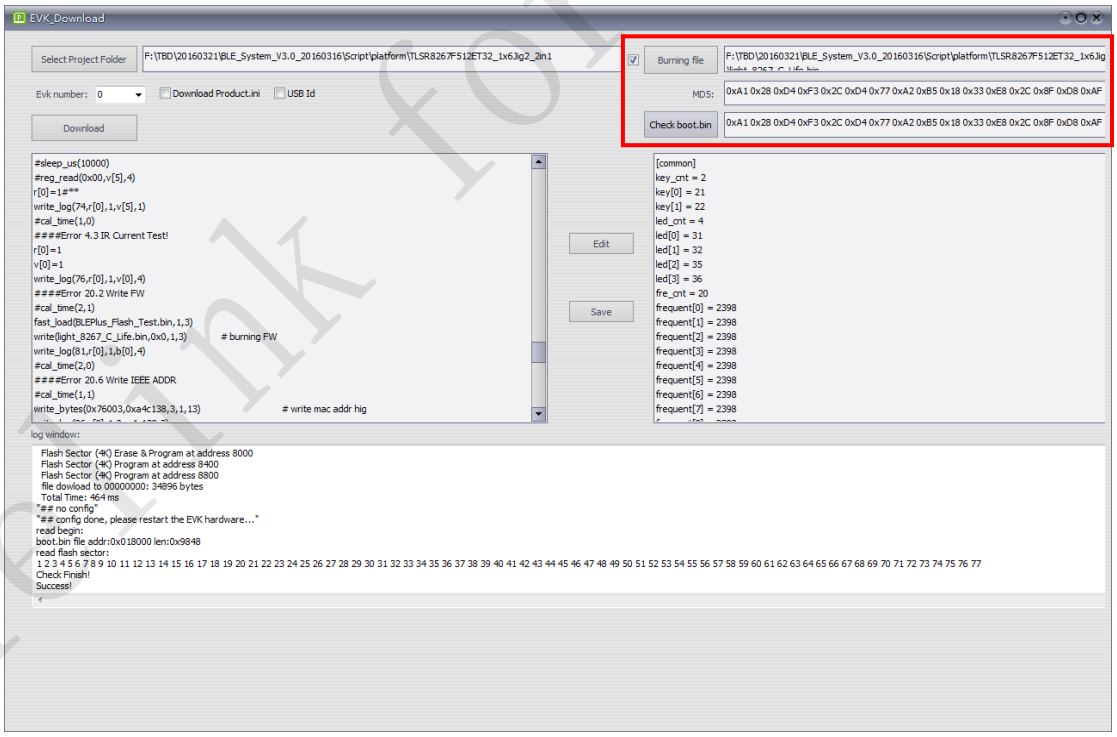
Connect Jig2 Site0 (i.e. EVK0) with PC via an USB cable.

**Note:** Only the target board should be connected with PC, while other Sites must be disconnected from PC.

Double click the "EvkMonitor.exe" under the folder "BLE_System_V3.2_xxx\Script\Monitor".



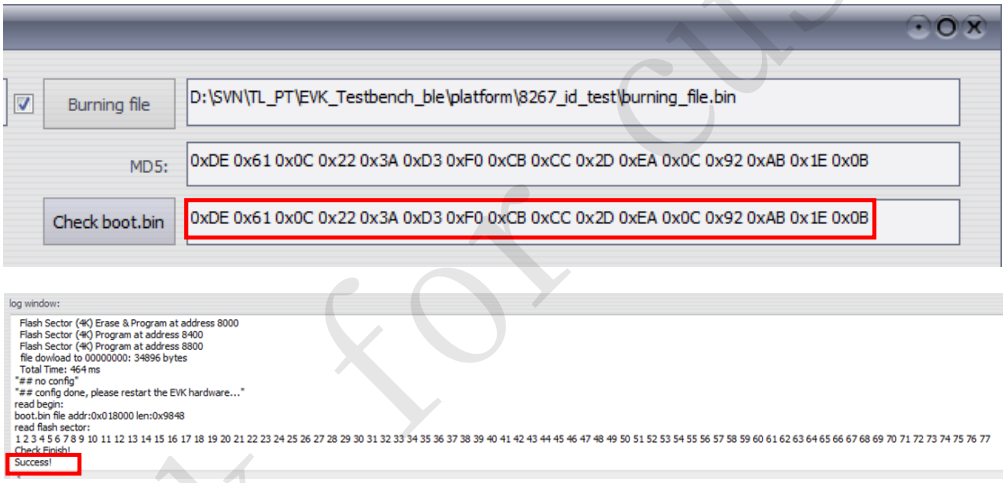

Click "download" under the menu "Evk" to open the burning interface.



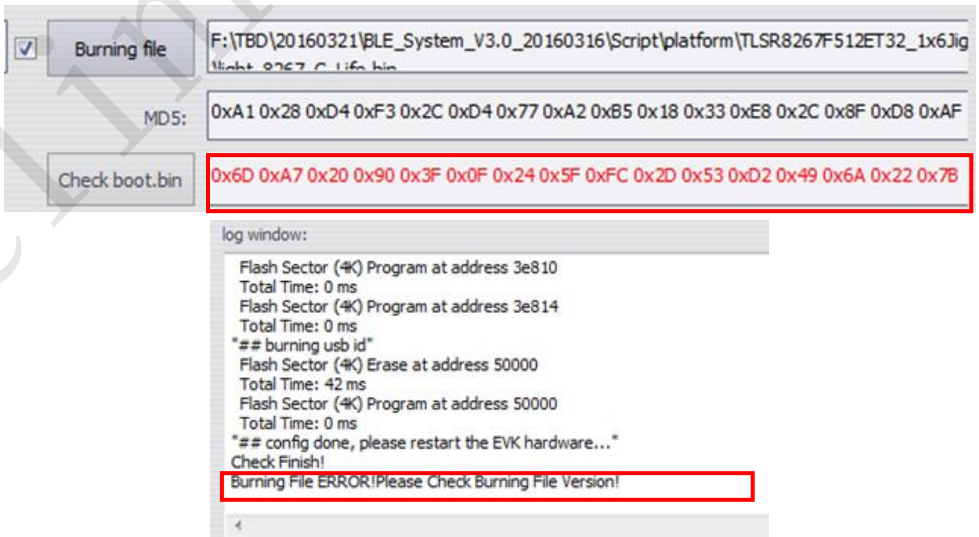

To update firmware only, it's not needed to modify test.tls and product.ini for the EVK daughter board.

1. Tick the box in front of “Burning file”. Then click the “Burning file” button and select the target bin file (no limitation to the file name) in the pop-out window. The path of the selected bin file will be available in the box behind the “Burning file” button. The MD5 code calculated by the bin file will be available in the box next to the “MD5”.
2. Click the “Download” button. The target bin file automatically replaces the previous boot.bin under the project directory, and it will be burned into the EVK daughter board.

After firmware is burned, user can check if the firmware is successfully updated in the EVK daughter board by clicking the “Check boot.bin” button. The result will be available in the log window and the box next to the “Check boot.bin” button.




Firmware update success




Firmware update failure

After the firmware for Jig2 Site0 is successfully updated, power cycle the EVK daughter board, then it's ready for use.

Similarly firmware can be updated for each Site of Jig2, as well as each Site of other Jigs.

# Appendix 1 Test Item List On PC Software "EvkMonitor"

Actual test items are determined by concrete test plan. Herein two examples are given.

1) Example 1: DUT is Remote Control board with flash, IR and audio input.

| Index | Name | Description | Parameter | Maintenance Suggestion |
|---|---|---|---|---|
| 0 | CurProtection | current protection:<br>test DUT current | current value | Maybe soldering problem.<br>Re-solder IC. |
| 1 | GpioShort | test if there is any GPIO pins short wired | show the two pins if there is a short;<br>if not, its value will be 0 | |
| 2 | TpHigh | TP high/ low frequency test:<br>Carry out Tx modulation calibration to ensure RF Tx quality | cap value | RF related.<br>Test again; if failed, temporarily mark it as rejected product, and wait for subsequent analysis. |
| 3 | TpLow | | cap value | |
| 4 | TxHiCnt | tx high frequency counting value/power/frequency offset/current test:<br>EVK receives packets transmitted by DUT at high frequency point, and thus to test DUT Tx performance at high frequency point.<br>Test parameters are DUT Tx packet number, DUT Tx power, DUT Tx frequency offset and DUT Tx current, successively. | cnt num | |
| 5 | TxHiPower | | rf energy | |
| 6 | TxHiFreoffset | | frequency offset | |
| 7 | TxHiCurrent | | current value | |
| 8 | TxLoCnt | tx low frequency counting value/power/frequency offset/current test:<br>EVK receives packets transmitted by DUT at low frequency point, and thus to test DUT Tx performance at low frequency point.<br>Test parameters are DUT Tx packet number, DUT Tx power, DUT Tx frequency offset and DUT Tx current, successively. | cnt num | |
| 9 | TxLoPower | | rf energy | |
| 10 | TxLoFreoffset | | frequency offset | |
| 11 | TxLoCurrent | | current value | |

| Index | Name | Description | Parameter | Maintenance Suggestion |
|---|---|---|---|---|
| 12 | RxLoCnt | rx low frequency counting value/power/current test:<br>DUT receives packets transmitted by EVK at low frequency point, and thus to test DUT Rx performance at low frequency point.<br>Test parameters are EVK Tx packet number, EVK Tx power and EVK Tx current, successively. | cnt num | RF related.<br>Test again; if failed, temporarily mark it as rejected product, and wait for subsequent analysis. |
| 13 | RxLoPower | | rf energy | |
| 14 | RxLoCurrent | | current value | |
| 15 | RxHiCnt | rx high frequency counting value/power/current test:<br>DUT receives packets transmitted by EVK at high frequency point, and thus to test DUT Rx performance at high frequency point.<br>Test parameters are EVK Tx packet number, EVK Tx power and EVK Tx current, successively. | cnt num | |
| 16 | RxHiPower | | rf energy | |
| 17 | RxHiCurrent | | current value | |
| 18 | CancleFlashProtection | cancel flash protection:<br>Cancel DUT flash write protection for following flash erase and test. | 0, always | Flash related.<br>Maybe soldering problem, re-solder pins related to Flash. |
| 19 | FlashZero | set flash as 0/ 0xff:<br>Write DUT flash with all “0” or all “1” to test flash write operation. | size | |
| 20 | FlashErase | | size | |
| 21 | DsSlpCur | deep sleep current/wakeup, suspend current/wakeup test:<br>Make DUT enter low-power mode (deep sleep/suspend) and then wake it up via EVK, thus to test current in deep sleep mode, wakeup function from deep sleep mode, current in suspend mode and wakeup function from suspend mode. | current value | Maybe bad contact with thimble. Check if there’s enough solder paste for the test points of thimble and PCBA. |
| 22 | DsSlpWkp | | reg value | |
| 23 | SuspendCur | | current value | |
| 24 | SuspendWkp | | reg value | |

| Index | Name | Description | Parameter | Maintenance Suggestion |
|---|---|---|---|---|
| 25 | IRCur | IR current test:<br>Make DUT enter IR state via EVK and test the current at IR state. | current value | IR current problem. Check IR circuit. |
| 26 | Amic | Amic test:<br>3V3DUT of EVK supplies power for buzzer, while PIN48 outputs high level to make buzzer board generate square wave signal which drives buzzer to beep. Test DUT register value at this state. | register value | Detect Amic circuit |
| 27 | FlashWrite | write flash:<br>write bin file into DUT flash | If err, err address;<br>if ok it's 0 | Flash related.<br>Maybe soldering problem, re-solder pins related to Flash. |
| 28 | WriteID | write id(part of ieee id):<br>write ID information into DUT flash | id | IEEE address to verify Jig status.<br>Index 27 is fixed value;<br>Index 28 is dynamically increasing value |
| 29 | WriteBytes | write bytes (part of ieee id):<br>write specific information into DUT flash | id | |
| 30 | FlashProtect | protect flash:<br>carry out write protect operation for DUT flash | 1, always | Flash related.<br>Maybe soldering problem, re-solder pins related to Flash. |
| 31 | FlashWriteLarger | write flash:<br>check DUT flash content to ensure correct burning operation | If err, err address;<br>if ok it's 0 | |
| 32 | Load | load status:<br>test connection between EVK and DUT | No para | Contact problem. Check contact between thimble and PCBA. |

2) Example 2: DUT is MKD (Mouse, Keyboard, Dongle) set with OTP.

| Index | Name | Description | Parameter | Maintenance Suggestion |
|---|---|---|---|---|
| 0 | CurProtection | current protection:<br>test DUT current | current value | Maybe soldering problem.<br>Re-solder IC. |
| 1 | GpioShort | test if there is any GPIO pins short wired | show the two pins if there is a short;<br>if not, its value will be 0 | |
| 2 | TpHigh | TP high/ low frequency test:<br>Carry out Tx modulation calibration to ensure RF Tx quality | cap value | RF related.<br>Test again; if failed, temporarily mark it as rejected product, and wait for subsequent analysis. |
| 3 | TpLow | | cap value | |
| 4 | TxHiCnt | tx high frequency counting value/power/frequency offset/current test:<br>EVK receives packets transmitted by DUT at high frequency point, and thus to test DUT Tx performance at high frequency point.<br>Test parameters are DUT Tx packet number, DUT Tx power, DUT Tx frequency offset and DUT Tx current, successively. | cnt num | |
| 5 | TxHiPower | | rf energy | |
| 6 | TxHiFreoffset | | frequency offset | |
| 7 | TxHiCurrent | | current value | |
| 8 | TxLoCnt | tx low frequency counting value/power/frequency offset/current test:<br>EVK receives packets transmitted by DUT at low frequency point, and thus to test DUT Tx performance at low frequency point.<br>Test parameters are DUT Tx packet number, DUT Tx power, DUT Tx frequency offset and DUT Tx current, successively. | cnt num | |
| 9 | TxLoPower | | rf energy | |
| 10 | TxLoFreoffset | | frequency offset | |
| 11 | TxLoCurrent | | current value | |

| Index | Name | Description | Parameter | Maintenance Suggestion |
|---|---|---|---|---|
| 12 | RxLoCnt | rx low frequency counting value/power/current test:<br>DUT receives packets transmitted by EVK at low frequency point, and thus to test DUT Rx performance at low frequency point.<br>Test parameters are EVK Tx packet number, EVK Tx power and EVK Tx current, successively. | cnt num | RF related.<br>Test again; if failed, temporarily mark it as rejected product, and wait for subsequent analysis. |
| 13 | RxLoPower | | rf energy | |
| 14 | RxLoCurrent | | current value | |
| 15 | RxHiCnt | rx high frequency counting value/power/current test:<br>DUT receives packets transmitted by EVK at high frequency point, and thus to test DUT Rx performance at high frequency point.<br>Test parameters are EVK Tx packet number, EVK Tx power and EVK Tx current, successively. | cnt num | |
| 16 | RxHiPower | | rf energy | |
| 17 | RxHiCurrent | | current value | |
| 18 | DsSlpCur | deep sleep current/wakeup, suspend current/wakeup test:<br>Make DUT enter low-power mode (deep sleep/suspend) and then wake it up via EVK, thus to test current in deep sleep mode, wakeup function from deep sleep mode, current in suspend mode and wakeup function from suspend mode. | current value | Maybe bad contact with thimble. Check if there's enough solder paste for the test points of thimble and PCBA. |
| 19 | DsSlpWkp | | reg value | |
| 20 | SuspendCur | | current value | |
| 21 | SuspendWkp | | reg value | |
| 22 | EnableVPP | DUT enables VPP voltage to prepare for following FW burning. | | Check soldering of external 1uF cap connected to the DUT's VPP pin. |

| Index | Name | Description | Parameter | Maintenance Suggestion |
|---|---|---|---|---|
| 23 | WriteFW | write bin file into DUT OTP | | |
| 24 | WriteID | write ID information into DUT OTP | | |
| 25 | WriteConfigPara | Write specific configuration information into DUT OTP | | |
| 26 | CheckFW | Check the contents of DUT OTP to confirm FW burning result | | |
| 27 | Load | load status:<br>test connection between EVK and DUT | No para | Contact problem. Check contact between thimble and PCBA. |

## Appendix 2： Hardware List

| Type | Number | Spec | Note |
|---|---|---|---|
| Main board | 1 | C1T42A19_V1.4 | Assembled on the Main board |
| BLE EVK daughter board | 6 | C1T42A20_V3.3 | |
| Power board | 1 | C1T42A36_V2.0 | |
| Flange plate | 6 | MA-SMA-KKF 2-head flange | |
| Screw | 12 | PM2.5X8 screw | |
| Nut | 12 | M2.5 nut | |
| Short RF cable | 6 | SMA-MMCX cable 4cm | |
| HDMI cable | 6 | HDMI1.4A/A-A interface/50cm | |
| Thimble board | 6 | C1T42A19_V3.1 | |
| Buzzer board | 6 | C1T64A3_V2.0 | Not supplied by default. Only supplied for DUT with MIC. |
| STP (Shielded Twisted Pair) cable | 1 | 2-cord/RV0.5/1.2m | |
| External antenna board | 6 | ANT_01 | |
| Long RF cable | 6 | SMA90°-SMA90° cable-30cm | |
| Display board | 1 | C1T42A19_V2.2 | |
| FC-40P gray flat cable | 6 | 2-end 2.54mm*2*12/28AWG/ 105℃/Grey/50cm | |
| 18P rainbow cable | 1 | 18-cord/16AWG/1m | |
| Power adapter | 1 | Lenovo ADP-90DD B<br>Input：100-240V 1.5A<br>Output：20V 4.5A | |
| USB2.0 hub | 1 | Unitek/7 interfaces/USB2.0 hub | |
| Micro USB cable | 6 | USB2.0/28AWG/30cm, 90°/30V/80℃/A3-B | |
| Carton, size 6 | 1 | Standard 3-layer 260*150*180mm | |

## Appendix 3： Pins on test site of Main board

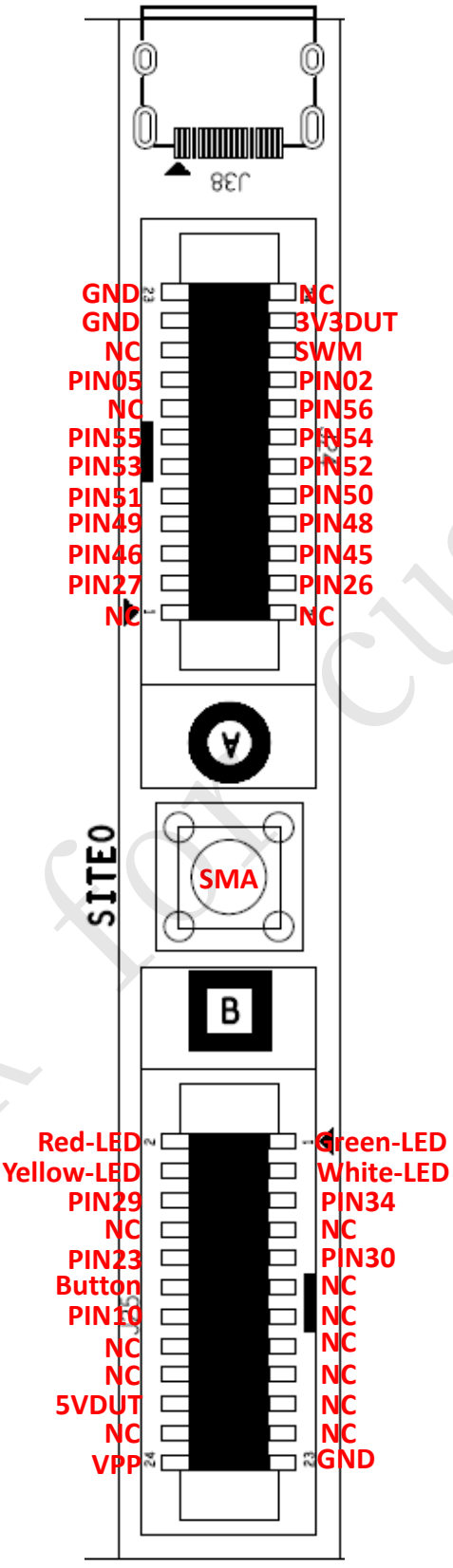



Figure 25 Pins on test site of Main board

***Notes:**

1) In Figure 25, NC indicates no connection.
2) Test pins on connector A should be connected by using STP (Shielded Twisted Pair) cables.

## Appendix 4: Dimension chart of Main board, Thimble board, Display board, EVK daughter board and Buzzer board

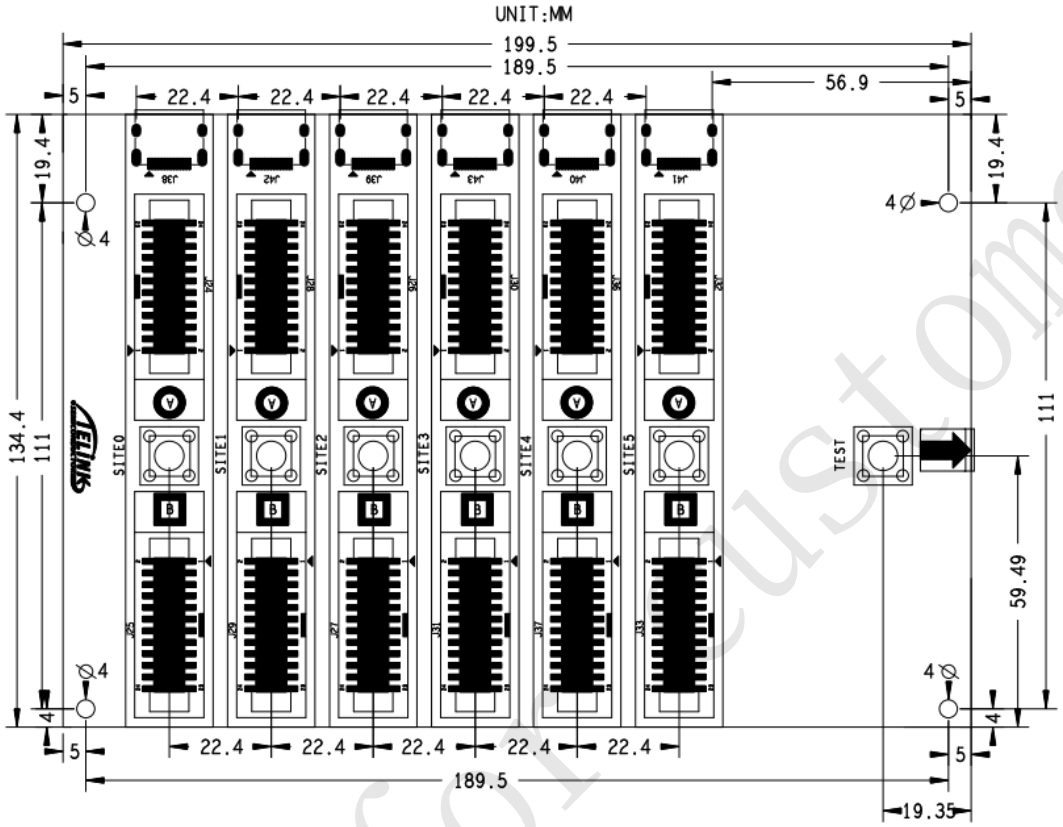



Figure 26 Dimension chart of Main board

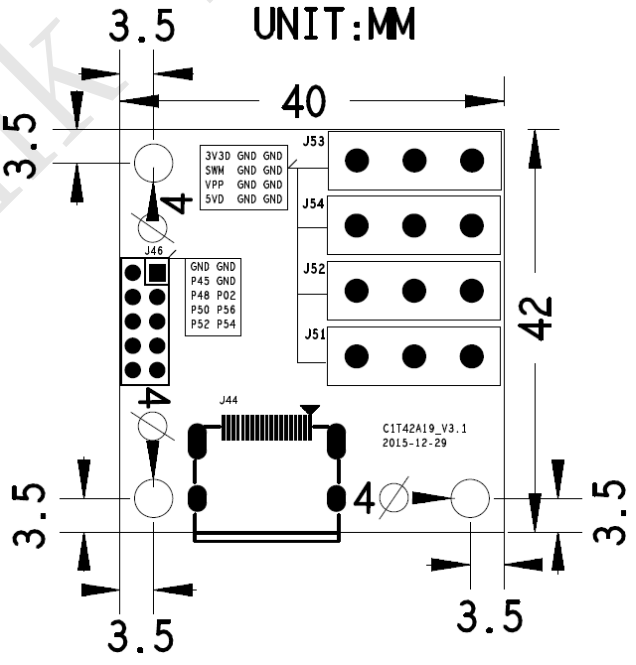



Figure 27 Dimension chart of Thimble board

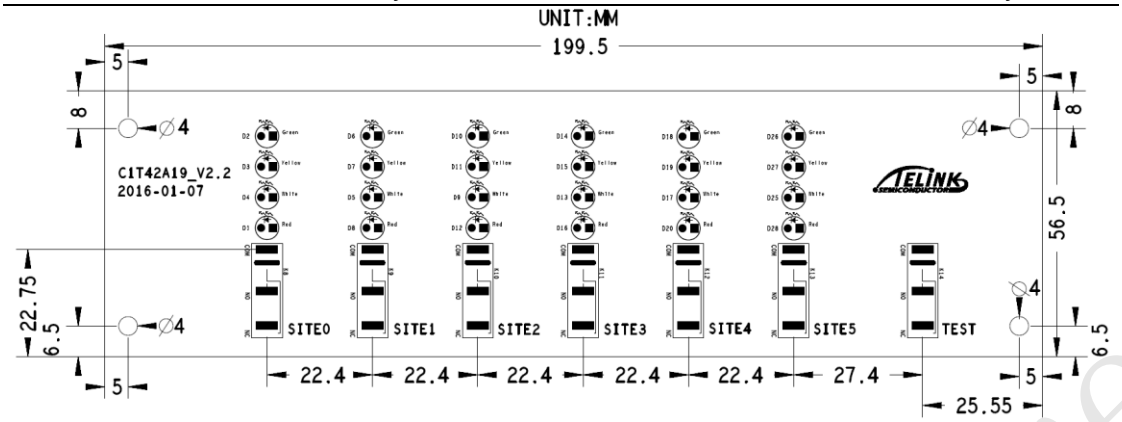



Figure 28 Dimension chart of Display board

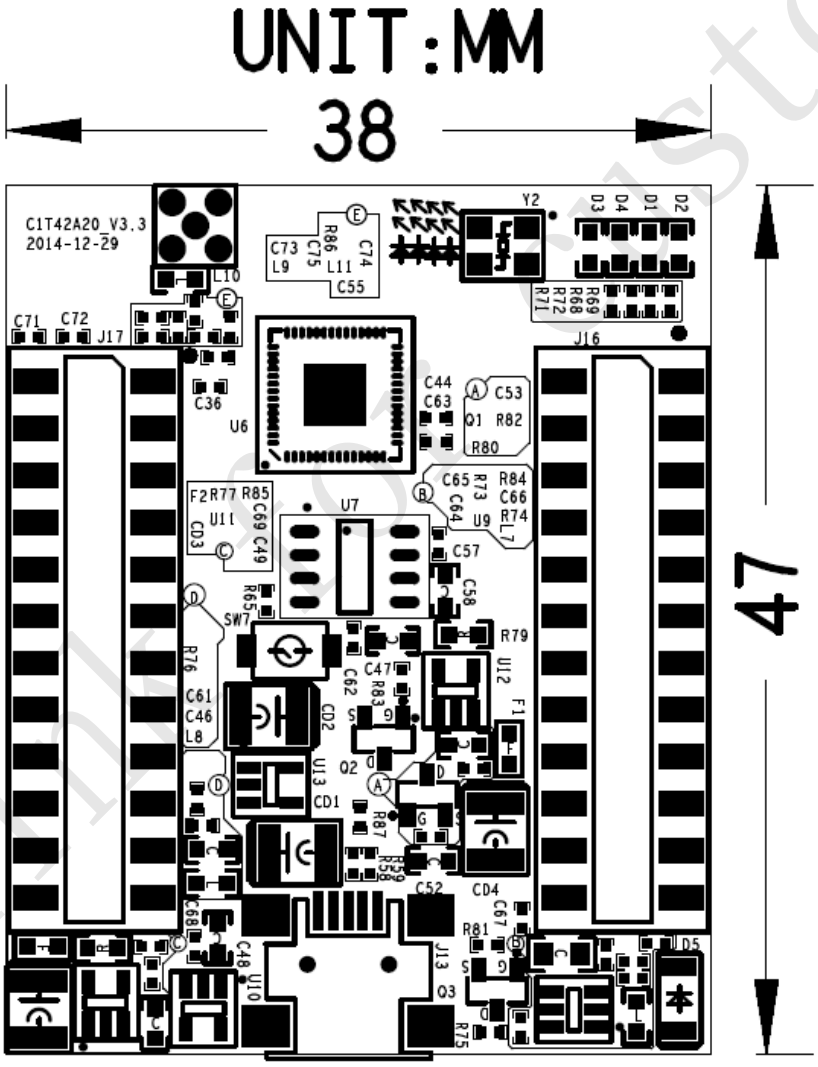



Figure 29 Dimension chart of EVK daughter board

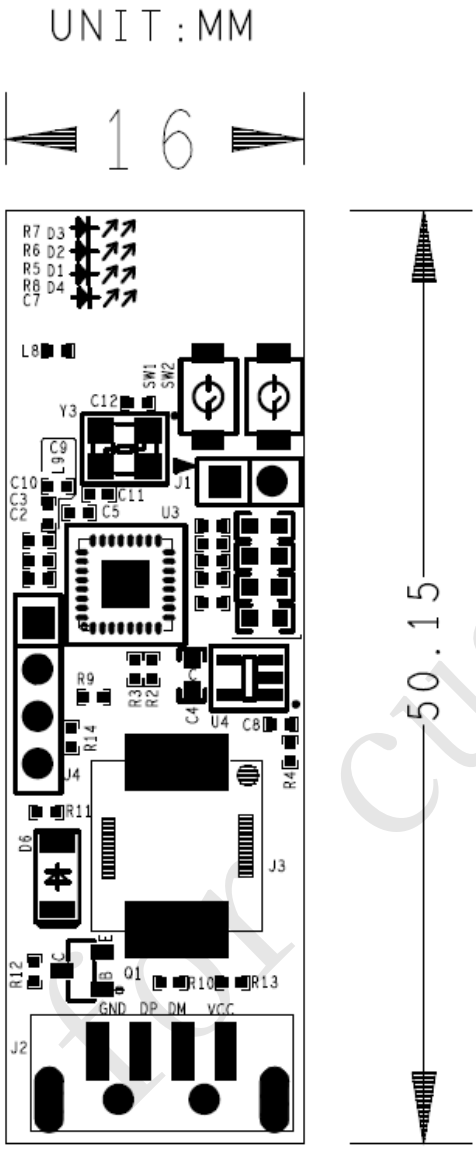



Figure 30 Dimension chart of Buzzer board