

ByteTransformer: A High-Performance Transformer Boosted for Variable-Length Inputs

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Abstract—Transformers have become keystone models in natural language processing over the past decade. They have achieved great popularity in deep learning applications, but the increasing sizes of the parameter spaces required by Transformer models generate a commensurate need to accelerate performance. Natural language processing problems can also be routinely faced with variable-length sequences, as word counts commonly vary among sentences. Existing deep learning frameworks pad variable-length sequences to a maximal length, which adds significant memory and computational overhead. In this paper, we present ByteTransformer, a high-performance Transformer boosted for variable-length inputs. We propose a padding-free algorithm that liberates the entire Transformer from redundant computations on wasted padded tokens. In addition to algorithmic-level optimization, we provide architecture-aware optimizations for Transformer functional modules, especially the performance-critical algorithm Multi-Head Attention (MHA). Experimental results on an NVIDIA A100 GPU with variable-length sequence inputs validate that our fused MHA outperforms the standard PyTorch MHA by 6.13x. The end-to-end performance of ByteTransformer for a standard BERT Transformer model surpasses state-of-the-art Transformer frameworks, such as PyTorch JIT, TensorFlow XLA, Tencent TurboTransformer and NVIDIA FasterTransformer, by 87%, 131%, 138% and 46%, respectively.

Index Terms—Transformer, BERT, Fused Multi-head Attention, Performance Optimization, GPU

I. INTRODUCTION

The Transformer model [1] is a proven effective architecture widely used in a variety of Deep Learning (DL) applications, such as language modeling [2]–[5], neural machine translation [1], [6] and recommendation systems [7], [8]. The last decade has witnessed rapid developments in natural language processing (NLP) pre-training models based on the Transformer model, such as Seq2seq [1], GPT-2 [9] and XLNET [3], which have also greatly accelerated the progress of NLP. Of all the pre-training models based on transformers, Bidirectional Encoder Representations from Transformers (BERT), proposed in 2018 [2], is arguably the most seminal, inspiring a series of subsequent works and outperforming reference models on a dozen NLP tasks at the time of creation.

BERT-like models consume increasingly larger parameter space and correspondingly more computational resources. When BERT was discovered, a large model required 340

million parameters [10], but currently a full GPT-3 model requires 170 billion parameters [11]. The base BERT model requires 6.9 billion floating-point operations to inference a 40-word sentence, and this number increases to 20 billion when translating a 20-word sentence using a base Seq2seq model [12]. The size of the parameter space and the computational demands increase the cost of the training and inference for BERT-like models, which requires the attention of the DL community in order to accelerate these models.

To exploit hardware efficiency, DL frameworks adopt a batching strategy, where multiple batches are executed concurrently. Since batched execution requires task shapes in different batches to be identical, DL frameworks presume fixed-length inputs when designing the software [13]–[16]. However, this assumption cannot always hold, because Transformer models are often faced with variable-length input problems [10], [12]. In order to deploy models with variable-length inputs directly to conventional frameworks that support only fixed-length models, a straightforward solution is to pad all sequences with zeros to the maximal sequence length. However, this immediately brings in redundant computations on wasted padded tokens. These padded zeros also introduce significant memory overhead that can hinder a large Transformer model from being efficiently deployed.

Existing popular DL frameworks, such as Google TensorFlow with XLA [17], [18], Meta PyTorch with JIT [19], and OctoML TVM [20], leverage domain-specific just-in-time compilation to boost performance. Another widely-adopted strategy to generate low-level performance optimization is delicate manual tuning: NVIDIA TensorRT [21], a DL runtime, falls into this category. Yet all of these frameworks require the input sequence lengths to be identical to exploit the speedup of batch processing. To lift the restriction on fixed sequence lengths, Tencent [12] and Baidu [10] provide explicit support for models with variable sequence lengths. They group sequences with similar lengths before launching batched kernels to minimize the padding overhead. However, this proactive grouping approach still introduces irremovable padding overhead when grouping and padding sequences with similar yet different lengths.

In contrast to training processes that can be computed

offline, the inference stage of a serving system must be processed online with low latency, which further raises the performance requirements of DL frameworks. A highly efficient DL inference framework for NLP models requires delicate kernel-level optimizations. When facing variable-length inputs, explicit end-to-end designs are also needed to avoid wasted computations on zero tokens. However, none of the existing DL frameworks are able to meet expectations from both perspectives. In order to remedy this deficit, we present ByteTransformer, a highly efficient Transformer framework optimized for variable-length inputs in NLP problems. We not only design an algorithm that frees the entire Transformer of padding when dealing with variable-length sequences, but also provide a set of hand-tuned fused GPU kernels to minimize the cost of accessing GPU global memory. More specifically, our contributions include:

- We design and develop ByteTransformer, a high-performance GPU-accelerated Transformer optimized for variable-length inputs. ByteTransformer has been deployed to serve world-class applications including TikTok and Douyin of ByteDance.
- We propose a padding-free algorithm that packs the input tensor with variable-length sequences and calculates the positioning offset vector for all Transformer operations to index. This algorithm keeps the whole Transformer pipeline free from padding and calculations on zero tokens.
- We propose a fused Multi-Head Attention (MHA) to alleviate the memory overhead of the intermediate matrix, which is quadratic to the sequence length, in MHA without introducing redundant calculations due to padding for variable-length inputs. Part of our fused MHA has been deployed in the production code base of NVIDIA CUTLASS.
- We hand-tune the memory footprints of layer normalization, adding bias and activation to squeeze the final performance of the system.
- We benchmark the performance of ByteTransformer on an NVIDIA A100 GPU. Experimental results demonstrate our fused MHA outperforms standard PyTorch attention by 6.13X. Regarding the end-to-end performance of standard BERT Transformer, ByteTransformer surpasses PyTorch, TensorFlow, Tencent TurboTransformer and NVIDIA FasterTransformer by 87%, 131%, 138% and 46%, respectively.

The rest of the paper is organized as follows: we introduce background and related works in Section II, and then detail our systematic optimization approach in Section III. Evaluation results are given in Section IV. We conclude our paper and present future work in Section V.

II. BACKGROUND AND RELATED WORKS

In this section, we overview the background information of a Transformer model, including the encoder-decoder architecture and multi-head attention (MHA). We also survey the related works on DL framework acceleration.

A. The Transformer architecture

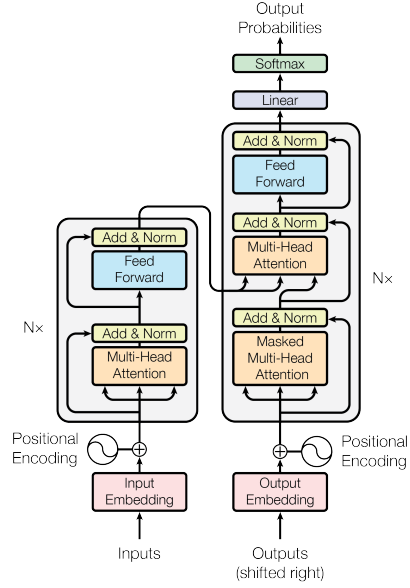


Fig. 1: The Transformer architecture [1]

Figure 1 shows the encoder-decoder model architecture of Transformer. A Transformer model is composed of stacks of multiple encoder and decoder layers. In an encoder layer, there is a multi-head attention (MHA) layer followed by a feed forward network (FFN) layer. A layer normalization (layernorm) operation is applied after both MHA and FFN. In a decoder layer, there are two sets of consecutive MHA layer and one FFN layer, where each operation is normalized by conducting layernorm. The FFN is used to improve the capacity of the model. In practice, FFN is implemented by multiplying the tensor by a larger scaled tensor using GEMM. Here we skip the embedding descriptions in the figure, and refer an interested reader to [1] for details. Although we show both encoder and decoder modules of a Transformer, a BERT Transformer model only contains the encoder part [2]. In this paper, we present optimizations for an encoder-only BERT Transformer model, and one can easily extend to other transformers that contain the decoder part using the optimizations and algorithm proposed in the paper.

Self-attention is a key module of the Transformer architecture. Conceptually, self-attention computes the significance of each position of the input sequence, with the information from other positions considered. A self-attention receives three input tensors: query (Q), key (K) and value (V). Self-attention can be split into multiple heads. The Q and K tensors are first multiplied (1^{st} GEMM) to compute dot product of the query against all keys. Softmax is then applied to calculate the weights corresponding to the value tensor. Each head of the output tensor is concatenated before going through another linear layer by multiplying against tensor V (2^{nd} GEMM). Expressing self-attention in mathematical formula, we have:

$$Attention(Q, K, V) = softmax(\frac{QK^T}{\sqrt{d_k}}) \times V \quad (1)$$

Whereas the formula of multi-head attention is: $Multihead(Q, K, V) = Concat(head_i, \dots, head_h)$, here $head_i = Attention(Q_i, K_i, V_i)$.

B. Related works on DL acceleration

Software systems employ architectural-aware optimizations to exploit the hardware efficiency [22]–[25]. Performance optimization for DL frameworks has been extensively studied. The conventional DL frameworks, such as PyTorch, TensorFlow, TVM and TensorRT are designed explicitly for fixed-length input tensors. When dealing with NLP problems with variable-length input, one must pad all sequences to the maximal length, which leads to significant wasted calculations on useless tokens. A few DL frameworks, such as Tencent TurboTransformer [12] and NVIDIA FasterTransformer [26], employ explicit designs for variable-length inputs. TurboTransformer designs run-time algorithms to group and pad sequences with similar lengths to minimize the padding overhead. It also proposes run-time memory scheduling strategy to improve the end-to-end performance. Since kernel-level optimizations are of the same significance as algorithmic optimizations, NVIDIA FasterTransformer is back-ended and accelerated by the vendor’s close-sourced libraries such as TensorRT and cuBLAS [27].

In addition to the end-to-end performance acceleration, the community has also made efforts on improving the key algorithm of Transformer — MHA. Among which, PyTorch provides a standard implementation of MHA [28]; NVIDIA TensorRT provides fused MHA for short sequences whose lengths are smaller than 512 [29]. To scale the fused MHA to long sequences, Stanford researchers propose FlashAttention [30], which assumes identical shapes of inputs and assigns the workload of a whole attention unit to a single CTA. However, FlashAttention brings significant wasted computations if input sequence lengths are variable. In contrast, our fused MHA provides high performance for both short and long sequences without redundant calculations for variable-length inputs.

TABLE I. Summarizing optimizations of state-of-the-art transformers.

	variable-len support	kernel tuning	fused MHA	kernel fusion
Tensorflow XLA	no	yes	no	no
PyTorch JIT	no	yes	no	no
FasterTransformer	yes	yes	≤ 512	no
TurboTransformer	yes	yes	no	partially
ByteTransformer	yes	yes	yes	yes

Table I surveys state-of-the-art transformers. TensorFlow and PyTorch provide tuned kernels but require padding for variable-length inputs. NVIDIA FasterTransformer and Tencent TurboTransformer, though support variable-length inputs, do not perform comprehensive kernel fusion or explicit optimization for the hot-spot algorithm MHA with any sequence lengths. Our ByteTransformer, in contrast, starting from a systemic profiling to locate bottleneck algorithms, precisely tunes a series of kernels including the key algorithm MHA.

We also propose the zero padding algorithm that completely enables the whole Transformer to be free from redundant calculations for variable-length inputs.

III. DESIGNS AND OPTIMIZATIONS

In this section, we present our algorithmic and kernel-level optimizations to improve the end-to-end performance of BERT Transformer under variable-length inputs.

A. Math expression of BERT Transformer encoder

Figure 2 (a) shows the basic architecture of the Transformer encoder. An input tensor is fed into the BERT pipeline. It is then multiplied against the built-in attribute matrix to perform the Q, K, V positioning encoding. This can be computed in three separated GEMMs, or in a batched manner if QKV matrices are packed to continuous memory space. In our implementation, we pack these three matrices and launch a single batched GEMM kernel to reduce the run-time kernel launch overhead. Bias matrices of QKV are added to the encoded tensor and then goes through the self-attention module. Besides multi-head attention, other functioning modules in BERT Transformer encode include projection, feed forward network and layer normalization. The encoder pipeline can be represented in a series of math operations, including six GEMMs (marked in light purple) and other memory-bound operations (marked in light blue).

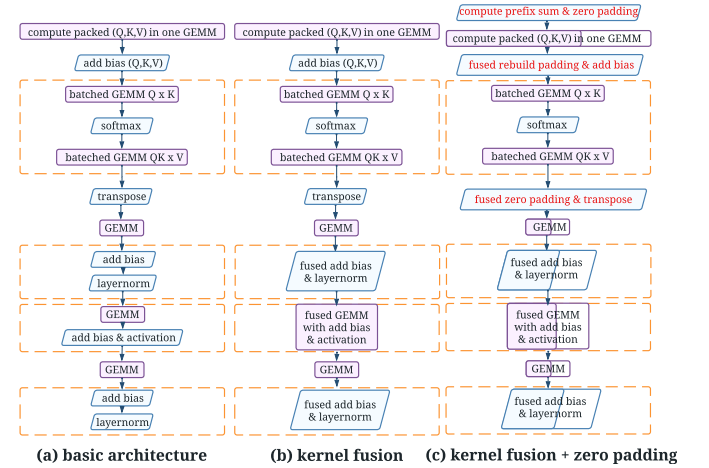


Fig. 2: BERT Transformer architecture and optimizations

B. Profiling for single-layer standard BERT Transformer

We implement the pipeline of Figure 2 (a) by calling cuBLAS and profile its single-layer performance on an NVIDIA A100 GPU. We adopt the standard BERT Transformer configuration (batch size: 16, head number: 12, head size: 64) and profile for two different sequence lengths: 256 and 1024.

Figure 3 shows the performance breakdown for two sequence lengths. GEMM0 to GEMM3 denote the consecutive four GEMMs, excluding batched GEMMs in the attention module, presented in Figure 2 (a). The two sets of *add*

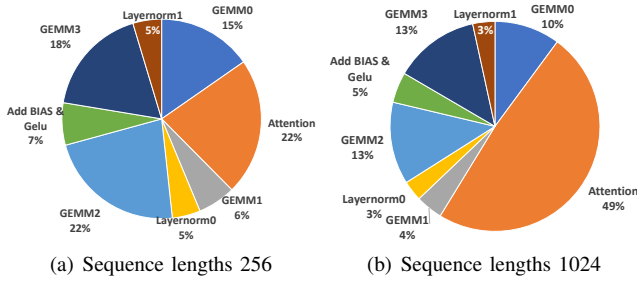


Fig. 3: Performance breakdown of BERT Transformer

bias and *layernorm* operations are denoted as `layernorm0` and `layernorm1`. The profiling results demonstrate that the compute-bound GEMM operations account for 61% and 40% of the total execution time for both test cases. The attention module, which contains a softmax and two batched GEMMs, is the most time-consuming part of the Transformer. As the sequence length increases to that of a GPT-2 model (1024), attention turns to accounts for 49% of the total execution time, while the remaining memory-bound operations (*layernorm*, *add bias* and *activation*) only takes 11%-17%.

C. Fusing memory-bound operations of BERT Transformer

Since cuBLAS integrates with delicate architectural-aware optimizations for extreme GEMM performance, presumably there remain very limited accelerating opportunities. Therefore, we turn our eyes to optimizing the modules containing memory-bound operations, such as attention (with softmax), feed forward network (with *layernorm*) and add bias followed by element-wise activation. We improve these operations by fusing separated kernels and re-use data in registers to reduce global memory access. Figure 2 (b) presents the BERT Transformer pipeline with memory-bound kernel fusion, where we fuse *layernorm* and activation with their consecutive kernels.

1) *Add bias and layer normalization*: These operations account for 10% and 6% of the overall execution time for sequence lengths 256 and 1024, respectively. After MHA, the result tensor (`valid_word_cnt × hidden_dim`) needs to first be added upon the input tensor (*bias*) and perform layer normalization. Here hidden dimension (`hidden_dim`) equals `head_num × head_size`. In standard BERT configuration, head number and head size are fixed to 12 and 64. The naive implementation introduces two rounds of memory access to load and store the tensor. We provide a fused kernel that only needs to access the global memory in one round to finish both *layernorm* and adding bias. Kernel fusion for this sub-kernel improves the performance by 61%, which accordingly increases the single-layer BERT Transformer performance by 3.2% for sequence lengths ranging 128 to 1024 in average.

2) *add bias and activation*: These operations account for 7% and 5% of the overall execution time for sequence lengths 256 and 1024, respectively. After the projection via matrix multiplication, the result tensor will be added against the input tensor and perform an element-wise activation using GELU [31]. Our fused implementation, rather than storing the GEMM

output to global memory and loading it again to conduct adding bias and activation, re-uses the GEMM result matrix at the register level by implementing a customized and fused CUTLASS [32] epilogue. Experimental results validate that our fused GEMM perfectly hides the memory latency of bias and GELU into GEMM. After this step, we further improve the single-layer BERT Transformer by 3.8%.

D. The zero padding algorithm for variable-length inputs

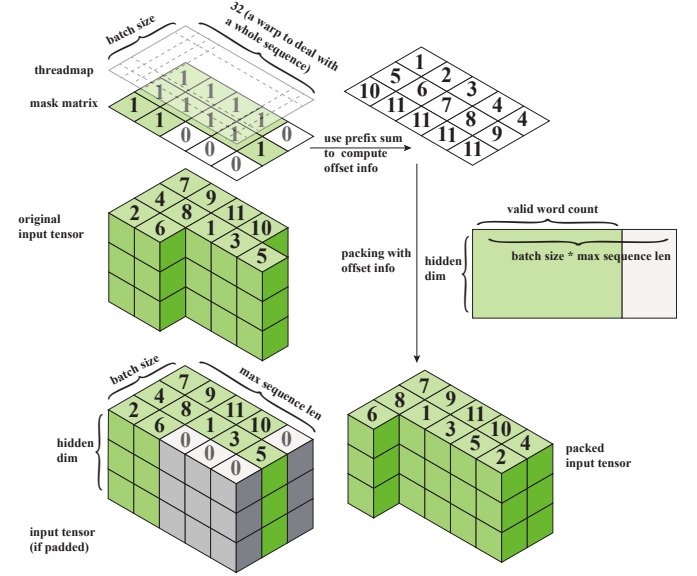


Fig. 4: The zero padding algorithm

Because the real-time serving process receives sentences with various words as input tensor, the sequence lengths can often be different among batches. For such an input tensor composed of sentences with variable lengths, the conventional solution is to pad them to the maximal sequence length with useless tokens, which leads to significant computational and memory overhead. In order to address this issue, we propose the zero padding algorithm to pack the input tensor and store the positioning information for other Transformer operations to index the original sequences.

Figure 4 presents the details of the zero padding algorithm. We use an input tensor with 3 sentences (proceeded in 3 batches) as an example. The longest sentence contains 5 word tokens while the other two have 2 and 4 words. The height of the sample input tensor is 3, which is equal to the hidden dimension. The conventional method is to pad all sentences to the maximal sequence length by filling zeros. Observing that the input mask matrix contains zeros and ones corresponding to the original input tensor, we calculate the prefix sum to obtain the position indices of each sequence in the packed matrix. We implement an efficient CUDA kernel to calculate the prefix sum and the position offset. Each warp computes the prefix sum for tokens of a whole sentence, so in total there are `batch_size` warps assigned in each threadblock for prefix sum calculation. Once the prefix sum is computed, we pack the input tensor to a condensed memory area so that the total number of words used in future calculations is reduced from

$\text{seq_len} \times \text{batch_size}$ to the actual valid word count of the packed tensor.

Figure 2 (c) presents the modifications on BERT Transformer by introducing our zero padding algorithm. Before conducting the positioning encoding, we calculate the prefix sum of the mask matrix to pack the input tensor so that we avoid computations on useless tokens in the first GEMM. Since batched GEMM in MHA requires identical problem shapes among different batches, we unpack the tensor before entering the attention module. Once MHA is completed, we pack the tensor again such that all remaining operations can benefit from the zero padding algorithm. It is worth mentioning that padding and remove padding operations are fused with existing memory-bound footprints such as adding bias and transpose to minimize the overhead led by this feature.

	Baseline	Zero Padding	Zero Padding + fused MHA
GEMM0	$6mk^2$	$6(\alpha \cdot m)k^2$	$6(\alpha \cdot m)k^2$
MHA	$4\frac{m^2}{bs}k$	$4\frac{m^2}{bs}k$	$4\frac{(\alpha \cdot m)^2}{bs}k$
GEMM1	$2mk^2$	$2(\alpha \cdot m)k^2$	$2(\alpha \cdot m)k^2$
GEMM2	$8mk^2$	$8(\alpha \cdot m)k^2$	$8(\alpha \cdot m)k^2$
GEMM3	$8mk^2$	$8(\alpha \cdot m)k^2$	$8(\alpha \cdot m)k^2$

TABLE II. The computation number needed for variable-length inputs, where average sequence length = $\alpha \cdot \text{maximum}$, m denotes $\text{batch_size} \cdot \text{max_seq_len}$, k is denote hidden dimension $\text{head_num} \cdot \text{head_size}$, bs denotes the batch size.

Table II counts the floating point computations of a single-layer BERT Transformer. The computations of memory-bound operations are not included since they are negligible compared with the listed modules. Enabling the zero padding algorithm eliminates redundant computations for all compute-intensive modules other than MHA due to the restrictions of batched GEMM. When the average sequence length is equal to 60% of the maximum, turning on the zero padding algorithm further accelerates the BERT Transformer by 24.7%.

E. Optimizing multi-head attention

The zero padding algorithm, although effectively reduces wasted calculations for variable-length inputs, cannot directly benefit batched GEMM operations in MHA. This disadvantage becomes even worse as the sequence length is increasing. Table II clearly demonstrates that the complexity of MHA is quadratic to the sequence length, while the complexity of all other GEMMs are linear to the sequence length. This motivates us to provide a high-performance fused MHA while maintaining the benefits of the zero padding algorithm. With our fused MHA, attention no longer faces redundant calculation on useless tokens, as shown in Table II.

1) *Unpadded fused MHA for short sequences*: For short input sequences, we hold the intermediate matrix in shared memory and register to fully eliminate the fusible memory overhead. Meanwhile, we access Q , K , V tensors according to the positioning information obtained in the prefix sum calculation step, enabling the MHA module to be free from redundant calculations on padding zeros.

Algorithm III.1: Unpadded fused MHA for short sequences

```

1 /* define skew offset to avoid bank conflict */
2 #define SKEW_HALF 8
3 Shared memory:
4 __half s_kv [max_seq_len][size_per_head + SKEW_HALF];
5 __half s_query [split_seq_len][size_per_head + SKEW_HALF];
6 __half s_logits [max_seq_len][size_per_head + SKEW_HALF];
7 /* warps collaboratively fill s_query with adding bias fused */
8 Load __half2 q_bias
9 for seq_id = warp_id : warp_num : split_seq_len do
10     query = Q[batch_seq_offset + seq_id + thread_offset];
11     offset = seq_id * (head_size + SKEW_HALF) + (lane_id * 2);
12     (__half2 *)s_query[offset] = fast_add(query, k_bias);
13 /* warps collaboratively fill s_kv with adding bias fused */
14 Load __half2 k_bias
15 for seq_id = warp_id : warp_num : batch_seq_len do
16     key = K[batch_seq_offset + seq_id + thread_offset];
17     offset = seq_id * (head_size + SKEW_HALF) + (lane_id * 2);
18     (__half2 *)s_kv[offset] = fast_add(key, k_bias);
19 /* compute Q*K using WMMA */
20 Clear wmma fragment QK to zero
21 for k_id = 0 : head_size / 16 do
22     Load 16x16 wmma fragments of Q
23     Load 16x16 wmma fragments of K
24     Update QK = Q * K + QK using wmma::mma_sync
25 Store fragment QK to s_logits using wmma::store_matrix_sync
26 /* Compute softmax */
27 for seq_id = warp_id : warp_num : batch_seq_len do
28     float logits[max_seq_len];
29     each thread loads a whole sequence to fill local registers
30     /* 1st round of reduction with register-level data re-use */
31     compute max_val in local registers
32     /* register-level data re-use */
33     compute  $P = \exp(P - \text{max})$  and update local registers
34     /* 2st round of reduction with register-level data re-use */
35     compute sum_val in local registers
36     /* register-level data re-use */
37     compute  $P = P / \text{sum\_val}$  and stream to s_logits
38 /* warps collaboratively fill s_kv with adding bias fused */
39 Load __half2 v_bias
40 for seq_id = warp_id : warp_num : batch_seq_len do
41     value = V[batch_seq_offset + seq_id + thread_offset];
42     offset = seq_id * (head_size + SKEW_HALF) + (lane_id * 2);
43     (__half2 *)s_kv[offset] = fast_add(value, v_bias);
44 /* Similar to Q * K so omitting details here */
45 Compute P * V using wmma and stream to global memory

```

Algorithm III.1 shows the pseudo code of our fused MHA for short sequences. We launch a 3-dimensional grid map: $\{\text{head_num}, \text{seq_len}/\text{split_seq_len}, \text{batch_size}\}$. Here split_seq_len is a user-defined parameter to determine the size of a sequence tile preceded by a thread-block (typically set to 32 or 48). The warp count of a threadblock is computed by the maximal sequence length: $\text{split_seq_len}/16 \times (\text{seq_len}/16)$. Each thread-block loads a chunk of Q ($\text{split_seq_len} \times \text{head_size}$), K ($\text{max_seq_len} \times \text{head_size}$) and V ($(\text{head_size} \times \text{max_seq_len})$) into shared memory and computes MHA for a tile of the result tensor. We allocate three shared-memory buffers to hold Q , K , V sub-matrices. Due to the algorithmic nature of MHA, we can re-use K and V chunks in the same shared-memory buffer s_kv . The intermediate matrix of MHA

is held and re-used in another pre-allocated shared-memory buffer `s_logits`.

The workflow of fused MHA for short sequences is straightforward yet efficient. Each thread first loads its own tile of Q and K into shared memory and computes GEMM for $P = Q \times K$. The element-wise adding bias and scaling operations are both fused with the load process to hide the memory latency. GEMM is computed using the CUDA `wmma` intrinsic to leverage tensor cores of NVIDIA Ampere GPUs. The intermediate matrix P is held in shared memory during the reduction. Because we explicitly design this algorithm for short sequences, each thread can load a whole sequence of P from shared memory into register files for both reduction and element-wise exponential transform in softmax. Once the softmax operation is completed, we load a K tile to shared memory to compute the second GEMM $O = P \times V$, and then store the result tensor O to the global memory.

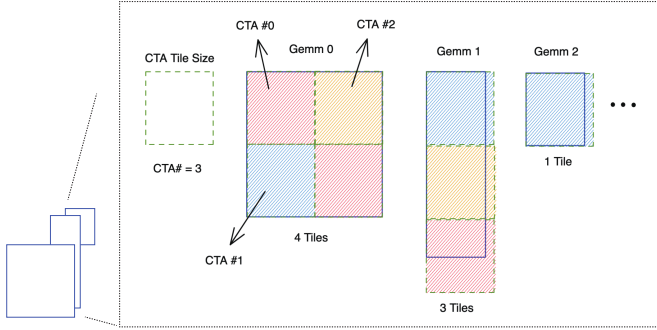


Fig. 5: Grouped GEMM demonstration

2) *Unpadded fused MHA for long sequences*: Because of the limited resources of register file and shared memory, the previous fused MHA is no longer feasible for long sequences. Therefore, we propose a grouped GEMM based fused MHA for large models with variable-length inputs.

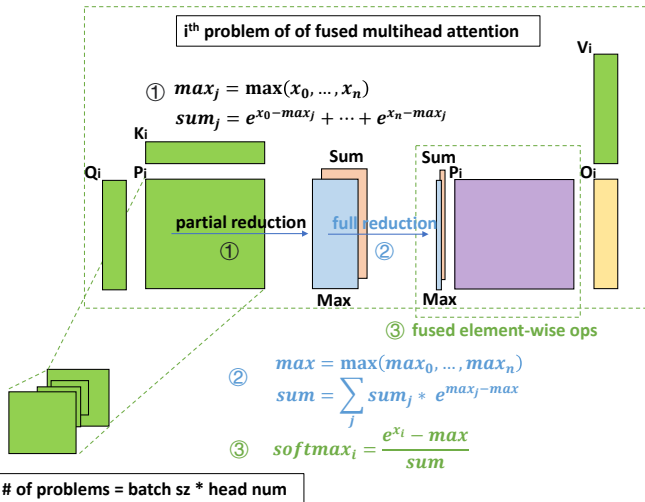


Fig. 6: Grouped GEMM based FMHA. The prototype of our fused MHA has been upstreamed to and released with CUTLASS 2.10. Source codes are available at [33].

The Grouped GEMM idea is first presented by NVIDIA CUTLASS [32]. Different from batched GEMM, where all GEMM sub-problems are required to have identical shapes, grouped GEMM allows arbitrary shapes for sub-problems. This is achieved by a built-in scheduler that iterates over all GEMM sub-problems in a round-robin manner. Figure 5 demonstrates the idea of grouped GEMM using an example with 3 sub-problems. Supposing 3 threadblocks (CTAs) are launched, each CTA calculates a fix-sized CTA tile at each step until all GEMM sub-problems have been covered. GPU computes in waves logically. In the first wave, All three CTAs calculate 3 tiles (light red, light yellow and light blue marked in the figure). And then in the second CTA wave, CTA #0 moves to the bottom-right tile of GEMM 0 while CTA #1 and CTA #2 move to sub-problems of GEMM 1. In the final CTA wave, CTA #0 and CTA #1 continue to compute tasks in GEMM 1 and GEMM 2 while CTA #2 keeps idle because there are no more available tiles in the computational graph.

Since Grouped GEMM lifts the restriction on the shape of sub-problems, it can directly benefit MHA problems with variable-length inputs. Figure 6 presents our grouped GEMM based fused MHA for long sequences. The total number of MHA problems is equal to `batch_size * head_num`. The MHA problems among different batches have different sequence lengths, while sequence lengths within the same batch are identical. The grouped GEMM scheduler iterates over all attention units in a round-robin manner. In each attention unit, we first compute GEMM $P_i = Q_i \times K_i$, and conduct softmax on P_i . The second GEMM $O_i = P_i \times V_i$ provides us with the final attention result. Here i indicates the i^{th} problem of grouped MHA with variable shapes. The softmax operation is fused with GEMMs to hide the memory latency.

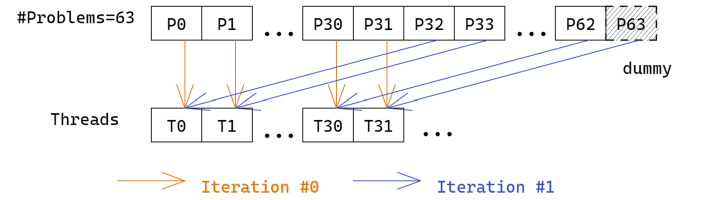


Fig. 7: Warp prefetching for grouped GEMM

Grouped GEMM frequently checks with the built-in scheduler on the current task assignments, which leads to the runtime overhead. To address this issue, we propose an optimization over the built-in CUTLASS group GEMM scheduler. Figure 7 shows our optimization for the original CUTLASS grouped GEMM scheduler. Rather than asking one thread to compute the current tasks metadata, we have all 32 threads in a warp compute the tile indices to visit at one time. Therefore, we achieve 32X fewer scheduler visit overhead. In practice, this strategy brings a $\sim 10\%$ improvement over the original CUTLASS grouped GEMM for standard BERT configurations. We have upstreamed the prototype of this idea to NVIDIA CUTLASS. We would refer an interested reader

to [34] for detailed source codes.

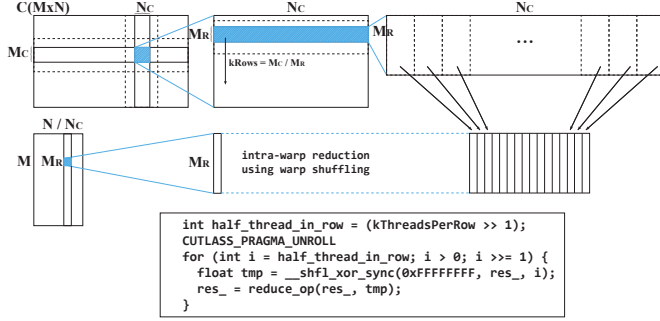


Fig. 8: Fused softmax reduction in grouped GEMM epilogue

In addition to optimizing the grouped GEMM scheduler, we fuse the memory footprints of softmax into two grouped GEMMs of MHA. Figure 8 shows the details of epilogue fusion for softmax reduction. A CTA computes an $M_C \times N_C$ sub-matrix. M_C and M_C are both set to 128 to maximize the performance of GEMM. Under the default CUTLASS threadmap assignment, there are 128 threads per CTA, and the threadmap is arranged as 8×16 , where each thread holds a 128-bit register tile in each step. After the intra-thread reduction, the $M_R \times N_C$ (8×128) sub-matrix is reduced to 8×16 , with one reduced result held by one thread. We then conduct an intra-warp reduction to further reduce from the column dimension, which is implemented via CUDA warp shuffling for efficiency. Similar reductions (intra-thread followed by intra-warp reduction) are performed to compute both max and sum in epilogue. Once max and sum are both reduced, we store them to global memory.

The reduction in epilogue only provides us with partial reduction within a threadblock because cross-threadblock communication is impractical under the current CUDA programming model.¹ Hence, we need to launch a separated lightweight kernel, as shown in Figure 6, to conduct the full reduction. In partial reduction, the target tensor of each attention unit is $\text{seq_len} \times \text{seq_len}$ while the full reduction just reduces a $\text{seq_len} \times \text{seq_len}/128$. Therefore, the workload of full reduction is negligible to that of partial reduction. In practice, the full reduction kernel only accounts for $\sim 2\%$ of total execution time in fused MHA.

Once we have obtained the fully reduced *max* and *sum* vectors, we are ready to proceed element-wise transform $\frac{e^{x_{ij} - \text{max}}}{\text{sum}}$ on the first GEMM’s output matrix. To hide the memory latency, we fuse these element-wise operations into the mainloop of the second GEMM. Algorithm III.2 presents our modifications (marked in red) of the original CUTLASS GEMM mainloop to enable softmax fusion. The original GEMM mainloop adopts the pipelining strategy to alleviate memory access latencies on both global memory and shared memory. For shared memory accesses, double register tiles are utilized to ensure that what is consumed in the current

¹Though CUDA collective kernel allows device-level synchronization, its kernel launch overhead and communication cost hinder it from being applied in DL inference, so we ignore it in discussion.

Algorithm III.2: Mainloop fusion of grouped FMHA

```

1 Register Tiles:
2 WarpLoadedFragmentA warp_loaded_frag_A[2];
3 WarpLoadedFragmentB warp_loaded_frag_B[2];
4 WarpLoadedFragmentNormSum warp_loaded_frag_norm_sum;
5 Shared memory: (kStages + 1) shared-memory tiles for A and B
6 /* prologue */
7 Load k-invariant fused softmax tile to warp_loaded_frag_norm_sum
8 Prefetch kStages - 1 tiles of A to shared memory using cp.async
9 Prefetch kStages - 1 tiles of B to shared memory using cp.async
10 Prefetch a tile of A from shared memory to warp_loaded_frag_A[0]
11 Prefetch a tile of B from shared memory to warp_loaded_frag_B[0]
12 /* fused element-wise operation */
13 /* A = exp(A - max) / sum */
14 elementwise_transform(
15     warp_loaded_frag_A[0],
16     warp_loaded_frag_norm_sum);
17 /* mainloop */
18 for k to -kStages + 1 do
19     /* Computes a warp-level GEMM */
20     /* with pipelined load during iterations */
21     for warp_mma_k = 0 to kWarpGemmIterations - 1 do
22         Prefetch warp_loaded_frag_A[(warp_mma_k + 1) % 2]
23         Prefetch warp_loaded_frag_B[(warp_mma_k + 1) % 2]
24         /* fused element-wise transform */
25         elementwise_transform(
26             warp_loaded_frag_A[(warp_mma_k + 1) % 2],
27             warp_loaded_frag_norm_sum);
28         /* Computes a warp-level GEMM */
29         /* on data loaded in previous iteration */
30         warp_mma(
31             accum,
32             warp_loaded_frag_A[warp_mma_k % 2],
33             warp_loaded_frag_B[warp_mma_k % 2],
34             accum);
35         Prefetch a tile of A to shared memory using cp.async
36         Prefetch a tile of B to shared memory using cp.async

```

iteration has always been loaded in the previous iteration. For global memory accesses, a multi-stage loading strategy is employed with the help of the `cp.async` instruction of NVIDIA Ampere GPUs. The `cp.async` instruction allows loading data asynchronously from global memory to shared memory without consuming registers. Multiple such transactions can be proceeded concurrently, and a stage barrier ensures selected stages to be synchronized. The number of load stages (`kStages`) is a compile-time constant defined by a user. Similar to shared memory accesses, loading from global memory is also pipelined to overlap memory latency with computation. Therefore, `kStages` pieces of shared memory buffers are needed under the multi-stage pipeline scheme. As shown in Algorithm III.2, we preload the k-invariant vectors *sum* and *max* in prologue, and conduct element-wise transform right after the matrix elements are loaded into registers. Since the fused vectors are loaded outside of the GEMM mainloop, only negligible overhead is brought into the baseline GEMM and the memory latency to perform element-wise transform is perfectly hidden with GEMM computations.

With the explicit design for both short and long sequences, our fused MHA alleviates the memory overhead of the intermediate matrix, which is quadratic to the sequence length, in MHA without introducing redundant calculations due to padding for variable-length inputs. Our highly optimized MHA outperforms the standard PyTorch MHA by 6.13X and accelerates the single-layer BERT Transformer further by 19% from

the previous step. Now this fully optimized version surpasses the baseline implementation in Figure 2 (a) by 60%. Since the remaining operations are all near-optimal GEMM operations, we conclude our optimizations at this step.

IV. EVALUATION

We evaluate our optimizations on an NVIDIA A100 GPU. The GPU device is connected to a node with four 32-core Intel Xeon Platinum 8336C CPUs, whose boost frequency is up to 4.00 GHz. The associated CPU main memory system is 2TB at 3200 MHz. We compile programs using CUDA 11.6u2 with the optimization flag O3. We compare the performance of ByteTransformer with latest versions of state-of-the-art transformers, such as TensorFlow 2.8, PyTorch 1.13, Tencent TurboTransformer 0.5.1 and NVIDIA FasterTransformer 5.1. All reported performance data are average results over tens of runs to minimize the fluctuation.

A. Kernel fusion for layernorm and add-bias operations

As shown in Figure 2, BERT Transformer is composed of a series of GEMM and memory-bound operations. Since GEMM are accelerated by near-optimal vendor’s libraries cuBLAS and CUTLASS, we focus on optimizing the modules containing memory-bound operations.

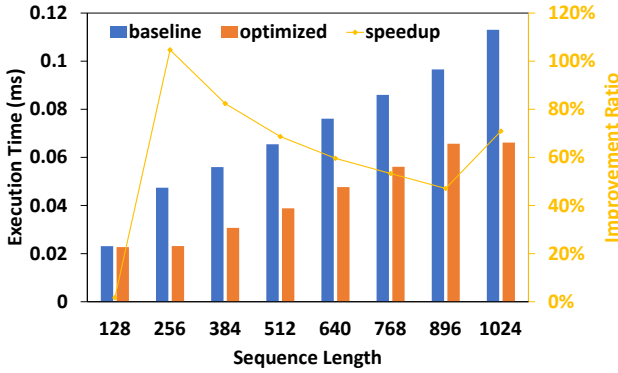


Fig. 9: Kernel fusion for add-bias and layernorm on a $(\text{batch_size} \cdot \text{seq_len}) \times \text{hidden_dim}$ tensor. Here we profile for 16 batches with the hidden dimension fixed to 768 under the standard BERT configuration.

The result tensor needs to be added by the input tensor and normalized after projection and feed forward network of BERT Transformer. Rather than launching two separated kernels, we fuse them into a single kernel and re-use data at the register level. In addition to kernel fusion. We leverage FP16 SIMD2 to increase the computational throughput of layernorm by assigning more workloads to a thread. As shown in Figure 9, the improved version with kernel fusion provides us with a 69% improvement in average over the unfused baseline for sequence lengths ranging 128 to 1024.

B. Kernel fusion for GEMM and add-bias & activation

Regarding the GEMM, add-bias and activation pattern in BERT Transformer, we also provide a fused kernel to reduce the global memory access. An unfused implementation is to call vendor’s GEMM, store the output to global memory, and

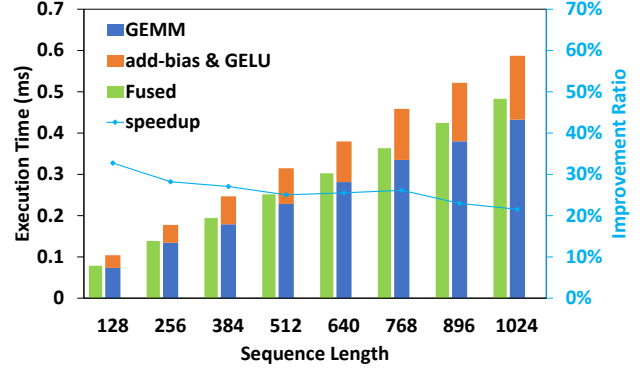


Fig. 10: Kernel fusion for GEMM, add-bias and GELU. The shape of output tensor is $(\text{batch_size} \cdot \text{seq_len}) \times (\text{scale} \cdot \text{hidden_dim})$. Here we profile for 16 batches with the hidden dimension and the scale factor fixed to 768 and 4 under the standard BERT configuration.

then load the result matrix from global memory for further element-wise operations. In our optimized version, when the result matrix of GEMM is held in registers, we conduct fused element-wise operations that re-use data at the register level. Once the element-wise transform (add-bias and GELU) is completed, we then store the results to the global memory. Figure 10 compares the performance of fused and unfused versions. In each clustered bar plot, the left bar shows the execution time of fused version, while the detailed performance breakdown for unfused implementation is shown in the stacked bar on the right. By fusing element-wise operations into the GEMM epilogue, we improve the performance by 24% on average for sequence lengths ranging 128 to 1024.

C. Optimizing multi-head attention

Figure 3 shows that MHA accounts for 22% - 49% of the total execution time. We optimize this key algorithm by fusing softmax into GEMMs without calculating for useless padded tokens under variable-length inputs. For short sequences, we hold the intermediate matrix in registers and shared memory. For long sequences, we adopt a grouped GEMM based fused MHA and fuse softmax operations into our customized GEMM epilogue and mainloop to hide the memory latency. In both implementations, the input matrices are accessed according to the position information obtained from the zero padding algorithm so that no redundant calculations are introduced.

Figure 11 compares the MHA performance for sequences shorter than 384. Here cuBLAS denotes the unfused implementation that calls cuBLAS for batched GEMM. The softmax operation between two batched GEMM can benefit from the zero padding algorithm, by only accessing unpadded tokens according to the known indices. This variant is denoted as *cuBLAS + zero padding* in the figure. cuBLAS batched GEMM improves the performance over stand PyTorch MHA by 5 folds while enabling the zero padding algorithm for softmax further improves the performance by 9%. By fully fusing softmax and two batched GEMMs into one kernel, our fused MHA achieves average speedup over all three variants

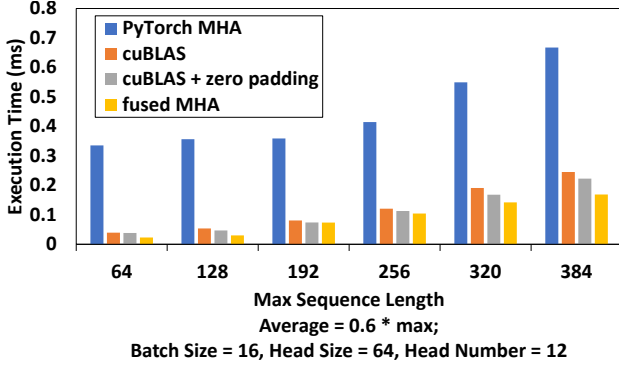


Fig. 11: Fused MHA for short sequences

by 617%, 42% and 30% for variable sequence lengths ranging 128 to 1024.

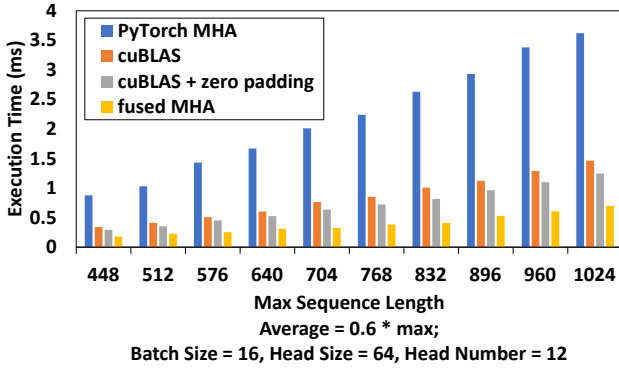


Fig. 12: Fused MHA for long sequences

Figure 12 compares the MHA performance for sequences longer than 512. The cuBLAS batched GEMM only triples the MHA performance over standard PyTorch, while eliminating wasted calculations in softmax further brings a 17% improvement. By introducing the high-performance grouped GEMM and fusing softmax into GEMMs, our fused MHA outperforms the variant MHA implementations by 451%, 110% and 79% for maximal sequence lengths ranging 128 to 1024, where the average sequence length is 60% of the maximum.

D. Benchmarking single-layer BERT Transformer with step-wise optimizations

Figure 13 compares the performance of a single-layer BERT Transformer to reflect our step-wise optimizations. At each step, we add a new optimization upon the previous variant. The baseline Transformer implements the workflow in Figure 2 (a) with padding. We then enable kernel fusion for adding bias and layernorm, which corresponds to *layernorm fusion* in the figure. The next step is to fuse adding bias and GELU into GEMM, denoted by *add bias & GELU fusion*. In order to avoid calculating padded tokens for the variable-length inputs, we further propose the zero padding algorithm as shown in Figure 2 (c). This is denoted by *rm padding* in the figure. Our ultimately optimized Transformer includes our high-performance fused MHA, as well as all previous optimizations.

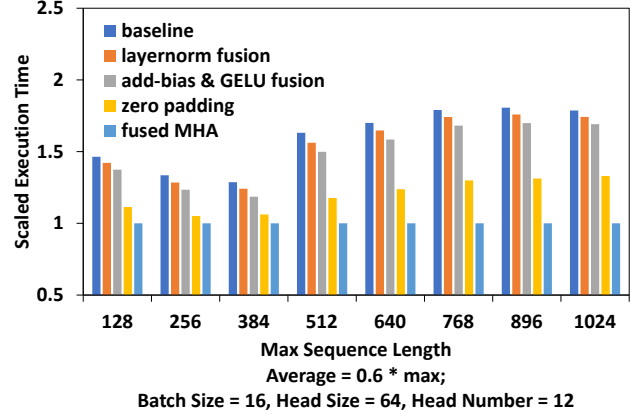


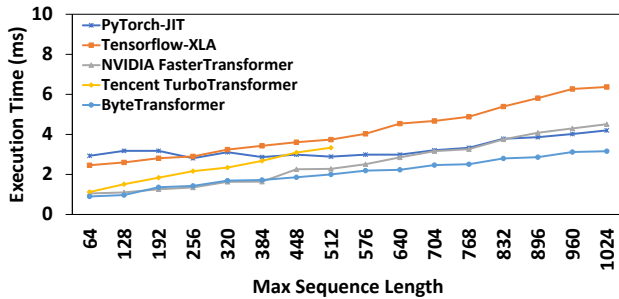
Fig. 13: Single-layer BERT Transformer with step-wise optimizations. Each variant includes all previous optimizations.

Fusing adding bias and layernorm into one kernel improves the performance by 3.2%. Fusing adding bias and activation into GEMM epilogue further improves the performance by 3.8%. These two optimizations together improve the overall performance by 7.1%. After bringing in the zero padding algorithm, the redundant calculations are eliminated in most modules other than MHA. We observe a 24% improvement from the previous step. Finally, our fused MHA removes wasted calculations on padded tokens and enables an additional 20% improvement. To summarize, the final version achieves 60% improvement over the baseline version on single-layer BERT Transformer.

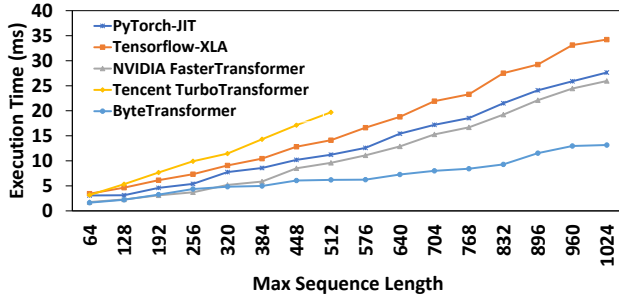
E. Benchmarking end-to-end performance of BERT

The standard BERT Transformer is a stacked structure of 12 layers of the encoder module. The output of each encoder module is utilized as an input tensor in the next iteration. Figure 14 shows the end-to-end performance of ByteTransformer and compares it against state-of-the-art Transformer implementations: PyTorch with JIT, TensorFlow with XLA acceleration, NVIDIA FasterTransformer and Tencent TurboTransformer. We adopt the standard BERT Transformer configuration for end-to-end benchmark: 12 heads, head size equal to 64 and 12 iterations (layers).

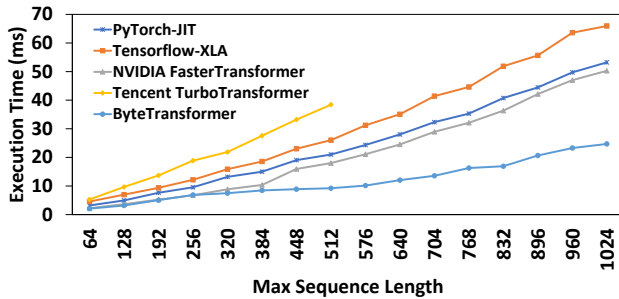
We benchmark for cases whose batch sizes are equal to 1, 8 and 16 and change sequence lengths from 128 to 1024. Compared with popular DL frameworks PyTorch and TensorFlow, our ByteTransformer achieves 87% and 131% faster end-to-end performance on average. When benchmarking Tencent TurboTransformer, we turn on the to reach optimal batching performance. Since TurboTransformer only supports sequence lengths smaller than 512, we do not benchmark longer sequences for it. TurboTransformer re-groups and pads similar sequences into a batch so it launches excessive kernels at the run-time. It is faced with significant performance degradation for models with large batch numbers and sequence lengths. NVIDIA FasterTransformer, although it supports long sequences regarding the functionality, its back-end TensorRT fused MHA cannot be scaled to long sequences due to the limited register. Therefore, its end-to-end efficiency cannot be



(a) Batch size = 1



(b) Batch size = 8



(c) Batch size = 16

Fig. 14: End-to-end benchmark for standard BERT Transformer, head size = 64, head number = 12, layer = 12, average sequence length = $0.6 * \text{max sequence length}$.

maintained when the sequence length becomes longer than 512. Experimental results in Figure 14 show that ByteTransformer outperforms TurboTransformer and FasterTransformer by 138% and 46% on average, respectively.

V. CONCLUSIONS

We have presented ByteTransformer, a high-performance Transformer optimized for variable-length sequences. ByteTransformer not only brings algorithmic level innovation that frees the Transformer from padding overhead, but also incorporates architecture-aware optimizations to accelerate functioning modules of the Transformer. Our optimized fused MHA, as well as other step-wise optimizations, together provide us with significant speedup over current state-of-the-art transformers. The end-to-end performance of the standard BERT Transformer benchmarked on an NVIDIA A100 GPU demonstrates that our ByteTransformer surpasses PyTorch, TensorFlow, Tencent TurboTransformer and NVIDIA FasterTransformer by 84%, 124%, 123% and 41%, respectively.

Future work will focus on pushing forward the internal process towards our vision of ByteTransformer being completely open-sourced. We are also extending the presented strategies to accelerate other BERT-like Transformer models.

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