H22S85 Chip Datasheet

SUMMARY DESCRIPTION

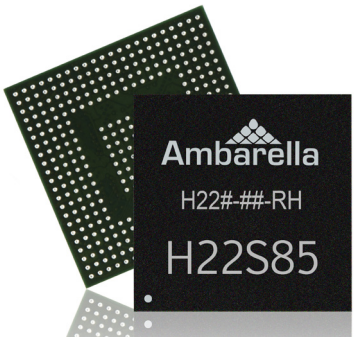
The H22S85 is an integrated system-on-a-chip (SoC) platform that targets drones (flying cameras), action cameras, and other high-performance video applications.

H22S85 chip provides a quad-core 1 GHz ARM Cortex-A53 CPU for custom applications, a high-performance digital signal processing (DSP) sub-system with an image sensor pipeline (ISP), and high-performance H.265 / HEVC and H.264 / AVC encoders capable of simultaneous video recording and streaming.

KEY FEATURES

- Embedded ARM quad-core Cortex-A53 1 GHz CPU with L2 cache
- Electronic Image Stabilization (EIS) with 6-axis correction (translational, pitch, yaw, and roll) and rolling shutter correction for drones and action cameras up to 4Kp30
- Advanced dynamic range (WDR and HDR) engine up to 4Kp30
- Dual sensor input and dual processing pipeline
- 3D motion-compensated noise reduction (MCTF)
- H.265 / H.264 encode performance up to 4KP60
- Simultaneous streaming of H.265 and H.264 encoded streams
- 369-pin, 0.65-mm pitch WFBGA package (14 mm x 14 mm)
- 14-nm CMOS Low Power (LP) technology
- Operating temperature from -20 °C to +85 °C

CONTENTS



1. OVERVIEW

This preliminary datasheet for the H22S85 processor from Ambarella begins with a brief introduction to the chip (Section 1.1) and a summary of key features (Section 1.2). Chapter 2 describes the H22S85 peripheral interfaces. For pin details and electrical characteristics refer to Chapter 3 and Chapter 4, respectively. See Chapter 5 for package information and Chapter 6 for Ambarella contact and ordering details.

Please note that the chip features described in this datasheet are subject to change. Details that have not been entirely finalized (e.g., encoding specifics) are provided using conservative estimates (i.e., final encoding performance is expected to meet or exceed the estimate provided). Please contact an Ambarella representative for additional information.

1.1 Introduction

The H22S85 is an integrated SoC platform that targets high-definition and ultra high-definition cameras with performance up to 4KP60. H22S85 chips provide a quad-core Cortex-A53 ARM CPU for custom applications, a digital signal processing (DSP) subsystem with an image sensor pipeline (ISP), and a high-performance H.265 / HEVC and H.264 / AVC encoding engine capable of simultaneous streaming. A functional block diagram of the H22S85 SoC is provided below.

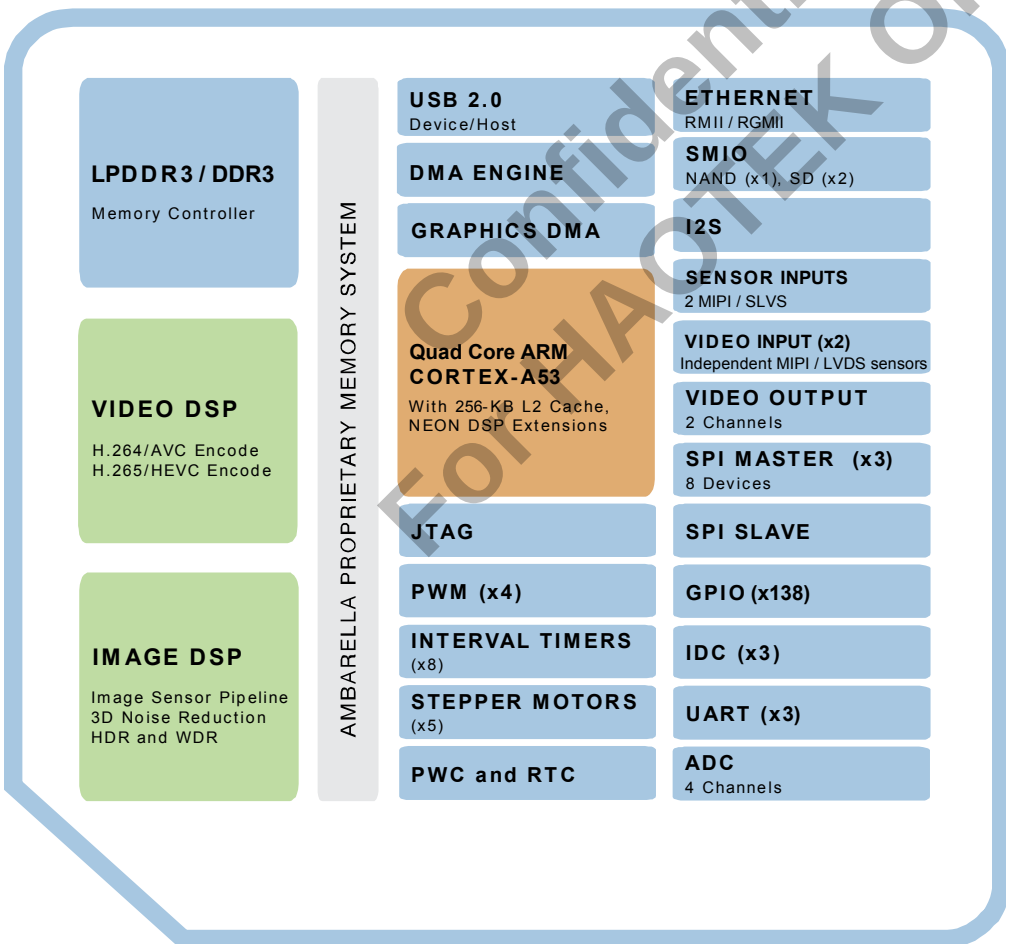


Figure 1-1. H22S85 Overview: Functional Block Diagram of the H22S85 SoC.

The H22S85 SoC provides a glueless interface to Serial sub-LVDS, SLVS, HiSPi, and MIPI interfaces, as well as parallel connections to popular CMOS image sensors. The ISP offers advanced image-processing features including improved multi-exposure high dynamic range (HDR) processing, wide dynamic range (WDR) single-exposure tone mapping with local contrast enhancement, 3D motion-compensated noise reduction (MCTF), edge enhancement, 3A, electronic image stabilization (EIS) and dewarping.

The H.264/H.265 codec engine delivers versatile encoding up to 4KP60 total performance, including simultaneous encode streams. The high-efficiency encoder implements full-function H.265/HEVC and H.264/AVC video encoding for the highest-quality and lowest possible bitrate. These functions include bidirectional prediction (B-frames), large motion-estimation search range, and macroblock-level quantization. Ambarella builds in flexibility with a multi-streaming function, allowing on-the-fly start/stop as well as the adjustment of the bitrate, frame rate, and GOP of each individual stream.

A 1 GHz quad-core ARM Cortex-A53 CPU with NEON DSP extensions and floating point support is available for implementing full-featured user applications.

The H22S85 chip is fabricated using low-power 14-nm CMOS technology and integrates advanced power-saving modes, such as utilizing DSP-subsystem memory resources to reduce external memory bandwidth and total camera system power requirements.

1.2 Feature List

Features of the H22S85 chip include:

- Embedded quad-core ARM Cortex-A53 CPU
  - Clock frequency up to 1 GHz
  - 32-KByte data / 32-KByte instruction cache
  - 256-KByte L2 cache
  - NEON SIMD acceleration
- DDR3 and LPDDR3 controller
  - Up to 1 GHz clock rate
  - 32-bit wide data bus
  - Maximum capacity of 16 Gbits (2 GByte)
- Image pipeline
  - More than 800 MPixel/s input pixel rate
  - Fish-eye lens dewarping and barrel distortion correction
  - 3D Electronic Image Stabilization (EIS) with 6-axis correction (translational, pitch, yaw, and roll) and rolling shutter correction
  - Black level correction
  - Dynamic and static defect pixel cluster correction
  - RGB Bayer demosaicing
  - Lens shading correction
  - 3D LUT color transform with gamma

- Advanced motion-compensated sharpening
- Advanced dynamic range (WDR and HDR) engine with multi-exposure fusion and motion artifact reduction
- 3D noise reduction (Motion Compensated Temporal Filter, or MCTF)
- Adjustable 3A; exposure, white balance and focus control (AE/AWB/AF)
- RGB and YUV statistics, histogram and AF focus value generation
- Luma sharpen and chroma noise filter
- Crop, mirror, flip, 90°/270° rotation
- Alpha-blending OSD up to full-frame overlay for text, image and privacy mask
- Flexible APIs and image-tuning tools

- Video engine
  - H.265/HEVC Main Profile Level 5.1 encoding
  - H.264 MP/HP Level 5.1 encoding
  - JPEG encoding
  - Maximum encode performance:
    - Main stream:
      - 4Kp60
      - 1920x1080p200
      - 1280x720p240
    - Secondary stream up to 720p30 (the performance is based on a combination of overall system load and features, and max preview resolution when recording at 4Kp60 is expected lower)
  - Advanced compression tools
    - I, IP, IBP modes (M=1,2,3,4…; IP, IBP, IBBP, IBBBP…)
    - B-frames and hierarchical GOP
    - Up to three reference frames
  - Flexible rate control
    - CBR, VBR and Constant QP with max bitrate control
    - Macroblock-level adaptive quantization
    - Bitrate control ranging from 16 kbit/s to 50 Mbit/s
    - Frame rate ranging from 1/16 fps to 120 fps
  - Dynamic ROI encoding per frame with up to 32 free-form areas at macroblock boundary
- Sensor/Video Input (VIN) interfaces
  - Two input channels with multiple input modes
    - Primary channel supports up to 8-lane sub-LVDS / SLVS / HiSPi input or up to 4-lane MIPI input
    - Secondary channel supports up to 4-lane SLVS / HiSPi / MIPI input
    - The primary and secondary input channels may be combined to support a single 10-lane SLVS / HiSPi sensor

        - Support for 14-bit parallel and LVCMOS sensors
    - Support for popular CMOS sensors: Sony, ON Semiconductor (Aptina), Panasonic, OmniVision, and others
    - Two clocking options (PLL-generated gclk_vin or SLVS bit clock)
    - 16-bit CCIR.601 video input with external sync signals
    - 8-bit, 10-bit, 12-bit or 14-bit BT.656-style video input with embedded sync codes including full-data-range support
- Video Output (VOUT) interfaces
    - Two logical channels to drive three video output ports
        - One logical channel drives HDMI or analog
        - One logical channel drives digital
    - Support for RGBA and YUVA OSD
    - Video DAC for 480i/576i composite PAL/NTSC output
    - HDMI 2.0 output with Consumer Electronics Control (CEC) and on-chip PHY
- AHB Bus DMA controller
    - Memory-to-memory transfers including support for transfers between memory and peripherals
    - Programmable transfer count up to 4 MB
    - DMA scatter/gather via chained descriptor list in memory with DMA control information source
- Dedicated DMA co-processor for graphics and image operations
    - Offers linear copy, 2-D copy, composite, and alpha-blend image operations
    - Supports 4- to 32-bit pixel formats
- I2S digital audio interface (stereo)
    - Audio record/playback
- Ethernet MAC controller
    - IEEE 802.3 compliant with full- and half-duplex (IEEE 802.3x flow-control) and Jumbo frames
    - IEEE 802.1Q VLAN tag detection
    - Checksum off-load for received IP and TCP/UDP packets
    - Dedicated pins for RMII or MII interface
    - FIFO (2 KB / 2 KB) and DMA support
- USB 2.0 interface
    - One port configurable as host or device, with built-in PHY
- Flexible Storage Media Input / Output (SMIO) interface
    - NAND Flash controller
        - Up to 8-Gbit device, 512-Byte and 2-KByte page sizes
        - 8-bit flash chip data bus
        - 4-bit and 8-bit SLC with ECC hardware and read-confirm support

    - BCH error correction and increased spare area available
  - Two SD controllers (SD0, SD1)
    - SD0:
      - SDIO v3.0, SD, SDHC, SDXC, MMC and eMMC operation with boot support and UHS-I speed
      - Support for 1-bit, 4-bit, and 8-bit SD mode
    - SD1:
      - SDIO v2.0, SD, SDHC, SDXC, MMC and eMMC operation
      - Support for 1-bit, 4-bit, and 8-bit SD mode
    - 32-GByte maximum capacity for SDHC SD Card
    - 2-TByte maximum capacity for SDXC SD Card
    - CRC7 for command and CRC16 for data integrity
- Multiple boot options
  - NOR-SPI, NAND Flash, USB and eMMC
- Generic interrupt controller including GIC CPU-offload functionality
- SSI / SPI controller interfaces
  - Two SSI / SPI masters with DMA support for up to eight device enables
  - One dedicated SSI / SPI slave port to connect to an external system master
- Two-wire serial Inter-Integrated Circuit (I2C / IDC) interfaces (x3)
  - Configurable IDC buses
- UART interfaces (x3)
  - DMA support
  - One interface supports flow control
- Up to 138 General Purpose Input/Output (GPIO) pins with individual pull-up/down control
- ADC (three channels) with high/low threshold interrupt generation and 12-bit resolution
- Built-in power controller for power-up/down sequencing
- Real Time Clock (RTC)
- Interval timing with eight general-purpose timers configurable as external event counters
- Watchdog timer
- Stepper motor interface (five channels) with four-channel Micro-Stepper interface
- Pulse Width Modulators (PWM) (x4)
- JTAG In-Circuit Emulator (ICE) interface for debugging
- 369-pin, 0.65-mm pitch WFBGA package (14 mm x 14 mm)
- 14-nm CMOS Low Power (LP) technology
- Operating temperature from -20 °C to +85 °C

2. INTERFACES

2.1 Overview

This section summarizes the peripheral interfaces for the H22S85 chip as follows:

2.2 SDRAM Interface

The H22S85 chip includes a synchronous DRAM interface, enabling high data-access rates in response to pipe-lined commands. The features of the H22S85 SDRAM interface include:

- Frequencies up to 1 GHz
- Support for the LPDDR3 / DDR3 / DDR3L low-power DDR interface
- Programmable I/O strength
- 32-bit data bus

Please contact an Ambarella representative to select a qualified Ambarella-approved DDR component.

2.3 Video Input (VIN) Interface

The H22S85 chip supports multiple serial and parallel input modes. The features of the H22S85 VIN interface include:

- Two sensor VIN instances - One VIN (Main) and one secondary:
- VIN (Primary, with all secondary units disabled):
  - 1-8 Lane SLVS (up to 3 Gbps per lane)
  - 1-4 Lane MIPI CSI-2 (up to 3 Gbps per lane)
  - 16-bit Parallel LVCMOS (up to 150 MHz) (YUV422)
  - Secondary:
    - 1-4 Lane SLVS (up to 3 Gbps per lane)
    - 1-4 Lane MIPI CSI-2 (up to 3 Gbps per lane)
  - Example use cases with 2 sensor inputs:
    - All 8 lanes are used by VIN
    - VIN and Secondary, each uses 4 lanes

Lane	VIN Only	VIN + Secondary
1	1 (VIN)	1 (VIN)
2	2 (VIN)	2 (VIN)
3	3 (VIN)	3 (VIN)
4	4 (VIN)	4 (VIN)
5	5 (VIN)	1 (Secondary)
6	6 (VIN)	2 (Secondary)
7	7 (VIN)	3 (Secondary)
8	8 (VIN)	4 (Secondary)

Table 2-1. Lane Sharing Between VIN and Secondary Inputs.

The H22S85 VIN module is part of the DSP cluster. Like other modules in the DSP cluster it is configured using a set of APIs. Please contact an Ambarella representative for information regarding VIN module configuration and other possible combinations for lane sharing.

2.4 Video Output (VOUT) Interfaces

The H22S85 Video Output (VOUT) interface supports a total of three output ports using two logical video channels.

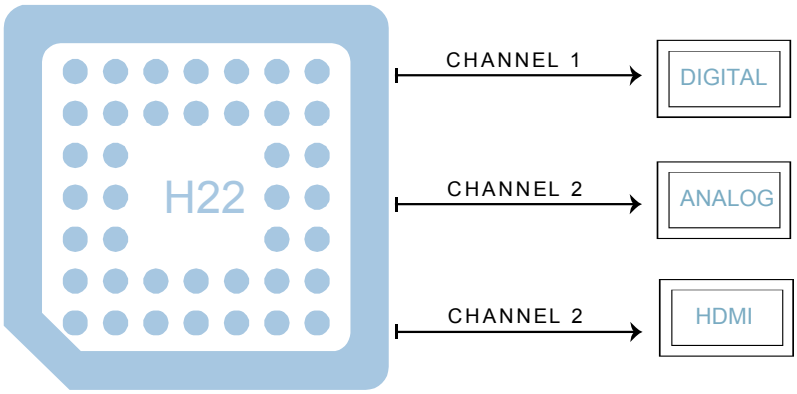


Figure 2-1. H22S85 Video Output Channels and Ports.

One VOUT channel is capable of driving digital output to RGB LCD panels, while the second VOUT channel drives either analog composite output or HDMI output to the on-chip HDMI transmitter (Tx) unit. The H22S85 chip supports simultaneous 1080i and 480i output rates.

2.4.1 Analog Video Output

The H22S85 video digital-to-analog converter (DAC) can drive standard-definition 480i/576i composite video outputs.

2.4.2 Digital Video Output

The H22S85 chip supports several digital video output modes including 8-bit or 16-bit {CbY, CrY}, LCD-RGB, and CCIR.601 as described in the tables below.

Bits	Mapped To Signal	Notes
VD0_OUT[15:8]	Unused	
VD0_OUT[7:0]	Interleaved R,G,B	**VD0_OUT[7]** is MSB

Table 2-2. Digital RGB Mode (Video Output Modes 0/1/2 for 3-bit Output to the LCD).

Bits	Mapped To Signal	Notes
VD0_OUT[15:11]	Upper 5 bits of the Red channel	**VD0_OUT[15]** is the MSB
VD0_OUT[10:5]	Upper 6 bits of the Green channel	**VD0_OUT[10]** is the MSB
VD0_OUT[4:0]	Upper 5 bits of the Blue channel	**VD0_OUT[4]** is the MSB

Table 2-3. 5:6:5 RGB Mode (Video Output Mode 3 for 16-bit RGB Output to the LCD).

Bits	Mapped To Signal	Notes
VD0_OUT[15:8]	Unused	

Bits	Mapped To Signal	Notes
VD0_OUT[7:0]	Interleaved Cb,Y,Cr,Y . . .	

Table 2-4. 8-bit YCbCr Mode (Video Output Mode 7).

Bits	Mapped To Signal	Notes
VD0_OUT[15:8]	Interleaved Cb,Cr	**VD0_OUT[15]** is the MSB
VD0_OUT[7:0]	Y	**VD0_OUT[7]** is the MSB

Table 2-5. 16-bit 601-YCbCr Mode (Video Output Mode 5).

Table 2-5 and Table 2-6 correspond to 4:2:2 output format.

2.4.3 HDMI Output

The H22S85 chip includes an embedded HDMI 2.0 transmitter that provides three lanes of transition-minimized differential signaling (TMDS) data and one clock lane. The features of the H22S85 HDMI interface include:

- Consumer Electronics Control (CEC) support, allowing command and control of up to 15 CEC-enabled devices
- An additional two-wire bus (IDC2) for secure key transfer (see Section 2.11)

2.5 I2S Audio Interface

The H22S85 chip provides an Integrated Interchip Sound (I2S) controller for two-channel audio support. Features of the I2S interface include:

- Support for audio using an external audio codec analog-to-digital converter (ADC)
- I2S host interface support
- All data lanes are clocked by the same clock signal

2.6 Digital Microphone Interface (DMIC)

The H22S85 chip provides a digital microphone interface (DMIC).

2.7 Gigabit Ethernet MAC

- The H22S85 Ethernet controller supports 10/100/1000-Mbps data transfer rates with IEEE 802.3-compliant RGMII/RMII (default) interface and communicates with an external Gigabit/Fast Ethernet PHY
- The Ethernet controller supports MDIO Master interface (optional) for PHY device configuration and

management

2.7.1 Enable / Disable Ethernet

Ethernet functionality is enabled / disabled with power-on configuration bit POC[23], whether the Gigabit function (RGMII) is enabled or Ethernet RMII is used.

2.8 USB Interface

The H22S85 SoC includes one USB 2.0 port configurable as host or device, with a built-in PHY. Features of the H22S85 USB interface include:

- One configurable USB host/device, with a built-in PHY
- USB power-on boot mode
- The USB device can be used to burn firmware to flash or to simulate Ethernet for debugging.
- The USB host can be used to connect a USB WiFi module, a USB card reader, or 3G/4G baseband.

2.9 Smart Media Input/Output (SMIO) Interface

The H22S85 chip provides Smart Media Input/Output (SMIO) pins as a flexible storage-media interface for NAND Flash and SD controllers. Features of the H22S85 SMIO interface include:

- NAND Flash controller
  - Up to 8-Gbit device, 512-Byte and 2-KByte page sizes
  - 8-bit flash chip data bus
  - 4-bit and 8-bit single-level cell (SLC) memory with error-correcting code (ECC) hardware and read-confirm support
- Two SD controllers (SD0, SD1)
  - SD0:
    - SDIO v3.0, SD, SDHC, SDXC, MMC and eMMC operation with boot support and UHS-I speed
    - Support for 1-bit, 4-bit, and 8-bit SD mode
  - SD1:
    - SDIO v2.0, SD, SDHC, SDXC, MMC and eMMC operation
    - Support for 1-bit, 4-bit, and 8-bit SD mode
  - 32-GByte maximum capacity for SDHC SD Card
  - 2-TByte maximum capacity for SDXC SD Card
  - Cyclic redundancy check 7 (CRC-7) for command, and cyclic redundancy check 16 (CRC-16) for data integrity
- Power-on NAND Flash and eMMC boot modes
- SD0 may be used to connect to an SD card or an SDIO Wi-Fi module.

2.10 SSI / SPI Interface

The H22S85 chip provides three Synchronous Serial Interface (SSI) / Serial Peripheral Interface (SPI) masters and one dedicated SSI / SPI slave for full-duplex data transmission support. Features of the H22S85 SSI / SPI interface include:

- SSI / SPI master control with DMA support for up to eight slave devices
- Dedicated SSI / SPI slave port for connection to an external system master
- SPI-NOR, SPI-EEPROM boot support included with DMA support

Master	Number of Device Enables	Device Enable Pins	SSI/SPI Function	Default Polarity[1]
SSI0	4	**SSI0EN0**	ssi0_en0 Device Enable	Active Low
		SSI0EN1	ssi0_en1 Device Enable	Active Low
		SC_E0	ssi0_en2 Device Enable	Active Low
		TIMER2	ssi0_en3 Device Enable	Active Low
SSI1	4	**ENET_RXD_0** or **SC_A3**	ssi1_en0 Device Enable	Active Low
		ENET_RXD_1 or **SC_B0**	ssi1_en1 Device Enable	Active Low
		ENET_RX_ER or **SC_B1**	ssi1_en2 Device Enable	Active Low
		ENET_CRS_DV or **SC_B2**	ssi1_en3 Device Enable	Active Low
SSI2	4	**SSI2EN0**	ssi2_en0 Device Enable	Active Low
		SSI2EN1	ssi2_en1 Device Enable	Active Low
		TIMER0	ssi2_en2 Device Enable	Active Low
		TIMER1	ssi2_en3 Device Enable	Active Low

Table 2-6. H22S85 SSI / SPI Master with Device Enable Detail.

Note:

1. Each SSI / SPI device-enable has programmable polarity; i.e., the polarity can be assigned to meet peripheral requirements without external glue logic.

2.11 I2C / IDC Interface

The H22S85 SoC includes three Inter-Integrated Circuit (I2C / IDC) interfaces to provide bidirectional data communication between the chip and its peripheral devices. Features of the H22S85 I2C / IDC interfaces include:

- Protocol speeds up to 400 Kbps
- Support for single-master mode

2.12 UART Interface

The H22S85 chip includes three Universal Asynchronous Receiver / Transmitter (UART) ports. Features of the H22S85 UART interface include:

- UART Port 0 doesn't have hardware flow control or direct memory access (DMA) support, and it is used for debugging
- UART Port 1 has hardware flow control and DMA support
- UART Port 2 (UART_AHB) is pin muxed with other functions and has hardware flow control and DMA support
- A maximum baud rate of 115.2 Kbps for UART0, based on per-port software settings
- UART_AHB can be used to connect to Bluetooth/GPS when other mux functions are not in use

2.13 General Purpose Input/Output (GPIO) Interface

The H22S85 SoC includes 138 CMOS pins which can be programmed for multi-use General Purpose Input/Output (GPIO) functions. Features of the H22S85 GPIO interface include:

- Pins with reduced electrostatic discharge sensitivity, tested to the latest JEDEC standard (*Joint Standard for Component-Level Electrostatic Discharge Sensitivity Testing*)
- Multiplexing support, allowing GPIO pins to be assigned multiple functions that can be independently enabled via software
- Individual pull-up/down control
- Individual drive strength control

2.14 Analog-to-Digital Converter (ADC) Interface

The H22S85 chip provides multiple channels for analog-to-digital conversion (ADC). Features of the H22S85 ADC interface include:

- Three channels
- High/low threshold interrupt generation
- 12-bit resolution

2.15 Real Time Clock (RTC) and Power Controller (PWC) Interfaces

To conserve power, the H22S85 system software optimizes clock and PLL frequencies according to operating mode. Peripheral clocks can be further optimized by the user through register programming.

Features of the power controller (PWC) and real-time clock (RTC) interfaces include:

- 32-bit embedded RTC maintained with one dedicated always-on power supply pin
- RTC provides current time, alarm set, and power-on and power-off sequence generation

2.16 Stepper, Micro-Stepper, and Pulse Width Modulator (PWM) Interfaces

2.16.1 Stepper and Micro-Stepper Motor Controllers

The H22S85 chip supports five stepper motor controller channels, each of which can be used for independent motor control. The chip also provides four sets of micro-stepper interfaces.

2.16.2 Pulse Width Modulator (PWM)

The H22S85 chip provides four pulse width modulation interfaces (PWMB0/B1/C0/C1):

- The four PWM outputs are referred to as pwm_[0:3]. Functionally:
  - PWMB0 is associated with pwm_0
  - PWMB1 is associated with pwm_1
  - PWMC0 is associated with pwm_2
  - PWMC1 is associated with pwm_3
- Note that in addition to the PWM controller embedded in the stepper motor controller, the H22S85 external pin **VD_PWM** can also serve as a PWM controller.
- Selection of PWM functions is executed via software. pwm_[0:3] are typically used for motor control and are sourced to the video input clock **CLK_SI**.

2.17 JTAG Interface

The H22S85 chip provides an interface for JTAG In-Circuit Emulator (ICE) debugging. Contact an Ambarella representative for more information regarding the JTAG interface.

3. PINS

3.1 Pins: Overview

The H22S85 SoC is equipped with 369 external physical pins including power balls, ground balls, and signal balls. This section provides pin details for the primary chip interfaces and functions.

- Refer to Section 4.4 for a list of fail-safe CMOS pins and their corresponding voltage thresholds.
- Refer to Chapter 7 for a complete list of pins sorted by their location on the H22S85 ball map.

3.2 Pins: Tables

This section lists the pins for each interface as follows:

For each pin listed, the following information is provided:

- Pin direction: (I) input, (O) output, (S) supply, (G) ground
- Pad type
- A brief description
- For complete multiplexing information, please refer to Section 3.2.12 and Chapter 7.

3.2.1 Pins: DRAM

Name	Location	Dir	Type	Description
DDR_CALIBR	A4	I/O	Analog	ZQ calibration
DDR_CK	K2	O	SSTL	DRAM clock per SDRAM
DDR_CK_BAR	K1	O	SSTL	DDR_CK and DDR_CK_BAR are differential clocks
DDR_CK_2_BAR	H1	O	SSTL	DDR_CK and DDR_CK_BAR are differential clocks
DDR_CK_2	H2	O	SSTL	DRAM clock per SDRAM
DDR_CKE_2	J1	O	SSTL	Clock enable for 2nd die
DDR_CKE	L1	O	SSTL	Clock enable
DDR_CS_2	C5	O	SSTL	Chip select for die 2
DDR_CS	B5	O	SSTL	Chip select for die 1
DDR_DM_[3:0]	D2, B3, R2, R3	O	SSTL	Data write mask (1 bit per 8 data bits)
DDR_DQ_[31:0]	B2, A1, C2, B1, F2, E1, E2, F1, A2, B4, A3, C4, F3, E4, E3, D4, P2, M1, N2, N1, T2, T1, U2, U1, M2, P4, M3, R4, T3, T4, U3, U4	I/O	SSTL	Bi-directional data bus
DDR_DQS_[3:0]	C1, C3, R1, P3	I/O	SSTL	Data strobe (1 bit per 8 data bits) Output with write data, center-aligned Input with read data, edge-aligned
DDR_DQS_BAR_[3:0]	D1, D3, P1, N3	I/O	SSTL	**DDR_DQS_[N]** and **DDR_DQS_BAR_[N]** are differential signals
DDR_VDDQ_CKE	E6	S	Digital Supply	Power for DDR_CKE and DDR_RESET pins
DDR_VDDQ	F5, G5, H5, J5, K5, L5, M5, N5	S	Digital Supply	DDR digital I/O power supply
DDR_ADDR_[15:0]	L2, K3, G1, G2, H3, K4, R5, J4, P5, J3, D5, G3, F4, E5, L3, G4	O	SSTL	Address for row address strobe (RAS) and column address strobe (CAS)
DDR_WE	H4	O	SSTL	Write enable (active low)
DDR_BA_[2:0]	U5, J2, T5	O	SSTL	Bank Address
DDR_ODT	L4	O	SSTL	SDRAM on-die termination control signal
DDR_RAS	M4	O	SSTL	Row address strobe (active low)
DDR_CAS	N4	O	SSTL	Column address strobe (active low)

Name	Location	Dir	Type	Description
DDR_VREF_[2:1]	A5, W5	I/O	SSTL	Reference Voltage for SSTL18 pad (0.5*DDR_ VDDQ)
DDR_RESET	V5	O	SSTL	DDR3 - Asynchronous reset LPDDR2 - NC

Table 3-1. DRAM Pins.

3.2.2 Pins: Sensor / Video Input

Name	Location	Dir	Type	Description
CLK_SI	U6	I/O	CMOS	Sensor master clock output
CLK_SI2	V6	I/O	CMOS	Sensor master clock output
SD_LVDS_N_[0:7]	B10, B9, B8, B7, B15, B14, B13, B12	I	Sub-LVDS/ SLVS/ LVCMOS /MIPI	Sensor data Differential for sub-LVDS and MIPI Single-ended for LVCMOS mode. Termination resistor built in for sub-LVDS / SLVS mode. Both single and double data rates supported.
SD_LVDS_P_[0:7]	A10, A9, A8, A7, A15, A14, A13, A12	I	Sub-LVDS/ SLVS/ LVCMOS /MIPI	
SHSYNC	D8	O	CMOS	H-Sync / H-Valid with Master mode configuration
SPCLK_LVDS_N_[0:1]	B11, B6	I	Sub-LVDS/ SLVS/ LVCMOS /MIPI	Sensor pixel clock Differential pairs for sub-LVDS and SLVS mode. **SPCLK_LVDS_P_0** is used for single-ended pixel clock with LVCMOS mode.
SPCLK_LVDS_P_[0:1]	A11, A6	I	Sub-LVDS/ SLVS/ LVCMOS /MIPI	
SVSYNC	D7	I/O	CMOS	V-Sync / V-Valid with Master mode configuration

Table 3-2. VIN Sensor Interface Pins.

3.2.3 Pins: Video Output

This section covers video output interface pins for Digital-to-Analog Conversion, Digital Video Output, and HDMI output.

3.2.3.1 VOUT Pins: Video Digital-to-Analog Conversion (DAC)

Name	Location	Dir	Type	Description
DAC_COMP	C9	I/O	Analog	Compensation pin
DAC_IO	D6	I/O	Analog	Composite CVBS output
DAC_RSET	C7	I/O	Analog	Reference resistor
DAC_VREFIN	C8	I/O	Analog	Voltage reference input

Table 3-3. Video DAC Pins.

3.2.3.2 VOUT Pins: Digital Video Output

Name	Location	Dir	Type	Description [1]
VD0_CLK	V4	I/O	CMOS	Video output clock
VD0_HSYNC	U8	I/O	CMOS	Video output HSync signal
VD0_HVLD	W7	I/O	CMOS	Video output valid signal
VD0_OUT_0	W6	I/O	CMOS	Video output data
VD0_OUT_1	W3	I/O	CMOS	Video output data
VD0_OUT_2	Y5	I/O	CMOS	Video output data
VD0_OUT_3	AA5	I/O	CMOS	Video output data
VD0_OUT_4	W1	I/O	CMOS	Video output data
VD0_OUT_5	Y3	I/O	CMOS	Video output data
VD0_OUT_6	W2	I/O	CMOS	Video output data
VD0_OUT_7	V7	I/O	CMOS	Video output data
VD0_OUT_8	U7	I/O	CMOS	Video output data
VD0_OUT_9	AA7	I/O	CMOS	Video output data
VD0_OUT_10	V3	I/O	CMOS	Video output data
VD0_OUT_11	W4	I/O	CMOS	Video output data
VD0_OUT_12	Y6	I/O	CMOS	Video output data
VD0_OUT_13	AA6	I/O	CMOS	Video output data
VD0_OUT_14	V1	I/O	CMOS	Video output data
VD0_OUT_15	V2	I/O	CMOS	Video output data
VD0_VSYNC	Y7	I/O	CMOS	Video output VSync signal

Table 3-4. Digital Video Output Pins.

Note:

1. H22S85 digital video output pins are used for power-on configuration (POC).

3.2.3.3 VOUT Pins: HDMI Output

Name	Location	Dir	Type	Description
HDMI_REXT	G21	I/O	Analog	Reference resistor - 10 KOhms (1% tolerance) (Required even if HDMI port is unused)
HDMI_AVDD33_ESD	A21	S	Analog Supply	HDMI analog power

Name	Location	Dir	Type	Description
HDMI_AVDD18_ESD	B21	S	Analog Supply	HDMI analog power
HDMI_CH2_M	C20	I/O	Analog	Transition-minimized differential signalling (TMDS) data out (open drain)
HDMI_CH2_P	C21			
HDMI_CH1_M	D20			
HDMI_CH1_P	D21			
HDMI_CH0_M	E20			
HDMI_CH0_P	E21			
HDMI_CLK_M	F20			
HDMI_CLK_P	F21			
CEC	F19	I/O	CMOS	Consumer Electronics Control (CEC) pin (3.3-V tolerance)
HPD	E19	I/O	CMOS	Hot-plug detect (3.3-V tolerance)

Table 3-5. HDMI Output Pins.

3.2.4 Pins: I2S Digital Audio

Name	Location	Dir	Type	Description
CLK_AU	AA12	O	CMOS	Master clock for external audio codec
I2S_CLK	U12	I/O	CMOS	I2S Controller audio bit clock
I2S_SI	V11	I	CMOS	I2S Controller serial data in
I2S_SO	W12	O	CMOS	I2S Controller serial data out
I2S_WS	Y12	I/O	CMOS	I2S Controller word select

Table 3-6. I2S Controller Pins.

3.2.5 Pins: Ethernet Interface

Name	Location	Dir	Type	Description
ENET_MDC	U9	I/O	CMOS	MII clock
ENET_CLK_RX	U10	I/O	CMOS	Reference clock
ENET_RXD_[3:0]	W11, W10, Y10, AA10	I/O	CMOS	Receive data
ENET_MDIO	V8	I/O	CMOS	MII data bus
ENET_CLK_TX	V9	I/O	CMOS	Transmit clock
ENET_GTX_CLK	Y9	I/O	CMOS	Ethernet clock
ENET_RXDV	Y11	I/O	CMOS	Receive data
ENET_TXD_[3:0]	AA9, AA8, Y8, W8	I/O	CMOS	Transmit data
ENET_TXEN	W9	I/O	CMOS	Transmit ready
ENET_EXT_OSC_CLK	AA11	I/O	CMOS	Ethernet external oscillator clock

Table 3-7. Ethernet Pins.

3.2.6 Pins: USB

Name	Location	Dir	Type	Description
GPIO_1	V16	I/O	CMOS	USB EHCI overcurrent detect input
GPIO_3	Y16	I/O	CMOS	USB EHCI port power enable out
DETECT_VBUS	D17	I/O	CMOS	USB slave bus detect
USB_DM	B16	I/O	Analog	USB data. DP/DM are differential signals.
USB_DP	A16	I/O	Analog	
USB_REXT	C17	I/O	Analog	USB resistor

Table 3-8. USB Interface Pins.

3.2.7 Pins: Smart Media Input/Output (SMIO)

- The Smart Media Input/Output (SMIO) pins are CMOS type and programmable input/output.
- SMIO pins are shared by controllers for NAND Flash (NAND) and SD / SDIO / SDHC / SDXC / MMC / eMMC (SD).
- SMIO pins use **SMIO_[N]** for the primary function name.

Name	Location	NAND		SD		Description
		Function	Dir	Function	Dir	
SMIO_0	R19	nand_ce	O			NAND chip enable
SMIO_1	R18	nand_rb	I/O			NAND ready / busy
SMIO_2	L19			sd_clk	O	SD0 clock
SMIO_3	M18			sd_cmd	I/O	SD0 command
SMIO_4	M20			sd_cd	I	SD0 card detect
SMIO_5	M19			sd_wp	I	SD0 write protect
SMIO_6	R20	nand_re	O			NAND read enable
SMIO_7	P21	nand_we	O			NAND write enable
SMIO_8	R21	nand_ale	O			NAND address latch enable
SMIO_9	P20	nand_d[0]	I/O			NAND data
SMIO_10	P19	nand_d[1]	I/O			NAND data
SMIO_11	P18	nand_d[2]	I/O			NAND data
SMIO_12	P17	nand_d[3]	I/O			NAND data
SMIO_13	N17	nand_d[4]	I/O			NAND data
SMIO_14	N18	nand_d[5]	I/O			NAND data
SMIO_15	N19	nand_d[6]	I/O			NAND data
SMIO_16	N20	nand_d[7]	I/O			NAND data
SMIO_17	N21	nand_cle	O			NAND command latch enable
SMIO_18	L20			sd_d[0]	I/O	SD0 data
SMIO_19	K21			sd_d[1]	I/O	SD0 data
SMIO_20	J17			sd_d[2]	I/O	SD0 data
SMIO_21	K17			sd_d[3]	I/O	SD0 data
SMIO_22	L21			sd_d[4]	I/O	SD0 data

Name	Location	NAND		SD		Description
		Function	Dir	Function	Dir	
SMIO_23	K20			sd_d[5]	I/O	SD0 data
SMIO_24	L18			sd_d[6]	I/O	SD0 data
SMIO_25	L17			sd_d[7]	I/O	SD0 data
SMIO_26	K19			sdxc_clk	O	SD1 clock
SMIO_27	K18			sdxc_cmd	I/O	SD1 command
SMIO_28	J18			sdxc_d[0]	I/O	SD1 data
SMIO_29	J19			sdxc_d[1]	I/O	SD1 data
SMIO_30	J20			sdxc_d[2]	I/O	SD1 data
SMIO_31	J21			sdxc_d[3]	I/O	SD1 data
SMIO_32	H21			sdxc_cd	I	SD1 card detect
SMIO_33	H20			sdxc_wp	I	SD1 write protect
SMIO_34	H19			sdxc_d[4]	I/O	SD1 data
SMIO_35	H18			sdxc_d[5]	I/O	SD1 data
SMIO_36	G18			sdxc_d[6]	I/O	SD1 data
SMIO_37	G19			sdxc_d[7]	I/O	SD1 data
SMIO_38	M17			sd_reser	O	SD0 reset
SMIO_39	G20			sdxc_reset	O	SD1 reset
WP	M21	nand_wp	O			NAND write protect

Table 3-9. Storage Media Interface Pins (SMIO) in NAND Flash and SD Modes.

3.2.8 Pins: SSI / SPI

Name	Location	Dir	Pad Type	Description
SSI0CLK	AA19	I/O	CMOS	ssi0 master port bit clock
SSI0EN0	R17	O	CMOS	ssi0_en0 device enable
SSI0EN1	T17	O	CMOS	ssi0_en1 device enable
TIMER2	AA20	I/O	CMOS	ssi0_en3 device enable
ENET_RXD_0	AA10	I/O	CMOS	ssi1_en0 device enable
ENET_RXD_1	Y10	I/O	CMOS	ssi1_en1 device enable
SSI0MISO	Y18	I	CMOS	ssi0 master port data in
SSI0MOSI	AA18	O	CMOS	ssi0 master port data out

Table 3-10. SSI / SPI Interface Pins.

3.2.9 Pins: I2C / IDC

Name	Location	Dir	Pad Type	Description
IDCCLK	AA15	I/O	CMOS	First IDC serial port - clock
IDCDATA	U14	I/O	CMOS	First IDC serial port - data
IDC2CLK	V13	I/O	CMOS	Second IDC serial port - clock

Name	Location	Dir	Pad Type	Description
IDC2DATA	W14	I/O	CMOS	Second IDC serial port - data
IDC3CLK	Y14	I/O	CMOS	Third IDC serial port - clock
IDC3DATA	AA14	I/O	CMOS	Third IDC serial port - data

Table 3-11. I2C / IDC Interface Pins.

3.2.10 Pins: UART

Name	Location	Dir	Pad Type	Description
UART0RX	AA17	I	CMOS	UART Port 0 receive
UART0TX	AA16	O	CMOS	UART Port 0 transmit
UART1RX	W17	I	CMOS	UART Port 1 receive
UART1TX	Y17	O	SMOS	UART Port 1 transmit
UART1CTSN	U16	I	CMOS	UART clear to send from modem
UART1RTSN	U17	O	CMOS	UART request to send from Terminal/computer

Table 3-12. UART Interface Pins.

3.2.11 Pins: InfraRed Remote

Name	Location	Dir	Pad Type	Description
IR_IN	C19	I	CMOS	InfraRed input

Table 3-13. InfraRed Remote Interface Pins.

3.2.12 Pins: General Purpose Input/Output (GPIO)

The table below lists the General-Purpose Input/Output (GPIO) pins on the H22S85 chip. GPIO pins have multi-function capabilities and are CMOS-type programmable input/output. The function name that appears on the chip ball map is indicated in the **Pin Name** column. Refer to Chapter 7 for map locations.

GPIO	Pin Name	Multiplexed Function				
		First	Second	Third	Fourth	Fifth
0	**GPIO_0**	sd_hs_sel				
1	**GPIO_1**	ehci_app_prt_ovcurr0	uart2_ahb_rx	ssis_sclk	sc_c0	
2	**GPIO_2**	ehci_app_prt_ovcurr1	uart2_ahb_tx	ssis_rxd	sc_c1	
3	**GPIO_3**	ehci_prt_pwr_0	uart2_ahb_cts_n	ssis_txd	sc_c2	
4	**GPIO_4**	ehci_prt_pwr_1	uart2_ahb_rts_n	ssis_en	sc_c3	
5	**GPIO_5**	pwm_1	idsp_pip_iopad_master_hsync	vin_strig0	sc_d0	uart2_ahb_cts_n

GPIO	Pin Name	Multiplexed Function				
		First	Second	Third	Fourth	Fifth
6	GPIO_6	pwm_2	idsp_pip_iopad_master_vsync	vin_strig1	sc_d1	uart2_ahb_rts_n
7	GPIO_7	sdxc_hs_sel				
8	SC_A0	sc_a0	ssi1_sclk	norspi_clk	pwm_0	
9	SC_A1	sc_a1	ssi1_txd	norspi_dq[0]	pwm_1	
10	SC_A2	sc_a2	ssi1_rxd	norspi_dq[1]	pwm_2	
11	SC_A3	sc_a3	ssi1_en0	norspi_dq[2]	pwm_3	
12	SC_B0	sc_b0	ssi1_en1	norspi_dq[3]		
13	SC_B1	sc_b1	ssi1_en2	norspi_en0	norspi_dq[2]	
14	SC_B2	sc_b2	ssi1_en3	norspi_en[1]	norspi_dq[3]	
15	SC_B3	sc_b3	pwm_3	norspi_en[2]		
16	SC_C0	sc_c0	uart2_ahb_rx	ssis_sclk		
17	SC_C1	sc_c1	uart2_ahb_tx	ssis_rxd		
18	SC_C2	sc_c2	uart2_ahb_cts_n	ssis_txd		
19	SC_C3	sc_c3	uart2_ahb_rts_n	ssis_en		
20	SC_D0	sc_d0	uart2_ahb_rx	ssis_sclk		pwm_0
21	SC_D1	sc_d1	uart2_ahb_tx	ssis_rxd		pwm_1
22	SC_D2	sc_d2	uart2_ahb_cts_n	ssis_txd		pwm_2
23	SC_D3	sc_d3	uart2_ahb_rts_n	ssis_en		pwm_3
24	SC_E0	sc_e0	ssi0_en2	norspi_en[3]		pwm_1
25	TIMER0	tm11_clk	ssi2_en2			
26	TIMER1	tm12_clk	ssi2_en3	idsp_pip_iopad_master_hsync		
27	TIMER2	tm13_clk	ssi0_en3	idsp_pip_iopad_master_vsync		
28	IDCCLK	idc0clk				
29	IDCDATA	idc0data				
30	IDC2CLK	idc1clk		norspi_dq[2]	norspi_en[2]	
31	IDC2DATA	idc1data		norspi_dq[3]	norspi_en[3]	
32	IDC3CLK	idc2clk	vin_strig0			
33	IDC3DATA	idc2data	vin_strig1			
34	IR_IN	ir_in				
35	SSI0CLK	ssi0_sclk	norspi_clk	uart2_ahb_rx	ssis_sclk	
36	SSI0MOSI	ssi0_txd	norspi_dq[0]	uart2_ahb_tx	ssis_rxd	
37	SSI0MISO	ssi0_rxd	norspi_dq[1]	uart2_ahb_cts_n	ssis_txd	
38	SSI0EN0	ssi0_en0	norspi_en[0]	uart2_ahb_rts_n	ssis_en	
39	SSI0EN1	ssi0_en1	norspi_en[1]			
40	SSI2CLK	ssi2_sclk	idc3clk			
41	SSI2MOSI	ssi2_txd	idc3data			
42	SSI2MISO	ssi2_rxd				
43	SSI2EN0	ssi2_en0				
44	SSI2EN1	ssi2_en1				
45	UART0RX	uart0rx	uart2_ahb_rx			
46	UART0TX	uart0tx	uart2_ahb_tx			
47	UART1RX	uart1_ahb_rx				
48	UART1TX	uart1_ahb_tx				

GPIO	Pin Name	Multiplexed Function				
		First	Second	Third	Fourth	Fifth
49	UART1CTSN	uart1_ahb_cts_n				
50	UART1RTSN	uart1_ahb_rts_n				
51	I2S_CLK	i2s_clk	dmic_clk			
52	I2S_SI	i2s_si	dmic_dat			
53	I2S_SO	i2s_so				
54	I2S_WS	i2s_ws				
55	CLK_AU	clk_au				
56	ENET_TXEN	enet_txen	sc_a0	enet_txen	ssi1_txd	norspi_en[0]
57	ENET_TXD_0	enet_txd_0	sc_a1	enet_txd_0	ssi1_en0	norspi_en[1]
58	ENET_TXD_1	enet_txd_1	sc_a2	enet_txd_1	ssi1_en1	norspi_en[2]
59	ENET_TXD_2		sc_a3	enet_txd_2	ssi1_en2	
60	ENET_TXD_3		sc_b0	enet_txd_3	ssi1_en3	
61	ENET_RXD_0	enet_rxd_0	sc_b1	enet_rxd_0	ssi1_rxd	norspi_dq[0]
62	ENET_RXD_1	enet_rxd_1	sc_b2	enet_rxd_1		norspi_dq[1]
63	ENET_RXD_2		sc_b3	enet_rxd_2		norspi_dq[2]
64	ENET_RXD_3			enet_rxd_3		norspi_dq[3]
65	ENET_RXDV	enet_rxdv		enet_rxdv		
66	ENET_MDC	enet_mdc		enet_mdc		
67	ENET_MDIO	enet_mdio		enet_mdio		
68	ENET_CLK_TX	enet_2nd_ref_clk		enet_clk_tx		
69	ENET_CLK_RX	enet_ref_clk		enet_clk_rx		
70	ENET_GTX_CLK	enet_gtx_clk		enet_gtx_clk		
71	ENET_EXT_OSC_CLK			enet_ext_osc_clk		
72	WP		nand_wp			
73	SMIO_0		nand_ce	norspi_clk		
74	SMIO_1		nand_rb	norspi_dq[4]		
75	SMIO_2		sd_clk			
76	SMIO_3		sd_cmd			
77	SMIO_4		sd_cd			
78	SMIO_5		sd_wp			
79	SMIO_6		nand_re	norspi_dq[5]		
80	SMIO_7		nand_we	norspi_dq[6]		
81	SMIO_8		nand_ale	norspi_dq[7]		
82	SMIO_9		nand_d[0]	norspi_en[0]		
83	SMIO_10		nand_d[1]	norspi_en[1]		
84	SMIO_11		nand_d[2]	norspi_en[2]		
85	SMIO_12		nand_d[3]	norspi_en[3]		

GPIO	Pin Name	Multiplexed Function				
		First	Second	Third	Fourth	Fifth
86	**SMIO_13**		nand_d[4]	norspi_dq[0]		
87	**SMIO_14**		nand_d[5]	norspi_dq[1]		
88	**SMIO_15**		nand_d[6]	norspi_dq[2]		
89	**SMIO_16**		nand_d[7]	norspi_dq[3]		
90	**SMIO_17**		nand_cle			
91	**SMIO_18**		sd_d[0]			
92	**SMIO_19**		sd_d[1]			
93	**SMIO_20**		sd_d[2]			
94	**SMIO_21**		sd_d[3]			
95	**SMIO_22**		sd_d[4]		sc_c0	ssis_sclk
96	**SMIO_23**		sd_d[5]		sc_c1	ssis_rxd
97	**SMIO_24**		sd_d[6]		sc_c2	ssis_txd
98	**SMIO_25**		sd_d[7]		sc_c3	ssis_en
99	**SMIO_26**		sdxc_clk			
100	**SMIO_27**		sdxc_cmd			
101	**SMIO_28**		sdxc_d[0]		sc_d0	ssis_sclk
102	**SMIO_29**		sdxc_d[1]		sc_d1	ssis_rxd
103	**SMIO_30**		sdxc_d[2]		sc_d2	ssis_txd
104	**SMIO_31**		sdxc_d[3]		sc_d3	ssis_en
105	**SMIO_32**		sdxc_cd			
106	**SMIO_33**		sdxc_wp			
107	**SMIO_34**		sdxc_d[4]			
108	**SMIO_35**		sdxc_d[5]			
109	**SMIO_36**		sdxc_d[6]			
110	**SMIO_37**		sdxc_d[7]			
111	**SMIO_38**		sd_reset			
112	**SMIO_39**		sdxc_reset			
113	**HPD**	hdmitx_hpd				
114	**CEC**	hdmitx_cec				
115	**SVSYNC**	vin_svsync	idsp_pip_iopad_master_hsync			
116	**SHSYNC**	vin_shsync	idsp_pip_iopad_master_vsync			
117	**SENSOR_RST**					
118	**VD0_OUT_0**	vd0_out[0]				
119	**VD0_OUT_1**	vd0_out[1]				
120	**VD0_OUT_2**	vd0_out[2]				
121	**VD0_OUT_3**	vd0_out[3]				
122	**VD0_OUT_4**	vd0_out[4]				
123	**VD0_OUT_5**	vd0_out[5]				
124	**VD0_OUT_6**	vd0_out[6]				
125	**VD0_OUT_7**	vd0_out[7]				
126	**VD0_OUT_8**	vd0_out[8]				
127	**VD0_OUT_9**	vd0_out[9]				
128	**VD0_OUT_10**	vd0_out[10]				

GPIO	Pin Name	Multiplexed Function				
		First	Second	Third	Fourth	Fifth
129	**VD0_ OUT_11**	vd0_out[11]				
130	**VD0_ OUT_12**	vd0_out[12]				
131	**VD0_ OUT_13**	vd0_out[13]				
132	**VD0_ OUT_14**	vd0_out[14]				
133	**VD0_ OUT_15**	vd0_out[15]				
134	**VD0_CLK**	vd0_clk				
135	**VD0_VSYNC**	vd0_vsync				
136	**VD0_HSYNC**	vd0_hsync				
137	**VD0_HVLD**	vd0_hvld				
138	**VD_PWM**	pwm_0				

Table 3-14. General Purpose Input Output (GPIO) Multifunction-Capable Pins.

3.2.13 Pins: Analog to Digital Conversion (ADC)

Name	Location	Dir	Type	Description
ADC_CH_[1:3]	E7, E8, E9	I	Analog	ADC analog input (3 channels)

Table 3-15. ADC Interface Pins.

3.2.14 Pins: Power Controller (PWC) and Real Time Clock (RTC)

Name	Location	Dir	Type	Description
XI_RTC	B18	I	XOSC	Connect to RTC crystal
XO_RTC	A18	O	XOSC	Connect to RTC crystal
PWC_WKUP	A19	I	CMOS	In the power-off state, a positive pulse can only trigger a power-on sequence
PWC_PSEQ[3:1]	B19, C18, A20	O	CMOS	Power up/ down control signals
PWC_RSTINB	B20	I	CMOS	PWC reset input. Usually pulled up to **PWC_PC_VDD** through an RC circuit.
PWC_AVDD33	D18	O	CMOS	PWC power
PWC_RSTOB	D19	O	CMOS	Reset signal out (also used as Power up/down signal)
PWC_AVDD18	E18	O	CMOS	UTE power

Table 3-16. PWC and RTC Interface Pins.

3.2.15 Pins: Real Time Clock (RTC)

Name	Location	Dir	Type	Description
PWC_AVDD18	E18	S	Analog Supply	Power for RTC module and on-chip RTC oscillator. When **RTC_CP** is less than a specified voltage, the power controller will shut down and all registers will reset.
XI_RTC	B18	I	XOSC	Connect to RTC crystal
XO_RTC	A18	O		

Table 3-17. RTC Interface Pins.

3.2.16 Pins: Timer

Name	Location	Dir	Type	Description
TIMER0	AA21	I/O	CMOS	Interval Timer 0 external clock source
TIMER1	W18	I/O	CMOS	Interval Timer 1 external clock source
TIMER2	AA20	I/O	CMOS	Interval Timer 2 external clock source

Table 3-18. Timer Pins.

3.2.17 Pins: Pulse Width Modulator (PWM)

Name	Location	Dir	Type	Description
VD_PWM	Y4	I/O	CMOS	Pulse Width Modulator Output

Table 3-19. PWM Pins.

3.2.18 Pins: JTAG Control

Name	Location	Dir	Pad Type	Description
JTAG_CLK	W13	I	CMOS	Clock
JTAG_RST_L	AA13	I	CMOS	Reset
JTAG_TDI	U13	I	CMOS	Data in
JTAG_TDO	Y13	O	CMOS	Data out
JTAG_TMS	V12	I	CMOS	Test mode select

Table 3-20. JTAG Pins.

3.2.19 Pins: Global and Test

Name	Location	Dir	Type	Description
POR_L	U11	I	CMOS	Power-on reset pin (active low)
TEST_MODE	V10	I	CMOS	0 - Normal mode 1 - Test mode
XIN	A17	I	XOSC	24-MHz or 48-MHz crystal or crystal oscillator input
XOUT	B17	O		
FSOURCE_0	Y19	S	Power / ground	Power supply for Efuse programming. Customer ties to digital ground for normal operation.
VDDWL_0	Y20	P	Power/ Ground	Power supply for Efuse programming. Customer ties to digital ground for normal operation.

Table 3-21. Global and Test Pins.

3.2.20 Pins: Power, Ground and PLL

Name	Location	Dir	Type	Description
AVDD33	E16	S	Analog Supply	3.3V Analog power supply
AVSS	C13, C14	G	Analog Ground	ADC analog ground
VDDI	H9, H11, H13, J9, J11, J13, K9, K11, K13, L9, L11, L13, M9, M11, M13, N9, N11, N13, P9,	S	Digital Supply	Digital power supply, 0.8V nominal
SD_VDDO	K14, L14	S	Digital Supply	SD controller digital IO power
VDDO	G17, P11, P12, P13	S	IO Power	IO Power
VDDP	F17, P8	S	IO Power	IO predriver Power, 1.8V nominal
VSSI	C6, C10, C11, C12, C15, C16, D9, D10, D11, E10, E11, E12, E13, E14, E15, F18, H8, H10, H12, H14, J8, J10, J12 J14, K8, K10, K12, L8, L10, L12, M8, M10, M12, M14, N8, N10, N12, N14, P10, P14	G	Digital Ground	Digital ground
AVDD	D13	S	Analog Supply	Analog power supply, 0.8V nominal
AVDD18	D12, D15	S	Analog Supply	Analog power supply, 1.8V nominal
MIPI_ANA_ AVDD18_IO	D14	P	Digital Power	MIPI CMOS IO Power for MIPI LS or LVCMOS RX
DVDD	D16	P	Digital Power	Digital Power Analog block, 0.8V nominal
SDXC_VDDO	E17	O	Digital Power	Digital IO Power for SDXC, 3.3V / 1.8V

Name	Location	Dir	Type	Description
NAND_VDDO	H17	P	Digital Power	Digital IO Power for NAND, 3.3V / 1.8V

Table 3-22. Power, Ground and PLL Pins.

4. ELECTRICAL CHARACTERISTICS

4.1 Electrical: Overview

This chapter provides details on the electrical characteristics of the H22S85 chip as follows:

- (Section 4.1) Electrical: Overview
- (Section 4.2) Electrical: Absolute Ratings
- (Section 4.3) Electrical: Recommended Operating Conditions
- (Section 4.4) Electrical: Fail-Safe Pins
- (Section 4.5) Electrical: Video Signal Wave Forms and Timing
- (Section 4.6) Electrical: SD Controller Timing
- (Section 4.7) Electrical: eMMC Boot Timing

Note that the electrical details provided in this chapter are preliminary estimates.

4.2 Electrical: Absolute Ratings

The following table provides absolute ratings for the nominal analog/digital voltages of the H22S85 power rails.

Parameter	Minimum	Maximum
Analog supply voltage (3.0 V)	-0.3 V	3.6 V
Digital supply voltage (3.0 V)	-0.3 V	3.6 V
Analog supply voltage (1.8 V)	-0.3 V	1.98 V
Digital supply voltage (1.8 V)	-0.3 V	1.98 V
Analog supply voltage (0.9 V)	-0.3 V	0.95 V
Digital supply voltage (0.8 V)	-0.3 V	0.95 V
Digital I/O range (V)	-0.3 V	3.6 V
	-0.3 V	1.98 V
Analog I/O range (V)	-0.3 V	3.6 V
	-0.3 V	1.98 V
Operating temperature (case) (°C)	-20 °C	85 °C

Table 4-1. Absolute Ratings.

This Ambarella part will support a full range of operation at the case temperature specified above, provided that the customer's PCB design, manufacturing processes, and power supply design are equal to those of the Ambarella reference hardware platform in terms of quality. All other components used during system design are also required to operate successfully at the case temperature range specified above to guarantee proper overall system operation.

4.3 Electrical: Recommended Operating Conditions

This section continues with recommended operating conditions for:

- (Section 4.3.1) Operating Conditions: Power Rails - DC Characteristics
- (Section 4.3.2) Operating Conditions: Digital I/O
- (Section 4.3.3) Operating Conditions: DRAM I/O
- (Section 4.3.4) Operating Conditions: PWC and RTC Power Supply
- (Section 4.3.5) Operating Conditions: Video Input
- (Section 4.3.6) Operating Conditions: Video DAC
- (Section 4.3.7) Operating Conditions: ADC Electrical Specifications
- (Section 4.3.8) Operating Conditions: Crystal and Reference Clock Requirements

4.3.1 Operating Conditions: Power Rails - DC Characteristics

Parameter [1]	Comments	Minimum	Typical	Maximum	Ripple
DDR[0:1]_VDDQ_CKE / DDR[0:1]_VDDQ	LPDDR2/3 Mode	1.14 V	1.2 V	1.3 V	2%
	DDR3 Mode	1.4 V	1.5 V	1.6 V	2%
	DDR3L Mode	1.28 V	1.35 V	1.45 V	2%
	-	-	-	-	-
AVDD		0.8 V	0.85 V	0.9 V	2%
DVDD		0.8 V	0.85 V	0.9 V	2%
AVDD18		1.7 V	1.8 V	1.9 V	2%
HDMI_AVDD18_ESD		1.7 V	1.8 V	1.9 V	2%
PWC_AVDD33		3.0 V	3.3 V	3.6 V	2%
PWC_AVDD18		0.7 V	1.8 V	1.98 V	2%
AVDD33		2.85 V	3.0 V	3.6 V	2%
VDDI		0.86 V	0.88 V	0.9 V	2%
VDDO	3.0-V mode	2.85 V	3.0 V	3.6 V	2%
	1.8-V mode	1.7 V	1.8 V	1.9 V	2%
VDDO_NAND	3.0-V mode	2.85 V	3.0 V	3.6 V	2%
	1.8-V mode	1.7 V	1.8 V	1.9 V	2%
VDDO_SD / VDDO_SDXC	SD / SDIO mode	2.85 V	3.0 V	3.6 V	2%
	SDXC mode	1.7 V	1.8 V	1.9 V	2%
VDDP		1.7 V	1.8 V	1.9 V	2%
-		-	-	-	-
-		-	-	-	-

Table 4-2. Power Rails: DC Characteristics (Preliminary and Subject to Change).

Note:

1. The electrical details provided in this chapter are preliminary estimates and are subject to change. Please contact an Ambarella representative for current electrical specifications.

2. Please ensure that the voltage setting is not lower than 0.69 V.

3.

4.3.2 Operating Conditions: Digital I/O

Parameter	Comments	Minimum	Typical	Maximum
VIL	Input Low Voltage	-0.3 V		0.7 V
VIH	Input High Voltage	2.0 V		3.6 V (for 3.3 V-tolerant pins)
VOL	Output Low Voltage			0.4 V
VOH	Output High Voltage	2.4 V		

Table 4-3. Digital I/O Characteristics (Preliminary).

4.3.3 Operating Conditions: DRAM I/O

4.3.3.1 DRAM: DC Supply Voltage Levels

Parameter	Comments	Minimum	Typical	Maximum
DDR[0:1]_VDDQ		See Section 4.3.1		
DDR[0:1]_VDDQ_CKE		See Section 4.3.1		
-		-		
-		-		
VTT	Termination voltage	DDR_VREF - 0.04 V	DDR_VREF	DDR_VREF + 0.04 V
DDR[0:1]_VREF	Input reference level	0.49 * DDR_VDDQ	0.5 * VDDQ	0.51 * DDR_VDDQ

Table 4-4. DRAM I/O Characteristics - DC Supply Voltage Levels (Preliminary).

4.3.3.2 DRAM: SSTL I/O DC Specifications

Parameter	Comments	Minimum	Typical	Maximum
VIHT	DC input logic threshold high			DDR_VREF + 0.05 V
VILT	DC input logic threshold low	DDR_VREF - 0.05 V		
VIH	DC input voltage high	DDR_VREF + 100 mV		VDDQ + 0.3 V

Parameter	Comments	Minimum	Typical	Maximum
VIL	DC input voltage low	-0.3 V		DDR_VREF - 100 mV
VOH	DC output logic high	DDR_VDDQ		
VOL	DC output logic low			0 V
RTT1	RTT effective impedance	60 Ohms	75 Ohms	90 Ohms
RTT2	RTT effective impedance	120 Ohms	150 Ohms	180 Ohms

Table 4-5. DRAM I/O Characteristics - SSTL I/O DC Specifications (Preliminary).

4.3.4 Operating Conditions: PWC and RTC Power Supply

Parameter	Comments	Minimum	Typical	Maximum
PWC_AVDD18	RTC module supply	0.7 V	1.8 V	1.98 V
PWC_AVDD33	Power management supply	3.0 V	3.3 V	
VIH	For PWC_WKUP	1.7 V		
VIL	For PWC_WKUP			1.0 V
VOH	PWC_PSEQ[1:3], PWC_ RSTOB	1.5 V		
VOL	VOH(min)=1.5V at 10uA loading; Need to add buffer for higher loadings.			0.5 V

Table 4-6. PWC and RTC Supply.

4.3.5 Operating Conditions: Video Input

4.3.5.1 VIN: SLVS / LVCMOS I/O

Parameter	Symbol	Comment	Min	Typ.	Max.
Digital Input Voltage	VIL	LVCMOS 1.2 V			0.5 V
		LVCMOS 1.8 V			0.6 V
	VIH	LVCMOS 1.2 V	0.8 V		
		LVCMOS 1.8 V	1.2 V		
Differential Input for SLVS	V_{CM}		0.2 V		1.0 V
	V_{DIFF}		70 mV		400 mV

Table 4-7. DC Characteristics: SLVS Interface.

4.3.6 Operating Conditions: Video DAC

Parameter	Comments	Minimum	Typical	Maximum
IO_{FS}	IO out current		34.6 mA	
I_{OP}	Operating Current		36 mA	
V(IO)	Out voltage full scale	1.17 V	1.28 V	1.43 V
Resolution	DAC resolution			10 bits
DNL	Differential non-linearity error			±1 LSB
INL	Integral non-linearity error			±2 LSB
VREF	Reference Voltage			1.22 V

Table 4-8. Video DAC Electrical Specifications.

4.3.7 Operating Conditions: ADC Electrical Specifications

4.3.7.1 ADC Electrical: DC Specification

Parameter	Comments	Minimum	Typical	Maximum
VREF	Reference Voltage (Top) (Low reference is ADC_AVSS)	ADC_AVDD	ADC_AVDD	ADC_AVDD
VIN	Analog input voltage	ADC_AVSS		VREF
N	Resolution		12 bits	
INL	INL		±1 LSB	±4 LSB
DNL	DNL		±0.5 LSB	±1 LSB

Table 4-9. ADC DC Specification.

4.3.7.2 ADC Electrical: AC Specification

Parameter	Comments	Minimum	Typical	Maximum
Fs	Sampling rate	50 K		1 MS/s
FCLK	Sampling clock		12 MHz	

Parameter	Comments	Minimum	Typical	Maximum
SNDR	Signal-to-noise and distortion ratio (Fclk = 5 MHz and AIN = 50 KHz*)	54 dB	60 dB	

Table 4-10. ADC AC Specification.

4.3.8 Operating Conditions: Crystal and Reference Clock Requirements

4.3.8.1 Crystal and Reference Clock Requirements: 24 MHz

Description	Minimum	Typical	Maximum
Crystal frequency	N/A	24 MHz only	N/A
Crystal accuracy			± 30 PPM
Cycle-to-cycle jitter			± 200 ps
Long-term jitter			± 500 ps

Table 4-11. Jitter Specifications.

4.3.8.2 Crystal and Reference Clock Requirements: 32.768 KHz

Description	Minimum	Typical	Maximum
Crystal accuracy			± 30 PPM

Table 4-12. Jitter Specifications (32.768 KHz).

4.4 Electrical: Fail-Safe Pins

The H22S85 chip provides a number of fail-safe CMOS pins that can have active signals at or below 3.6 V when the H22S85 is powered down.

GPIO	Pin Name	Multiplexed Function				
		First	Second	Third	Fourth	Fifth
0	**GPIO_0**	sd_hs_sel				
1	**GPIO_1**	ehci_app_prt_ovcurr0	uart2_ahb_rx	ssis_sclk	sc_c0	
2	**GPIO_2**	ehci_app_prt_ovcurr1	uart2_ahb_tx	ssis_rxd	sc_c1	
3	**GPIO_3**	ehci_prt_pwr_0	uart2_ahb_cts_n	ssis_txd	sc_c2	
4	**GPIO_4**	ehci_prt_pwr_1	uart2_ahb_rts_n	ssis_en	sc_c3	
5	**GPIO_5**	pwm_1	idsp_pip_iopad_master_hsync	vin_strig0	sc_d0	uart2_ahb_cts_n
6	**GPIO_6**	pwm_2	idsp_pip_iopad_master_vsync	vin_strig1	sc_d1	uart2_ahb_rts_n

GPIO	Pin Name	Multiplexed Function				
		First	Second	Third	Fourth	Fifth
7	GPIO_7	sdxc_hs_sel				
8	SC_A0	sc_a0	ssi1_sclk	norspi_clk	pwm_0	
9	SC_A1	sc_a1	ssi1_txd	norspi_dq[0]	pwm_1	
10	SC_A2	sc_a2	ssi1_rxd	norspi_dq[1]	pwm_2	
11	SC_A3	sc_a3	ssi1_en0	norspi_dq[2]	pwm_3	
12	SC_B0	sc_b0	ssi1_en1	norspi_dq[3]		
13	SC_B1	sc_b1	ssi1_en2	norspi_en0	norspi_dq[2]	
14	SC_B2	sc_b2	ssi1_en3	norspi_en[1]	norspi_dq[3]	
15	SC_B3	sc_b3	pwm_3	norspi_en[2]		
16	SC_C0	sc_c0	uart2_ahb_rx	ssis_sclk		
17	SC_C1	sc_c1	uart2_ahb_tx	ssis_rxd		
18	SC_C2	sc_c2	uart2_ahb_cts_n	ssis_txd		
19	SC_C3	sc_c3	uart2_ahb_rts_n	ssis_en		
20	SC_D0	sc_d0	uart2_ahb_rx	ssis_sclk		pwm_0
21	SC_D1	sc_d1	uart2_ahb_tx	ssis_rxd		pwm_1
22	SC_D2	sc_d2	uart2_ahb_cts_n	ssis_txd		pwm_2
23	SC_D3	sc_d3	uart2_ahb_rts_n	ssis_en		pwm_3
24	SC_E0	sc_e0	ssi0_en2	norspi_en[3]		pwm_1
25	TIMER0	tm11_clk	ssi2_en2			
26	TIMER1	tm12_clk	ssi2_en3	idsp_pip_iopad_master_hsync		
27	TIMER2	tm13_clk	ssi0_en3	idsp_pip_iopad_master_vsync		
28	IDCCLK	idc0clk				
29	IDCDATA	idc0data				
30	IDC2CLK	idc1clk		norspi_dq[2]	norspi_en[2]	
31	IDC2DATA	idc1data		norspi_dq[3]	norspi_en[3]	
32	IDC3CLK	idc2clk	vin_strig0			
33	IDC3DATA	idc2data	vin_strig1			
34	IR_IN	ir_in				
35	SSI0CLK	ssi0_sclk	norspi_clk	uart2_ahb_rx	ssis_sclk	
36	SSI0MOSI	ssi0_txd	norspi_dq[0]	uart2_ahb_tx	ssis_rxd	
37	SSI0MISO	ssi0_rxd	norspi_dq[1]	uart2_ahb_cts_n	ssis_txd	
38	SSI0EN0	ssi0_en0	norspi_en[0]	uart2_ahb_rts_n	ssis_en	
39	SSI0EN1	ssi0_en1	norspi_en[1]			
40	SSI2CLK	ssi2_sclk	idc3clk			
41	SSI2MOSI	ssi2_txd	idc3data			
42	SSI2MISO	ssi2_rxd				
43	SSI2EN0	ssi2_en0				
44	SSI2EN1	ssi2_en1				
45	UART0RX	uart0rx	uart2_ahb_rx			
46	UART0TX	uart0tx	uart2_ahb_tx			
47	UART1RX	uart1_ahb_rx				
48	UART1TX	uart1_ahb_tx				
49	UART1CTSN	uart1_ahb_cts_n				
50	UART1RTSN	uart1_ahb_rts_n				
51	I2S_CLK	i2s_clk	dmic_clk			

GPIO	Pin Name	Multiplexed Function				
		First	Second	Third	Fourth	Fifth
52	I2S_SI	i2s_si	dmic_dat			
53	I2S_SO	i2s_so				
54	I2S_WS	i2s_ws				
55	CLK_AU	clk_au				
56	ENET_TXEN	enet_txen	sc_a0	enet_txen	ssi1_txd	norspi_en[0]
57	ENET_ TXD_0	enet_txd_0	sc_a1	enet_txd_0	ssi1_en0	norspi_en[1]
58	ENET_ TXD_1	enet_txd_1	sc_a2	enet_txd_1	ssi1_en1	norspi_en[2]
59	ENET_ TXD_2		sc_a3	enet_txd_2	ssi1_en2	
60	ENET_ TXD_3		sc_b0	enet_txd_3	ssi1_en3	
61	ENET_ RXD_0	enet_rxd_0	sc_b1	enet_rxd_0	ssi1_rxd	norspi_dq[0]
62	ENET_ RXD_1	enet_rxd_1	sc_b2	enet_rxd_1		norspi_dq[1]
63	ENET_ RXD_2		sc_b3	enet_rxd_2		norspi_dq[2]
64	ENET_ RXD_3			enet_rxd_3		norspi_dq[3]
65	ENET_RXDV	enet_rxdv		enet_rxdv		
66	ENET_MDC	enet_mdc		enet_mdc		
67	ENET_MDIO	enet_mdio		enet_mdio		
68	ENET_CLK_ TX	enet_2nd_ref_ clk		enet_clk_tx		
69	ENET_CLK_ RX	enet_ref_clk		enet_clk_rx		
70	ENET_GTX_ CLK	enet_gtx_clk		enet_gtx_clk		
71	ENET_EXT_ OSC_CLK			enet_ext_osc_ clk		
72	WP		nand_wp			
73	SMIO_0		nand_ce	norspi_clk		
74	SMIO_1		nand_rb	norspi_dq[4]		
75	SMIO_2		sd_clk			
76	SMIO_3		sd_cmd			
77	SMIO_4		sd_cd			
78	SMIO_5		sd_wp			
79	SMIO_6		nand_re	norspi_dq[5]		
80	SMIO_7		nand_we	norspi_dq[6]		
81	SMIO_8		nand_ale	norspi_dq[7]		
82	SMIO_9		nand_d[0]	norspi_en[0]		
83	SMIO_10		nand_d[1]	norspi_en[1]		
84	SMIO_11		nand_d[2]	norspi_en[2]		
85	SMIO_12		nand_d[3]	norspi_en[3]		
86	SMIO_13		nand_d[4]	norspi_dq[0]		
87	SMIO_14		nand_d[5]	norspi_dq[1]		
88	SMIO_15		nand_d[6]	norspi_dq[2]		

GPIO	Pin Name	Multiplexed Function				
		First	Second	Third	Fourth	Fifth
89	**SMIO_16**		nand_d[7]	norspi_dq[3]		
90	**SMIO_17**		nand_cle			
91	**SMIO_18**		sd_d[0]			
92	**SMIO_19**		sd_d[1]			
93	**SMIO_20**		sd_d[2]			
94	**SMIO_21**		sd_d[3]			
95	**SMIO_22**		sd_d[4]		sc_c0	ssis_sclk
96	**SMIO_23**		sd_d[5]		sc_c1	ssis_rxd
97	**SMIO_24**		sd_d[6]		sc_c2	ssis_txd
98	**SMIO_25**		sd_d[7]		sc_c3	ssis_en
99	**SMIO_26**		sdxc_clk			
100	**SMIO_27**		sdxc_cmd			
101	**SMIO_28**		sdxc_d[0]		sc_d0	ssis_sclk
102	**SMIO_29**		sdxc_d[1]		sc_d1	ssis_rxd
103	**SMIO_30**		sdxc_d[2]		sc_d2	ssis_txd
104	**SMIO_31**		sdxc_d[3]		sc_d3	ssis_en
105	**SMIO_32**		sdxc_cd			
106	**SMIO_33**		sdxc_wp			
107	**SMIO_34**		sdxc_d[4]			
108	**SMIO_35**		sdxc_d[5]			
109	**SMIO_36**		sdxc_d[6]			
110	**SMIO_37**		sdxc_d[7]			
111	**SMIO_38**		sd_reset			
112	**SMIO_39**		sdxc_reset			
113	**HPD**	hdmitx_hpd				
114	**CEC**	hdmitx_cec				
115	**SVSYNC**	vin_svsync	idsp_pip_iopad_master_hsync			
116	**SHSYNC**	vin_shsync	idsp_pip_iopad_master_vsync			
117	**SENSOR_RST**					
118	**VD0_OUT_0**	vd0_out[0]				
119	**VD0_OUT_1**	vd0_out[1]				
120	**VD0_OUT_2**	vd0_out[2]				
121	**VD0_OUT_3**	vd0_out[3]				
122	**VD0_OUT_4**	vd0_out[4]				
123	**VD0_OUT_5**	vd0_out[5]				
124	**VD0_OUT_6**	vd0_out[6]				
125	**VD0_OUT_7**	vd0_out[7]				
126	**VD0_OUT_8**	vd0_out[8]				
127	**VD0_OUT_9**	vd0_out[9]				

GPIO	Pin Name	Multiplexed Function				
		First	Second	Third	Fourth	Fifth
128	**VD0_ OUT_10**	vd0_out[10]				
129	**VD0_ OUT_11**	vd0_out[11]				
130	**VD0_ OUT_12**	vd0_out[12]				
131	**VD0_ OUT_13**	vd0_out[13]				
132	**VD0_ OUT_14**	vd0_out[14]				
133	**VD0_ OUT_15**	vd0_out[15]				
134	**VD0_CLK**	vd0_clk				
135	**VD0_VSYNC**	vd0_vsync				
136	**VD0_HSYNC**	vd0_hsync				
137	**VD0_HVLD**	vd0_hvld				
138	**VD_PWM**	pwm_0				

Table 4-13. Fail-Safe Pins Which Can Have Active Signals At or Below 3.6 V When the H22S85 is Powered Down.

4.5 Electrical: Video Signal Wave Forms and Timing

4.5.1 Video Waveform: Video Input (VIN) LVCMOS Timing

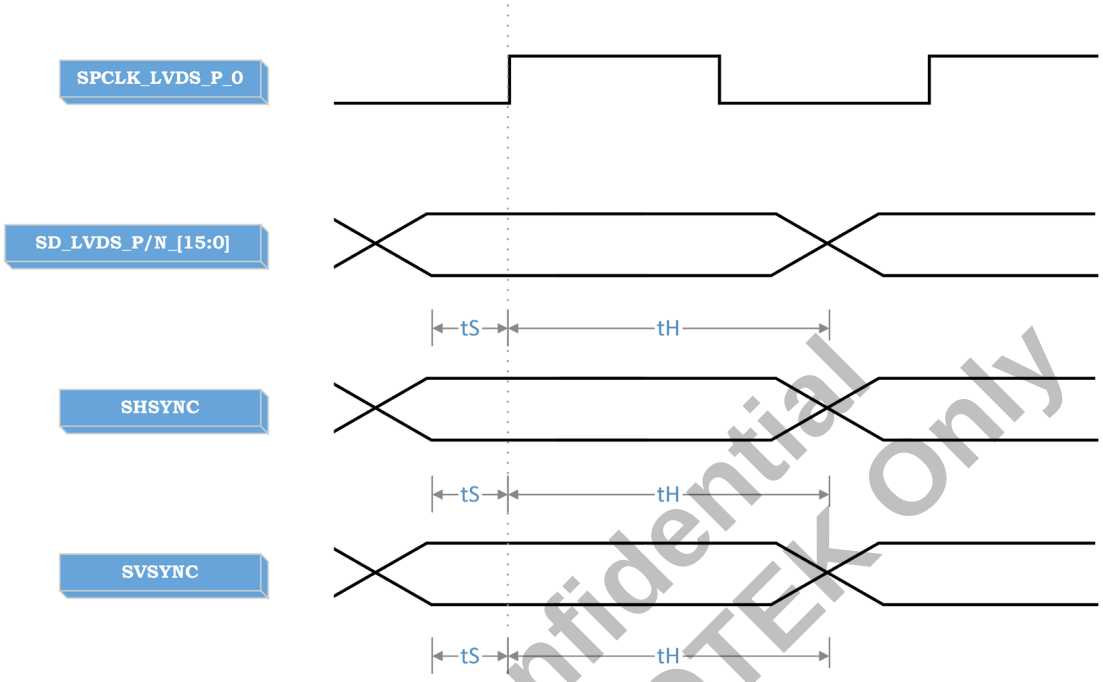


Figure 4-1. Video Input (VIN) LVCMOS Timing.

Parameter	Setup (tS)	Hold (tH)	Comment
Data: **SD_LVDS_P/N_[16:0]**	2 ns	2 ns	Assume the rising edge of the pixel clock **SPCLK_LVDS_P_0** is used to latch the data.
HSync: **SHSYNC**	2 ns	2 ns	
VSync: **SVSYNC**	2 ns	2 ns	
SField: (See Section 2.3)	2 ns	2 ns	

*Table 4-14. LVCMOS Video Input Timing Setup/Hold With Respect to **SPCLK_LVDS_P/N_[N]**.*

4.5.2 Video Waveform: Video Input (VIN) SLVS Timing

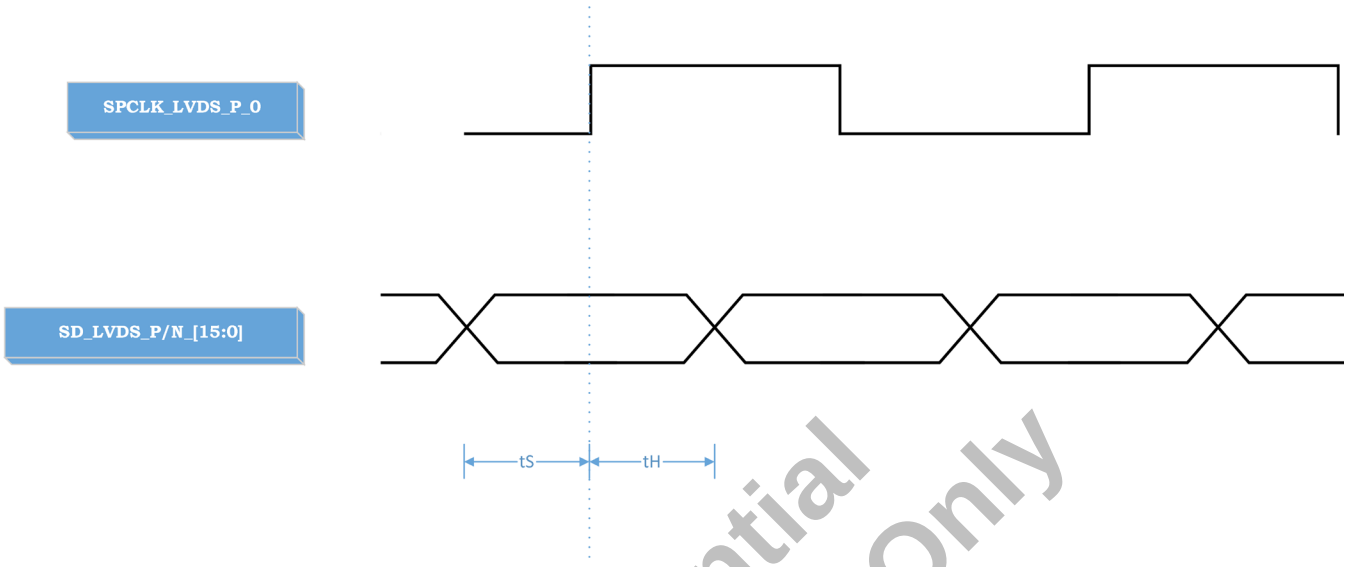


Figure 4-2. Video Input (VIN) SLVS Timing.

Parameter	Setup (tS)	Hold (tH)	Comment
Data: **SD_LVDS_P/N_[16:0]**	150 ps	150 ps	Assume the rising edge of the pixel clock **SPCLK_LVDS_P_0** is used to latch the data.

*Table 4-15. SLVS Video Input Timing Setup/Hold With Respect to **SPCLK_LVDS_P/N_[N]**.*

4.5.3 Video Waveform: Video Output (VOUT) Timing

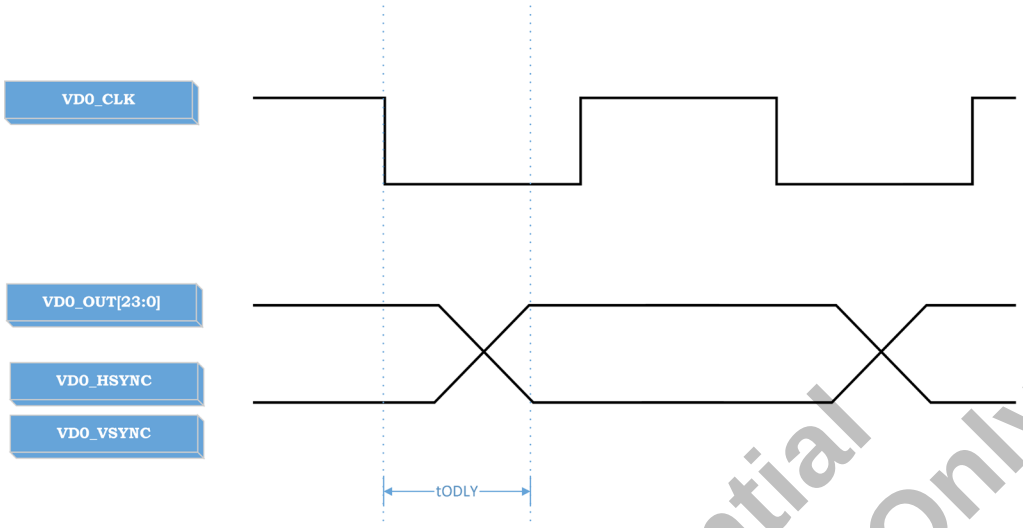


Figure 4-3. Video Output Timing.

Parameter	Minimum	Typical	Maximum	Comment
VD0_CLK Frequency		Resolution Dependent		Assume the data is latched out at the falling edge of **VD0_CLK**.
VD0_CLK Duty	40%	50%	60%	
tODLY Output Delay	-2 ns		2 ns	

*Table 4-16. Video Output Timing Setup/Hold With Respect to **VD0_CLK**.*

4.6 Electrical: SD Controller Timing

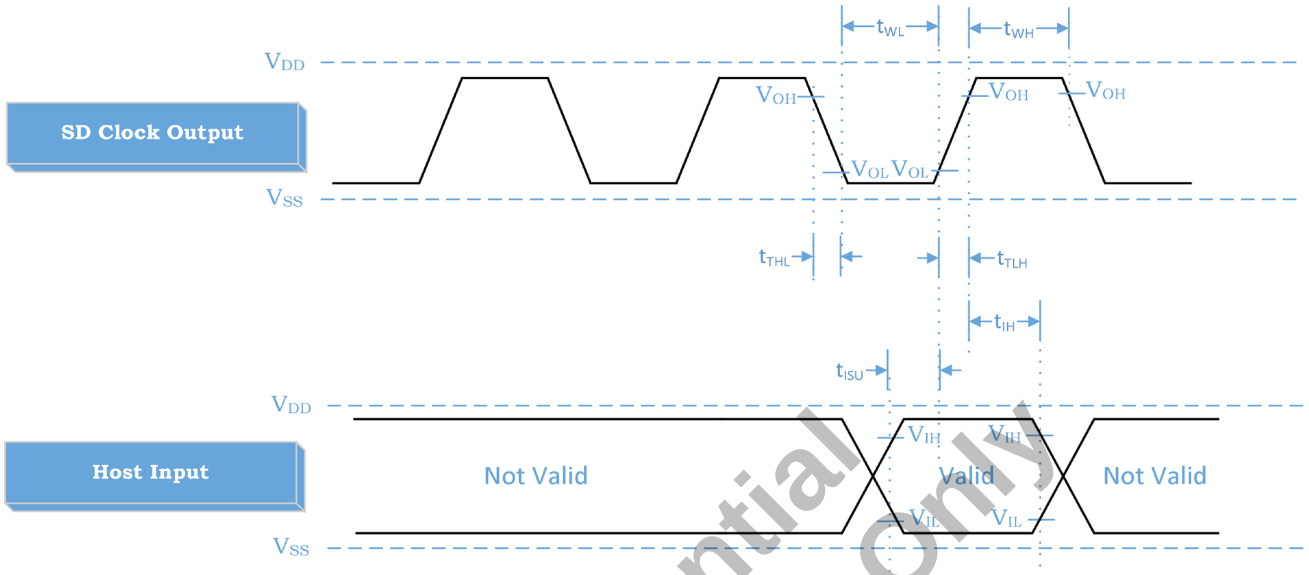


Figure 4-4. SD Host Input Timing.

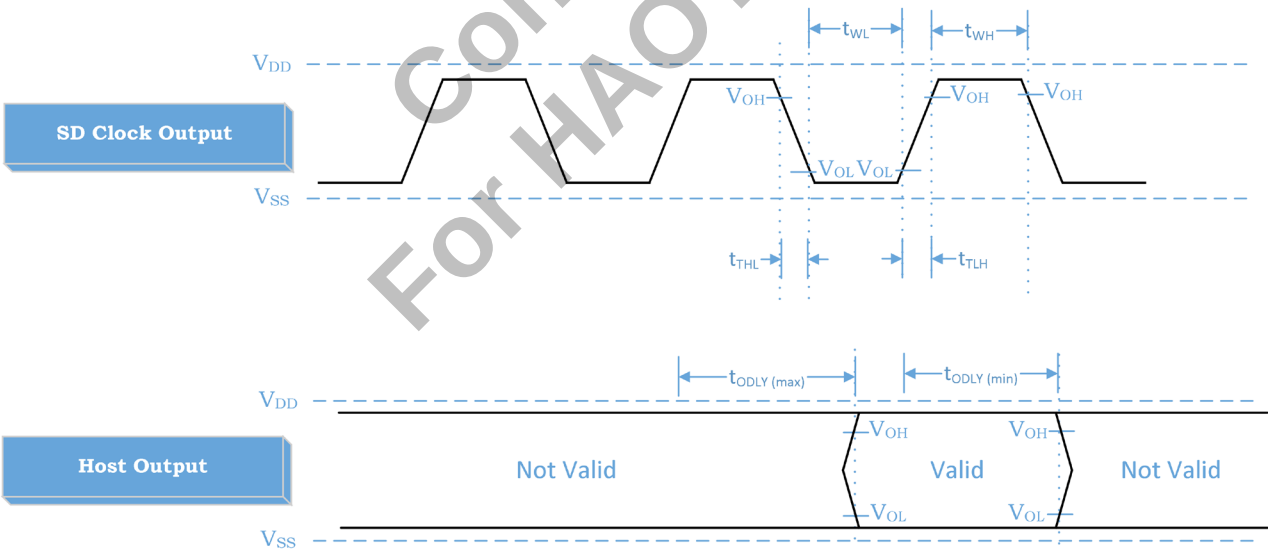


Figure 4-5. SD Host Output Timing.

Parameter	Symbol	Min	Max	Unit	Comment
Clock CLK: All values are referred to as min (VIH) and max (VIL)					
Clock Frequency: Data Transfer Mode	f_{PP}	0	48	MHz	C_{CARD} ≤ 10 pF (1 Card)
Clock Frequency: Identification Mode	f_{OD}	0/100	400	kHz	C_{CARD} ≤ 10 pF (1 Card)
Clock Low Time	t_{WL}	7		ns	C_{CARD} ≤ 10 pF (1 Card)
Clock High Time	t_{WH}	7		ns	C_{CARD} ≤ 10 pF (1 Card)
Clock Rise Time	t_{TLH}		3	ns	C_{CARD} ≤ 10 pF (1 Card)
Clock Fall Time	t_{THL}		3	ns	C_{CARD} ≤ 10 pF (1 Card)
Inputs CMD, DAT: Referenced to CLK					
Input Set-Up Time	t_{ISU}	6		ns	C_{CARD} ≤ 10 pF (1 Card)
Input Hold Time	t_{IH}	1.5		ns	C_{CARD} ≤ 10 pF (1 Card)
Outputs CMD, DAT: Referenced to CLK at 48 MHz					
Output Delay Time	t_{ODLY}	8.5	12.5	ns	C_L ≤ 40 pF (1 Card)

Table 4-17. SD Controller Timing Parameters.

4.7 Electrical: eMMC Boot Timing

To successfully boot from eMMC, the eMMC device should return boot data with the following timing constraints.

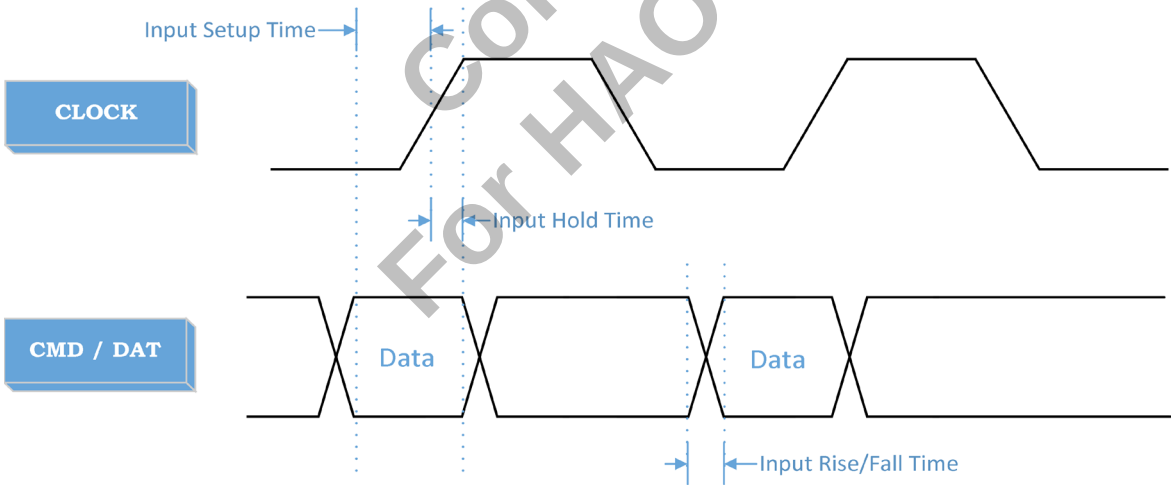


Figure 4-6. eMMC Boot Timing Diagram.

Parameter	Minimum	Maximum
Host CMD / DAT Input Timing		
Input Setup Time	6 ns	
Input Hold Time	1.5 ns	
Signal Rise Time		3 ns
Signal Fall Time		3 ns

Table 4-18. eMMC Boot Timing.

Note:

1. CMD / DAT input rise and fall time are measured by VIL and VIH.

5. PACKAGE

The H22S85 chip has a 369-pin WFBGA package (14 mm x 14 mm).

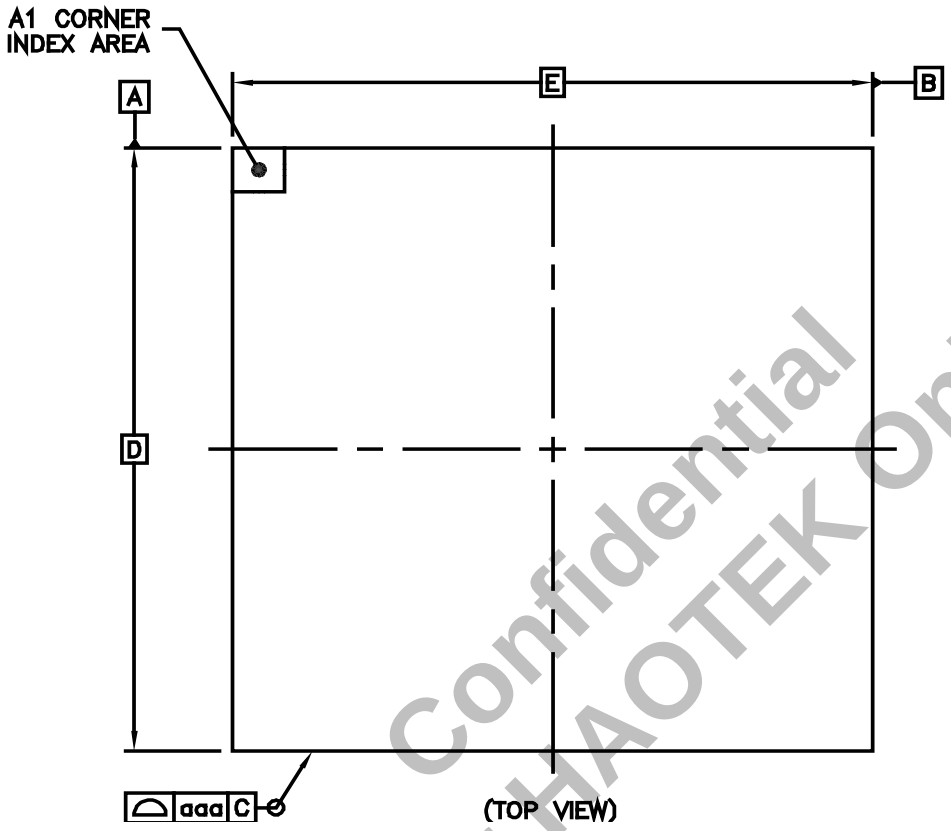


Figure 5-1. Top View of the H22S85 Package.

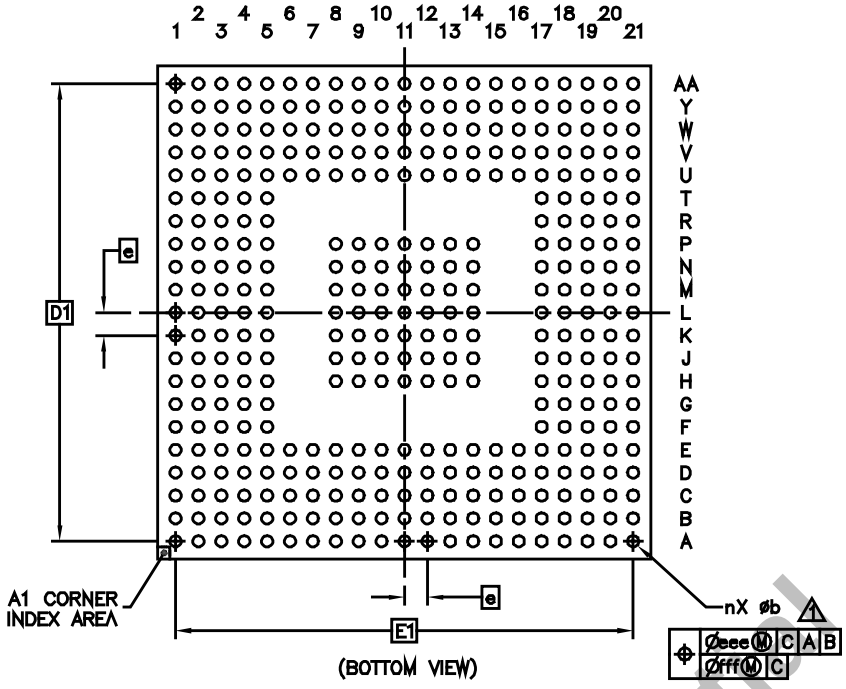


Figure 5-2. Bottom View of the H22S85 Package.

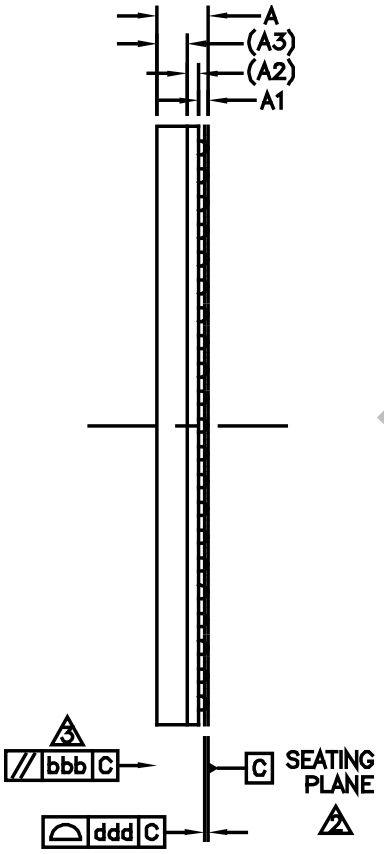


Figure 5-3. Side View of the H22S85 Package.

Description	Symbol	Minimum	Nominal	Maximum
Total Thickness	A			1.3
Stand Off	A1	0.16		0.26
Substrate Thickness	A2		0.24 REF	
Mold Thickness	A3		0.7 REF	
Body Size	D		14 BSC	
	E		14 BSC	
Ball Diameter			0.3	
Ball Opening			0.275	
Ball Width	b	0.27		0.37
Ball Pitch	e		0.65 BSC	
Ball Count	n		369	
Edge Ball Center to Center	D1		13 BSC	
	E1		13 BSC	
Body Center to Contact Ball	SD			
	SE			
Package Edge Tolerance	aaa		0.1	
Mold Flatness	bbb		0.2	
Coplanarity	ddd		0.08	
Ball Offset (Package)	eee		0.15	
Ball Offset (Ball)	fff		0.08	

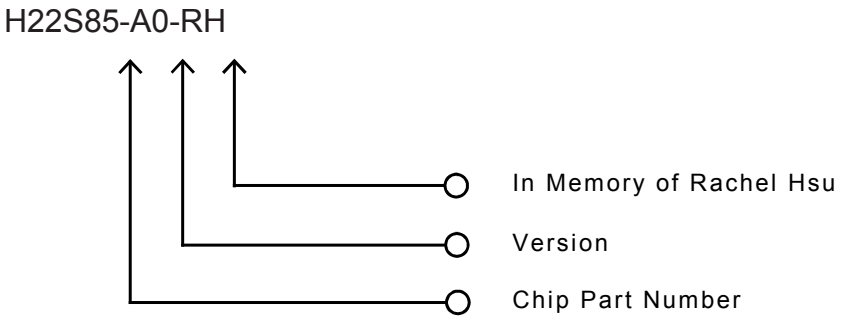
Table 5-1. Dimensions of the H22S85 Package (millimeters).

Notes for table and figures:

1. All dimensions are in millimeters.
2. Dimension b is measured at the maximum solder ball diameter, parallel to Datum Plane C.
3. Datum C (Seating Plane) is defined by the spherical crowns of the solder balls.
4. Parallelism measurement excludes any effect of mark on top surface of the package.
5. Dimension and Tolerances: ASME Y14.5M

6. CONTACT AND ORDER INFORMATION

All chips in the H22S85 series are Lead-Free, Halogen-Free and RoHS compliant.



For complete Ambarella contact information, please visit www.ambarella.com.

7. PIN LIST AND MAPPING TABLE

This section provides a list of the 369 external pins according to their location on the H22S85 chip. Figure 7-1 below indicates the orientation of the pins by column (numbers) and row (letters).

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	
A	ddr_dq_30	ddr_dq_23	ddr_dq_21	ddr_calibr	ddr_vref_2	spclk_lvds_p	sd_lvds_p_4	sd_lvds_p_5	sd_lvds_p_6	sd_lvds_p_7	spclk_lvds_p_	sd_lvds_p_0	sd_lvds_p_1	sd_lvds_p_2	sd_lvds_p_3	usb_dp	xin	xo_rtc	pwc_wkup	pwc_pseq1	hdmi_avdd33	A
B	ddr_dq_28	ddr_dq_31	ddr_dm_2	ddr_dq_22	ddr_cs	spclk_lvds_n	sd_lvds_n_4	sd_lvds_n_5	sd_lvds_n_6	sd_lvds_n_7	spclk_lvds_n	sd_lvds_n_0	sd_lvds_n_1	sd_lvds_n_2	sd_lvds_n_3	usb_dm	xout	xi_rtc	pwc_pseq3	pwc_rstinb	hdmi_avdd18	B
C	ddr_dqs_3	ddr_dq_29	ddr_dqs_2	ddr_dq_20	ddr_cs_2	VSSi	dac_reset	dac_vrefin	dac_comp	VSSi	VSSi	VSSi	avss	avss	VSSi	VSSi	usb_rext	pwc_pseq2	ir_in	hdmi_ch2_m	hdmi_ch2_p	C
D	ddr_dqs_bar	ddr_dm_3	ddr_dqs_bar	ddr_dq_16	ddr_addr_5	dac_io	svsync	shsync	VSSi	VSSi	VSSi	avdd18	avdd	mipi_ana_avd	avdd18	dvdd	detect_vbus	pwc_avdd33	pwc_rstob	hdmi_ch1_m	hdmi_ch1_p	D
E	ddr_dq_26	dr_dq_25	ddr_dq_17	ddr_dq_18	ddr_addr_2	ddr_vddq_cke	adc_ch_1	adc_ch_2	adc_ch_3	VSSi	VSSi	VSSi	VSSi	VSSi	VSSi	avdd33	sdxc_vddo	pwc_avdd18	hpd	hdmi_ch0_m	hdmi_ch0_p	E
F	ddr_dq_24	ddr_dq_27	ddr_dq_19	ddr_addr_3	ddr_vddq												vddp	VSSi	cec	hdmi_clk_m	hdmi_clk_p	F
G	ddr_addr_13	ddr_addr_12	ddr_addr_4	ddr_addr_0	ddr_vddq												vddo	smio_36	smio_37	smio_39	hdmi_rext	G
H	ddr_ck_2_bar	ddr_ck_2	ddr_addr_11	ddr_we	ddr_vddq			VSSi	VDDi	VSSi	VDDi	VSSi	VDDi	VSSi			nand_vddo	smio_35	smio_34	smio_33	smio_32	H
J	ddr_cke_2	ddr_ba_1	ddr_addr_6	ddr_addr_8	ddr_vddq			VSSi	VDDi	VSSi	VDDi	VSSi	VDDi	VSSi			smio_20	smio_28	smio_29	smio_30	smio_31	J
K	ddr_ck_bar	ddr_ck	ddr_addr_14	ddr_addr_10	ddr_vddq			VSSi	VDDi	VSSi	VDDi	VSSi	VDDi	sd_vddo			smio_21	smio_27	smio_26	smio_23	smio_19	K
L	ddr_cke	ddr_addr_15	ddr_addr_1	ddr_odt	ddr_vddq			VSSi	VDDi	VSSi	VDDi	VSSi	VDDi	sd_vddo			smio_25	smio_24	smio_2	smio_18	smio_22	L
M	ddr_dq_14	ddr_dq_7	ddr_dq_5	ddr_ras	ddr_vddq			VSSi	VDDi	VSSi	VDDi	VSSi	VDDi	VSSi			smio_38	smio_3	smio_5	smio_4	wp	M
N	ddr_dq_12	ddr_dq_13	ddr_dqs_bar	ddr_cas	ddr_vddq			VSSi	VDDi	VSSi	VDDi	VSSi	VDDi	VSSi			smio_13	smio_14	smio_15	smio_16	smio_17	N
P	ddr_dqs_bar_	ddr_dq_15	ddr_dqs_0	ddr_dq_6	ddr_addr_7			vddp	VDDi	VSSi	vddo	vddo	vddo	VSSi			smio_12	smio_11	smio_10	smio_9	smio_7	P
R	ddr_dqs_1	ddr_dm_1	ddr_dm_0	ddr_dq_4	ddr_addr_9												ssi0en_0	smio_1	smio_0	smio_6	smio_8	R
T	ddr_dq_10	ddr_dq_11	ddr_dq_3	ddr_dq_2	ddr_ba_0												ssi0en_1	sc_d0	sc_c0	sc_b0	sc_a0	T
U	ddr_dq_8	ddr_dq_9	ddr_dq_1	ddr_dq_0	ddr_ba_2	clk_si	vd0_out_8	vd0_hsync	enet_mdc	enet_clk_rx	por_l	i2s_clk	jtag_tdi	idcdata	gpio_4	uart1ctsn	uart1rtsn	sc_d1	sc_c1	sc_b1	sc_a1	U
V	vd0_out_14	vd0_out_15	vd0_out_10	vd0_clk	ddr_reset	clk_si2	vd0_out_7	enet_mdio	enet_clk_tx	test_mode	i2s_si	jtag_tms	idc2clk	gpio_5	gpio_0	gpio_1	sc_d2	sc_d3	sc_c2	sc_b2	sc_a2	V
W	vd0_out_4	vd0_out_6	vd0_out_1	vd0_out_11	ddr_vref_1	vd0_out_0	vd0_hvld	enet_txd_0	enet_txen	enet_rxd_2	enet_rxd_3	i2s_so	jtag_clk	idc2data	gpio_6	gpio_2	uart1rx	timer1	sc_c3	sc_b3	sc_a3	W
Y	ssi2en_1	ssi2miso	vd0_out_5	vd_pwm	vd0_out_2	vd0_out_12	vd0_vsync	enet_txd_1	enet_gtx_clk	enet_rxd_1	enet_rxdv	i2s_ws	jtag_tdo	idc3clk	gpio_7	gpio_3	uart1tx	ssi0miso	fsource_0	vddwl_0	sc_e0	Y
AA	ssi2en_0	ssi2mosi	sensorrst	ssi2clk	vd0_out_3	vd0_out_13	vd0_out_9	enet_txd_2	enet_txd_3	enet_rxd_0	enet_ext_osc_c	clk_au	jtag_rstl	idc3data	idcclk	uart0tx	uart0rx	ssi0mosi	ssi0clk	timer2	timer0	AA
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	

Figure 7-1. Pin Map for the H22S85 Chip.

The table below lists all of the external pins on the H22S85 chip in alphabetic order by map location. Each entry provides the pin name as it appears on the ball map, the location of the pin on the map and on schematics, the functional group, and multiplexed functionality detail if applicable.

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
A1	**DDR_DQ_30**	DDR	SSTL						
A2	**DDR_DQ_23**	DDR	SSTL						
A3	**DDR_DQ_21**	DDR	SSTL						
A4	**DDR_CAL-IBR**	DDR	SSTL						

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
A5	**DDR_ VREF_2**	DDR	SSTL						
A6	**SPCLK_ LVDS_P_1**	Sensor	Sub_ LVDS / SLVS / LVC-MOS / MIPI						
A7	**SD_ LVDS_P_4**	Sensor	Sub_ LVDS / SLVS / LVC-MOS / MIPI						
A8	**SD_ LVDS_P_5**	Sensor	Sub_ LVDS / SLVS / LVC-MOS / MIPI						
A9	**SD_ LVDS_P_6**	Sensor	Sub_ LVDS / SLVS / LVC-MOS / MIPI						
A10	**SD_ LVDS_P_7**	Sensor	Sub_ LVDS / SLVS / LVC-MOS / MIPI						
A11	**SPCLK_ LVDS_P_0**	Sensor	Sub_ LVDS / SLVS / LVC-MOS / MIPI						
A12	**SD_ LVDS_P_0**	Sensor	Sub_ LVDS / SLVS / LVC-MOS / MIPI						
A13	**SD_ LVDS_P_1**	Sensor	Sub_ LVDS / SLVS / LVC-MOS / MIPI						

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
A14	**SD_ LVDS_P_2**	Sensor	Sub_ LVDS / SLVS / LVC-MOS / MIPI						
A15	**SD_ LVDS_P_3**	Sensor	Sub_ LVDS / SLVS / LVC-MOS / MIPI						
A16	**USB_DP**	USB	Analog						
A17	**XIN**	Global	XOSC						
A18	**XO_RTC**	RTC	Analog						
A19	**PWC_WKUP**	PWC	Analog						
A20	**PWC_PSEQ1**	PWC	Analog						
A21	**HDMI_ AVDD33_ ESD**	HDMI	Analog Supply						
B1	**DDR_DQ_28**	DDR	SSTL						
B2	**DDR_DQ_31**	DDR	SSTL						
B3	**DDR_DM_2**	DDR	SSTL						
B4	**DDR_DQ_22**	DDR	SSTL						
B5	**DDR_CS**	DDR	SSTL						
B6	**SPCLK_ LVDS_N_1**	Sensor	Sub_ LVDS / SLVS / LVC-MOS / MIPI						
B7	**SD_ LVDS_N_4**	Sensor	Sub_ LVDS / SLVS / LVC-MOS / MIPI						
B8	**SD_ LVDS_N_5**	Sensor	Sub_ LVDS / SLVS / LVC-MOS / MIPI						
B9	**SD_ LVDS_N_6**	Sensor	Sub_ LVDS / SLVS / LVC-MOS / MIPI						

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
B10	**SD_ LVDS_N_7**	Sensor	Sub_ LVDS / SLVS / LVC-MOS / MIPI						
B11	**SPCLK_ LVDS_N_0**	Sensor	Sub_ LVDS / SLVS / LVC-MOS / MIPI						
B12	**SD_ LVDS_N_0**	Sensor	Sub_ LVDS / SLVS / LVC-MOS / MIPI						
B13	**SD_ LVDS_N_1**	Sensor	Sub_ LVDS / SLVS / LVC-MOS / MIPI						
B14	**SD_ LVDS_N_2**	Sensor	Sub_ LVDS / SLVS / LVC-MOS / MIPI						
B15	**SD_ LVDS_N_3**	Sensor	Sub_ LVDS / SLVS / LVC-MOS / MIPI						
B16	**USB_DM**	USB	Analog						
B17	**XOUT**	Global	XOSC						
B18	**XI_RTC**	RTC	Analog						
B19	**PWC_PSEQ3**	PWC	Analog						
B20	**PWC_RST-INB**	PWC	Analog						
B21	**HDMI_ AVDD18_ ESD**	HDMI	Analog Supply						
C1	**DDR_DQS_3**	DDR	SSTL						
C2	**DDR_DQ_29**	DDR	SSTL						
C3	**DDR_DQS_2**	DDR	SSTL						
C4	**DDR_DQ_20**	DDR	SSTL						
C5	**DDR_CS_2**	DDR	SSTL						

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
C6	**VSSI**	Power	Ground						
C7	**DAC_RSET**	DAC	Analog						
C8	**DAC_VREFIN**	DAC	Analog						
C9	**DAC_COMP**	DAC	Analog						
C10	**VSSI**	Power	Ground						
C11	**VSSI**	Power	Ground						
C12	**VSSI**	Power	Ground						
C13	**AVSS**	Power	Ground						
C14	**AVSS**	Power	Ground						
C15	**VSSI**	Power	Ground						
C16	**VSSI**	Power	Ground						
C17	**USB_REXT**	USB	Analog						
C18	**PWC_PSEQ2**	PWC	Analog						
C19	**IR_IN**	IR	CMOS	ir_in					34
C20	**HDMI_ CH2_M**	HDMI	Analog						
C21	**HDMI_CH2_P**	HDMI	Analog						
D1	**DDR_DQS_ BAR_3**	DDR	SSTL						
D2	**DDR_DM_3**	DDR	SSTL						
D3	**DDR_DQS_ BAR_2**	DDR	SSTL						
D4	**DDR_DQ_16**	DDR	SSTL						
D5	**DDR_ ADDR_5**	DDR	SSTL						
D6	**DAC_IO**	DAC	Analog						
D7	**SVSYNC**	Sensor	CMOS	vin_svsync	idsp_pip_ iopad_mas- ter_hsync				115
D8	**SHSYNC**	Sensor	CMOS	vin_shsync	idsp_pip_ iopad_mas- ter_vsync				116
D9	**VSSI**	Power	Ground						
D10	**VSSI**	Power	Ground						
D11	**VSSI**	Power	Ground						
D12	**AVDD18**	Power	Analog Supply						
D13	**AVDD**	Power	Analog Supply						
D14	**MIPI_ANA_ AVDD18_IO**	Power	Analog Supply						
D15	**AVDD18**	Power	Analog Supply						
D16	**DVDD**	Power	Digital Supply						
D17	**DETECT_ VBUS**	USB	CMOS						
D18	**PWC_ AVDD33**	PWC	Analog						

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
D19	**PWC_RSTOB**	PWC	Analog						
D20	**HDMI_ CH1_M**	HDMI	Analog						
D21	**HDMI_CH1_P**	HDMI	Analog						
E1	**DDR_DQ_26**	DDR	SSTL						
E2	**DDR_DQ_25**	DDR	SSTL						
E3	**DDR_DQ_17**	DDR	SSTL						
E4	**DDR_DQ_18**	DDR	SSTL						
E5	**DDR_ ADDR_2**	DDR	SSTL						
E6	**DDR_VDDQ_ CKE**	Power	DDR HOST Supply						
E7	**ADC_CH_1**	ADC	Analog						
E8	**ADC_CH_2**	ADC	Analog						
E9	**ADC_CH_3**	ADC	Analog						
E10	**VSSI**	Power	Ground						
E11	**VSSI**	Power	Ground						
E12	**VSSI**	Power	Ground						
E13	**VSSI**	Power	Ground						
E14	**VSSI**	Power	Ground						
E15	**VSSI**	Power	Ground						
E16	**AVDD33**	Power	Analog Supply						
E17	**SDXC_VDDO**	Power	IO Power						
E18	**PWC_ AVDD18**	PWC	Analog Supply						
E19	**HPD**	GPIO	CMOS	hdmitx_hpd					113
E20	**HDMI_ CH0_M**	HDMI	Analog						
E21	**HDMI_CH0_P**	HDMI	Analog						
F1	**DDR_DQ_24**	DDR	SSTL						
F2	**DDR_DQ_27**	DDR	SSTL						
F3	**DDR_DQ_19**	DDR	SSTL						
F4	**DDR_ ADDR_3**	DDR	SSTL						
F5	**DDR_VDDQ**	Power	DDR HOST Supply						
F17	**VDDP**	Power	Pre-driver Supply						
F18	**VSSI**	Power	Ground						
F19	**CEC**	HDMI	CMOS	hdmitx_cec					114
F20	**HDMI_ CLK_M**	HDMI	Analog						
F21	**HDMI_CLK_P**	HDMI	Analog						

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
G1	DDR_ ADDR_13	DDR	SSTL						
G2	DDR_ ADDR_12	DDR	SSTL						
G3	DDR_ ADDR_4	DDR	SSTL						
G4	DDR_ ADDR_0	DDR	SSTL						
G5	DDR_VDDQ	Power	DDR HOST Supply						
G17	VDDO	Power	IO Power						
G18	SMIO_36	SMIO	CMOS		sdxc_d[6]				109
G19	SMIO_37	SMIO	CMOS		sdxc_d[7]				110
G20	SMIO_39	SMIO	CMOS		sdxc_reset				112
G21	HDMI_REXT	HDMI	Analog						
H1	DDR_CK_2_ BAR	DDR	SSTL						
H2	DDR_CK_2	DDR	SSTL						
H3	DDR_ ADDR_11	DDR	SSTL						
H4	DDR_WE	DDR	SSTL						
H5	DDR_VDDQ	Power	DDR HOST Supply						
H8	VSSI	Power	Ground						
H9	VDDI	Power	Digital Supply						
H10	VSSI	Power	Ground						
H11	VDDI	Power	Digital Supply						
H12	VSSI	Power	Ground						
H13	VDDI	Power	Digital Supply						
H14	VSSI	Power	Ground						
H17	NAND_VDDO								
H18	SMIO_35	SMIO	CMOS		sdxc_d[5]				108
H19	SMIO_34	SMIO	CMOS		sdxc_d[4]				107
H20	SMIO_33	SMIO	CMOS		sdxc_wp				106
H21	SMIO_32	SMIO	CMOS		sdxc_cd				105
J1	DDR_CKE_2	DDR	SSTL						
J2	DDR_BA_1	DDR	SSTL						
J3	DDR_ ADDR_6	DDR	SSTL						
J4	DDR_ ADDR_8	DDR	SSTL						

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
J5	**DDR_VDDQ**	Power	DDR HOST Supply						
J8	**VSSI**	Power	Ground						
J9	**VDDI**	Power	Digital Supply						
J10	**VSSI**	Power	Ground						
J11	**VDDI**	Power	Digital Supply						
J12	**VSSI**	Power	Ground						
J13	**VDDI**	Power	Digital Supply						
J14	**VSSI**	Power	Ground						
J17	**SMIO_20**	SMIO	CMOS		sd_d[2]				93
J18	**SMIO_28**	SMIO	CMOS		sdxc_d[0]		sc_d0	ssis_sclk	101
J19	**SMIO_29**	SMIO	CMOS		sdxc_d[1]		sc_d1	ssis_rxd	102
J20	**SMIO_30**	SMIO	CMOS		sdxc_d[2]		sc_d2	ssis_txd	103
J21	**SMIO_31**	SMIO	CMOS		sdxc_d[3]		sc_d3	ssis_en	104
K1	**DDR_CK_BAR**	DDR	SSTL						
K2	**DDR_CK**	DDR	SSTL						
K3	**DDR_ADDR_14**	DDR	SSTL						
K4	**DDR_ADDR_10**	DDR	SSTL						
K5	**DDR_VDDQ**	Power	DDR HOST Supply						
K8	**VSSI**	Power	Ground						
K9	**VDDI**	Power	Digital Supply						
K10	**VSSI**	Power	Ground						
K11	**VDDI**	Power	Digital Supply						
K12	**VSSI**	Power	Ground						
K13	**VDDI**	Power	Digital Supply						
K14	**SD_VDDO**	Power	IO Power						
K17	**SMIO_21**	SMIO	CMOS		sd_d[3]				94
K18	**SMIO_27**	SMIO	CMOS		sdxc_cmd				100
K19	**SMIO_26**	SMIO	CMOS		sdxc_clk				99
K20	**SMIO_23**	SMIO	CMOS		sd_d[5]		sc_c1	ssis_rxd	96
K21	**SMIO_19**	SMIO	CMOS		sd_d[1]				92
L1	**DDR_CKE**	DDR	SSTL						
L2	**DDR_ADDR_15**	DDR	SSTL						
L3	**DDR_ADDR_1**	DDR	SSTL						

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
L4	**DDR_ODT**	DDR	SSTL						
L5	**DDR_VDDQ**	Power	DDR HOST Supply						
L8	**VSSI**	Power	Ground						
L9	**VDDI**	Power	Digital Supply						
L10	**VSSI**	Power	Ground						
L11	**VDDI**	Power	Digital Supply						
L12	**VSSI**	Power	Ground						
L13	**VDDI**	Power	Digital Supply						
L14	**SD_VDDO**	Power	IO Power						
L17	**SMIO_25**	SMIO	CMOS		sd_d[7]		sc_c3	ssis_en	98
L18	**SMIO_24**	SMIO	CMOS		sd_d[6]		sc_c2	ssis_txd	97
L19	**SMIO_2**	SMIO	CMOS		sd_clk				75
L20	**SMIO_18**	SMIO	CMOS		sd_d[0]				91
L21	**SMIO_22**	SMIO	CMOS		sd_d[4]		sc_c0	ssis_sclk	95
M1	**DDR_DQ_14**	DDR	SSTL						
M2	**DDR_DQ_7**	DDR	SSTL						
M3	**DDR_DQ_5**	DDR	SSTL						
M4	**DDR_RAS**	DDR	SSTL						
M5	**DDR_VDDQ**	Power	DDR HOST Supply						
M8	**VSSI**	Power	Ground						
M9	**VDDI**	Power	Digital Supply						
M10	**VSSI**	Power	Ground						
M11	**VDDI**	Power	Digital Supply						
M12	**VSSI**	Power	Ground						
M13	**VDDI**	Power	Digital Supply						
M14	**VSSI**	Power	Ground						
M17	**SMIO_38**	SMIO	CMOS		sd_reset				111
M18	**SMIO_3**	SMIO	CMOS		sd_cmd				76
M19	**SMIO_5**	SMIO	CMOS		sd_wp				78
M20	**SMIO_4**	SMIO	CMOS		sd_cd				77
M21	**WP**	GPIO	CMOS		nand_wp				72
N1	**DDR_DQ_12**	DDR	SSTL						
N2	**DDR_DQ_13**	DDR	SSTL						
N3	**DDR_DQS_BAR_0**	DDR	SSTL						
N4	**DDR_CAS**	DDR	SSTL						

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
N5	**DDR_VDDQ**	Power	DDR HOST Supply						
N8	**VSSI**	Power	Ground						
N9	**VDDI**	Power	Digital Supply						
N10	**VSSI**	Power	Ground						
N11	**VDDI**	Power	Digital Supply						
N12	**VSSI**	Power	Ground						
N13	**VDDI**	Power	Digital Supply						
N14	**VSSI**	Power	Ground						
N17	**SMIO_13**	SMIO	CMOS		nand_d[4]	norspi_ dq[0]			86
N18	**SMIO_14**	SMIO	CMOS		nand_d[5]	norspi_ dq[1]			87
N19	**SMIO_15**	SMIO	CMOS		nand_d[6]	norspi_ dq[2]			88
N20	**SMIO_16**	SMIO	CMOS		nand_d[7]	norspi_ dq[3]			89
N21	**SMIO_17**	SMIO	CMOS		nand_cle				90
P1	**DDR_DQS_ BAR_1**	DDR	SSTL						
P2	**DDR_DQ_15**	DDR	SSTL						
P3	**DDR_DQS_0**	DDR	SSTL						
P4	**DDR_DQ_6**	DDR	SSTL						
P5	**DDR_ ADDR_7**	DDR	SSTL						
P8	**VDDP**	Power	Pre-driver Supply						
P9	**VDDI**	Power	Digital Supply						
P10	**VSSI**	Power	Ground						
P11	**VDDO**	Power	IO Power						
P12	**VDDO**	Power	IO Power						
P13	**VDDO**	Power	IO Power						
P14	**VSSI**	Power	Ground						
P17	**SMIO_12**	SMIO	CMOS		nand_d[3]	norspi_ en[3]			85
P18	**SMIO_11**	SMIO	CMOS		nand_d[2]	norspi_ en[2]			84
P19	**SMIO_10**	SMIO	CMOS		nand_d[1]	norspi_ en[1]			83

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
P20	**SMIO_9**	SMIO	CMOS		nand_d[0]	norspi_ en[0]			82
P21	**SMIO_7**	SMIO	CMOS		nand_we	norspi_ dq[6]			80
R1	**DDR_DQS_1**	DDR	SSTL						
R2	**DDR_DM_1**	DDR	SSTL						
R3	**DDR_DM_0**	DDR	SSTL						
R4	**DDR_DQ_4**	DDR	SSTL						
R5	**DDR_ ADDR_9**	DDR	SSTL						
R17	**SSI0EN0**	GPIO	CMOS	ssi0_en0	norspi_ en[0]	uart2_ahb_ rts_n	ssis_en		38
R18	**SMIO_1**	SMIO	CMOS		nand_rb	norspi_ dq[4]			74
R19	**SMIO_0**	SMIO	CMOS		nand_ce	norspi_clk			73
R20	**SMIO_6**	SMIO	CMOS		nand_re	norspi_ dq[5]			79
R21	**SMIO_8**	SMIO	CMOS		nand_ale	norspi_ dq[7]			81
T1	**DDR_DQ_10**	DDR	SSTL						
T2	**DDR_DQ_11**	DDR	SSTL						
T3	**DDR_DQ_3**	DDR	SSTL						
T4	**DDR_DQ_2**	DDR	SSTL						
T5	**DDR_BA_0**	DDR	SSTL						
T17	**SSI0EN1**	GPIO	CMOS	ssi0_en1	norspi_ en[1]				39
T18	**SC_D0**	GPIO	CMOS	sc_d0	uart2_ahb_ rx	ssis_sclk		pwm_0	20
T19	**SC_C0**	GPIO	CMOS	sc_c0	uart2_ahb_ rx	ssis_sclk			16
T20	**SC_B0**	GPIO	CMOS	sc_b0	ssi1_en1	norspi_ dq[3]			12
T21	**SC_A0**	GPIO	CMOS	sc_a0	ssi1_sclk	norspi_clk	pwm_0		8
U1	**DDR_DQ_8**	DDR	SSTL						
U2	**DDR_DQ_9**	DDR	SSTL						
U3	**DDR_DQ_1**	DDR	SSTL						
U4	**DDR_DQ_0**	DDR	SSTL						
U5	**DDR_BA_2**	DDR	SSTL						
U6	**CLK_SI**	Sensor	CMOS						
U7	**VD0_OUT_8**	VOUT	CMOS	vd0_out[8]					126
U8	**VD0_HSYNC**	VOUT	CMOS	VD0_ HSYNC					136
U9	**ENET_MDC**	ENET	CMOS	enet_mdc		enet_mdc			66
U10	**ENET_CLK_ RX**	ENET	CMOS	enet_ref_clk		enet_clk_ rx			69
U11	**POR_I**								
U12	**I2S_CLK**	I2S	CMOS	i2s_clk	dmic_clk				51
U13	**JTAG_TDI**	JTAG	CMOS						

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
U14	**IDCDATA**	IDC	CMOS	idc0data					29
U15	**GPIO_4**	GPIO	CMOS	ehci_prt_pwr_1	uart2_ahb_rts_n	ssis_en	sc_c3		4
U16	**UART1CTSN**	GPIO	CMOS	uart1_ahb_cts_n					49
U17	**UART1RTSN**	GPIO	CMOS	uart1_ahb_rts_n					50
U18	**SC_D1**	GPIO	CMOS	sc_d1	uart2_ahb_tx	ssis_rxd		pwm_1	21
U19	**SC_C1**	GPIO	CMOS	sc_c1	uart2_ahb_tx	ssis_rxd			17
U20	**SC_B1**	GPIO	CMOS	sc_b1	ssi1_en2	norspi_en[0]	norspi_dq[2]		13
U21	**SC_A1**	GPIO	CMOS	sc_a1	ssi1_txd	norspi_dq[0]	pwm_1		9
V1	**VD0_OUT_14**	VOUT	CMOS	vd0_out[14]					132
V2	**VD0_OUT_15**	VOUT	CMOS	vd0_out[15]					133
V3	**VD0_OUT_10**	VOUT	CMOS	vd0_out[10]					128
V4	**VD0_CLK**	VOUT	CMOS	vd0_clk					134
V5	**DDR_RESET**	DDR	SSTL						
V6	**CLK_SI2**	Sensor	CMOS						
V7	**VD0_OUT_7**	VOUT	CMOS	vd0_out[7]					125
V8	**ENET_MDIO**	ENET	CMOS	enet_mdio		enet_mdio			67
V9	**ENET_CLK_TX**	ENET	CMOS	enet_2nd_ref_clk		enet_clk_tx			68
V10	**TEST_MODE**	GLOB-AL	CMOS						
V11	**I2S_SI**	GPIO	CMOS	i2s_si	dmic_dat				52
V12	**JTAG_TMS**	JTAG	CMOS						
V13	**IDC2CLK**	IDC	CMOS	idc1clk		norspi_dq[2]	norspi_en[2]		30
V14	**GPIO_5**	GPIO	CMOS	pwm_1	idsp_pip_iopad_mas-ter_hsync	vin_strig0	sc_d0	uart2_ahb_cts_n	5
V15	**GPIO_0**	GPIO	CMOS	sd_hs_sel					0
V16	**GPIO_1**	GPIO	CMOS	ehci_app_prt_ovcurr0	uart2_ahb_rx	ssis_sclk	sc_c0		1
V17	**SC_D2**	GPIO	CMOS	sc_d2	uart2_ahb_cts_n	ssis_txd		pwm_2	22
V18	**SC_D3**	GPIO	CMOS	sc_d3	uart2_ahb_rts_n	ssis_en		pwm_3	23
V19	**SC_C2**	GPIO	CMOS	sc_c2	uart2_ahb_cts_n	ssis_txd			18
V20	**SC_B2**	GPIO	CMOS	sc_b2	ssi1_en3	norspi_en[1]	norspi_dq[3]		14
V21	**SC_A2**	GPIO	CMOS	sc_a2	ssi1_rxd	norspi_dq[1]	pwm_2		10
W1	**VD0_OUT_4**	VOUT	CMOS	vd0_out[4]					122

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
W2	**VD0_OUT_6**	VOUT	CMOS	vd0_out[6]					124
W3	**VD0_OUT_1**	VOUT	CMOS	vd0_out[1]					119
W4	**VD0_OUT_11**	VOUT	CMOS	vd0_out[11]					129
W5	**DDR_ VREF_1**	DDR	SSTL						
W6	**VD0_OUT_0**	VOUT	CMOS	vd0_out[0]					118
W7	**VD0_HVLD**	VOUT	CMOS	vd0_hvld					137
W8	**ENET_TXD_0**	ENET	CMOS	enet_txd_0	sc_a1	enet_txd_0	ssi1_en0	norspi_ en[1]	57
W9	**ENET_TXEN**	ENET	CMOS	enet_txen	sc_a0	enet_txen	ssi1_txd	norspi_ en[0]	56
W10	**ENET_ RXD_2**	ENET	CMOS		sc_b3	enet_rxd_2		norspi_ dq[2]	63
W11	**ENET_ RXD_3**	ENET	CMOS			enet_rxd_3		norspi_ dq[3]	64
W12	**I2S_SO**	I2C	CMOS	i2s_so					53
W13	**JTAG_CLK**	JTAG	CMOS						
W14	**IDC2DATA**	IDC	CMOS	idc1data		norspi_ dq[3]	norspi_ en[3]		31
W15	**GPIO_6**	GPIO	CMOS	pwm_2	idsp_pip_ iopad_mas- ter_vsync	vin_strig1	sc_d1	uart2_ ahb_rts_n	6
W16	**GPIO_2**	GPIO	CMOS	ehci_app_ prt_ovcurr1	uart2_ahb_ tx	ssis_rxd	sc_c1		2
W17	**UART1RX**	GPIO	CMOS	uart1_ahb_rx					47
W18	**TIMER1**	GPIO	CMOS	tm12_clk	ssi2_en3	idsp_ pip_io- pad_mas- ter_hysnc			26
W19	**SC_C3**	GPIO	CMOS	sc_c3	uart2_ahb_ rts_n	ssis_en			19
W20	**SC_B3**	GPIO	CMOS	sc_b3	pwm_3	norspi_ en[2]			15
W21	**SC_A3**	GPIO	CMOS	sc_a3	ssi1_en0	norspi_ dq[2]	pwm_3		11
Y1	**SSI2EN1**	GPIO	CMOS	ssi2_en1					44
Y2	**SSI2MISO**	GPIO	CMOS	ssi2_rxd					42
Y3	**VD0_OUT_5**	VOUT	CMOS	vd0_out[5]					123
Y4	**VD_PWM**	VOUT	CMOS	pwm_0					138
Y5	**VD0_OUT_2**	VOUT	CMOS	vd0_out[2]					120
Y6	**VD0_OUT_12**	VOUT	CMOS	vdo_out[12]					130
Y7	**VD0_VSYNC**	VOUT	CMOS	vd0_vsync					135
Y8	**ENET_TXD_1**	ENET	CMOS	enet_txd_1	sc_a2	enet_txd_1	ssi1_en1	norspi_ en[2]	58
Y9	**ENET_GTX_ CLK**	ENET	CMOS	enet_gtx_clk		enet_gtx_ clk	ssi1_sclk	norspi_clk	70
Y10	**ENET_ RXD_1**	ENET	CMOS	enet_rxd_1	sc_b2	enet_rxd_1		norspi_ dq[1]	62

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
Y11	**ENET_RXDV**	ENET	CMOS	enet_rxdv		enet_rxdv			65
Y12	**I2S_WS**	I2C	CMOS	i2s_ws					54
Y13	**JTAG_TDO**	JTAG	CMOS						
Y14	**IDC3CLK**	IDC	CMOS	idc2clk	vin_strig0				32
Y15	**GPIO_7**	GPIO	CMOS	sdxc_hs_sel					7
Y16	**GPIO_3**	GPIO	CMOS	ehci_prt_pwr_0	uart2_ahb_cts_n	ssis_txd	sc_c2		3
Y17	**UART1TX**	GPIO	CMOS	uart1_ahb_tx					48
Y18	**SSI0MISO**	GPIO	CMOS	ssi0_rxd	norspi_dq[1]	uart2_ahb_cts_n	ssis_txd		
Y19	**FSOURCE_0**	GLOB-AL	Supply / GND						
Y20	**VDDWL_0**	POW-ER	IO POW-ER						
Y21	**SC_E0**	GPIO	CMOS	sc_e0	ssi0_en2	norspi_en[3]		pwm_1	24
AA1	**SSI2EN0**	GPIO	CMOS	ssi2_en0					43
AA2	**SSI2MOSI**	GPIO	CMOS	ssi2_txd	idc3data				41
AA3	**SENSOR_RST**	GPIO	CMOS						117
AA4	**SSI2CLK**	GPIO	CMOS	ssi2_sclk	idc3clk				40
AA5	**VD0_OUT_3**	VOUT	CMOS	vd0_out[3]					121
AA6	**VD0_OUT_13**	VOUT	CMOS	vd0_out[13]					131
AA7	**VD0_OUT_9**	VOUT	CMOS	vd0_out[9]					127
AA8	**ENET_TXD_2**	ENET	CMOS		sc_a3	enet_txd_2	ssi1_en2		59
AA9	**ENET_TXD_3**	ENET	CMOS		sc_b0	enet_txd_3	ssi1_en3		60
AA10	**ENET_RXD_0**	ENET	CMOS	enet_rxd_0	sc_b1	enet_rxd_0	ssi1_rxd	norspi_dq[0]	61
AA11	**ENET_EXT_OSC_CLK**	ENET	CMOS			enet_ext_osc_clk			71
AA12	**CLK_AU**	GPIO	CMOS	clk_au	clk_au3				55
AA13	**JTAG_RST_I**	JTAG	CMOS						
AA14	**IDC3DATA**	IDC	CMOS	idc2data	vin_strig1				
AA15	**IDCCLK**	IDC	CMOS	idc0clk					28
AA16	**UART0TX**	GPIO	CMOS	uart0tx	uart2_ahb_tx				46
AA17	**UART0RX**	GPIO	CMOS	uart0rx	uart2_ahb_rx				45
AA18	**SSI0MOSI**	GPIO	CMOS	ssi0_txd	norspi_dq[0]	uart2_ahb_tx	ssis_rxd		36
AA19	**SSI0CLK**	GPIO	CMOS	ssi0_sclk	norspi_clk	uart2_ahb_rx	ssis_sclk		35
AA20	**TIMER2**	GPIO	CMOS	tm13_clk	ssi0_en3	IDSP_PIP_IOPAD_MASTER_VSYNC			27

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
AA21	TIMER0	GPIO	CMOS	tm11_clk	ssi2_en2				25

Table 7-1. Pin List and Mapping Table for the H22S85 Chip.

8. IMPORTANT NOTICE

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9. TYPOGRAPHICAL CONVENTIONS

This document provides technical detail using a set of consistent typographical conventions to help the user differentiate key concepts at a glance. Conventions include:

Example	Description
AmbaGuiGen, **DirectUSB** **Save, File > Save** **Power, Reset**, **Home**	Software names GUI commands and command sequences Computer / Hardware buttons
Flash_IO_control **da**, **status**, **enable**	Register names and register fields. For example, **Flash_IO_control** is the register for global control of Flash I/O, and bit 17 (**da)** is used for DMA acknowledgement.
GPIO81, **CLK_AU**	Hardware external pins
VIL, VIH, VOL, VOH	Hardware pin parameters
INT_O, RXDATA_I	Hardware pin signals
amb_performance_t **amb_operating_mode_t** **amb_set_operating_mode()**	API details (e.g., functions, structures, and type definitions)
`/usr/local/bin` `success = amb_set_operating_mode (amb_xx_base_address, &operating_mode)`	User entries into software dialogues and GUI windows File names and paths Command line scripting and Code

Table 9-1. Typographical Conventions for Technical Documents.

Additional Ambarella typographical conventions include:

- Acronyms are given in UPPER CASE using the default font (e.g., AHB, ARM11 and DDRIO).
- Names of Ambarella documents and publicly available standards, specifications, and databooks appear in *italic* type.

10. REVISION HISTORY

Our goal is to provide our customers with the highest-quality documentation possible, and to continuously improve our publications to ensure that your experience with Ambarella's products is a positive one. If you have any questions or comments regarding this document, please contact the Technical Writing team at docs@ambarella.com. Your feedback is welcomed and appreciated.

NOTE: Page/chapter numbers for previous drafts may differ from those in the current version.

Version	Date	Comments
0.1	14 March, 2017	Initial draft
0.2	20 June, 2017	Updated Table 2-6: SSI / SPI Master with Device Enable Detail Fixed typos and updated ADC to three channels in Chapter 1 and 2 Updated VDD spec to 0.88 V typical value Updated secondary stream to 720p30 when main stream is 4Kp60

Table 10-1. Revision History.