A12 EVK Dragonfly V11A

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Title	A12 EVK Dragonfly Option-A	
	Cover Sheet	
Size B	Document Number AB120-101-V11A-150323	Rev 1.1A
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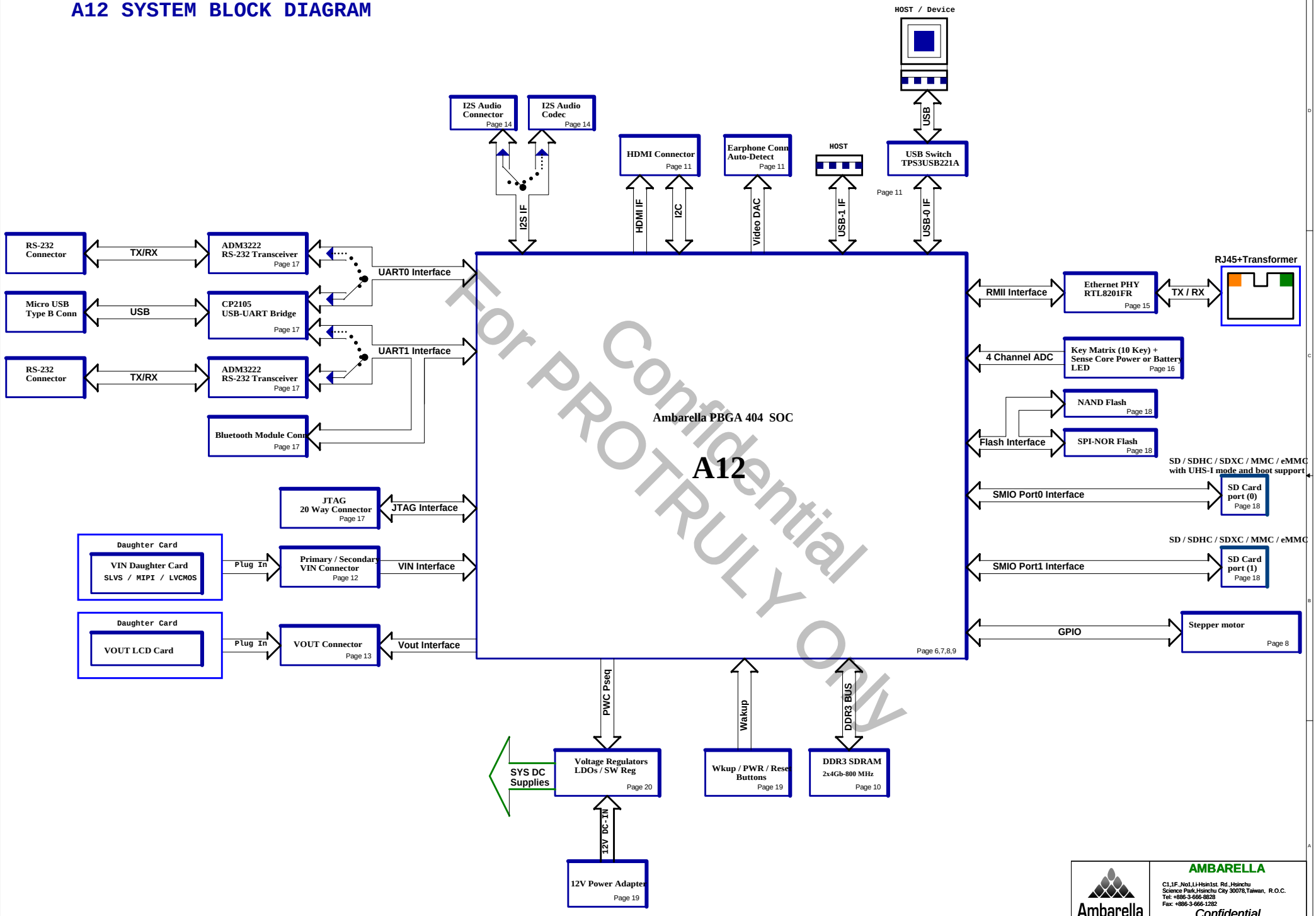
A12 SYSTEM BLOCK DIAGRAM



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	System Block Diagram
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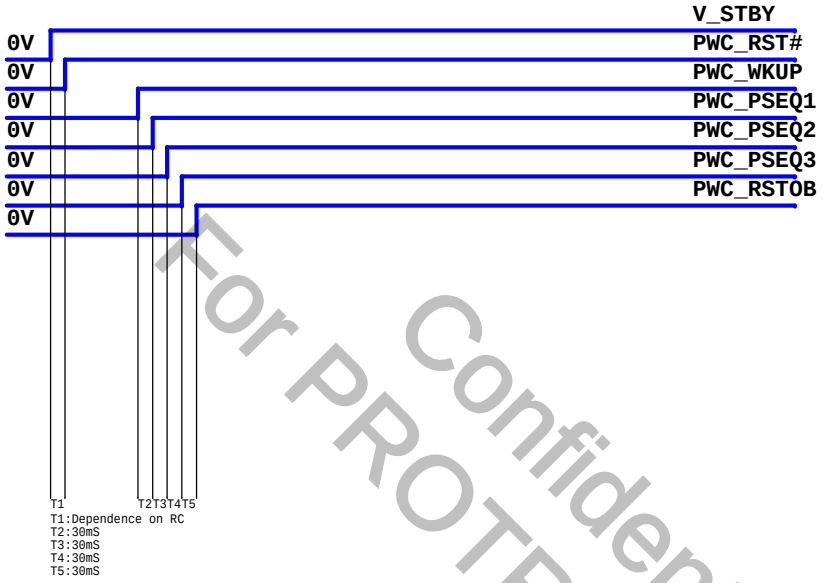
Power On Sequence

SOC_VDD/SOC_VDDA --> SOC_VDDA18/SOC_VDRAM --> DRAM_VDRAM --> SOC_VCC/SOC_VCCA/V_SD



Power-off sequence is in reverse order of power-on sequence

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	PM_Diagram	
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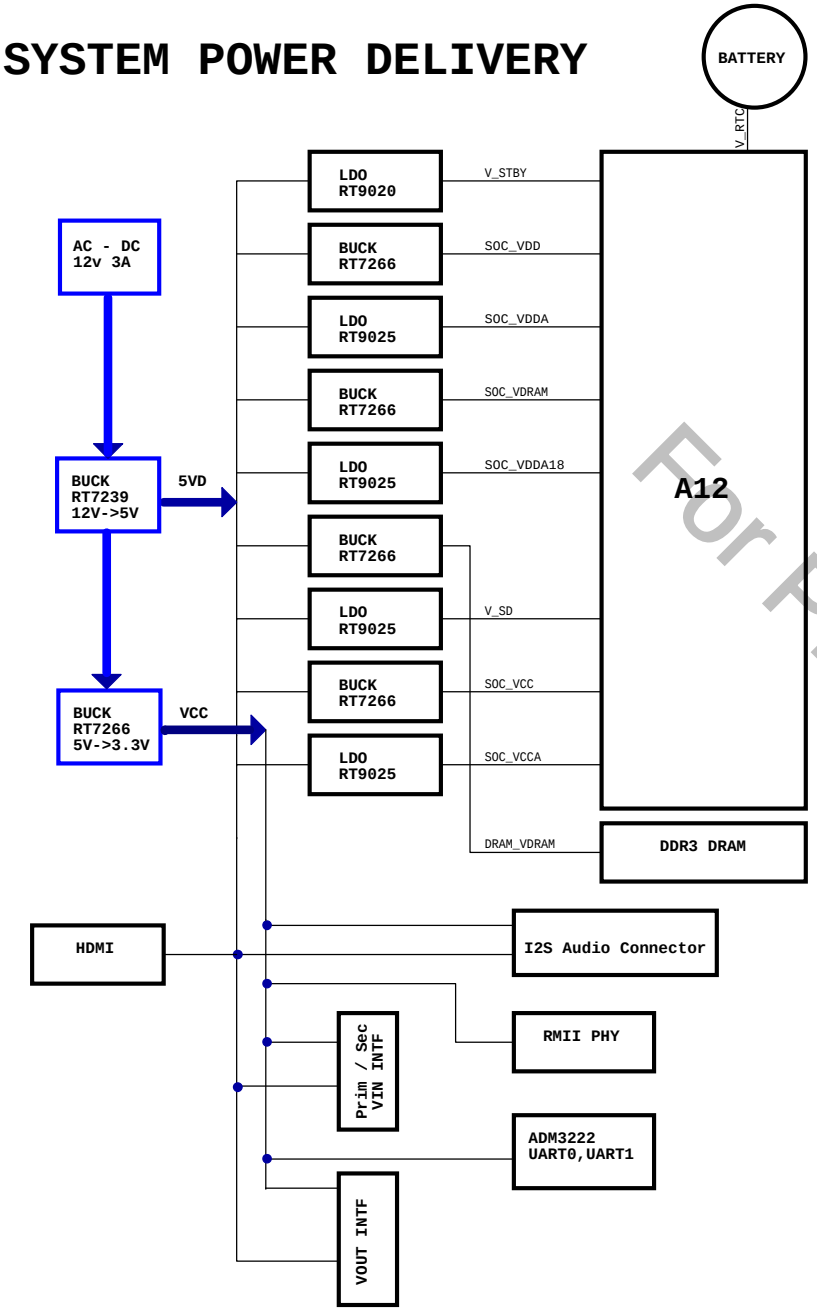
SYSTEM POWER DELIVERY



POWER MAPPING TABLE

3VSB=3.125V
VCC12=12V
SOC_VDRAM=1.5V
DRAM_VDRAM=1.5V
SOC_VDD=1.0V
SOC_VDDA=1.0V
SOC_VCC=3.0V
SOC_VCCA=3.0V
SOC_VDDA18=1.8V
V_SD=3.3/1.8V
V_SDIO=3.3/1.8V
VCC=3.0V
VCC5=5V
HDMI_VCC5=5V

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	Power Tree	
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A12 GPIO Alternate Function Table

PIN NANE	Function
GPIO0	SD_HS_SEL
GPIO1	EHCI_APP_PRT_OVCURR0, UART_AHB_RX, SSIS_SCLK, SC_C0
GPIO2	EHCI_APP_PRT_OVCURR1, UART_AHB_TX, SSIS_RXD, SC_C1
GPIO3	EHCI_PRT_PWR_0, UART_AHB_CTS_N, SSIS_TXD, SC_C2
GPIO4	EHCI_PRT_PWR_1, UART_AHB_RTS_N, SSIS_EN, SC_C3
GPIO5	PWM_1, IDSP_PIP_IOPAD_MASTER_HSYNC, VIN_STRIG0, SC_D0, UART_AHB_CTS_N
GPIO6	PWM_2, IDSP_PIP_IOPAD_MASTER_VSYNC, VIN_STRIG1, SC_D1, UART_AHB_RTS_N
GPIO7	SC_A0, SSI1_SCLK, NORSPI_CLK, PWM_0, SDXC_CMD
GPIO8	SC_A1, SSI1_TXD, NORSPI_DQ[0], PWM_1, SDXC_CD
GPIO9	SC_A2, SSI1_RXD, NORSPI_DQ[1], PWM_2, SDXC_WP
GPIO10	SC_A3, SSI1_EN0, NORSPI_DQ[2], PWM_3, SDXC_D[0]
GPIO11	SC_B0, SSI1_EN1, NORSPI_DQ[3], SDXC_D[1]
GPIO12	SC_B1, SSI1_EN2, NORSPI_EN[0], NORSPI_DQ[2], SDXC_D[2]
GPIO13	SC_B2, SSI1_EN3, NORSPI_EN[1], NORSPI_DQ[3], SDXC_D[3]
GPIO14	SC_B3, PWM_3, NORSPI_EN[2], SDXC_D[4]
GPIO15	SC_C0, UART_AHB_RX, SSIS_SCLK, SDXC_D[5]
GPIO16	SC_C1, UART_AHB_TX, SSIS_RXD, ENET_CRS, SDXC_D[6]
GPIO17	SC_C2, UART_AHB_CTS_N, SSIS_TXD, ENET_TX_RXD_2, SDXC_D[7]
GPIO18	SC_C3, UART_AHB_RTS_N, SSIS_EN, ENET_CRS_RXD_3, SDXC_CLK
GPIO19	SC_D0, UART_AHB_RX, SSIS_SCLK, ENET_COL, PWM_0
GPIO20	SC_D1, UART_AHB_TX, SSIS_RXD, ENET_TX_CLK, PWM_1
GPIO21	SC_D2, UART_AHB_CTS_N, SSIS_TXD, ENET_TX_ER, PWM_2
GPIO22	SC_D3, UART_AHB_RTS_N, SSIS_EN, ENET_TXD_2, PWM_3
GPIO23	SC_E0, SSI0_EN2, NORSPI_EN[3], ENET_TXD_3, PWM_1
GPIO24	TM11_CLK, ENET_2ND_REF_CLK
GPIO25	TM12_CLK, IDSP_PIP_IOPAD_MASTER_HSYNC, ENET_MDC
GPIO26	TM13_CLK, SS0_EN3, IDSP_PIP_IOPAD_MASTER_VSYNC, ENET_MDIO
GPIO27	IDC0CLK
GPIO28	IDC0DATA
GPIO29	IDC1_CLK, NORSPI_DQ[2], NORSPI_EN[2]
GPIO30	IDC1_DATA, NORSPI_DQ[3], NORSPI_EN[3]
GPIO31	IDC2_CLK, VIN_STRIG0
GPIO32	IDC2_DATA, VIN_STRIG1
GPIO33	IR_IN
GPIO34	SSI0_SCLK, NORSPI_CLK, UART_AHB_RX, SSIS_SCLK
GPIO35	SSI0_TXD, NORSPI_DQ[0], UART_AHB_TX, SSIS_RXD
GPIO36	SSI0_RXD, NORSPI_DQ[1], UART_AHB_CTS_N, SSIS_TXD
GPIO37	SSI0_EN0, NORSPI_EN[0], UART_AHB_RTS_N, SSIS_EN
GPIO38	SSI0_EN1, NORSPI_EN[1]
GPIO39	UART0RX, UART_AHB_RX
GPIO40	UART0TX, UART_AHB_TX
GPIO41	I2S_CLK
GPIO42	I2S_SI
GPIO43	I2S_S0
GPIO44	I2S_WS
GPIO45	N/A
GPIO46	ENET_TXEN, SC_A0, ENET_TXEN, SSI1_SCLK, NORSPI_CLK
GPIO47	ENET_TXD_0, SC_A1, ENET_TXD_0, SSI1_TXD, NORSPI_DQ[0]
GPIO48	ENET_TXD_1, SC_A2, ENET_TXD_1, SSI1_RXD, NORSPI_DQ[1]
GPIO49	ENET_RXD_0, SC_A3, ENET_RXD_0, SSI1_EN0, NORSPI_EN[0]
GPIO50	ENET_RXD_1, SC_B0, ENET_RXD_1, SSI1_EN1, NORSPI_EN[1]
GPIO51	ENET_RXER, SC_B1, ENET_RXER, SSI1_EN2, NORSPI_EN[2]
GPIO52	ENET_CRS_DV, SC_B2, ENET_CRS_DV, SSI1_EN3, NORSPI_DQ[2]
GPIO53	ENET_REF_CLK, SC_B3, ENET_RX_CLK, NORSPI_DQ[3]
GPIO54	NAND_WP
GPIO55	NAND_CE, NORSPI_CLK
GPIO56	NAND_RB, NORSPI_DQ[4]
GPIO57	SD_CLK
GPIO58	SD_CMD
GPIO59	SD_CD
GPIO60	SD_WP

PIN NANE	Function
GPIO61	NAND_RE, NORSPI_DQ[5]
GPIO62	NAND_WE, NORSPI_DQ[6]
GPIO63	NAND_ALE, NORSPI_DQ[7]
GPIO64	NAND_D[0], NORSPI_EN[0]
GPIO65	NAND_D[1], NORSPI_EN[1]
GPIO66	NAND_D[2], NORSPI_EN[2]
GPIO67	NAND_D[3], NORSPI_EN[3]
GPIO68	NAND_D[4], NORSPI_DQ[0]
GPIO69	NAND_D[5], NORSPI_DQ[1]
GPIO70	NAND_D[6], NORSPI_DQ[2]
GPIO71	NAND_D[7], NORSPI_DQ[3]
GPIO72	NAND_CLE
GPIO73	SD_D[0]
GPIO74	SD_D[1]
GPIO75	SD_D[2]
GPIO76	SD_D[3]
GPIO77	SD_D[4], SC_C0, SSIS_SCLK
GPIO78	SD_D[5], SC_C1, SSIS_RXD
GPIO79	SD_D[6], SC_C2, SSIS_TXD
GPIO80	SD_D[7], SC_C3, SSIS_EN
GPIO81	SDIO_CLK
GPIO82	SDIO_CMD
GPIO83	SDIO_D[0], SC_D0, SSIS_SCLK
GPIO84	SDIO_D[1], SC_D1, SSIS_RXD
GPIO85	SDIO_D[2], SC_D2, SSIS_TXD
GPIO86	SDIO_D[3], SC_D3, SSIS_EN
GPIO87	SDIO_CD
GPIO88	SDIO_WP
GPIO89	HDMITX_HPD
GPIO90	HDMITX_CEC, ENET_2ND_REF_CLK
GPIO91	VIN_SVSYNC, IDSP_PIP_IOPAD_MASTER_HSYNC
GPIO92	VIN_SHSYNC, IDSP_PIP_IOPAD_MASTER_VSYNC
GPIO93	VD0_OUT[0]
GPIO94	VD0_OUT[1]
GPIO95	VD0_OUT[2]
GPIO96	VD0_OUT[3]
GPIO97	VD0_OUT[4]
GPIO98	VD0_OUT[5]
GPIO99	VD0_OUT[6]
GPIO100	VD0_OUT[7]
GPIO101	VD0_OUT[8]
GPIO102	VD0_OUT[9]
GPIO103	VD0_OUT[10]
GPIO104	VD0_OUT[11]
GPIO105	VD0_OUT[12]
GPIO106	VD0_OUT[13]
GPIO107	VD0_OUT[14]
GPIO108	VD0_OUT[15]
GPIO109	VD0_CLK
GPIO110	VD0_VSYNC
GPIO111	VD0_HSYNC
GPIO112	VD0_HVLD
GPIO113	PWM_0

```
A12 POWER ON CONFIG( POC[31:0])

=======POC pin mapping =========

POC_[15:0] => VD0_OUT[15:0]
POC_16 = > I2S_SO
POC_17 => VD0_HSYNC
POC_18 => ENET_TXD0
POC_19 => ENET_TXD1
POC_[27:20] => No pins
POC_28 => VD0_CLK
POC_29 => VD0_VSYNC
POC_30 => No pin
POC_31 => VD0_HVLD
====================================
POC Pin Description
====================================
POC_0
ENET SEL
0: disable,   1: enable
====================================
POC_[3:1]
      VDSP/IDSP/DRAM/CORTEX
000:  312 / 408 / 600 / 816 Mhz
001:  252 / 348 / 396 / 720 Mhz
010:  240 / 336 / 528 / 720 Mhz
011:  144 / 144 / 396 / 672 Mhz
100:  432 / 408 / 600 / 792 Mhz
101:  312 / 432 / 336 / 504 Mhz
110:  348 / 408 / 600 / 1008 Mhz
111:  216 / 216 / 216 / 216 Mhz
====================================
POC_[5:4]
Boot Mode[1:0]
00: SPI-NOR Flash
01: NAND
10: MMC
11: SPI-EEPROM
====================
POC_6
ENET_PHY_ENET_SEL
0: MII
1: RMII
====================
POC_7
USB_PHY_12Mhz
0: default 24Mhz
1: 12Mhz
====================
POC_8
Boot Bypass
0: disable
1: enable
====================
POC_9
Freq RAMP Enable
0: Disable
1: Enable
====================
POC_10
Force USB boot
0: Disable
1: Enable
====================
POC_[12:11]
CLOCK SRC MODE[1:0]
00: normal mode
01: ref clock
10: reserved
11: reserved
====================
POC_13
Ref clock is 48Mhz
0: Disable
1: Enable
====================

POC_[19:14]
Boot Options [5:0]

(See table below)
====================================
POC_[27:20]
No Pins (always 0)
====================================
POC_28
USB0_MASK_IDDIG0
0: Use IDDIG0 signal from PHY to configure
    it as Host or Device
1: Mask IDDIG0 signal from PHY and use
   POC_29 for USB type selection
====================================
POC_29
USB0_TYP_SEL Configure USBPHY0
0: Host
1: Device
Note: valid only when POC_28 is set to 1
POC_[29:28] are ignored when POC_10 is 1
====================================
POC_31
Source of sys config data
0: config data is set by pins
1: config data is read from on-chip efuse rom
====================================
```

	SPINOR	NAND	MMC	SPI	Force USB
boot_option[5]	--	2*2k page boot mode.	--	--	--
boot_option[4]	Use 2 bytes address	NAND page size	--	byte_address[1]	--
boot_option[3]	Use alternative clock	NAND read confirm	sd4_boot	byte_address[0]	--
boot_option[2]	SPI mode selection	NAND ECC BCH enable	sd8_boot	--	--
boot_option[1]	LSB first	NAND spare cell 2X	hs_boot	--	--
boot_option[0]	Boot pin selection. 0: Use xx_sc_* f or NOR_SPI. 1: Use xx_smio_* for NOR_SPI.	Flash fast boot	ddr_boot	--	--

boot_option[5:0] Table

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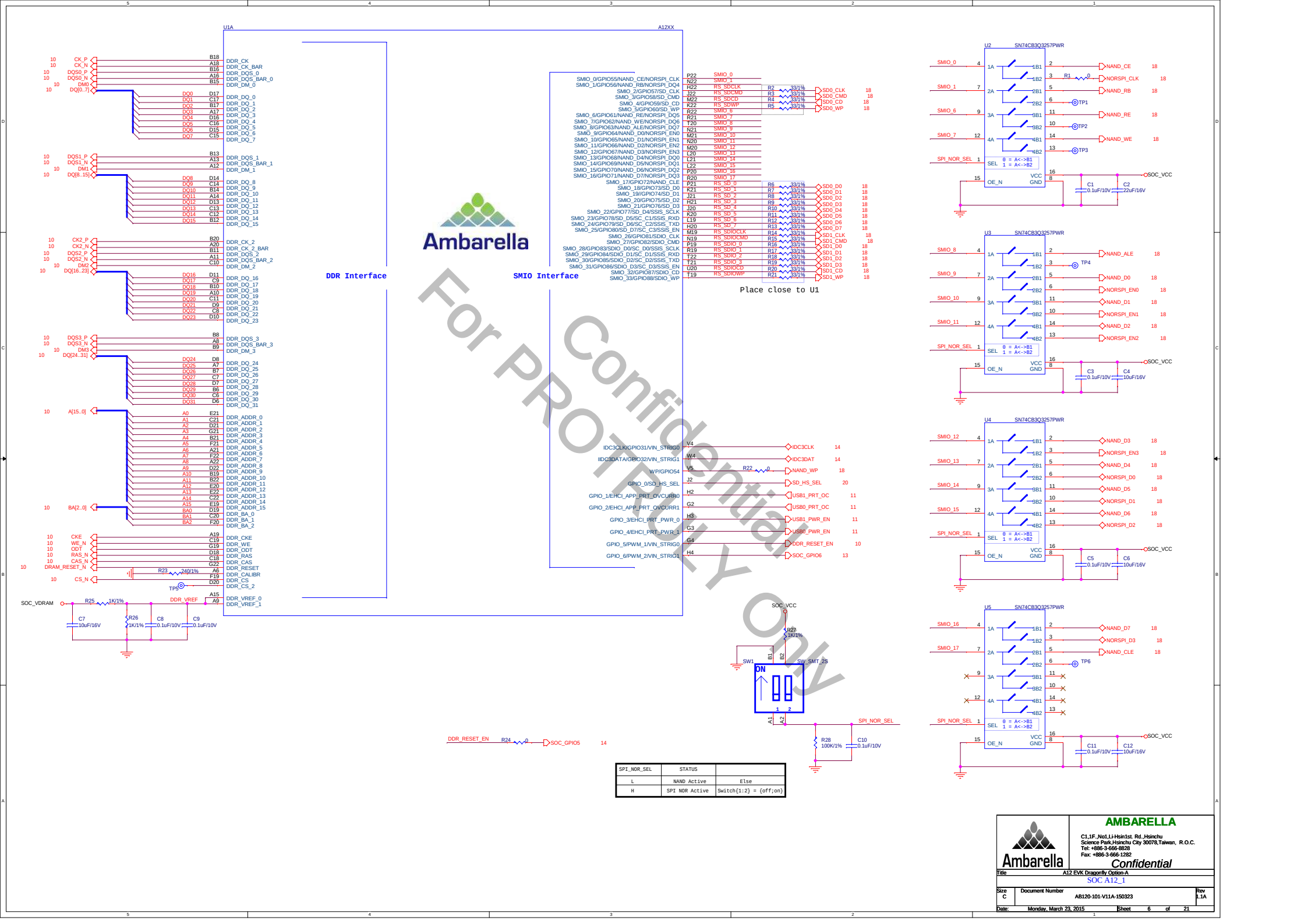

SPI_NOR_SEL	STATUS	
L	NAND Active	Else
H	SPI NOR Active	Switch{1:2} = {off;on}

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Title	A12 EVK Dragonfly Option-A		
	SOC A12_1		
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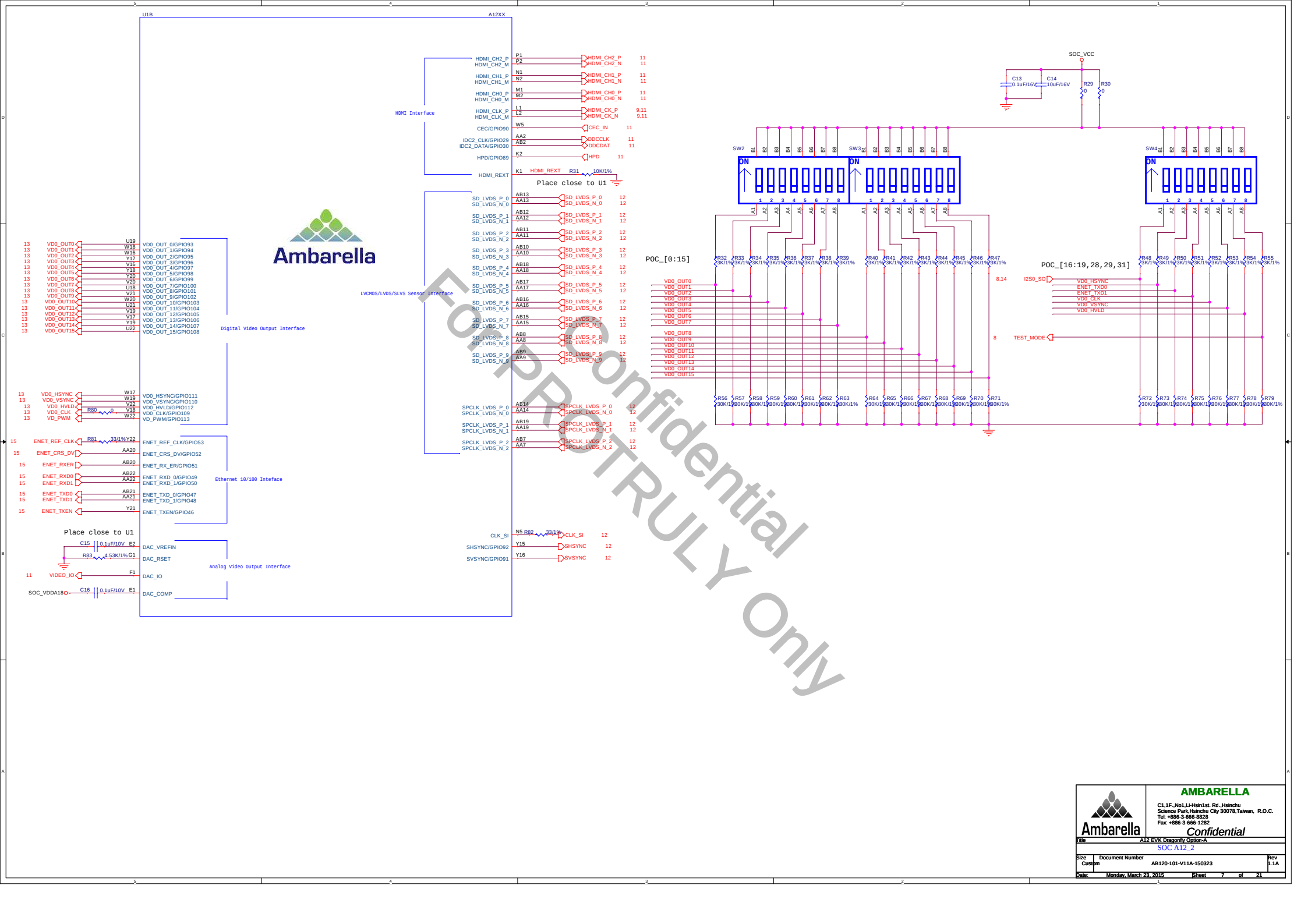

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	SOC A12_2
Size: Custom	Document Number: AB120-101-V11A-150323
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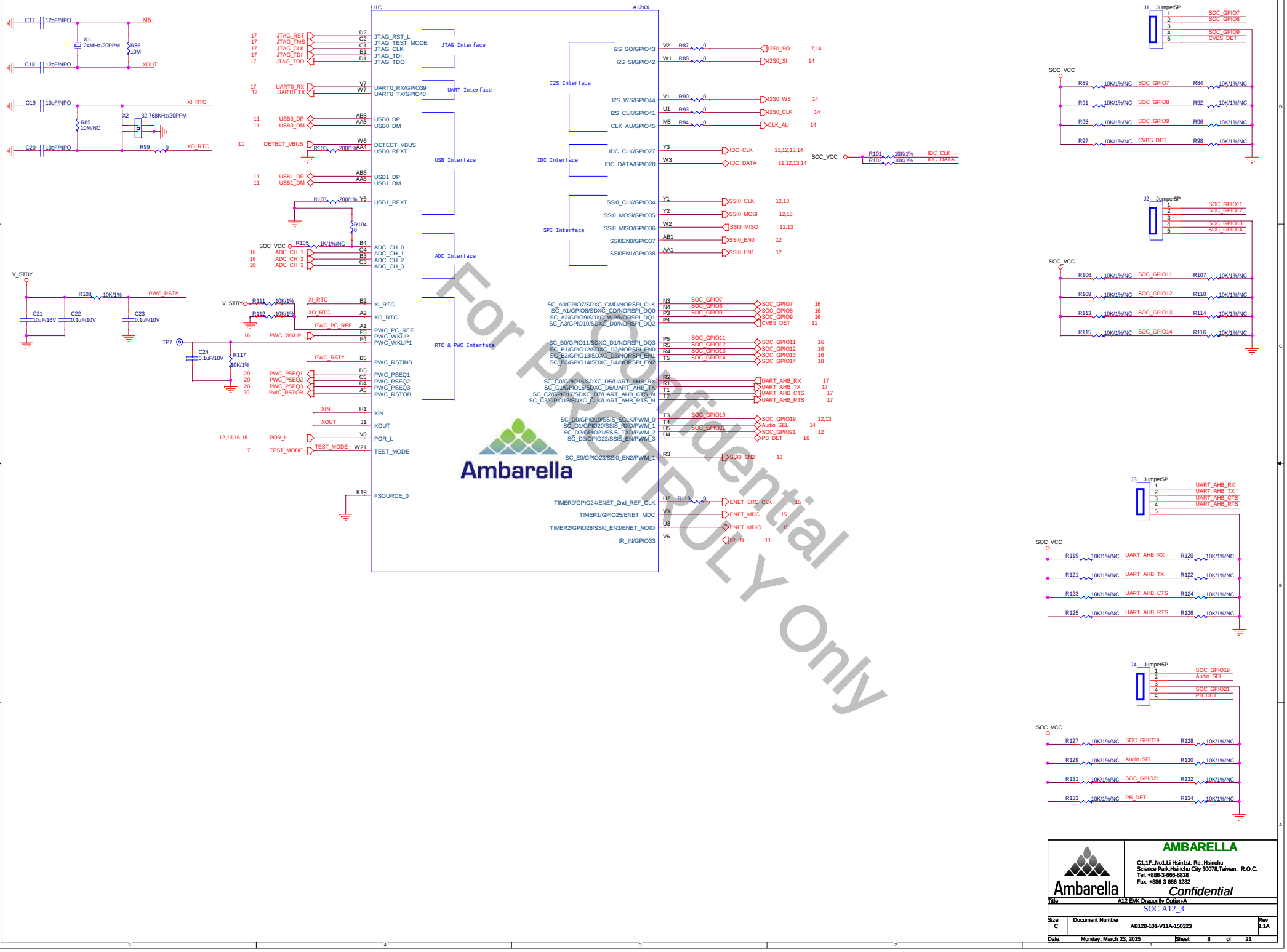

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	SOC A12_3	
Size C	Document Number AB120-101-V11A-150323	Rev 1.1A
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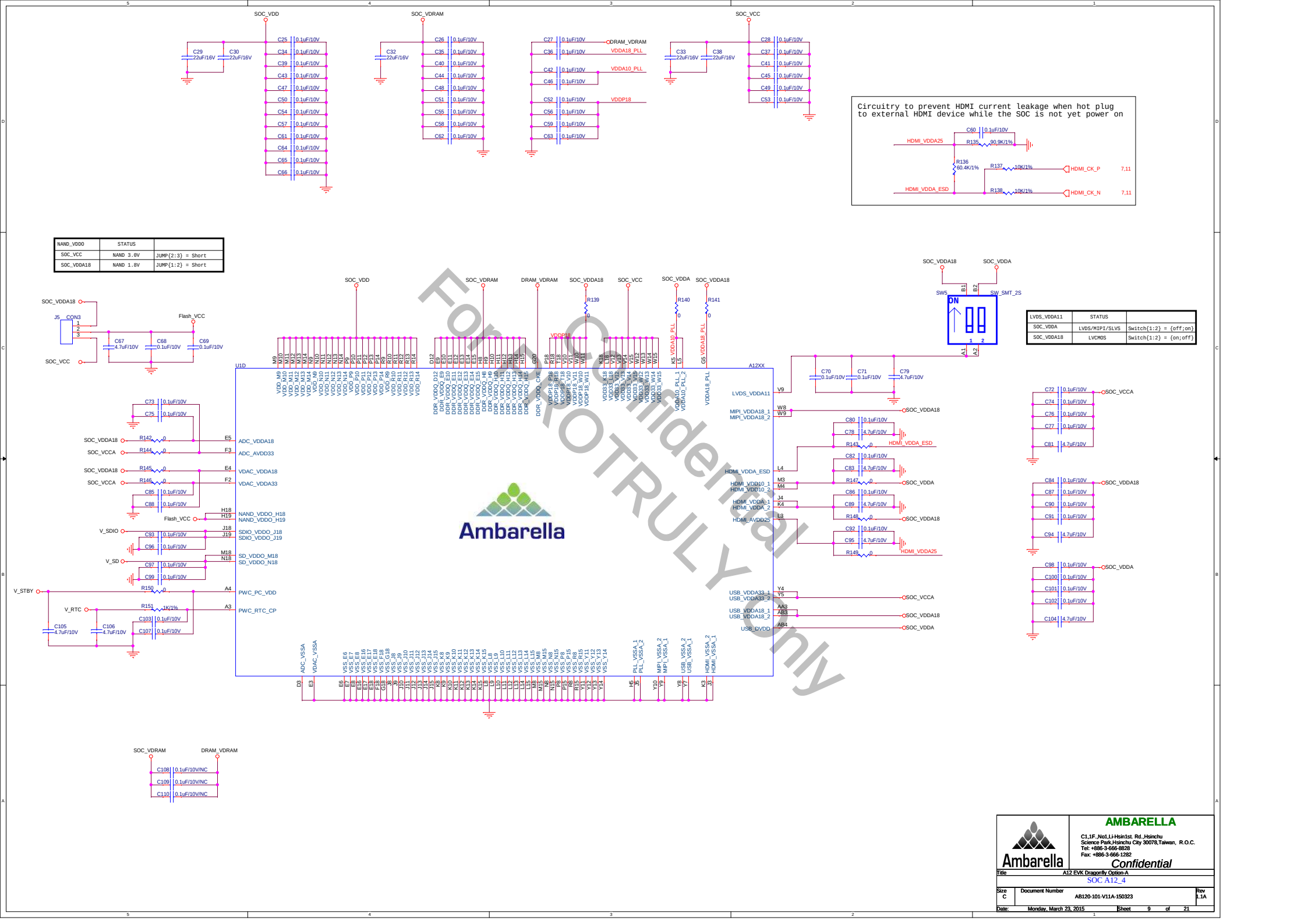

NAND_VDDO	STATUS	
SOC_VCC	NAND 3.0V	JUMP{2:3} = Short
SOC_VDDA18	NAND 1.8V	JUMP{1:2} = Short

LVDS_VDDA11	STATUS	
SOC_VDDA	LVDS/MIPI/SLVS	Switch{1:2} = {off;on}
SOC_VDDA18	LVCMOS	Switch{1:2} = {on;off}

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Title	A12 EVK Dragonfly Option-A	
	SOC A12_4	
Size C	Document Number AB120-101-V11A-150323	Rev 1.1A
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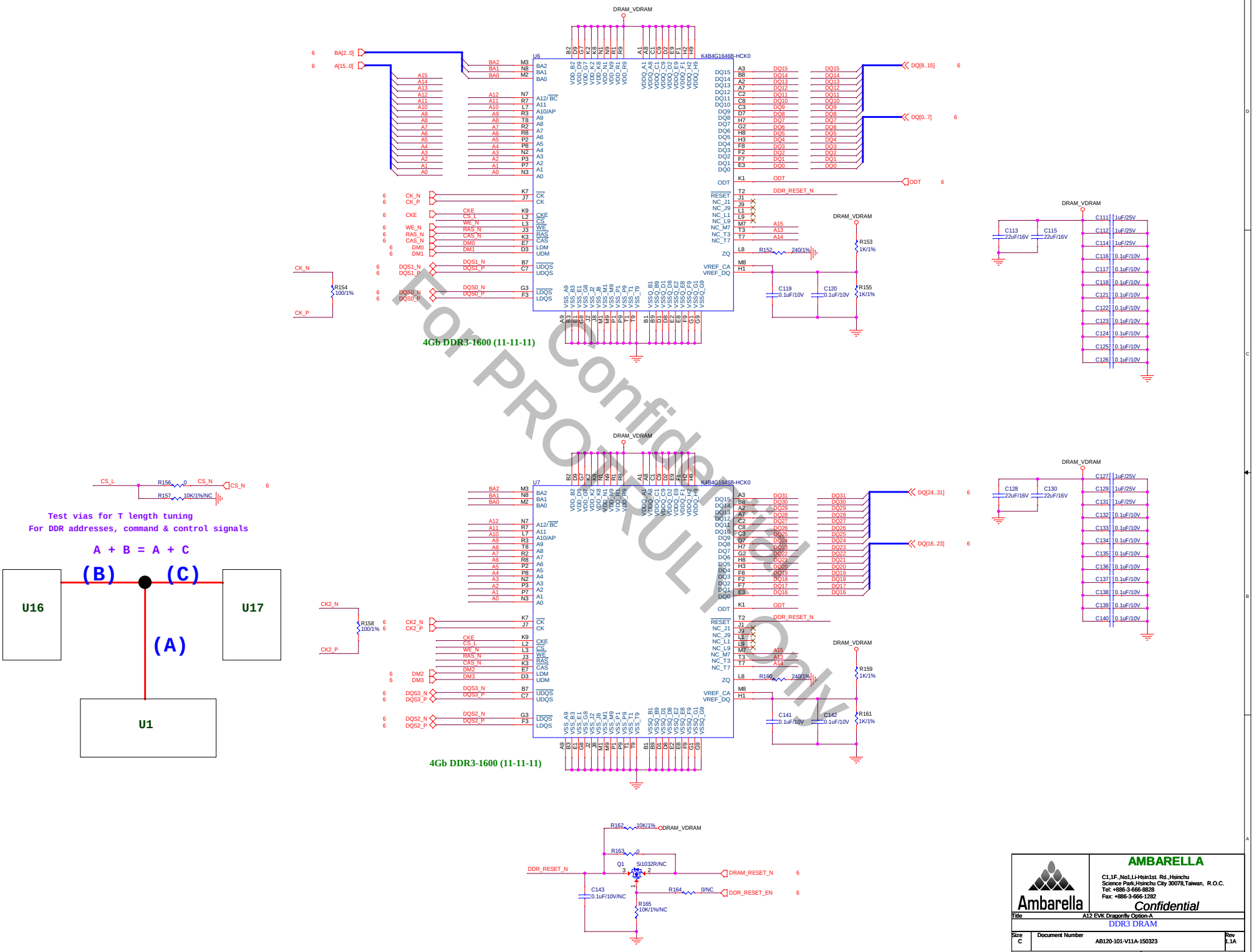

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Title	A12 EVK Dragonfly Option-A
	DDR3 DRAM
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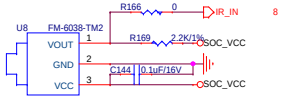
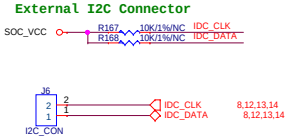
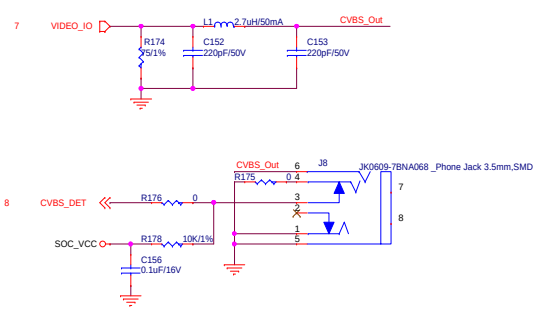
IR Receive Module

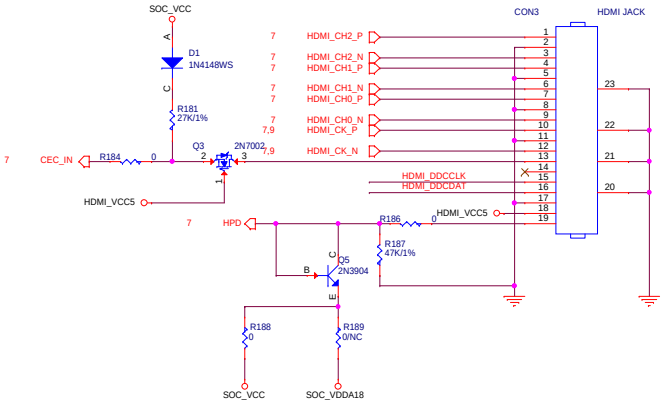


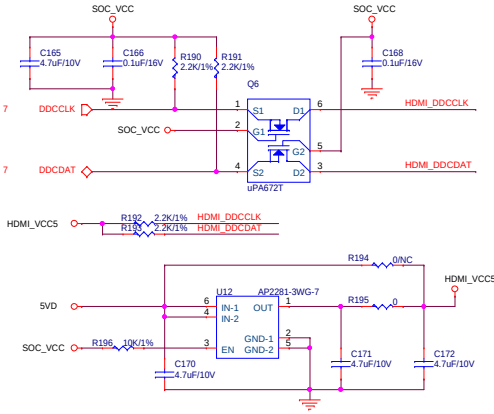
External I2C Connector

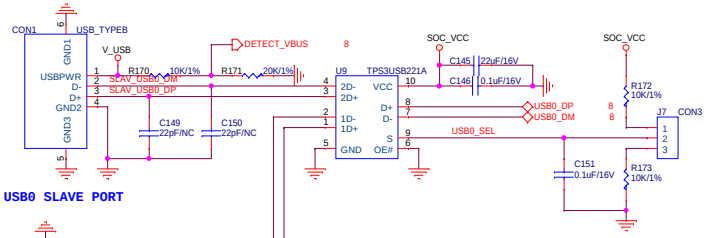


CVBS

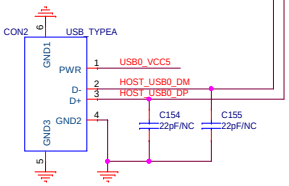








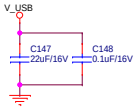
USB0 SLAVE PORT



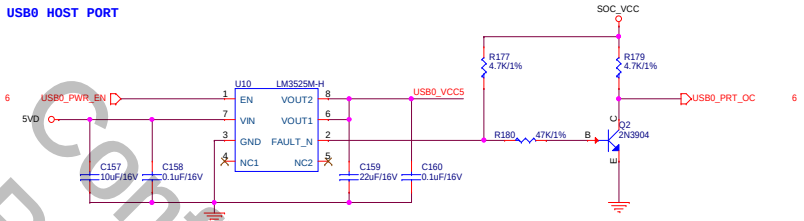
USB0 HOST PORT

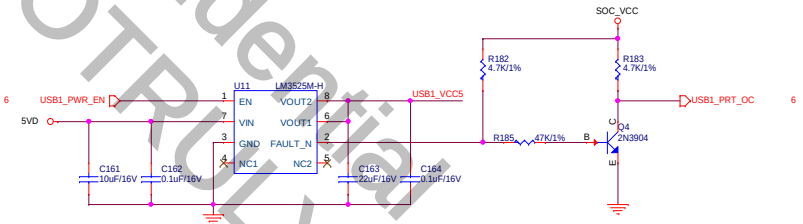
USB0 Port Select:

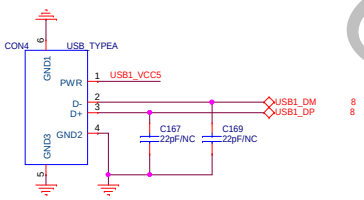
0 -> Host
1 -> Slave



USB0_SEL	STATUS	
0	HOST	JUMP{2:3} = Short
1	SLAVE	JUMP{1:2} = Short







USB1 Host Port

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Title	A12 EVK Dragonfly Option-A	
	USB/HDMI/Analog Vout	
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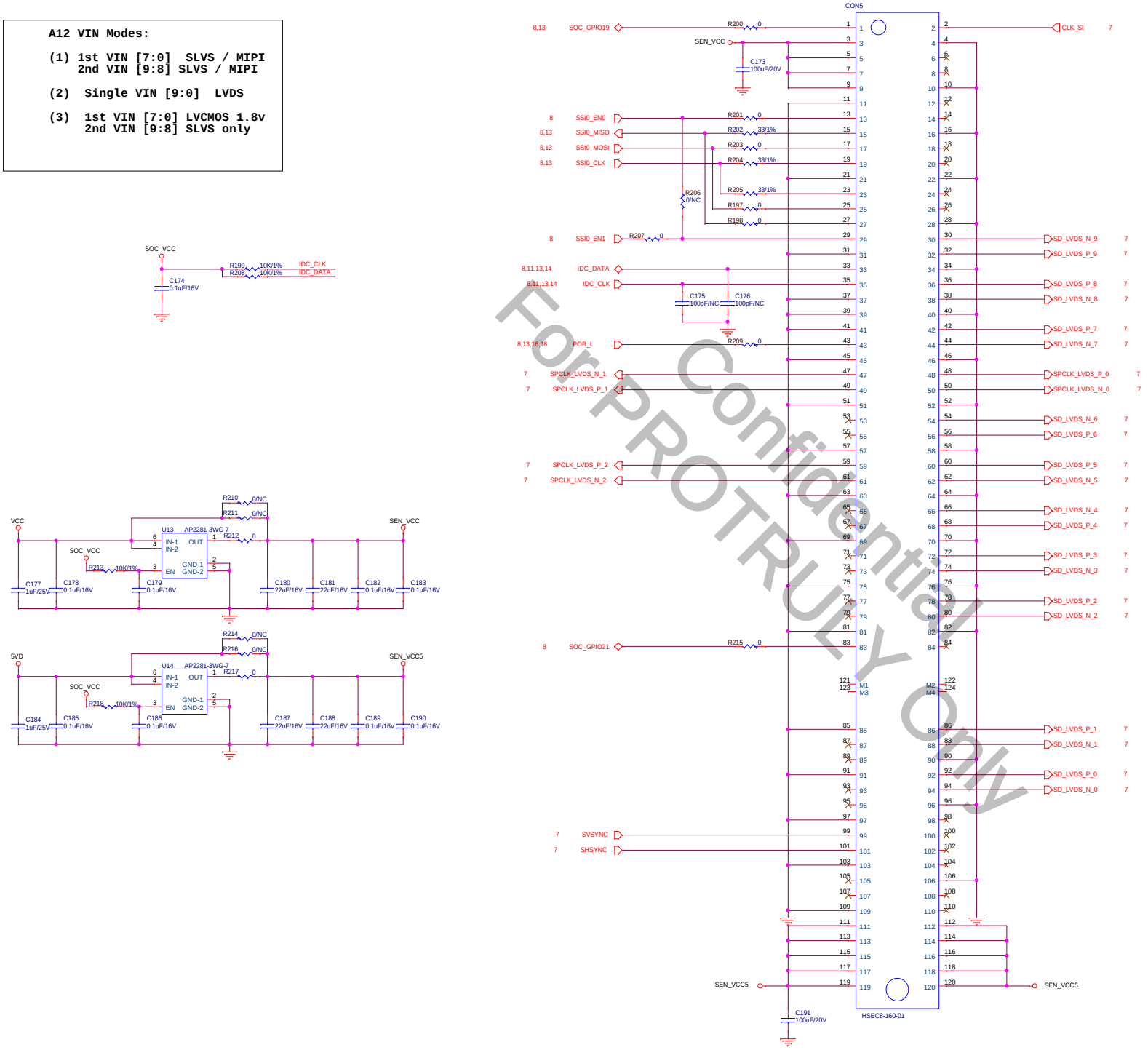
A12 VIN Modes:

(1) 1st VIN [7:0] SLVS / MIPI
2nd VIN [9:8] SLVS / MIPI

(2) Single VIN [9:0] LVDS

(3) 1st VIN [7:0] LVCMOS 1.8v
2nd VIN [9:8] SLVS only



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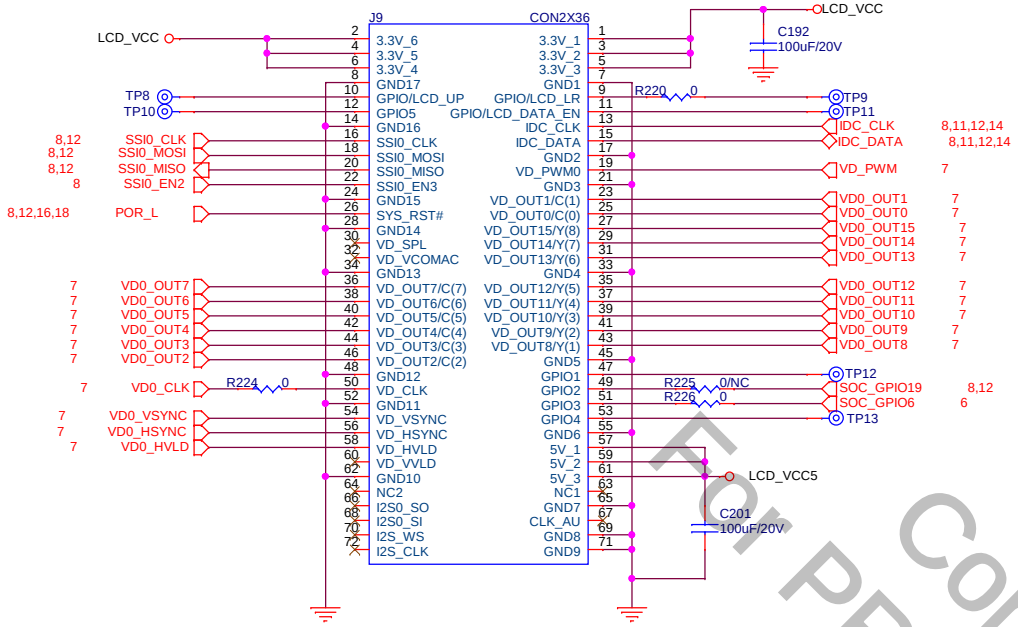
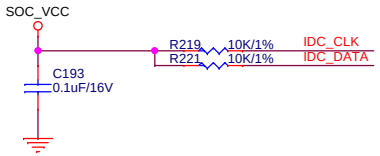
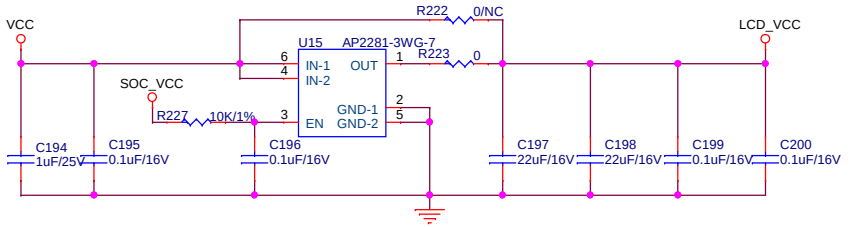
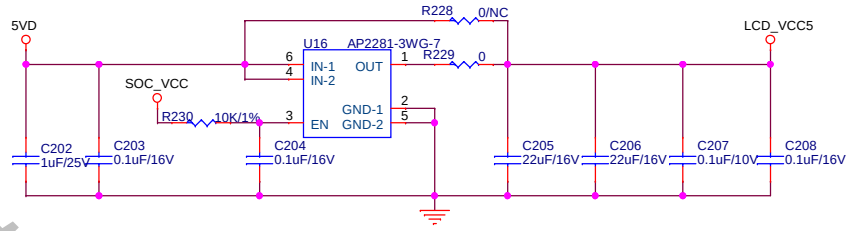
Title	A12 EVK Dragonfly Option-A
	Primary/Secondary VIN
Size C	Document Number AB120-101-V11A-150323 Rev 1.1A
Date: Monday, March 23, 2015	Sheet 12 of 21









Video output modes:

Digital RGB mode (video output modes 0/1/2 for 3-bit output to the LCD)

Bits	Mapped to signal	Notes
VD0_OUT[15:8] VD0_OUT[7:0]	Unused Interleaved R,G,B	VD0_OUT[7] is MSB

5:6:5 RGB Mode (Video Output Mode 3 for 16-bit RGB Output to the LCD)

Bits	Mapped to signal	Notes
VD0_OUT[15:11] VD0_OUT[10:5] VD0_OUT[4:0]	Upper 5 bits of the Red channel Upper 6 bits of the Green channel Upper 5 bits fo the Blue channel	VD0_OUT[15] is MSB VD0_OUT[10] is MSB VD0_OUT[4] is MSB

656 YCbCr Mode (Video Output Mode 4 for D1 - 480i and 576 Resolution)

Bits	Mapped to signal	Notes
VD0_OUT[15:8] VD0_OUT[7:0]	Unused Interleaved Cb, Y, Cr, Y ...	Output data rate is 13.5 MHz Clock rate is 27 MHz

16-bit 656 YCbCr Mode (Video Output Mode 4) and 16-bit YCbCr Mode (Video Output Mode 5)

Bits	Mapped to signal	Notes
VD0_OUT[15:8] VD0_OUT[7:0]	Interleaved Cb, Cr Y	VD0_OUT[15] is MSB VD0_OUT[7] is MSB

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Title	A12 EVK Dragonfly Option-A	
	Digital Vout	
Size B	Document Number AB120-101-V11A-150323	Rev 1.1A
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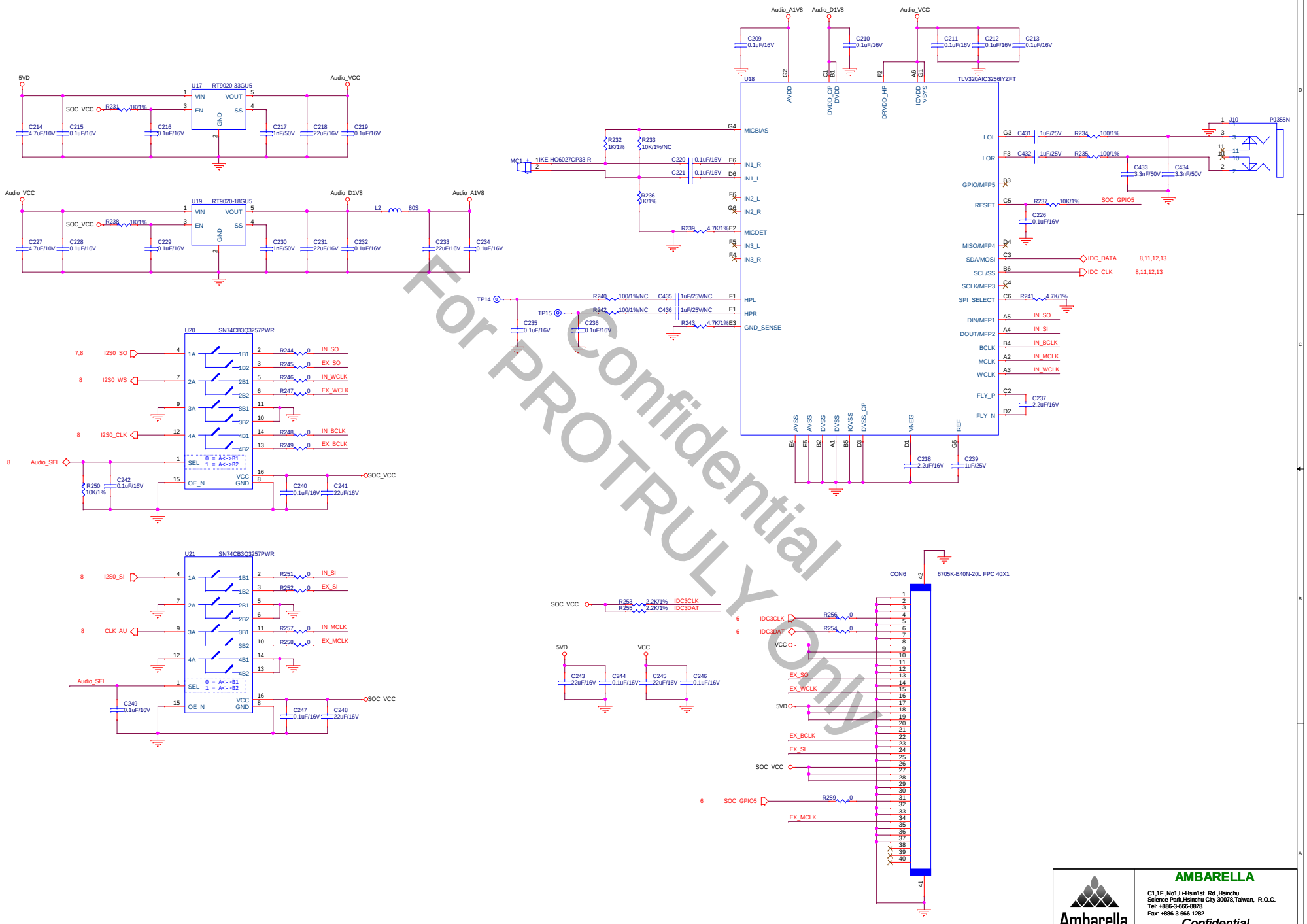

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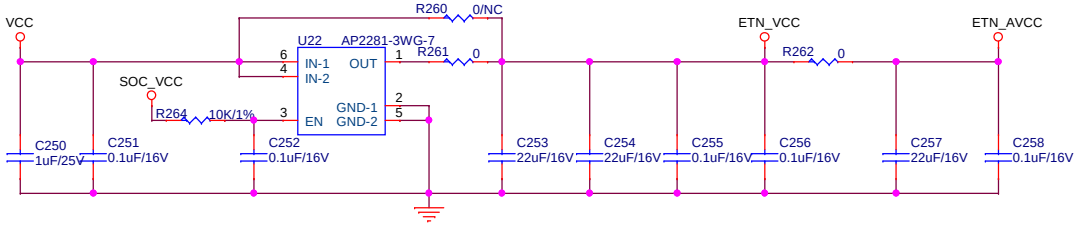
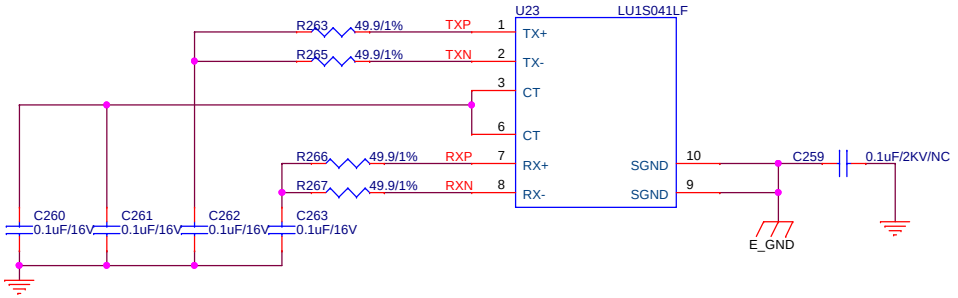
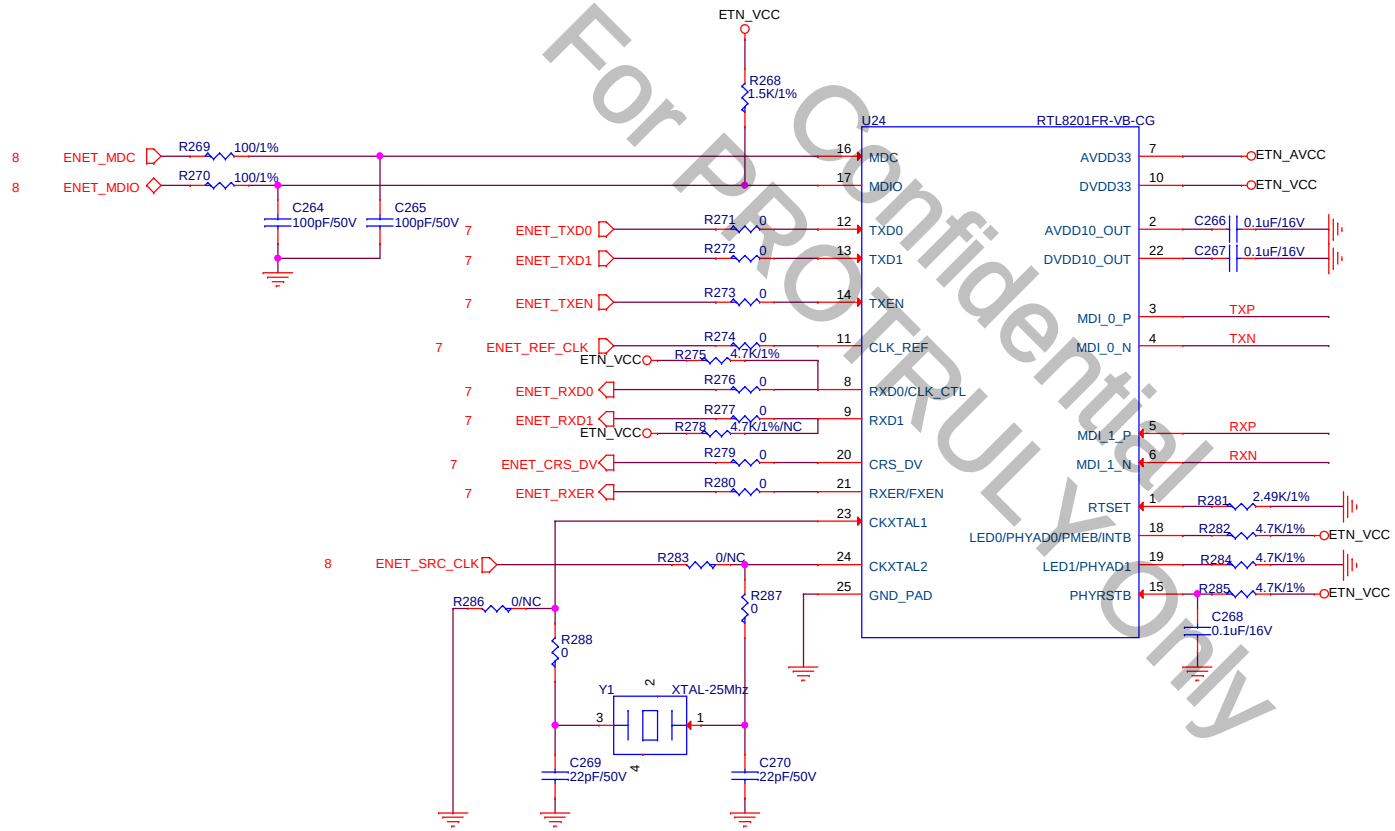
Title	A12 EVK Dragonfly Option-A	
	Audio	
Size C	Document Number AB120-101-V11A-150323	Rev 1.1A
Date: Monday, March 23, 2015	Sheet 14 of 21	







Strap pins

RXD0 -> 0 CLK_REF ouput
1 CLK_REF input from MAC (default)

RXD1 -> 0 (default) LED mode
1 WOL mode

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Title	A12 EVK Dragonfly Option-A	
	ETN	
Size B	Document Number AB120-101-V11A-150323	Rev 1.1A
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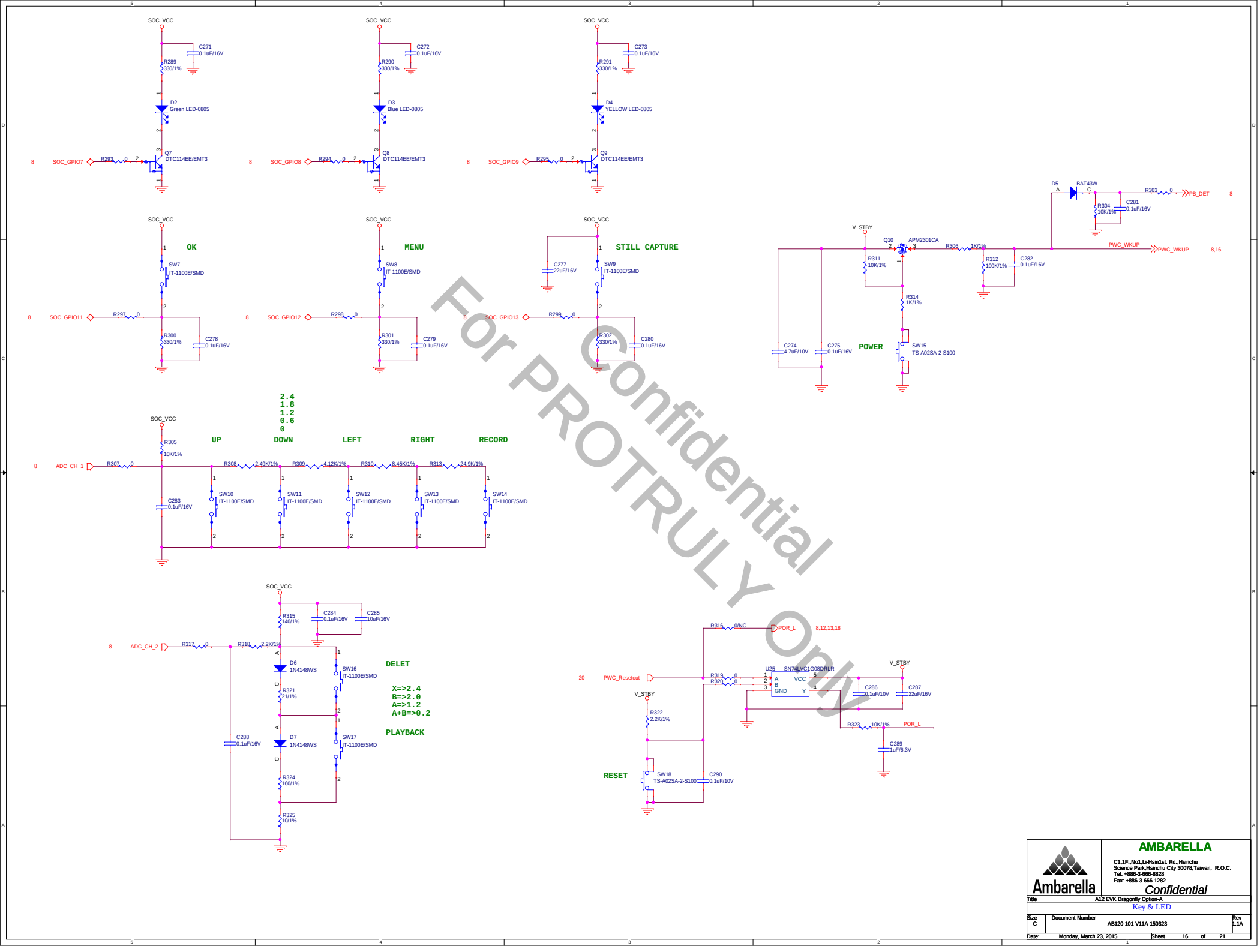

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Title	A12 EVK Dragonfly Option-A		
	Key & LED		
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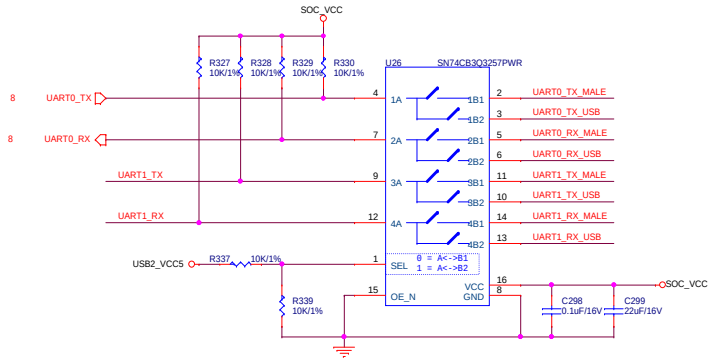
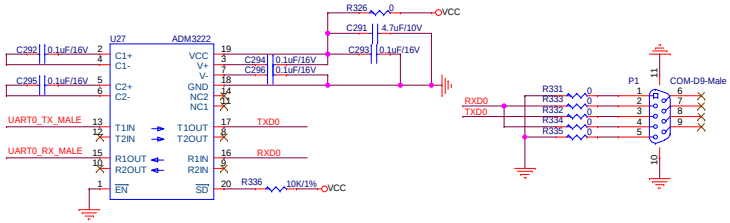
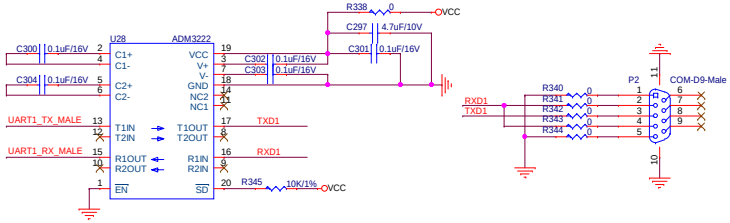
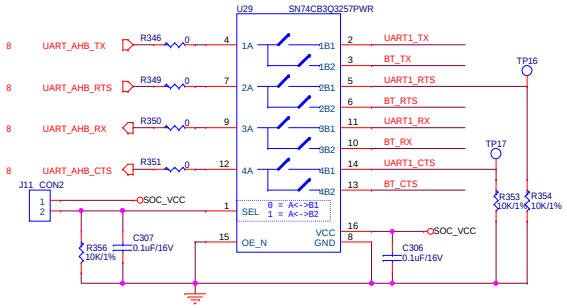
UART

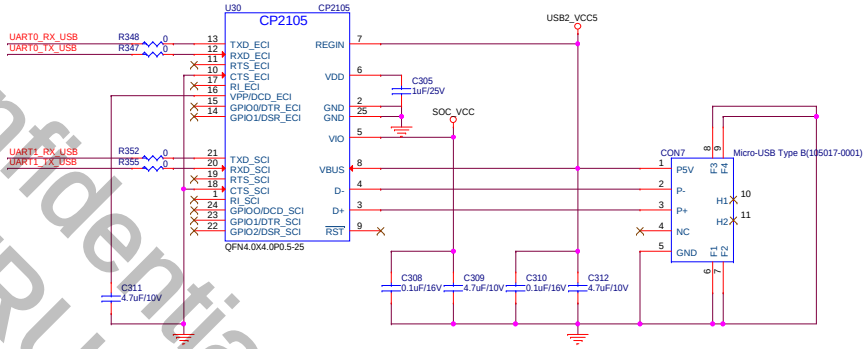


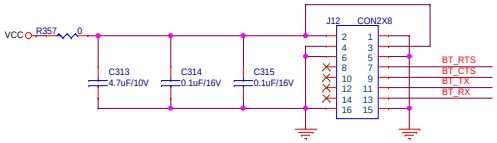


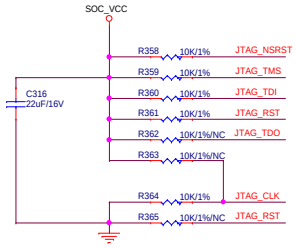


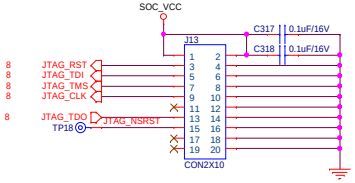


BT_SEL	STATUS	
0	Debug Port	JUMP{1:2} = Open
1	Bluetooth	JUMP{1:2} = Short









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Title	A12 EVK Dragonfly Option-A	
	UART & JTAG	
Size C	Document Number AB120-101-V11A-150323	Rev 1.1A
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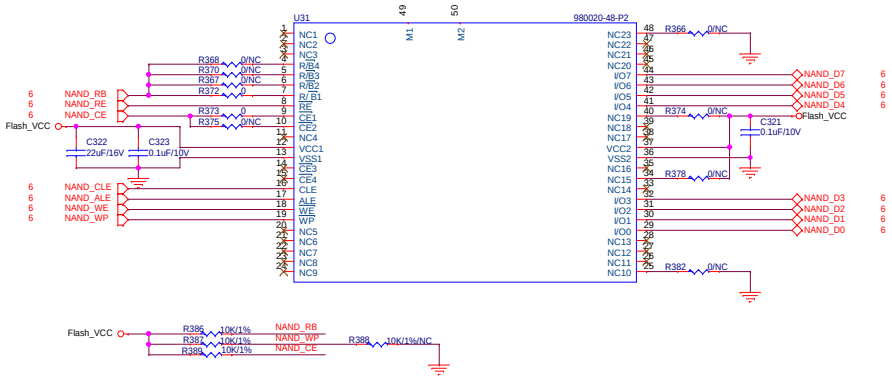
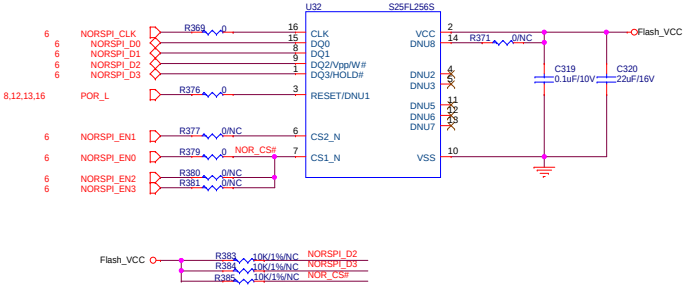
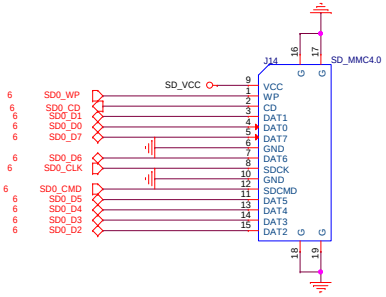
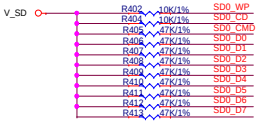
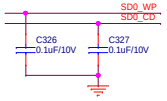


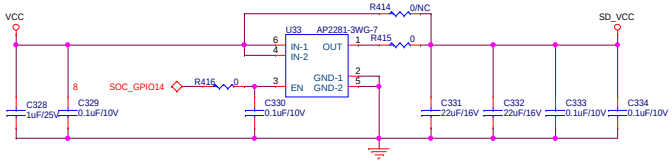


SD / SDHC / SDXC with UHS-I support (SD Port-0)

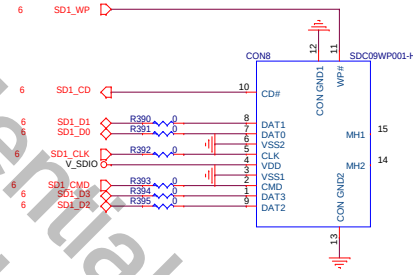


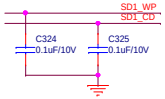




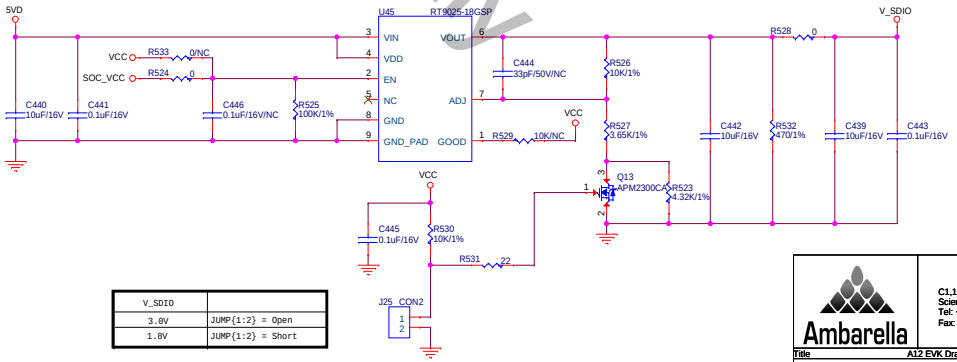


SD / SDHC / SDXC (SD Port-1) FOR WIFI





V_SDIO 3.0V@2A For SD Port 1



V_SDIO	
3.0V	JUMP{1:2} = Open
1.8V	JUMP{1:2} = Short

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Title	A12 EVK Dragonfly Option-A	
	NAND & SDIO	
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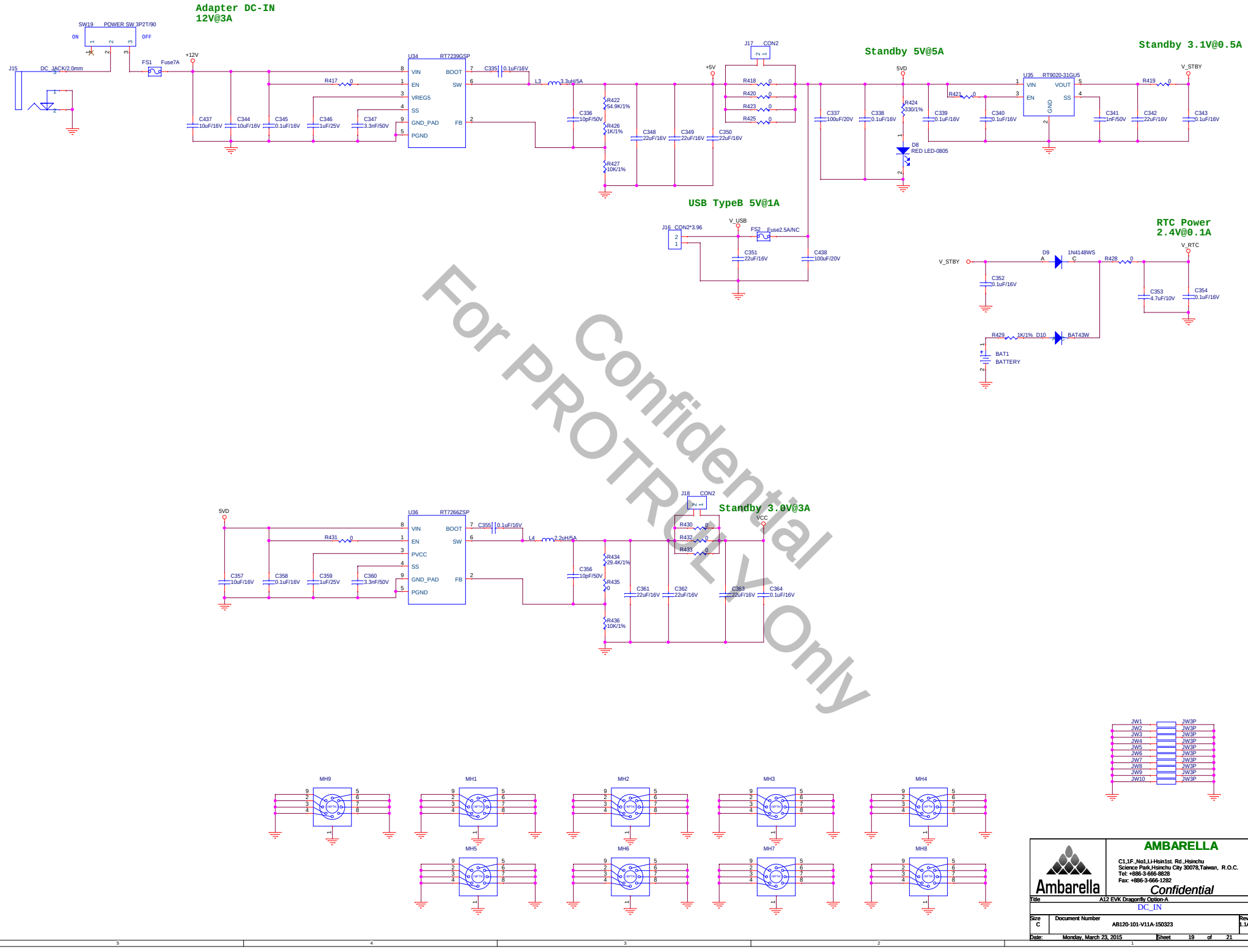
Adapter DC-IN
12V@3A
SW19 POWER SW 3P2T/90
ON
OFF
J15 DC_JACK/2.0mm
FS1 Fuse7A
+12V
U34 RT7239GSP
VIN
EN
VREG5
SS
GND_PAD
PGND
BOOT
SW
FB
C335 0.1uF/16V
L3 3.3uH/5A
R417 0
C437 10uF/16V
C344 10uF/16V
C345 0.1uF/16V
C346 1uF/25V
C347 3.3nF/50V
C336 10pF/50V
R422 54.9K/1%
R426 1K/1%
R427 10K/1%
C348 22uF/16V
C349 22uF/16V
C350 22uF/16V
+5V
J17 CON2
R418 0
R420 0
R423 0
R425 0
Standby 5V@5A
5VD
C337 100uF/20V
C338 0.1uF/16V
R424 330/1%
D8 RED LED-0805
Standby 3.1V@0.5A
U35 RT9020-31GU5
VIN
VOUT
EN
SS
GND
R421 0
C339 0.1uF/16V
C340 0.1uF/16V
C341 1nF/50V
C342 22uF/16V
C343 0.1uF/16V
R419 0
V_STBY
USB TypeB 5V@1A
J16 CON2*3.96
V_USB
FS2 Fuse2.5A/NC
C351 22uF/16V
C438 100uF/20V
RTC Power
2.4V@0.1A
V_STBY
D9 1N4148WS
R428 0
V_RTC
C352 0.1uF/16V
C353 4.7uF/10V
C354 0.1uF/16V
R429 1K/1%
D10 BAT43W
BAT1 BATTERY
Standby 3.0V@3A
5VD
U36 RT7266ZSP
VIN
EN
PVCC
SS
GND_PAD
PGND
BOOT
SW
FB
C355 0.1uF/16V
L4 2.2uH/5A
R431 0
C357 10uF/16V
C358 0.1uF/16V
C359 1uF/25V
C360 3.3nF/50V
C356 10pF/50V
R434 29.4K/1%
R435 0
R436 10K/1%
C361 22uF/16V
C362 22uF/16V
C363 22uF/16V
C364 0.1uF/16V
J18 CON2
VCC
R430 0
R432 0
R433 0
JW1 JW3P
JW2 JW3P
JW3 JW3P
JW4 JW3P
JW5 JW3P
JW6 JW3P
JW7 JW3P
JW8 JW3P
JW9 JW3P
JW10 JW3P
MH9
MH1
MH2
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MH8
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Title A12 EVK Dragonfly Option-A
DC_IN
Size C
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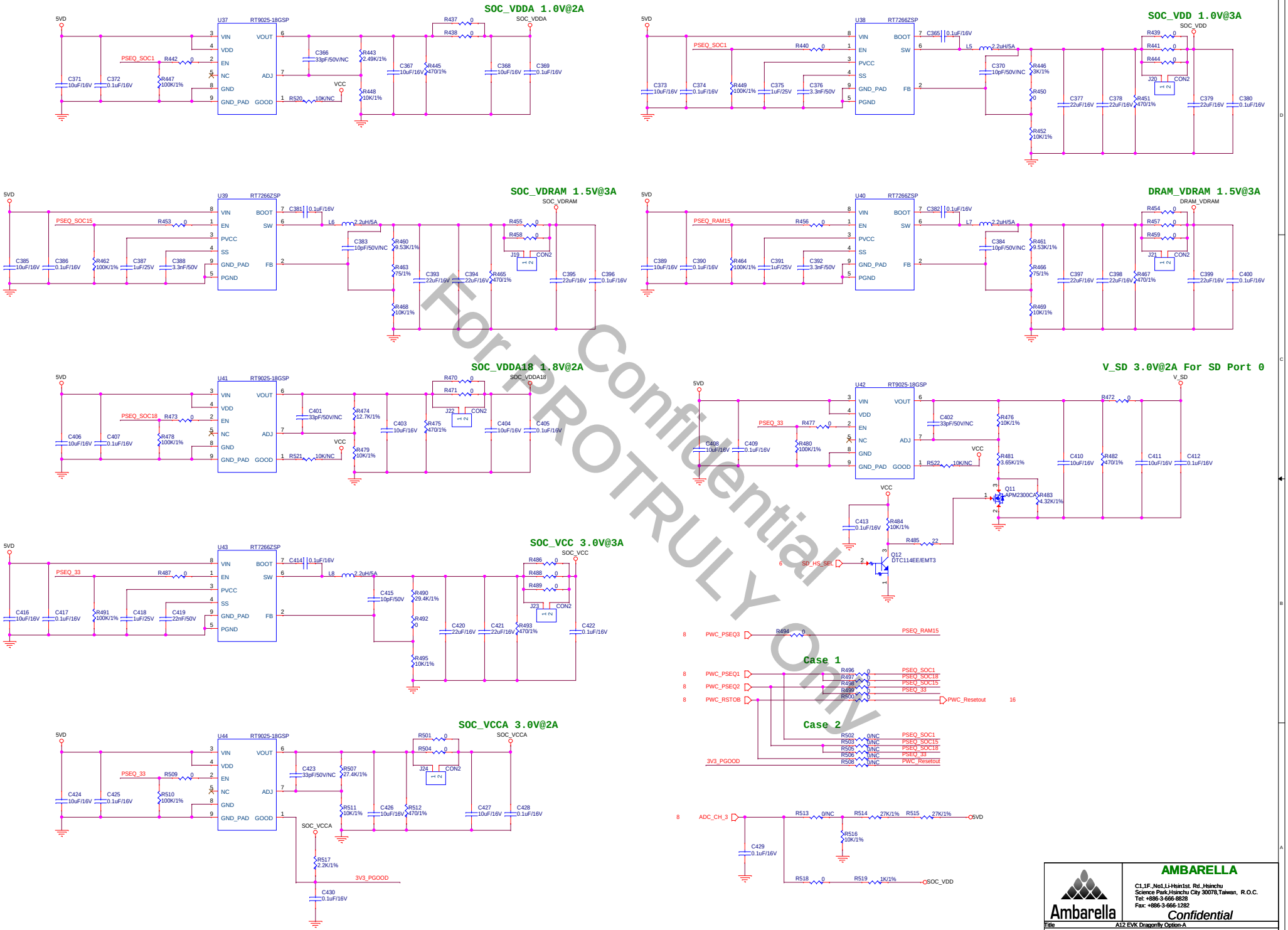

Revision History

Revision	History	Date	Note
V10A	Initiated schematics (first draft)	April 1, 2014	
V11A-140701	Add U45	June 6, 2014	
V11A-150323	Change SOC_VDD & SOC_VDDA from 1.1V to 1.0V Support 2 Vin	January 31, 2015	R446: 4.32K/1% -> 3K/1% R443: 3.74K/1% -> 2.49K/1% R200: 0/NC -> 0 R225: 0 -> 0/NC R204: 0 -> 33/1% R205: 0 -> 33/1% R206: 0 -> 0/NC R207: 0/NC -> 0 R150: 1K/1% -> 0

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Title	A12 EVK Dragonfly Option-A Revision History	
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