A12 Application Note: System Hardware

SUMMARY DESCRIPTION

This document provides system hardware details for the Ambarella A12 system-on-a-chip (SoC) processor.

Guidelines for power management, the implementation of various peripheral interfaces, and PCB layout are presented.

Because best practices for camera design and board layout are strongly application-dependent, this document should be considered as a general reference guide only.

Ambarella offers board design review services as well as additional documentation to qualified customers.

KEY TOPICS

- Power-on and power-off sequence information
- Pin detail for the VIN module, including sensor connection, power and IO, and interface disconnect information
- VOUT interface detail
- GPIO pin characteristics, including IO and pull-high/low information
- ADC channel requirements and disconnect information
- Detail regarding the JTAG pins and UART interfaces
- PCB layout guidelines for DRAM, VIN, VOUT, SMIO, USB, the A12 power rails and more

CONTENTS

1. INTRODUCTION

1.1 Introduction: Overview

This document provides system hardware details for the Ambarella A12 system-on-a-chip (SoC) processor.

The document is intended to support A12-based camera design efforts by offering guidelines for power management, the implementation of various peripheral interfaces, and PCB layout.

Note that this reference material is supplemental in nature. The document does not duplicate details from other documents, nor does it discuss every A12 interface or implementation case. Because best practices for camera design and board layout are strongly application-dependent, this document should be considered as a reference guide only.

The document is organized as follows:

1.2 Introduction: Background Information

Users of this document are referred to the resources listed below.

- The A12 family of datasheets provides chip-specific information on performance features, peripheral interfaces, external pins, electrical characteristics, and package information.
- The "*A12 Hardware Programming Reference Manual*" (*A12 PRM*) lists software-programmable registers accessible from the CPU core, including detailed information on each field of each register, and should be considered the primary resource for programming A12 peripheral drivers. The *A12 PRM* also provides overviews of the system memory map, power-on configuration details, and ARM interrupts.

2. PWC, RTC AND POWER-ON SEQUENCE

2.1 PWC, RTC and Power-On: Overview

This chapter provides power-on / power-off information regarding the Power Controller (PWC) and the Real-Time Clock (RTC), and includes the power-on sequence for the A12 power rails. The chapter is organized as shown below:

Note that this document uses approximate / representative voltages to describe the A12 power rails in a relative sense. Refer to the A12 chip datasheet for absolute operation range and DC characteristics.

See Also:

- The A12 chip datasheet provides power pin electrical characteristics.
- The "*A12 Hardware Programming Reference Manual*" includes power-on configuration information.

2.2 PWC, RTC and Power-On: Power Controller (PWC)

The A12 Power Controller (PWC) is an efficient power-management module which can be used to simplify the design of low-power camera systems. The PWC module draws minimal quiescent current while the camera is in battery-mode or using standby power. In addition, the PWC uses the Real-Time Clock (RTC) for current time and alarm settings, increasing the accuracy of power-on / power-off sequence generation.

2.3 PWC, RTC and Power-On: PWC / RTC Timing Diagrams

This section describes PWC and RTC timing cycles as follows:

- (Section 2.3.5) PWC / RTC Timing: Input Voltage Reference

2.3.1 PWC / RTC Timing: PWC Wake-Up

The following diagram illustrates the Inactive, Transient, and Active signal states during the A12 PWC power-on / power-off cycles.

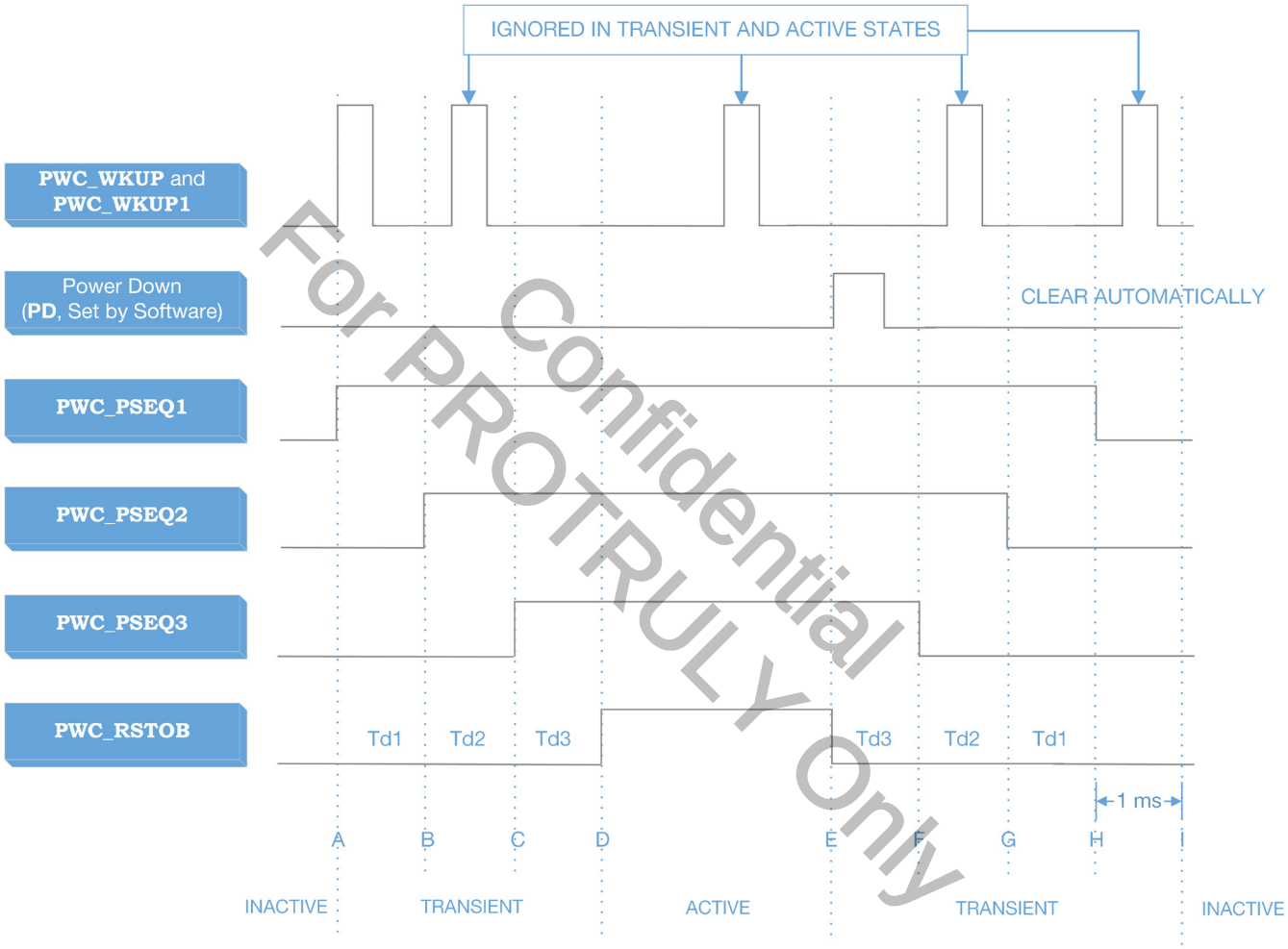

Figure 2-1. Inactive, Transient, and Active States During PWC Power-On / Power-Off Cycles.

Notes:

1. When the PWC is in an inactive state, the **PWC_WKUP** rising edge wakes-up the PWC module and issues the power sequence and reset accordingly. Note that **PWC_WKUP** events are ignored if the control module is in an Active state. Only a power-down (**PD**, set by software) can enable the power-off sequence. Refer to Section 2.3.3 for additional detail.

2. **PWC_WKUP** signals are ignored if the control module is in a Transient state, including those occurring during a power-on or power-off period. For a Transient state that occurs during power-off, there is a 1-ms extension after **PWC_PSEQ1** goes from High to Low.

3. The wake-up rising edge takes effect only if all other wake-up input pins stay low. If one wakeup pin stays high, triggers from all other wake-up pins will be blocked.

4. The PWC operates in conjunction with the Real-Time Clock (RTC) module. The **Td** timers (**Td1**, **Td2**, **Td3**) run on the RTC; therefore, in the absence of the RTC clock, the wake-up signal may have no effect. Refer to Section 2.3.2 for additional detail.

5. If the external reset signal in pin **PWC_RSTINB** stays low, the PWC module is in a reset state. Note that the PWC and RTC operate only when the PWC is not in a reset state. Refer to Section 2.3.4 for related detail.

6. **PWC_WKUP1** can be used flexibly. **PWC_WKUP** has reset functionality if held high for a long period of time.

2.3.2 PWC / RTC Timing: Timers (Td)

The A12 timers are described as follows:

- **Td[n]** are programmable timers used for 1-ms to 255-ms periods. The initial setting for all timers is 32 ms.
- The **Td[n]** register settings are maintained by **PWC_RTC_CP**, which is the RTC power pin.
- While the RTC power is active, the **Td[n]** value does not reset. In other words, the system does not reset even for a system power-off, a sudden power loss (e.g., accidental battery removal), or if the PWC reset signal **PWC_RSTINB** is issued, provided **PWC_RTC_CP** remains active.

2.3.3 PWC / RTC Timing: Power Down (PD)

The A12 **PD** is a pin internal to the RTC that can power-down all switchable domains by turning off the **PWC_PSEQ[1:3]** and **PWC_RSTOB** pins. Additional information regarding **PD** is provided below.

- **PD** maintains a control register that includes a power-down register bit (**pd**). Refer to the "*A12 Hardware Programming Reference Manual*" for register programming information.
- The PWC initiates a power-off sequence after **pd** is set by software.
- The **pd** bit is cleared automatically after the A12 SoC loses power. The **pd** bit is always zero in this case.

2.3.4 PWC / RTC Timing: PWC Reset

The A12 external pin **PWC_RSTINB** resets the power control module. The figures below illustrate the effect of **PWC_RSTINB** after power module wake-up:

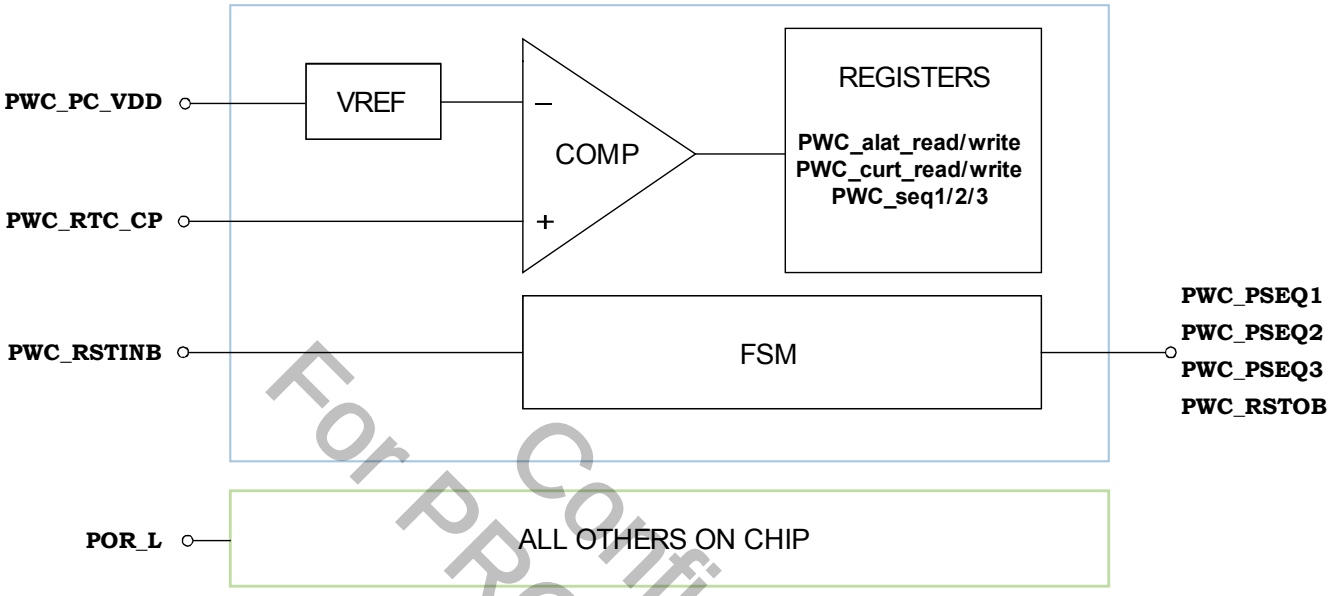

Figure 2-2. Power Control Reset Diagram.

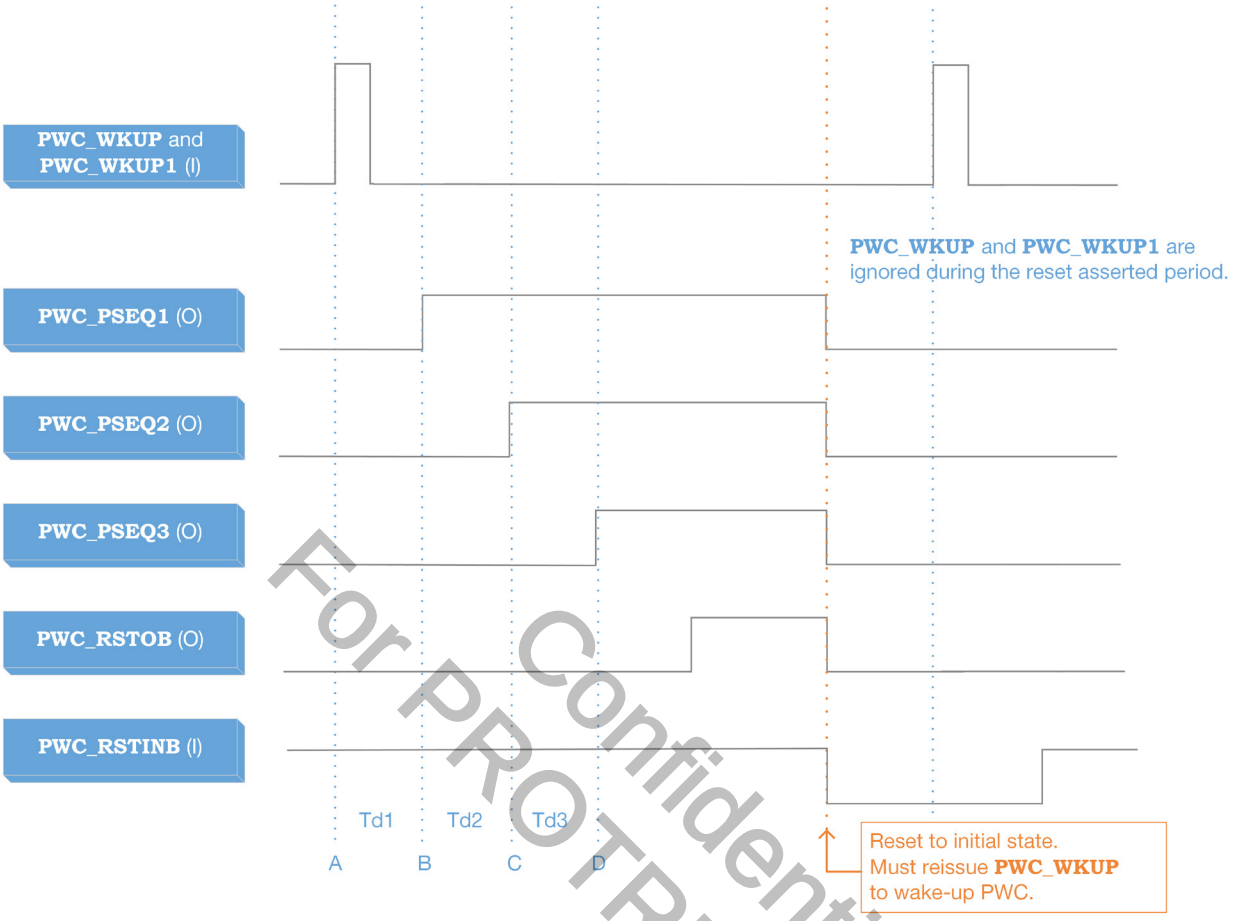

Figure 2-3. Power Control Reset Timing.

Notes:

1. Assertion of **PWC_RSTINB** drives **PWC_PSEQ[1:3]** and **PWC_RSTOB** to low, but the PWC registers maintain their value (**PWC_seq1/2/3**, **PWC_alat_read/write**, and **PWC_curt_read/write**).

2. Hardware uses **PWC_RSTINB** to reset the **PWC_PSEQ[1:3]**, and **PWC_RSTOB** pins. The mechanism is ARM- and DSP-independent, and the **PWC_RSTINB** function is not affected by software.

3. The global reset pin **POR_L** resets the entire chip with the exception of the PWC module.

2.3.5 PWC / RTC Timing: Input Voltage Reference

The A12 external pin **PWC_PC_REF** serves as a low-voltage alert reference when compared with an internal reference voltage. Information regarding **PWC_PC_REF** is included below. Please refer to the chip A12 datasheet for further details.

- When **PWC_PC_REF** is lower than the reference voltage, an alert bit is asserted. The nominal reference voltage is 1.2-V. Software applications can use this bit-detection to enable a system power-off sequence.
- Note that a low **PWC_PC_REF** voltage does not block wake-up events. Wake-up events will continue to function when the **PWC_PC_REF** voltage falls below the reference voltage.
- **PWC_PC_REF** should be maintained below 1.8 V.

2.4 PWC, RTC and Power-On: PWC / RTC Electrical Characteristics

Refer to the chip A12 datasheet for PWC and RTC electrical characteristics.

2.5 PWC, RTC and Power-On: External Power Control Module

For camera systems that lack a power-on/off button application, the use of an external Power Control Module (PCM) is recommended. The following are two A12 configuration examples in which an external PCM is used:

- Example 1: Use the internal RTC with an external PCM, pull low all PWC input pins, and leave the PWC output pins floating (unconnected).
- Example 2: Use an external RTC with an external PCM, and leave all PWC and RTC pins floating, including power pins on both blocks.

2.6 PWC, RTC and Power-On: RTC Disconnect

The RTC clock is typically maintained with one dedicated always-on power supply pin, so the clock remains active even when the core powers off. However, the RTC can be disconnected if not in use. Information regarding connection/disconnection of the RTC is provided below.

- Note that the RTC must be connected to run the PWC.
- If the RTC is active, the **XI_RTC**, **XO_RTC** and **PWC_RTC_CP** pins must be connected.
- If the RTC is not in use and the PWC is not required, the RTC power rails may be left unconnected (floating).

2.7 PWC, RTC and Power-On: PWC Disconnect

When running the A12 chip without the PWC:

- **PWC_PSEQ[1:3]** and **PWC_RSTOB** can be left unconnected (floating) when not in use.
- All other PWC pins should remain connected.

2.8 PWC, RTC and Power-On: Power-On / Off Sequence

This section describes the A12 power-on sequence, which uses only the power rails and related pins required for power-on. Refer to the "*A12 Hardware Programming Reference Manual*" for Power-On Configuration (POC) detail.

This section is organized as follows:

2.8.1 Power-On / Off: Power-On Sequence Pin Groups

The A12 power-on pins can be divided into three groups (1, 2 and 3), which should be powered up sequentially. These power-on sequence groups are shown in the table below.

Power-On Sequence Group	Pin Name
1	**HDMI_VDD10_[L]**
	LVDS_VDDA11 (Primary sensor in SLVS/MIPI Mode)
	USB_DVDD
	VDD_[L]
	VDDA10_PLL_[L]
2	**DDR_VDDQ_CKE /DDR_VDDQ**
	ADC_VDDA18
	HDMI_VDDA_[L]
	HDMI_AVDD25
	LVDS_VDDA11 (If primary sensor is in LVCMOS mode)
	LVDS_VDDA18_[L]
	USB_VDDA18_[L]
	VDAC_VDDA18
	VDDA18_PLL
	VDDP18_[L]
3	**ADC_VDDA33**
	HDMI_AVDDFLESD
	USB_VDDA33_[L]
	VDAC_VDDA33
	VDD33_[L]
	NAND_VDDO_[L]
	SD_VDDO_[L] / SDIO_VDDO_[L]

Table 2-1. Power-On-Sequence Groups for A12 Camera Applications.

Notes:

- When DDR Self-Refresh is enabled, **DDR_VDDQ_CKE** should remain powered when the chip is powered down. No external circuit is required.
- **DDR_VDDQ** and **DDR_VDDQ_CKE** rails as well as the 1.8-V rail for all 1.8-V domains can be turned ON/OFF simultaneously during power ON and OFF sequences.

2.8.2 Power-On / Off: Power-On Sequence Timing

The figure below illustrates the general timing for the A12 power-on sequence groups as defined in Table 2-1.

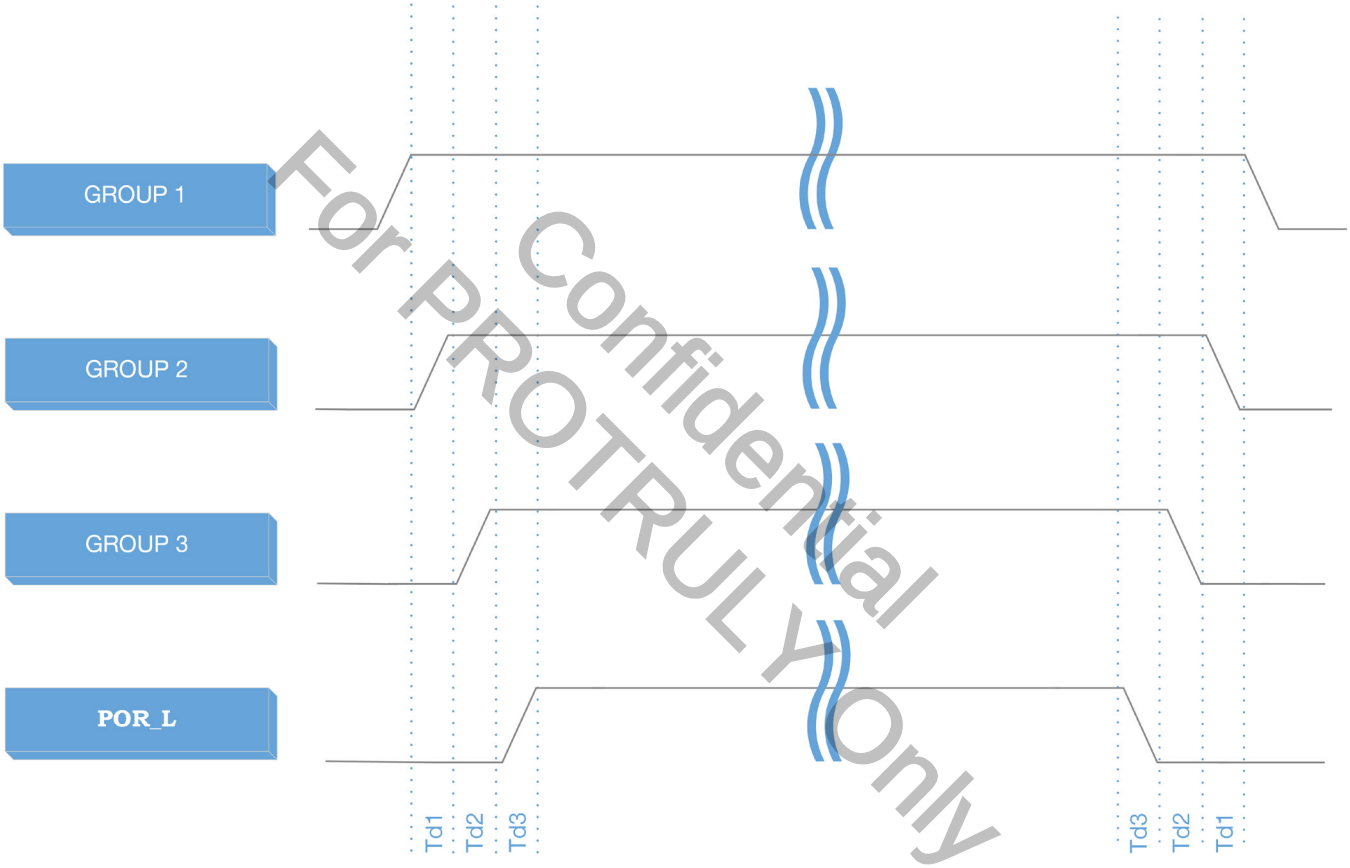

Figure 2-4. Power-On Sequence Timing for Power Rail Groups.

Notes:

- The global reset pin **POR_L** should be asserted (Low), then released or deasserted (High) after all power rails come up (Figure 2-4).
- The default time interval **Td** (Section 2.3.2) is 32 ms for any consecutive sequence. The actual value depends on the system-level design and is programmable by software for an embedded PWC module.
  - Timing per group (**Td1**, **Td2**, **Td3** and **POR_L**) should be maintained at 10 ms or more.
  - If the power ramp-up time exceeds 10 ms, the value of **Td** should be increased (Section 2.3.2).

The following figure illustrates a specific example showing the power-on sequence groups (Table 2-1) and sequence timing (Figure 2-4) for representative voltage levels and functional group names.

Note that the voltage levels shown in the diagram are relative and are provided for illustrative purposes only. Please refer to the chip A12 datasheet for the electrical characteristics of individual Ambarella chips.

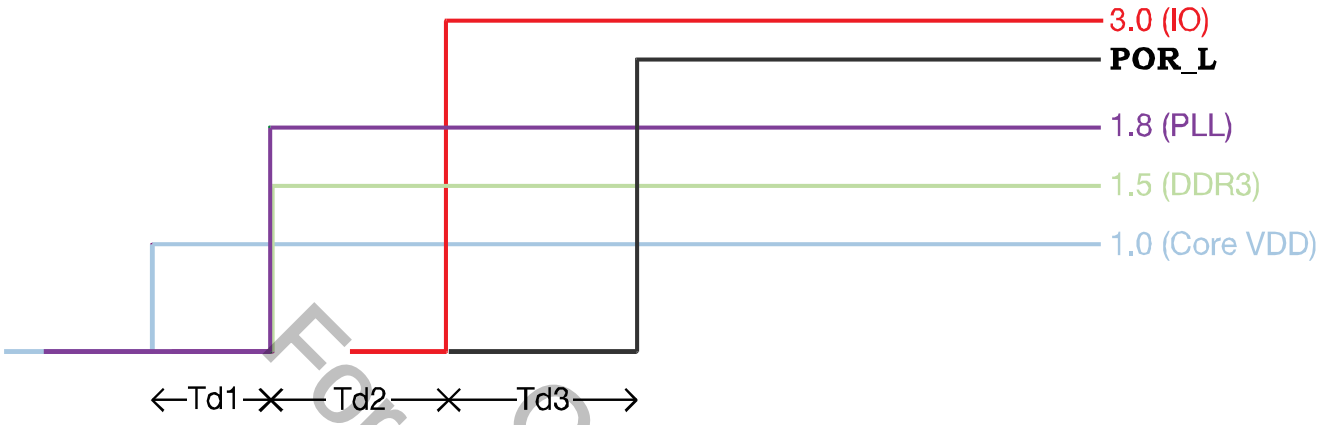

Figure 2-5. Power-On Sequence Timing Example with Representative Voltage and Functional Groups. (Please Refer to the Datasheet for Voltage Levels for Individual A12 Chips.)

In the above example, the power supplies are powered-up in the following sequence:

1. 1.0-V rails (Core VDD and associated 1.0-V power rails)
2. 1.5-V rails (DDR3) and 1.8-V rails (PLL)
3. 3.0-V rails (IO)
4. **POR_L** external reset pin

2.8.3 Power-On / Off: Power-Off Sequence

The power-off sequence is a reversal of the power-on sequence.

2.9 PWC, RTC and Power-On: External Clock Source for Core and Real-Time Clock

1. For core clock that is configured to 24 MHz via an external clock oscillator, connect the 24 MHz clock with 0V ~ 1.8V amplitude to XIN pins.
2. For core clock that is configured to 24 MHz via the built-in crystal oscillator, connect the 24 MHz crystal to the XIN/XOUT pins.
3. For the real-time clock (RTC) with 32.768 KHz frequency driven by an external clock oscillator, connect the 32.768 KHz clock with 0V ~ 1.8V amplitude to **XO_RTC** and tie **XI_RTC** to GND.

4. For the real-time clock (RTC) with 32.768 KHz frequency driven by a crystal oscillator, connect the 32.768 KHz crystal to **XO_RTC** and tie **XI_RTC** pins.

3. VIDEO INPUT

3.1 VIN: Overview

This chapter provides system hardware detail for the A12 Video Input (VIN) module. The chapter covers pin connections for the primary and secondary sensors, power and IO levels, flash strobe control, sync, termination, and VIN interface disconnect.

The chapter is organized as follows:

Primary Sensor Connections:

- (Section 3.2) VIN: Primary Video / Sensor LVCMOS Interface
- (Section 3.3) VIN: Primary Video / Sensor Sub-LVDS Interface
- (Section 3.4) VIN: Primary Video / Sensor SLVS Interface
- (Section 3.5) VIN: Primary Video / Sensor MIPI CSI Interface
- (Section 3.6) VIN: Primary Video / Sensor Fast External YUV Interface

Secondary Sensor Connections:

- (Section 3.7) VIN: Secondary Video / Sensor Interface

Power, IO, and Misc Details:

- (Section 3.8) VIN: Power and I/O Level
- (Section 3.9) VIN: Flash Strobe Control
- (Section 3.10) VIN: VIN_STRIG
- (Section 3.11) VIN: Sensor VSync Connection and Voltage Notice
- (Section 3.12) VIN: Termination
- (Section 3.13) VIN: Disconnect

3.2 VIN: Primary Video / Sensor LVCMOS Interface

This section provides information regarding the A12 LVCMOS interface.

- LVCMOS 8-, 10-, 12-, and 14-bit modes are supported
- The sensor input pins are mapped for LVCMOS use according to the table in Section 3.2.1.
- Refer to the A12 chip datasheet Chapter 2 for an implementation example.

3.2.1 Primary Sensor LVCMOS Mode: Pin Map

Pin Name	Sensor LVCMOS Single-End Parallel Interface			
	8 bits	10 bits	12 bits	14 bits
SD_LVDS_P_0	D0, LSB	D0, LSB	D0, LSB	D0, LSB
SD_LVDS_P_1	D1	D1	D1	D1
SD_LVDS_P_2	D2	D2	D2	D2
SD_LVDS_P_3	D3	D3	D3	D3
SD_LVDS_P_4	D4	D4	D4	D4
SD_LVDS_P_5	D5	D5	D5	D5
SD_LVDS_P_6	D6	D6	D6	D6
SD_LVDS_P_7	D7	D7	D7	D7
SD_LVDS_P_8				
SD_LVDS_P_9				
SD_LVDS_N_0		D8	D8	D8
SD_LVDS_N_1		D9	D9	D9
SD_LVDS_N_2			D10	D10
SD_LVDS_N_3			D11	D11
SD_LVDS_N_4				D12
SD_LVDS_N_5				D13
SD_LVDS_N_6				
SD_LVDS_N_7				
SD_LVDS_N_8				
SD_LVDS_N_9				
SPCLK_LVDS_P_0	SPCLK_IN	SPCLK_IN	SPCLK_IN	SPCLK_IN
SPCLK_LVDS_P_1	SFIELD_IN	SFIELD_IN	SFIELD_IN	SFIELD_IN
SPCLK_LVDS_P_2				
SPCLK_LVDS_N_0	HSYNC_IN	HSYNC_IN	HSYNC_IN	HSYNC_IN
SPCLK_LVDS_N_1	VSYNC_IN	VSYNC_IN	VSYNC_IN	VSYNC_IN
SPCLK_LVDS_N_2				
SHSYNC (output)	(HD, Sensor is slave)	(HD, Sensor is slave)	(HD, Sensor is slave)	(HD, Sensor is slave)
SVSYNC (output)	(VD, Sensor is slave)	(VD, Sensor is slave)	(VD, Sensor is slave)	(VD, Sensor is slave)

Table 3-1. LVCMOS Mapping for Sensor / Video Input Pins.

3.3 VIN: Primary Video / Sensor Sub-LVDS Interface

- A12 chips support sub-LVDS input with 8 or 10 data lanes.
- The sub-LVDS interface requires no external termination (refer to Section 3.1).
- Unused sub-LVDS input signals should be ganged and tied to ground. Software can be used to program these pins to LVCMOS mode to conserve power (refer to Section 3.12.1).
- The sensor input pins are mapped for sub-LVDS use according to the table in Section 3.2.1.
- Refer to the A12 chip datasheet Chapter 2 for an implementation example.

3.3.1 Primary Sensor Sub-LVDS Mode: Pin Map

Pin Name	Sensor Sub-LVDS Interface	
	8-Lane	10-Lane
SD_LVDS_P_0	D0_P	D0_P
SD_LVDS_P_1	D1_P	D1_P
SD_LVDS_P_2	D2_P	D2_P
SD_LVDS_P_3	D3_P	D3_P
SD_LVDS_P_4	D4_P	D4_P
SD_LVDS_P_5	D5_P	D5_P
SD_LVDS_P_6	D6_P	D6_P
SD_LVDS_P_7	D7_P	D7_P
SD_LVDS_P_8		D8_P
SD_LVDS_P_9		D9_P
SD_LVDS_N_0	D0_N	D0_N
SD_LVDS_N_1	D1_N	D1_N
SD_LVDS_N_2	D2_N	D2_N
SD_LVDS_N_3	D3_N	D3_N
SD_LVDS_N_4	D4_N	D4_N
SD_LVDS_N_5	D5_N	D5_N
SD_LVDS_N_6	D6_N	D6_N
SD_LVDS_N_7	D7_N	D7_N
SD_LVDS_N_8		D8_N
SD_LVDS_N_9		D9_N
SPCLK_LVDS_P_0	CLK_P	CLK_P
SPCLK_LVDS_P_1		
SPCLK_LVDS_P_2		
SPCLK_LVDS_N_0	CLK_N	CLK_N
SPCLK_LVDS_N_1		
SPCLK_LVDS_N_2		
SHSYNC (output)	(HD, Sensor is slave)	(HD, Sensor is slave)
SVSYNC (output)	(VD, Sensor is slave)	(VD, Sensor is slave)

Table 3-2. Sub-LVDS Mapping for Sensor / Video Input Pins.

3.4 VIN: Primary Video / Sensor SLVS Interface

- A12 chips support SLVS input with 1, 2, 4, or 8 data lanes. The chip also supports a single 10-lane SLVS sensor when the primary and secondary input channels are combined.
- The SLVS interface requires no external termination (see Section 3.1).
- Unused SLVS input signals should be ganged and tied to ground. Software can be used to program these pins to LVCMOS mode to conserve power (see Section 3.12.1)
- The sensor input pins are mapped for SLVS use according to the table in Section 3.4.1.
- Refer to the chip A12 datasheet Chapter 2 for an implementation example.

3.4.1 Primary Sensor SLVS Mode: Pin Map

Pin Name	Sensor SLVS Serial Interface				
	1-Lane	2-Lane	4-Lane	8-Lane	10-Lane
SD_LVDS_P_0	D0_P	D0_P	D0_P	D0_P	D0_P
SD_LVDS_P_1		D1_P	D1_P	D1_P	D1_P
SD_LVDS_P_2			D2_P	D2_P	D2_P
SD_LVDS_P_3			D3_P	D3_P	D3_P
SD_LVDS_P_4				D4_P	D4_P
SD_LVDS_P_5				D5_P	D5_P
SD_LVDS_P_6				D6_P	D6_P
SD_LVDS_P_7				D7_P	D7_P
SD_LVDS_P_8					D8_P
SD_LVDS_P_9					D9_P
SD_LVDS_N_0	D0_N	D0_N	D0_N	D0_N	D0_N
SD_LVDS_N_1		D1_N	D1_N	D1_N	D1_N
SD_LVDS_N_2			D2_N	D2_N	D2_N
SD_LVDS_N_3			D3_N	D3_N	D3_N
SD_LVDS_N_4				D4_N	D4_N
SD_LVDS_N_5				D5_N	D5_N
SD_LVDS_N_6				D6_N	D6_N
SD_LVDS_N_7				D7_N	D7_N
SD_LVDS_N_8					D8_N
SD_LVDS_N_9					D9_N
SPCLK_LVDS_P_0	CLK_P	CLK_P	CLK_P	CLK_P	CLK_P
SPCLK_LVDS_P_1				(CLK1_P)	(CLK1_P)
SPCLK_LVDS_P_2					(CLK2_P)
SPCLK_LVDS_N_0	CLK_N	CLK_N	CLK_N	CLK_N	CLK_N
SPCLK_LVDS_N_1				(CLK1_N)	(CLK1_N)
SPCLK_LVDS_N_2					(CLK2_N)
SHSYNC (output)	(HD, Sensor is slave)	(HD, Sensor is slave)	(HD, Sensor is slave)	(HD, Sensor is slave)	(HD, Sensor is slave)
SVSYNC (output)	(VD, Sensor is slave)	(VD, Sensor is slave)	(VD, Sensor is slave)	(VD, Sensor is slave)	(VD, Sensor is slave)

Table 3-3. SLVS Mapping for Sensor / Video Input Pins.

Note:

- The skew between **SPCLK_LVDS_P/N_0/1/2** must be maintained at less than 600 ps.

3.5 VIN: Primary Video / Sensor MIPI CSI Interface

- A12 chips support 1-, 2- and 4-lane MIPI Camera Serial Interface (CSI) input.
- The MIPI CSI interface requires no external termination.
- Unused input signals should be tied to ground. Software can be used to program these pins to LVC-MOS mode to conserve power.
- The sensor input pins are mapped for MIPI CSI according to the table in Section 3.5.1.
- Refer to the A12 chip datasheet Chapter 2 for an implementation example.

3.5.1 Primary Sensor MIPI CSI Mode: Pin Map

Pin Name	MIPI CSI Data		
	1-Lane	2-Lane	4-Lane
SD_LVDS_P_0	D0_P	D0_P	D0_P
SD_LVDS_P_1		D1_P	D1_P
SD_LVDS_P_2			D2_P
SD_LVDS_P_3			D3_P
SD_LVDS_P_4			
SD_LVDS_P_5			
SD_LVDS_P_6			
SD_LVDS_P_7			
SD_LVDS_P_8			
SD_LVDS_P_9			
SD_LVDS_N_0	D0_N	D0_N	D0_N
SD_LVDS_N_1		D1_N	D1_N
SD_LVDS_N_2			D2_N
SD_LVDS_N_3			D3_N
SD_LVDS_N_4			
SD_LVDS_N_5			
SD_LVDS_N_6			
SD_LVDS_N_7			
SD_LVDS_N_8			
SD_LVDS_N_9			
SPCLK_LVDS_P_0	CLK_P	CLK_P	CLK_P
SPCLK_LVDS_P_1			
SPCLK_LVDS_P_2			
SPCLK_LVDS_N_0	CLK_N	CLK_N	CLK_N
SPCLK_LVDS_N_1			
SPCLK_LVDS_N_2			

Pin Name	MIPI CSI Data		
	1-Lane	2-Lane	4-Lane
SHSYNC (output)			
SVSYNC (output)			

Table 3-4. MIPI CSI Mapping for Sensor Input Pins.

3.6 VIN: Primary Video / Sensor Fast External YUV Interface

- A12 chips support 8-bit and 16-bit YUV input.
- A12 8-bit mode supports external sync.
- A12 16-bit mode supports only embedded sync; i.e., there is no pin assignment for HSYNC and VSYNC.
- Unused input signals should be tied to ground. Software can be used to program these pins to LVC-MOS mode to conserve power.
- The sensor input pins are mapped for fast external YUV input according to the table in Section 3.6.1.
- Refer to the A12 chip datasheet Chapter 2 for an implementation example.

3.6.1 Primary Sensor YUV Mode: Pin Map

Pin Name	YUV Data	
	8-bit	16-bit
SD_LVDS_P_0	D0	D0
SD_LVDS_P_1	D1	D1
SD_LVDS_P_2	D2	D2
SD_LVDS_P_3	D3	D3
SD_LVDS_P_4	D4	D4
SD_LVDS_P_5	D5	D5
SD_LVDS_P_6	D6	D6
SD_LVDS_P_7	D7	D7
SD_LVDS_P_8		
SD_LVDS_P_9		
SD_LVDS_N_0		D8
SD_LVDS_N_1		D9
SD_LVDS_N_2		D10
SD_LVDS_N_3		D11
SD_LVDS_N_4		D12
SD_LVDS_N_5		D13
SD_LVDS_N_6		D14
SD_LVDS_N_7		D15
SD_LVDS_N_8		
SD_LVDS_N_9		
SPCLK_LVDS_P_0	SPCLK_IN	SPCLK_IN
SPCLK_LVDS_P_1	SFIELD_IN	SFIELD_IN
SPCLK_LVDS_P_2		
SPCLK_LVDS_N_0	HSYNC_IN	HSYNC_IN
SPCLK_LVDS_N_1	VSYNC_IN	VSYNC_IN
SPCLK_LVDS_N_2		
SHSYNC (output)		
SVSYNC (output)		

Table 3-5. Sensor / Video Input Pins in Fast External YUV Input Mode.

3.7 VIN: Secondary Video / Sensor Interface

- The A12 secondary VIN interface supports up to 2-lane SLVS / HiSPi / MIPI inputs. The chip can also support a single 10-lane SLVS sensor when the primary and secondary input channels are combined.
- The secondary VIN input pins are mapped according to the table in Section 3.2.1.
- When the secondary VIN interface is active, the primary VIN uses data lanes **SD_LVDS_N_[0:7]** and **SD_LVDS_P_[0:7]**.

3.7.1 Secondary Sensor Interface: Pin Map

Pin Name	Secondary VIN Interface Data	
	1-Lane	2-Lane
SD_LVDS_P_8	D8_P	D8_P
SD_LVDS_P_9		D9_P
SD_LVDS_N_8	D8_N	D8_N
SD_LVDS_N_9		D9_N
SPCLK_LVDS_P_2	CLK_P	CLK_P
SPCLK_LVDS_N_2	CLK_N	CLK_N

Table 3-6. Mapping for Secondary Sensor Interface Input Pins.

3.8 VIN: Power and I/O Level

The sensor power and IO levels are described in the table below:

Mode	Power Rail	
	LVDS_VDDA18[L]	LVDS_VDDA11
Sub-LVDS (Primary Sensor)	1.8 V	1.0 V
SLVS (Primary Sensor)	1.8 V	1.0 V
LVCMOS (Primary Sensor)	1.8 V	1.8 V
Fast External YUV (Primary Sensor)	1.8 V	1.8 V
MIPI CSI (Primary Sensor)	1.8 V	1.0 V
Secondary Sensor (SLVS Mode)	1.8 V	1.0 V or 1.8 V
Secondary Sensor (MIPI Mode)	1.8 V	1.0 V

Table 3-7. VIN Power Rails.

Notes:

- If the primary VIN interface is in LVCMOS mode, only SLVS sensors are supported for the secondary VIN interface.
- Note that A12 offers 1.0-V and 1.8-V video input modes and does not support 3.3-V sensor interface power. Refer to the A12 chip datasheet for operating range and additional electrical characteristics.

3.9 VIN: Flash Strobe Control

The A12 flash strobe is controlled using stepper control functions. Refer to the "*A12 Hardware Programming Reference Manual*" for information regarding the stepper controller interface.

3.10 VIN: VIN_STRIG

VIN_STRIG may be used to debug the VIN status. It is recommended to reserve the test point for VIN/STRIG to 0 or 1 in order to do so.

3.11 VIN: Sensor VSync Connection and Voltage Notice

Sensor operation modes and characteristics vary with sensor design. When configuring VSync signal connections (e.g., sensor vertical sync, frame sync, or frame valid) between the A12 chip and an associated sensor, please note that a high degree of care should be exercised.

3.12 VIN: Termination

The receiver (A12 side) of the A12 Sub-LVDS interface provides a built-in 100-Ohm termination. This eliminates the need to incorporate termination resistors in the external circuit during PCB design.

3.13 VIN: Disconnect

When running the A12 chip without the Video / Sensor interface:

- Input pins **SD_LVDS_N/P_[0:9]** and **SPCLK_LVDS_N/P_[0:2]** can be ganged and connected to ground if not used.
- Output pins **SHSYNC** and **SVSYNC** may be left unconnected (floating).

4. VIDEO OUTPUT

4.1 VOUT: Overview

This chapter provides system hardware detail for the A12 Video Output (VOUT) interfaces. The chapter is organized as follows:

See Also:

- The A12 chip datasheet provides additional VOUT interface and pin-related information.
- The "*A12 Hardware Programming Reference Manual*" includes analog and digital VOUT register programming detail.

4.2 VOUT: Interfaces

The Video Output (VOUT) interface supports one digital video output, one CVBS analog output, and one HDMI output. The output ports are on two logical video channels as shown in the diagram below.

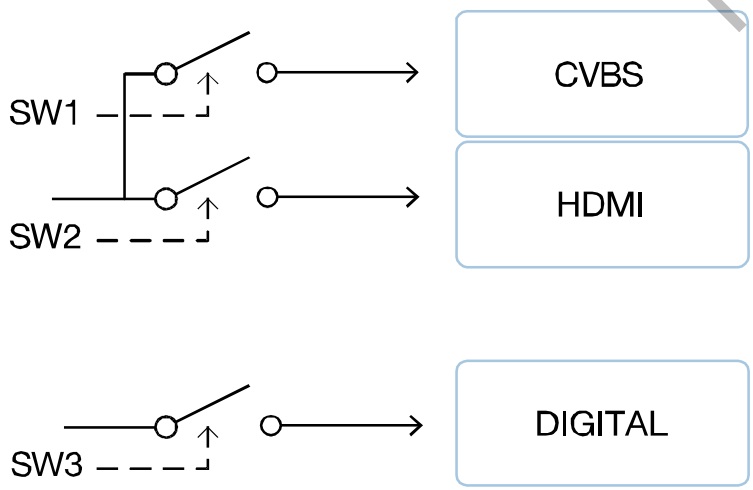

Figure 4-1. A12 Video Output Channels and Ports.

Refer to the chip A12 datasheet for information regarding the supported video output resolutions.

4.3 VOUT: Digital

A12 digital video output is covered in this section as follows:

- (Section 4.3.1) Digital VOUT: Pins
- (Section 4.3.2) Digital VOUT: Formats

4.3.1 Digital VOUT: Pins

The A12 digital video output pins are used for power-on configuration (POC) and are multiplexed with GPIO functionality. Please refer to the A12 chip datasheet and the "*A12 Hardware Programming Reference Manual*" for complete information regarding A12 VOUT pin capabilities.

4.3.2 Digital VOUT: Formats

The A12 digital video output port is dedicated for LCD display (preview screen) usage. The A12 chip supports various digital output modes as described in the following table.

Pin	Digital RGB [1] (Mode 0, 1, 2)	5:6:5 RGB [2] (Mode 3)	8-bit [3] 656 YCbCr (Mode 4)	16-bt [4] 601/656 YCbCr (Mode 4, 5)
VD0_OUT0	Interleaved R/G/B, LSB	Blue, LSB	Interleaved Y/C, LSB	Y, LSB
VD0_OUT1	Interleaved R/G/B	Blue	Interleaved Y/C	Y
VD0_OUT2	Interleaved R/G/B	Blue	Interleaved Y/C	Y
VD0_OUT3	Interleaved R/G/B	Blue	Interleaved Y/C	Y
VD0_OUT4	Interleaved R/G/B	Blue, MSB	Interleaved Y/C	Y
VD0_OUT5	Interleaved R/G/B	Green, LSB	Interleaved Y/C	Y
VD0_OUT6	Interleaved R/G/B	Green	Interleaved Y/C	Y
VD0_OUT7	Interleaved R/G/B, MSB	Green	Interleaved Y/C, MSB	Y, MSB
VD0_OUT8		Green		Interleaved Cb/Cr, LSB
VD0_OUT9		Green		Interleaved Cb/Cr
VD0_OUT10		Green, MSB		Interleaved Cb/Cr
VD0_OUT11		Red, LSB		Interleaved Cb/Cr
VD0_OUT12		Red		Interleaved Cb/Cr
VD0_OUT13		Red		Interleaved Cb/Cr
VD0_OUT14		Red		Interleaved Cb/Cr
VD0_OUT15		Red, MSB		Interleaved Cb/Cr, MSB
VD0_HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VD0_VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
VD0_CLK	PIXCLK	PIXCLK	PIXCLK	PIXCLK
VD0_HVLD	(DE)	(DE)	DE	DE

Table 4-1. A12 Digital Video Output Formats.

Notes:

1. Digital RGB Mode corresponds to Video Output Modes 0/1/2 for 8-bit output to the LCD.
2. 5:6:5 RGB Mode corresponds to Video Output Mode 3 for 16-bit RGB output to the LCD.
3. 656 YCbCr Mode corresponds to Video Output Mode 4 for D1--480i and 576--resolution. Output data rate is 13.5 MHz. Output Clock rate is 27 MHz. 4:2:2 output format.
4. 16-bit 656-YCbCr Mode (Video Output Mode 4) and 16-bit 601-YCbCr Mode (Video Output Mode 5). 4:2:2 output format.

4.4 VOUT: Analog

The A12 video Digital-to-Analog Converter (DAC) drives standard-definition composite video output. Please refer to the A12 chip datasheet and the "*A12 Hardware Programming Reference Manual*" for complete information regarding the A12 DAC pins.

4.5 VOUT: HDMI

The A12 chip includes an embedded HDMI 1.4b-compliant transmitter, which enables three lanes of differential TMDS data and one clock lane with an additional two-wire IDC setup for secure key transfer. This section discusses the A12 HDMI interface as follows:

4.5.1 HDMI: Pins

Please refer to the A12 chip datasheet and the "*A12 Hardware Programming Reference Manual*" for complete information regarding the A12 HDMI and IDC pins.

4.5.2 HDMI: Recommended Circuit

A recommended circuit model for the A12 HDMI interface is shown in Figure 4-2 on the following page.

When creating a connection to a television, increase the tolerance to 5 V using a metal-oxide-semiconductor field-effect transistor (MOSFET). The circuit shown in Figure 4-2 uses an N-Channel Enhancement Mode MOSFET (part number APM2324) to achieve compliance by reducing leakage on the CEC path between the A12 chip (CEC pin) and the HDMI connector (CEC connection).

Note that the IDC channel is 3.3-V tolerant by design.

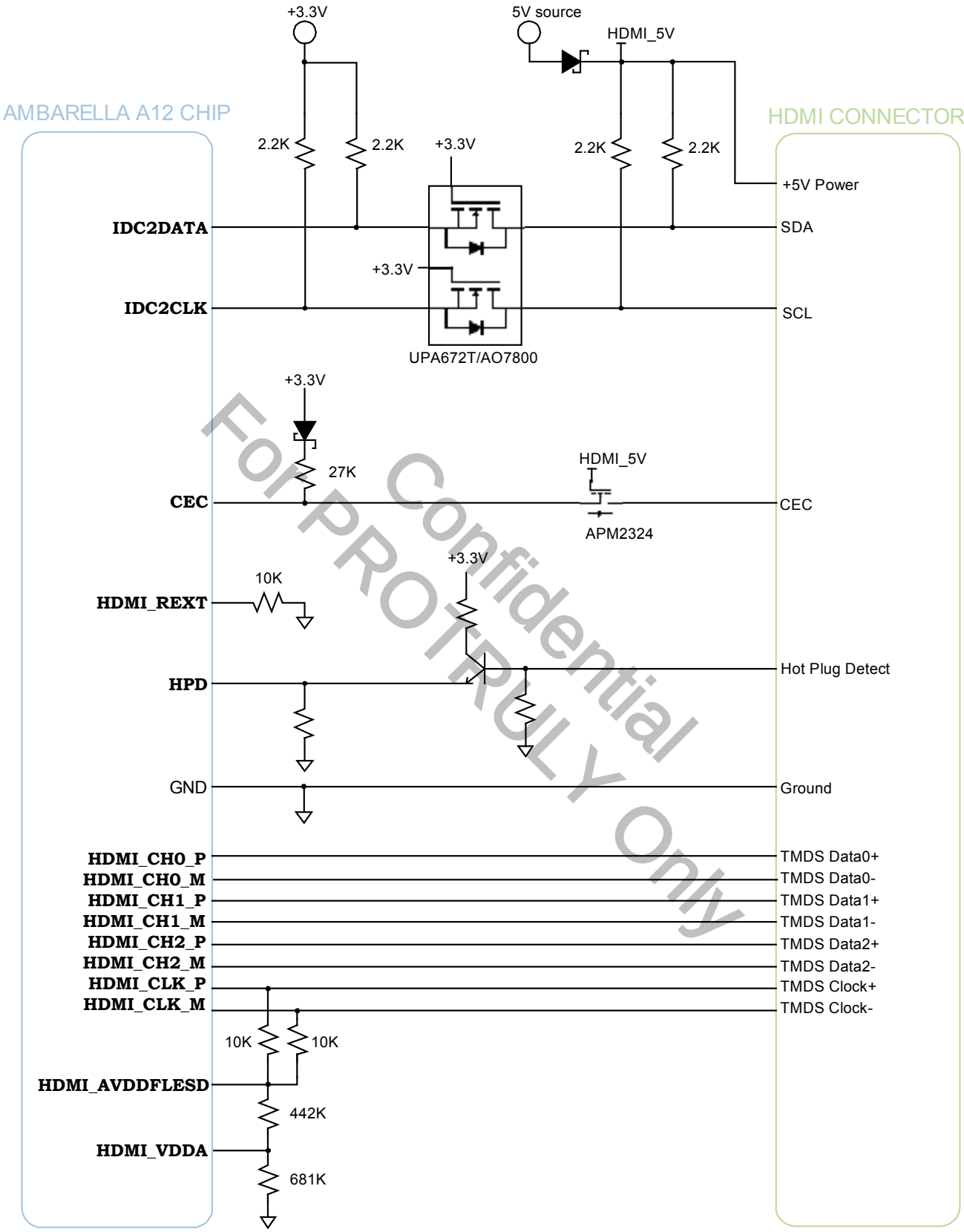

Figure 4-2. Recommended Circuit for HDMI TV Connection.

4.6 VOUT: Disconnect

4.6.1 Disconnect: Digital Video

When running the A12 chip without digital video output:

- Digital video output pins **VD0_CLK**, **VD0_HSYNC**, **VD0_VSYNC**, **VD0_HVLD** and **VD0_OUT_[0:15]** can be left floating.
- The A12 digital video output pins are used for power-on configuration (POC) as described in the "*A12 Hardware Programming Reference Manual*". If the A12 chip is run without the digital video output interface, then power-on configuration should be performed via eFUSE ROM.

4.6.2 Disconnect: DAC

When running the A12 chip without the DAC module:

- Analog power pins **VDAC_VDDA18** and **VDAC_VDDA33** may be left unconnected (floating).
- **VDAC_VSSA** should be tied to ground.
- All other DAC pins **(DAC_COMP, DAC_IO, DAC_RSET** and **DAC_VREFIN)** may also be left unconnected (floating).

4.6.3 Disconnect: HDMI

When running the A12 chip without the HDMI interface:

- The power / ground pins **HDMI_VDD10_[L]**, **HDMI_VDDA_[L]**, **HDMI_VSSA_[L]** and the **HDMI_REXT** pin must remain connected at all times.
- **HDMI_AVDD25** may be left unconnected (floating).
- The electrostatic discharge pin **HDMI_AVDDFLESD** may be left unconnected (floating).
- Analog I/O pins **HDMI_CH[N]_P/M** may be left unconnected (floating).
- CMOS I/O pins **CEC** and **HPD** should be pulled-down individually using resistors.
- The IDC2 functions **IDC2CLK** and **IDC2DATA** are on GPIO pins and are individually pulled up/down with register programming.

5. GENERAL PURPOSE INPUT / OUTPUT PINS

5.1 GPIO: Overview

This chapter provides system hardware detail for A12 multi-function general purpose input / output (GPIO) pins. The chapter is organized as follows:

See Also:

- The A12 chip datasheet provides a complete multi-function pin list, including map locations.
- The "*A12 Hardware Programming Reference Manual*" contains GPIO register programming detail.

5.2 GPIO: Characteristics

- There are 114 GPIO pins included on A12 SoCs, each with multi-function capabilities.
- A12 GPIO pins are:
  - CMOS type and programmable input / output
  - Interrupt-capable
  - Initialized to be inputs during reset assertion
  - Bidirectional under software control

5.3 GPIO: IO and Pull-High/Low Defaults

The table below provides the default input / output direction and pull-high / low characteristics for the A12 GPIO pins. Refer to the A12 chip datasheet for a full list of functions and descriptions.

GPIO	Pin Name	Primary Function	Input / Output (Default)	Pull High / Low (Default)
0	**GPIO_0**	sd_hs_sel	Input	Pull High
1	**GPIO_1**	ehci_app_prt_ovcurr0	Input	Pull High
2	**GPIO_2**	ehci_app_prt_ovcurr1	Input	Pull High
3	**GPIO_3**	ehci_prt_pwr_0	Input	Pull High
4	**GPIO_4**	ehci_prt_pwr_1	Input	Pull High
5	**GPIO_5**	pwm_1	Input	Pull High
6	**GPIO_6**	pwm_2	Input	Pull High
7	**SC_A0**	sc_a0	OutputX	Pull High
8	**SC_A1**	sc_a1	OutputX	Pull High
9	**SC_A2**	sc_a2	OutputX	Pull High
10	**SC_A3**	sc_a3	OutputX	Pull High
11	**SC_B0**	sc_b0	OutputX	Pull High
12	**SC_B1**	sc_b1	OutputX	Pull High
13	**SC_B2**	sc_b2	OutputX	Pull High
14	**SC_B3**	sc_b3	Input	Pull High
15	**SC_C0**	sc_c0	Input	Pull High
16	**SC_C1**	sc_c1	Input	Pull High
17	**SC_C2**	sc_c2	Input	Pull High
18	**SC_C3**	sc_c3	Input	Pull High
19	**SC_D0**	sc_d0	Input	Pull High
20	**SC_D1**	sc_d1	Input	Pull High
21	**SC_D2**	sc_d2	Input	Pull High
22	**SC_D3**	sc_d3	Input	Pull High
23	**SC_E0**	sc_e0	Input	Pull High
24	**TIMER0**	tm11_clk	Input	Pull High
25	**TIMER1**	tm12_clk	Input	Pull High
26	**TIMER2**	tm13_clk	Input	Pull High
27	**IDCCLK**	idc0clk	Input	No Drive
28	**IDCDATA**	idc0data	Input	No Drive
29	**IDC2CLK**	idc1clk	Input	No Drive
30	**IDC2DATA**	idc1data	Input	No Drive
31	**IDC3CLK**	idc2clk	Input	No Drive
32	**IDC3DATA**	idc2data	Input	No Drive
33	**IR_IN**	ir_in	Input	Pull High
34	**SSI0CLK**	ssi0_sclk	Input	No Drive
35	**SSI0MOSI**	ssi0_txd	Input	No Drive
36	**SSI0MISO**	ssi0_rxd	Input	No Drive
37	**SSI0EN0**	ssi0_en0	Input	Pull High
38	**SSI0EN1**	ssi0_en1	Input	Pull High
39	**UART0RX**	uart0rx	Input	Pull High
40	**UART0TX**	uart0tx	Input	Pull High
41	**I2S_CLK**	i2s_clk	Input	Pull High

GPIO	Pin Name	Primary Function	Input / Output (Default)	Pull High / Low (Default)
42	**I2S_SI**	i2s_si	Input	Pull High
43	**I2S_SO**	i2s_so	Input	No Drive
44	**I2S_WS**	i2s_ws	Input	Pull High
45	**CLK_AU**		Input	No Drive
46	**ENET_TXEN**	enet_txen	Input	No Drive
47	**ENET_TXD_0**	enet_txd_0	Input	No Drive
48	**ENET_TXD_1**	enet_txd_1	Input	No Drive
49	**ENET_RXD_0**	enet_rxd_0	Input	No Drive
50	**ENET_RXD_1**	enet_rxd_1	Input	No Drive
51	**ENET_RX_ER**	enet_rxer	Input	No Drive
52	**ENET_CRS_DV**	enet_crs_dv	Input	No Drive
53	**ENET_REF_CLK**	enet_ref_clk	Input	No Drive
54	**WP**		Input	No Drive
55	**SMIO_0**		Output 1	Pull Disabled
56	**SMIO_1**		Input	No Drive
57	**SMIO_2**		Input	No Drive
58	**SMIO_3**		Input	Pull High
59	**SMIO_4**		Input	No Drive
60	**SMIO_5**		Input	Pull High
61	**SMIO_6**		Output 1	Pull Disabled
62	**SMIO_7**		Output 1	Pull Disabled
63	**SMIO_8**		Input	No Drive
64	**SMIO_9**		Input	No Drive
65	**SMIO_10**		Input	No Drive
66	**SMIO_11**		Input	No Drive
67	**SMIO_12**		Input	No Drive
68	**SMIO_13**		Input	No Drive
69	**SMIO_14**		Input	No Drive
70	**SMIO_15**		Input	No Drive
71	**SMIO_16**		Input	No Drive
72	**SMIO_17**		Input	No Drive
73	**SMIO_18**		Input	Pull High
74	**SMIO_19**		Input	Pull High
75	**SMIO_20**		Input	Pull High
76	**SMIO_21**		Input	Pull High
77	**SMIO_22**		Input	Pull High
78	**SMIO_23**		Input	Pull High
79	**SMIO_24**		Input	Pull High
80	**SMIO_25**		Input	Pull High
81	**SMIO_26**		Input	No Drive
82	**SMIO_27**		Input	Pull High
83	**SMIO_28**		Input	Pull High
84	**SMIO_29**		Input	Pull High
85	**SMIO_30**		Input	Pull High
86	**SMIO_31**		Input	Pull High

GPIO	Pin Name	Primary Function	Input / Output (Default)	Pull High / Low (Default)
87	**SMIO_32**		Input	No Drive
88	**SMIO_33**		Input	Pull High
89	**HPD**	hdmitx_hpd	Input	No Drive
90	**CEC**	hdmitx_cec	Input	No Drive
91	**SVSYNC**	vin_svsync	Input	Pull High
92	**SHSYNC**	vin_shsync	Input	Pull High
93	**VD0_OUT_0**	vd0_out[0]	Input	No Drive
94	**VD0_OUT_1**	vd0_out[1]	Input	No Drive
95	**VD0_OUT_2**	vd0_out[2]	Input	No Drive
96	**VD0_OUT_3**	vd0_out[3]	Input	No Drive
97	**VD0_OUT_4**	vd0_out[4]	Input	No Drive
98	**VD0_OUT_5**	vd0_out[5]	Input	No Drive
99	**VD0_OUT_6**	vd0_out[6]	Input	No Drive
100	**VD0_OUT_7**	vd0_out[7]	Input	No Drive
101	**VD0_OUT_8**	vd0_out[8]	Input	No Drive
102	**VD0_OUT_9**	vd0_out[9]	Input	No Drive
103	**VD0_OUT_10**	vd0_out[10]	Input	No Drive
104	**VD0_OUT_11**	vd0_out[11]	Input	No Drive
105	**VD0_OUT_12**	vd0_out[12]	Input	No Drive
106	**VD0_OUT_13**	vd0_out[13]	Input	No Drive
107	**VD0_OUT_14**	vd0_out[14]	Input	No Drive
108	**VD0_OUT_15**	vd0_out[15]	Input	No Drive
109	**VD0_CLK**	vd0_clk	Input	No Drive
110	**VD0_VSYNC**	vd0_vsync	Input	No Drive
111	**VD0_HSYNC**	vd0_hsync	Input	No Drive
112	**VD0_HVLD**	vd0_hvld	Input	No Drive
113	**VD_PWM**	pwm_0	Input	No Drive

Table 5-1. General Purpose Input Output (GPIO) Pin Default Characteristics.

Notes:

1. The typical pull-high (deasserted) and pull-low (asserted) characteristics for A12 GPIO pins are as follows:

Characteristic	Pull-High, Pull-Low Resistance		
Parameter	Worst	Typical	Best
	3.00 V	3.30 V	3.60 V
	T=125 ºC	T=25 ºC	T=40 ºC
	Process=Slow	Process=Nominal	Process=Fast
Pull-High	145K Ohms	80K Ohms	46K Ohms
Pull-Low	162K Ohms	85K Ohms	49K Ohms

Table 5-2. GPIO Pull High/Low Characteristics.

5.4 GPIO: SD Interface Pull-High/Low Requirements

SD Interface Type	SD Card	WiFi	eMMC	Unused
sd / sdio_cd	Pull-High	Floating	Pull-Low	Pull-High
sd / sdio_wp	Depends on SD socket structure	Floating	Pull-Low	Pull-High

Table 5-3. GPIO: SD Interface Pull-High/Low Control.

Note:

- The pull-high/low state should be controlled by external resistor.

5.5 GPIO: Disconnect

Multi-function GPIO pins are used to enable various interfaces and functions on the A12 chip including video output, UART, interval timers, and more. Selection, control, and disconnection of these functions is performed via software.

Refer to the "*A12 Hardware Programming Reference Manual*" for GPIO register programming and function selection detail.

5.6 GPIO: Implementing USB Host Function

To implement the USB host function, GPIO1 and GPIO2 must be programmed to the hardware function (overcurrent protection) and pulled low.

6. ETHERNET

6.1 Ethernet: Overview

This chapter summarizes the A12 Ethernet interface as follows:

- (Section 6.2) Ethernet: Pins
- (Section 6.3) Ethernet: Disconnect

See Also:

- The A12 chip datasheet contains complete Ethernet interface and pin details.
- The "*A12 Hardware Programming Reference Manual*" includes power-on configuration detail for the Ethernet interface.

6.2 Ethernet: Pins

Note that **ENET_REF_CLK** is output only when RMII is active. The Ethernet PHY side must support input with respect to this clock.

Please refer to the A12 chip datasheet and the "*A12 Hardware Programming Reference Manual*" for complete information regarding A12 Ethernet pin functionality.

6.3 Ethernet: Disconnect

The A12 Ethernet interface uses multi-function GPIO pins. Selection, control, and disconnection of these functions is performed via software.

7. IDC PORTS

7.1 IDC: Overview

This chapter summarizes the A12 IDC and SSI / SPI ports as follows:

- (Section 7.2) IDC Ports

See Also:

- The A12 chip datasheet contains comprehensive IDC interface and pin details.
- The "*A12 Hardware Programming Reference Manual*" includes register programming information for the IDC interface.

7.2 IDC Ports

The IDC interfaces control a two-wire, bi-directional bus that provides data communication between the chip and peripheral devices with protocol speeds up to 400 Kbps. The chip includes a total of three IDC ports. All of the A12 IDC interfaces support single-master mode.

Note that the timing margin for IDC interfaces 1 and 3 is critical. When supporting multiple IDC devices, a 100-pF capacitor must be added to the **IDC_CLK** line to delay the clock.

8. ANALOG TO DIGITAL CONVERSION

8.1 ADC: Overview

This chapter provides system hardware detail for the Analog-to-Digital Converter (ADC) on the A12 chip. The chapter is organized as follows:

- (Section 8.2) ADC: Channel Requirements
- (Section 8.3) ADC: Disconnect

See Also:

- The A12 chip datasheet contains comprehensive ADC interface and pin information.
- The "*A12 Hardware Programming Reference Manual*" includes ADC register programming information.

8.2 ADC: Channel Requirements

The A12 chip includes a four-channel Analog-to-Digital Converter (ADC). The input range is programmable through external pins. The dynamic range is shown in the table below.

Pin Name	Type	Electrical
ADC_CH_0	Input	Input range: 0 to 1.8 V
ADC_CH_1	Input	Input range: 0 to 3.3 V
ADC_CH_2		
ADC_CH_3		
ADC_VDDA18	Analog Power Supply	ADC analog power supply
ADC_VDDA33	Analog Ground	ADC analog power supply
ADC_VSSA	Analog Ground	ADC analog ground

Table 8-1. Electrical Requirements for A12 ADC Channels.

Notes:

- Input should not exceed the electrical range stated above.

8.3 ADC: Disconnect

When running the A12 chip without the ADC interface:

- Core power / ground rails must remain connected at all times.
- **ADC_CH0** should be grounded.
- Analog supply / ground pins **ADC_VDDA18** and **ADC_VSSA** should be tied down.
- Analog supply pin **ADC_VDDA33** may be left unconnected (floating).
- All other ADC pins may be left unconnected (floating).

9. JTAG AND UART INTERFACES

9.1 JTAG and UART: Overview

This chapter covers the A12 JTAG and UART interfaces as follows:

- (Section 9.2) JTAG and UART: JTAG
- (Section 9.3) JTAG and UART: UART
- (Section 9.4) JTAG and UART: Disconnect

See Also:

- The A12 chip datasheet contains comprehensive interface and pin detail.
- The "*A12 Hardware Programming Reference Manual*" provides register programming information.

9.2 JTAG and UART: JTAG

The A12 chip includes an interface for a JTAG In-Circuit Emulator (ICE). This is primarily used for debugging purposes. Information regarding the JTAG interface is provided below.

- JTAG chaining is not supported.
- The **JTAG_CLK** pin should be pulled low.
- The reset pin **JTAG_RST_L** should be pulled low during the power-up period.
- **JTAG_TDI** / **JTAG_TMS** should be pulled high to save power (and to avoid power leakage).

9.3 JTAG and UART: UART

The A12 chip includes two industry-standard 16550 UART programming interfaces (UART0 and UART1).

- UART1 supports hardware flow control and may be used to communicate with external devices.
- The UART0 interface is generally used for debugging purposes and does not provide hardware flow control.
  - The software transmits debug-related information through UART0 for print-out on the serial console. To increase system robustness after the debug board is removed, pull-up or pull-down the Tx / Rx signals to eliminate unwanted noise/crosstalk (and unexpected interrupts).
  - The UART0 interrupt should be disabled after system development is completed. While this eliminates debugging output through UART0, it increases system robustness and is therefore recommended.

9.4 JTAG and UART: Disconnect

9.4.1 Disconnect: JTAG

When running the A12 chip without the JTAG interface:

- Pull-up the **JTAG_TMS** and **JTAG_TDI** input pins.
- Pull-down the **JTAG_CLK** and **JTAG_RST** input pins.
- Leave the output pin **JTAG_TDO** unconnected (floating).

9.4.2 Disconnect: UART

The UART interfaces are enabled with multi-function GPIO pins. Selection, control, and disconnection of these functions is performed via software.

- Individual GPIO functions are selected via register programming.
- The GPIO pins are individually pulled up/down using register programming.

Refer to the "*A12 Hardware Programming Reference Manual*" for details.

10. PCB LAYOUT REFERENCE

10.1 PCB Layout: Overview

This chapter provides A12 PCB layout information as a reference to be considered during board development. Note that actual PCB layouts are strongly application-dependent, and designs should be based on a variety of factors including PCB stack-up parameters and SI simulations.

Also note that Ambarella provides qualified customers with hardware reference designs to aid in board layout and development, as well as design review services. It is expected that users will both refer to Ambarella-provided reference designs and consult directly with an Ambarella representative during product development efforts.

The chapter is organized as follows:

10.2 PCB Layout: DRAM

PCB layout guidelines for DRAM are provided in this section as follows:

Contact an Ambarella representative for assistance in selecting a qualified DRAM component.

10.2.1 DRAM: Placement

The following is a diagram roughly illustrating the recommended placement of DRAM modules relative to the A12 SoC. Please contact an Ambarella representative for further detail.

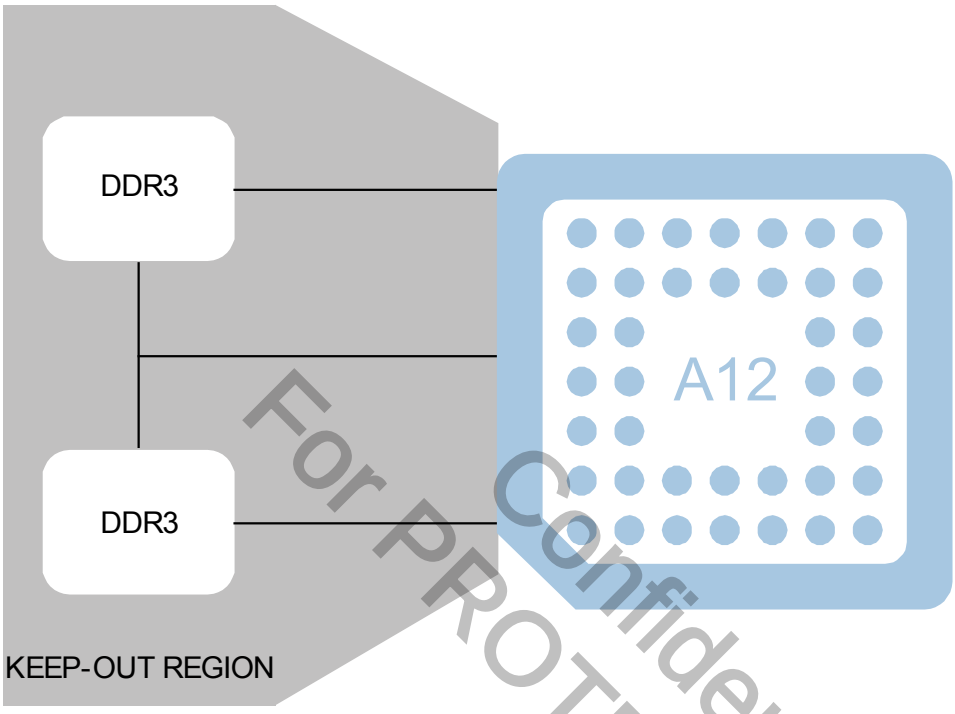

Figure 10-1. PCB Board Layout: DRAM Placement Recommendation.

Note:

- DRAM modules should be placed as close to the A12 SoC as possible, given the guidelines below.

10.2.2 DRAM: Standard Guidelines

This section contains a list of commonly accepted guidelines for DRAM placement on a PCB board.

- For the ground reference plane, there should be a full, contiguous ground plane next to every DRAM routing layer.
- The keep-out region, which varies with individual design, is used to prevent other signals from interfering with the DRAM interface. The only signals allowed in the region (i.e., on the DRAM signal layers) are those for this interface. Do not route DRAM-irrelative traces in the DRAM keep-out region.
- Ground plane cuts are not permitted in the DRAM keep-out region. The 1.5-V power partial plane should encompass at least the entire DRAM region.
- The DRAM power integrated circuit (IC) is designed to allow the DRAM device and the A12 chip to achieve the shortest power-ground loop with the lowest degree of interference possible.
- Trace lengths should be set as short as possible to improve signal integrity.

10.2.3 DRAM: Decoupling Capacitors

- Decoupling capacitors should be placed near the device being decoupled.
- The distance from the capacitor to the power pins being decoupled should not exceed 125 mils.
- Each decoupling capacitor requires two vias (i.e., one for each pin). Via-sharing for decoupling capacitors is not permitted.

10.2.4 DRAM: Reference Voltage

- The reference voltage **DDR_VREF_[N]** divider resistors are placed between the DRAM devices and the A12 chip.
- The minimum nominal trace width for **DDR_VREF_[N]** is 20 mils. Necking down **DDR_VREF_[N]** to accommodate a BGA escape and localized via congestion is acceptable, but **DDR_VREF_[N]** should be kept as close as possible to 20-mils width.
- The **DDR_VREF_[N]** trace length should be as short as possible.

10.2.5 DRAM: Signal Routing Example for DDR3 / DDR3L DRAM

- The impedance (Z) should be in the range of +/-10% tolerance for the Memory Bus. A key consideration for the DRAM interface layout is impedance matching and delay/length matching. Thus, the trace width varies with different routing PCB layers. With the two-chip design, use T-type topology for the layout of DRAM common signals.

- Clock Signal Group:
  - Signal List: **DDR_CK** / **DDR_CK_BAR, DDR_CK_2** / **DDR_CK_2_BAR**
  - Trace lengths are 600 mils to 1400 mils
  - Length matching is to +/- 5 mils for **DDR_CK** to **DDR_CK_BAR** and **DDR_CK_2** to **DDR_CK_2_BAR**
  - Target 100-Ohm differential impedance
  - Route **DDR_CK** / **DDR_CK_BAR, DDR_CK_2** / **DDR_CK_2_BAR** in parallel
  - Trace space depends on differential impedance requirement
  - Trace space to other signal groups is twice the trace width

- Command and Address Signal Group:
  - Signal List: **DDR_BA_[0:2]**, **DDR_ADDR_[0:15]**, **DDR_RAS**, **DDR_CAS**, and **DDR_WE**
  - Length matching to +/- 200 mils (or +/- 32 ps of skew) of **DDR_CK**
  - Target 50-Ohm single-ended trace impedance
  - Trace space to other signal groups is twice the trace width

- Control Signal Group:
  - Signal List: **DDR_CKE**, **DDR_ODT**
  - **DDR_CKE** is static and can be freely routed
  - **DDR_ODT** length matching to +/- 200 mils (or +/- 32 ps of skew) of **DDR_CK**
  - Target 50-Ohm trace impedance
  - Trace space to other signal groups is twice the trace width

- Data Strobe Signal Group:
  - Signal List: **DDR_DQS_[0:3]** / **DDR_DQS_BAR_[0:3]**
  - Length matching is to:
    - +/- 5 mils for **DDR_DQS_[N]** to **DDR_DQS_BAR_[N]**
    - +/- 500 mils (or +/- 80 ps of skew) of **DDR_CK**
    - All four **DQS** pairs match to 200 mils (32 ps) from min to max
  - Target 100-Ohm differential trace impedance
  - **DDR_DQS_[N]** / **DDR_DQS_BAR_[N]** routing should be parallel
  - Trace space depends on differential trace impedance requirement
  - Trace space to other signal groups is twice the trace width

- Data Signal Group:
  - Signal List: **DDR_DQ_[0:31]**, **DDR_DM_[0:3]**.
  - Length matching for:
    - **DDR_DQS** / **DDR_DQ** / **DDR_DM** of the same byte group matches to +/- 50 mils (or +/- 8 ps of skew)
    - **DDR_DQ_[0:31]**, **DDR_DM_[0:3]** is to +/- 500 mils (or +/- 80 ps of skew) of **DDR_CK** (the best case is a perfect match to **DDR_DQS_[0:3]**).
  - Target 50-Ohm single-ended trace impedance
  - Trace space to other signal groups is twice the trace width
  - **DDR_DQS** / **DDR_DQ** / **DDR_DM** from the same byte group should remain on the same layer
  - **DDR_DQ** bits can be swapped within the same byte group to facilitate layout
  - Byte groups as a whole can be swapped to facilitate layout
  - Signals on the inner layer propagate 27% slower than signals on the top and bottom layers. This delay difference must be considered during length matching.

10.2.6 DRAM: Signal Routing Example for LPDDR2 and LPDDR3 DRAM

- Clock Signal Group
  - Same as the Clock Signal Group shown in Section 10.2.5 “DRAM: Signal Routing Example for DDR3 / DDR3L DRAM”.

- Command and Address Signal Group
  - Signal List:

    DDR_ADDR_8 » CA0
    DDR_ADDR_13 » CA1
    DDR_ADDR_9 » CA2
    DDR_ADDR_11 » CA3
    DDR_ADDR_4 » CA4
    DDR_ADDR_6 » CA5
    DDR_ADDR_7 » CA6
    DDR_ADDR_1 » CA7
    DDR_ADDR_2 » CA8
    DDR_ADDR_5 » CA9

  - Length matching for CA[9:0] and **DDR_CKE** matches to +/- 50 mils (or +/- 8 ps of skew) of **DDR_CK** / **DDR_CK_BAR**
  - Target 50-Ohm single-ended trace impedance
  - Trace space to other signal groups is twice the trace width
  - Signals on the inner layer propagate 27% slower than signals on the top and bottom layers. This delay difference must be considered during length matching.
  - Ideally, all CA signals should be routed either on inner layers or on top/bottom layers. Signals should not be routed using a combination of both inner and top/bottom layers; otherwise, the delay difference between layers must be taken into account (refer to the bullet point above).

- Data Strobe Signal Group:
  - Same as the Data Strobe Signal Group shown in Section 10.2.5 “DRAM: Signal Routing Example for DDR3 / DDR3L DRAM”.

- Data Signal Group:
  - Same as the Data Signal Group shown in Section 10.2.5 “DRAM: Signal Routing Example for DDR3 / DDR3L DRAM”.

10.2.7 DRAM: Internal Length

Proper DRAM module layout requires consideration of the A12 chip internal lengths. Refer to the table below in order to maintain the total trace length balance on the layout.

Pin	Length (microns)
DDR_ADDR_0	8130.057
DDR_ADDR_1	8857.217
DDR_ADDR_2	8105.727
DDR_ADDR_3	9299.998
DDR_ADDR_4	8862.915
DDR_ADDR_5	8437.432
DDR_ADDR_6	9345.042

Pin	Length (microns)
DDR_ADDR_7	8124.263
DDR_ADDR_8	8096.126
DDR_ADDR_9	8201.758
DDR_ADDR_10	8788.814
DDR_ADDR_11	8317.844
DDR_ADDR_12	8641.678
DDR_ADDR_13	8236.526
DDR_ADDR_14	8574.157
DDR_ADDR_15	9288.992
DDR_BA_0	8916.467
DDR_BA_1	8188.026
DDR_BA_2	8934.851
DDR_CAS	8766.73
DDR_CK	9240.775
DDR_CKE	9230.501
DDR_CK_BAR	9097.555
DDR_CK_2	8505.481
DDR_CK_2_BAR	8888.17
DDR_CS	8150.516
DDR_CS_2	8316.324
DDR_ODT	9458.705
DDR_RAS	8111.502
DDR_WE	8160.722
DDR_DM_0	5298.103
DDR_DQS_BAR_0	5528.583
DDR_DQS_0	5258.945
DDR_DQ_0	5301.232
DDR_DQ_1	5243.048
DDR_DQ_2	5528.308
DDR_DQ_3	5658.499
DDR_DQ_4	5304.104
DDR_DQ_5	5264.487
DDR_DQ_6	5179.108
DDR_DQ_7	5272.439
DDR_DM_1	5551.916
DDR_DQS_BAR_1	5408.348
DDR_DQS_1	5204.268
DDR_DQ_8	5285.06
DDR_DQ_9	5104.648
DDR_DQ_10	5452.04
DDR_DQ_11	5350.667
DDR_DQ_12	5051.354
DDR_DQ_13	5031.841
DDR_DQ_14	5442.566
DDR_DQ_15	5527.693
DDR_DM_2	6030.66
DDR_DQS_BAR_2	5976.381
DDR_DQS_2	5913.809

Pin	Length (microns)
DDR_DQ_16	6006.641
DDR_DQ_17	6516.613
DDR_DQ_18	6196.51
DDR_DQ_19	5891.525
DDR_DQ_20	5865.091
DDR_DQ_21	6356.419
DDR_DQ_22	6324.937
DDR_DQ_23	6267.756
DDR_DM_3	5790.175
DDR_DQS_BAR_3	6040.113
DDR_DQS_3	6023.947
DDR_DQ_24	5892.888
DDR_DQ_25	6376.395
DDR_DQ_26	6261.163
DDR_DQ_27	5926.44
DDR_DQ_28	5988.604
DDR_DQ_29	6247.321
DDR_DQ_30	5977.778
DDR_DQ_31	5889.413

Table 10-1. DDR Recommended Internal Length.

10.2.8 DRAM: Enabling 16-Bit Mode

To enable 16-bit DRAM mode, leave the upper 16 bits of **DDR_DQS**, **DDR_DQ**, and **DDR_DM** floating.

10.3 PCB Layout: Sensor / Video Input

10.3.1 VIN: LVCMOS Mode

- Signal List: HSync / VSync (i.e. **SD_LVDS_N_[6:7]**), Pixel Clock (i.e., **SPCLK_LVDS_P_0**), DATA [0:13] (i.e., **SD_LVDS_P_[0:9]**, **SD_LVDS_N_[0:3]**)
  - Trace length should be kept as short as possible to lower noise, lower crosstalk, and shorten group delay.
  - Length matching is to +/- 50 mils among the signals listed above.
- **SPCLK_LVDS_P_0** is a clock pin with high clock rate (e.g., 96 MHz). Consider SI and EMC during layout.

10.3.2 VIN: Sub-LVDS / SLVS / MIPI CSI Modes

- Signal List: **SD_LVDS_P/N_[0:9]**, **SPCLK_LVDS_P/N_[0:2]**
  - Trace lengths are 4500 mils or less.
  - Length matching is to:
    - +/- 5 mils between P and N.
    - +/- 10 mils among pairs.
  - Impedance is 100 Ohms +/- 10% for differential pairs.
  - Trace space depends on the differential impedance requirement.
  - Trace space to adjacent signal traces is at least two times trace width (mils).
- Always keep P and N routed in parallel.
- Route P/N with less than two vias and minimum corners.
- Use arcs at corners.
- P/N differential signal pair should not cross routes with different power/ground planes.
- The P/N differential signal pairs must be routed together and should not be parallel with other signal traces in order to minimize crosstalk.
- The trace space to clock signal should be approximately 50 mils or greater.

10.4 PCB Layout: Video Output

10.4.1 VOUT: Digital

- Signal List: **VD0_CLK**, **VD0_HSYNC**, **VD0_VSYNC**, **VD0_HVLD** and **VD0_OUT[0:15]**.
- Trace lengths are 2000 mils or less.

- Keep all signal traces to the same length (or same trace delay and impedance).
- Length matching is to +/- 50 mils.

10.4.2 VOUT: Analog

- IO (CVBS) should not have routes that cross different power/ground planes.
- The IO (CVBS) signal refers to analog ground.
- The output connector should be placed as close as possible to the DAC.
- Keep the analog output traces as short as possible (short analog output traces reduce noise pickup due to neighboring digital circuitry and minimize reflection).
- The DAC termination resistors should be placed as close as possible to the DAC outputs and should overlay the PCB ground plane.

10.4.3 VOUT: HDMI

- Signal List: **HDMI_CLK_P/M**, **HDMI_CH[0:2]_P/M**.
  - Trace lengths are 1500 mils or less.
  - Length matching is to +/- 5 mils between P and M.
  - Impedance is 100 Ohms +/- 10% for differential pairs.
  - P and M trace-to-trace spacing depends on PCB topology structure to achieve 100 Ohms differential impedance.
  - Trace space to adjacent signal traces is greater than two times trace width.
- Keep P and M routing in parallel (higher priority than keeping traces length-matched).
- Route P/M with minimum vias (less than two) and minimum corners.
- Use arcs at corners.
- The P/M signals must have a solid reference plane (preferably the ground plane) and should not be routed over two split reference planes.
- The P/M signal pairs must be routed together and not parallel with other signal traces to minimize crosstalk.
- Trace space to clock signals should be approximately 50 mils or greater.

10.5 PCB Layout: Ethernet

- Transmit Signal list: Ethernet pins **ENET_TXD_[0:1]** and **ENET_TXEN**
  - Keep all signal traces to the same length (or same trace delay and impedance).
  - Length matching is to +/- 20 mils.

- Receive Signal list: Ethernet pins **ENET_RX_ER**, **ENET_CRS_DV**, and **ENET_RXD[0:1]**
  - Keep all signal traces to the same length (or same trace delay and impedance).
  - Length matching is to +/- 20 mils.

10.6 PCB Layout: SMIO

- Signal List: Refer to the A12 chip datasheet.
- Signal traces should be approximately the same length (or have the same trace delay and impedance).
- Length Matching is to +/- 20 mils.

10.7 PCB Layout: USB

- Signal List: **USB[0:1]_DP**, **USB[0:1]_DM**.
  - Note:
    - **GPIO1** (OVT0) / **GPIO3** (PWR0) internal are used for USB1
    - **GPIO2** (OVT1) / **GPIO4** (PWR1) internal are used for USB0
  - Trace lengths are 2000 mils or less.
  - Length matching is to +/- 5 mils between **DP** and **DM**.
  - Differential trace impedance is 90 Ohms.
  - Trace space depends on the differential impedance request.
  - Trace space to adjacent signal traces is at least two times trace width (mils).
- Always keep P/M routes in parallel (higher priority than keeping traces length-matched).
- Route P/M to minimize vias (less than two) and corners.
- Use arcs at corners.
- P/M routes should not cross different power/ground planes.
- The P/M signal pair must be routed together and not parallel with other signal traces in order to minimize crosstalk.
- Trace space to clock signals should be approximately 50 mils or greater.
- Do not route USB traces under crystal, oscillators, clock synthesizers, magnetic devices or integrated circuits that use and/or duplicate clocks.
- USB traces should be at least 90 mils from the edge of the plane (power and ground).

10.8 PCB Layout: Oscillator

- Signal List: **XIN**
- Trace lengths should be 500 mils or less.
- Trace width is 5 mils or greater.
- Trace space to adjacent signal traces is approximately 45 mils.

10.9 PCB Layout: Crystal

- Signal List: **XIN**, **XOUT**, **XI_RTC**, **XO_RTC**
- Trace lengths should be 500 mils or less.
- Input / output trace length difference should be 5 mils or less.
- Trace space to adjacent signal traces is 45 mils.

10.10 PCB Layout: Power Rails

- Add LC filter for all analog and PLL power rails.
- Place the power source as closely as possible to the power balls as shown on the reference board layout.
- Do not use thin traces for power delivery (i.e., ensure that the traces are wide and thick).

10.11 PCB Layout: Miscellaneous

- All ground planes in different layers should connect with vias every 1 cm to 1.5 cm.
- All power trace widths should be 60 mils or greater.
- Place at least one 22-uF decoupling capacitor within every 6-inch^2 area.

11. AMBARELLA CONTACT INFORMATION

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12. ADDITIONAL RESOURCES

Ambarella documents of potential interest include:

- *A12 Datasheet*
- *A12 Hardware Programming Reference Manual*

13. IMPORTANT NOTICE

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14. TYPOGRAPHICAL CONVENTIONS

This document provides technical detail using a set of consistent typographical conventions to help the user differentiate key concepts at a glance. Conventions include:

Example	Description
AmbaGuiGen, **DirectUSB** **Save**, **File > Save** **Power**, **Reset**, **Home**	Software names GUI commands and command sequences Computer / Hardware buttons
Flash_IO_control **da**, **status**, **enable**	Register names and register fields. For example, **Flash_IO_control** is the register for global control of Flash I/O, and bit 17 (**da**) is used for DMA acknowledgement.
GPIO81, **CLK_AU**	Hardware external pins
VIL, VIH, VOL, VOH	Hardware pin parameters
INT_O, RXDATA_I	Hardware pin signals
amb_performance_t **amb_operating_mode_t** **amb_set_operating_mode()**	API details (e.g., functions, structures, and type definitions)
`/usr/local/bin` `success = amb_set_operating_mode (amb_hal_base_address, & operating_mode)`	User entries into software dialogues and GUI windows File names and paths Command line scripting and Code

Table 14-1. Typographical Conventions for Technical Documents.

Additional Ambarella typographical conventions include:

- Acronyms are given in UPPER CASE using the default font (e.g., AHB, ARM11 and DDRIO).
- Names of Ambarella documents and publicly available standards, specifications, and databooks appear in *italic* type.

15. REVISION HISTORY

NOTE: Page/chapter numbers for previous drafts may differ from those in the current version.

Version	Date	Comments
1.0	17 Sept 2013	Draft Original
1.1	3 Oct 2013	Update Chapters 2, 3, 5, 7 and 9
1.2	24 April 2014	Add USB-related information to Chapter 9; add HDMI update to Chapter 4; changes to power groupings; miscellaneous changes to p. 9, 13, 14, 17, 19, 31, 32 and 33; add IDC section; update PCB layout chapter; formatting
1.3	23 Oct 2014	Add guidelines for enabling 16-bit DRAM
1.4	12 November 2014	Add Sections 2.9 and 5.6
1.5	15 December 2014	Update power specs for secondary sensor; Add HDMI_AVDD25 detail
1.6	6 May 2015	Updated Sections 2.9 and 5.3
1.7	15 May 2015	Updated Section 3.7 Add Section 3.10