

B5Nd De-Serializer Chip Datasheet

SUMMARY DESCRIPTION

Ambarella B5 companion chips enable the multi-stream capture of full-HD video for automotive or sports camera applications. The B5 family of chips can be configured to establish 360-degree coverage, without the introduction of latency or a loss of signal integrity.

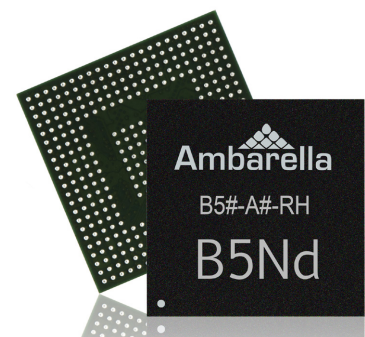
The Ambarella B5Nd two-channel de-serializer chip combines the multiple-video stream transferred by the B5F serializer, then outputs the stitched picture in SLVS format to an Ambarella DSP.

KEY FEATURES

- Supports up to two channels of input with three possible modes:
 - Serializer-Deserializer (SERDES) Input
 - Sensor Input
 - SERDES / Sensor Mixed Input
- Supports up to 1080p60 per input
- Performs all sensor synchronization tasks
- 32 General Purpose Input / Output (GPIO) pins
- Bit error correction
- 168-pin FBGA package (10 mm x 10 mm)

CONTENTS

1. Overview	1
2. Peripheral Interfaces	4
3. Pins	7
4. Electrical Characteristics	17
5. Package	23
6. Contact and Order Information.....	26
7. Pin List and Mapping Table.....	27
8. Important Notice	33
9. Typographical Conventions.....	34
10. Revision History.....	35



The material in this document is for information only. Ambarella assumes no responsibility for errors or omissions and reserves the right to change, without notice, product specifications, operating characteristics, packaging, ordering, etc. Ambarella assumes no liability for damage resulting from the use of information contained in this document. All brands, product names and company names are trademarks of their respective owners. Further information, including additional disclaimers, appears in the Important Notice at the end of this document.

1. OVERVIEW

This datasheet for the B5Nd de-serializer chip from Ambarella begins with a brief introduction to the B5 family of co-processors ([Section 1.1](#)) and a summary of the key features of the two-channel-capable B5Nd ([Section 1.2](#)). Chapter 2 describes the B5Nd modules and interfaces. For pin details and electrical characteristics refer to Chapter 3 and Chapter 4, respectively. See Chapter 5 for package information and Chapter 6 for Ambarella contact and ordering details.

1.1 Introduction to B5 Co-Processors from Ambarella

Ambarella B5 companion chips enable the multi-stream capture of full-HD video for automotive and sports camera applications. Designed to support complex systems requiring multiple image sensors deployed over a vehicle, building, or within a single camera body, the B5 family of co-processors serves as a highly efficient bridge between the digital signal processor (DSP) and up to four image sensors, allowing 360-degree coverage without the introduction of latency or a loss of signal integrity. Moreover, B5 chips enable full HD-resolution Bayer RGB sensor data to be transferred using a simple low-cost twisted pair cable.

The Ambarella B5 family is composed of the following co-processor types.

1. **B5F:** (Far-end) The B5F serializer chip captures Bayer RGB sensor input, serving as a bridge between one remotely-located sensor and a B5N co-processor.
2. **B5N:** (Near-end) The B5N de-serializer chip (B5Nq or B5Nd) combines the multiple-video stream and sends it in SLVS format to the DSP.

B5 co-processors can be used in a variety of configurations depending on specific application needs. The **B5 Dual-Channel Use Case**—an automotive video camera application—provides a two-channel configuration.

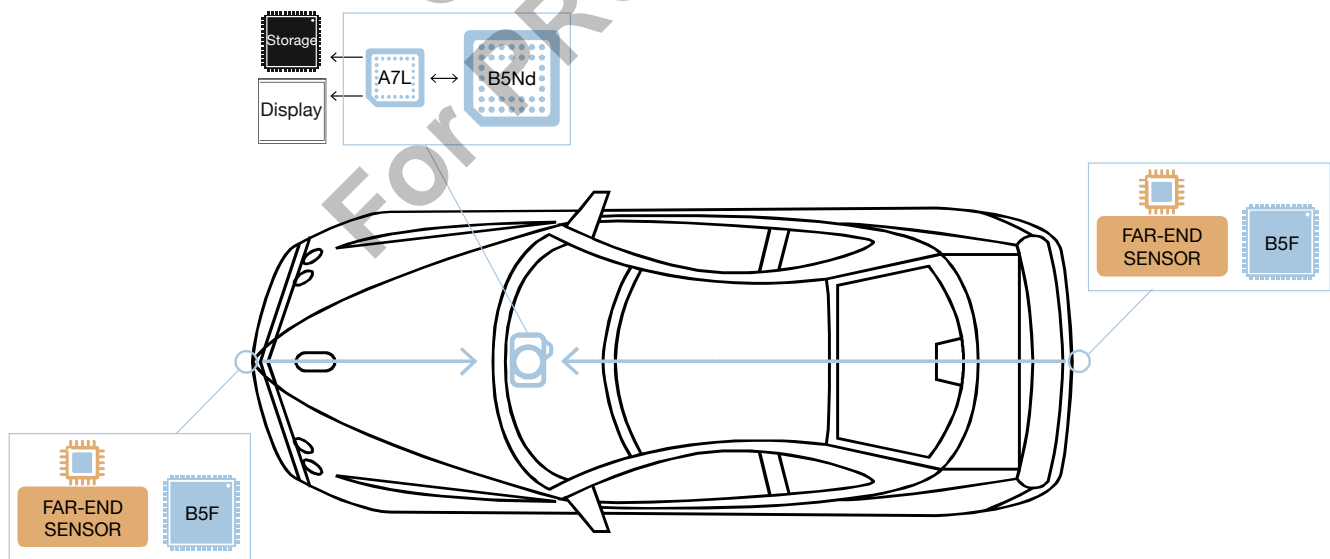


Figure 1-1. B5 Processor Dual-Channel Use Case: Automotive Video Camera Application.

Note the following system features of the **B5 Dual-Channel Use Case**:

- Two far-end sensors contained in camera modules located at the front and rear of the vehicle
- Two B5F serializer chips
- One B5Nd two-channel de-serializer chip (B5Nq can also be used in a dual-channel configuration)
- One high-performance DSP (Ambarella A7L processor), which performs the sensor data processing and conversion to video, dewarping and display.
- USB cable (up to 7.5 m) / HDMI cable (up to 10 m) connecting the camera modules to the main camera body. Note that if a cable is disconnected while the system is active, the specific channel will be dropped; however, overall system operations will not be disrupted.

1.2 Introduction to the B5Nd

The following is a functional block diagram showing the active modules of the B5Nd co-processor.

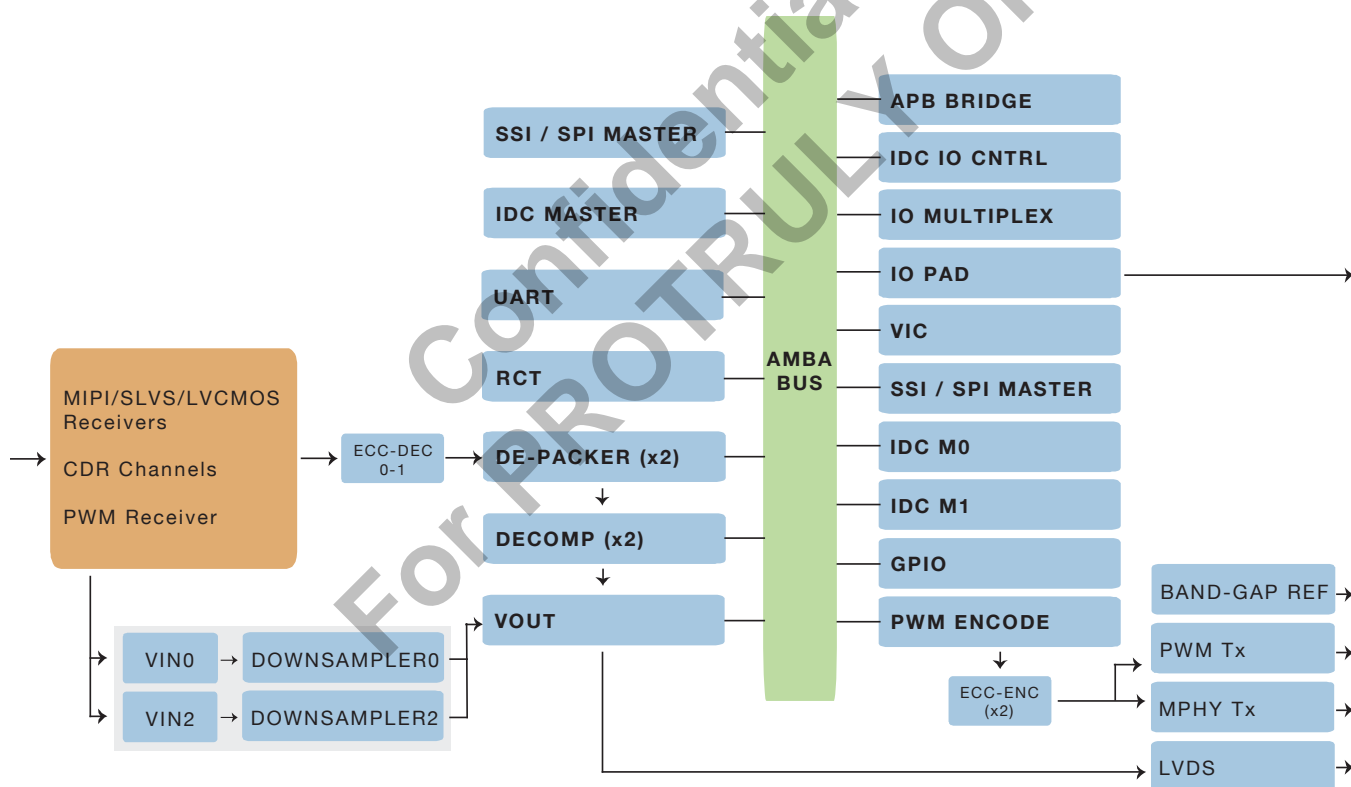


Figure 1-2. Introduction to B5Nd: Functional Block Diagram of the B5Nd Chip.

Features of the B5Nd de-serializer chip are as follows:

- Input Modules

- Support for up to two channels of input with three possible modes:
 - **Serializer-Deserializer (SERDES) Input Mode:** Two SERDES inputs from B5F chips
 - **Sensor Input Mode:** Two channels of 4-lane SLVS/MIPI sensor input, or two channels of 12-bit LVCMOS sensor input
 - **SERDES / Sensor Mixed Mode:**
 - Either of the two channels can be configured to support SERDES
 - One channel can be configured to support LVCMOS input
 - Note that all sensors must be the same type, and must be configured identically.
 - B5Nd performs all sensor synchronization tasks.
- Supports up to 1080p60 per input
- Depacker reassembles SERDES data into a single video channel
- Selectable SPI / SSI or IDC interface for sensor configuration
- Video Stream Output (VOUT) Module
 - Supports up to two inputs plus depacker/decompressor
 - BT.656 embedded SYNC
 - Supports 1, 2, 4, 8 or 10 SLVS lanes
- USB cable (up to 7.5 m) or HDMI cable (up to 10 m) required for connection to far-end sensors
- 32 General Purpose Input / Output (GPIO) pins
- Bit error correction
- ECC encoder and decoder
- VIC handles local and remote (B5F) interrupt status
- Four PLLs: Core, Sensor, VOUT, and PHY
 - To reduce the possibility of electromagnetic interference (EMI), spread spectrum techniques can be applied to the one-wire interface by modulating the fractional bits of the PLL via software.
- 168-pin FBGA package (10 mm x 10 mm)
- Temperature range: -20 °C to +85 °C

2. PERIPHERAL INTERFACES

2.1 Interfaces: Overview

This chapter provides summary information regarding the B5Nd peripheral interfaces. The chapter is organized as follows:

- (Section 2.2) Input Interface
- (Section 2.3) Video Output Formatter (VOUTF) Interface
- (Section 2.4) IDCS Bridge Module
- (Section 2.5) SSI Host Interface

2.2 Input Interface

The B5Nd input interface supports two separate input instances simultaneously, each with independent programming and operation.

The following diagram shows the basic input pipeline for the B5Nd co-processor.

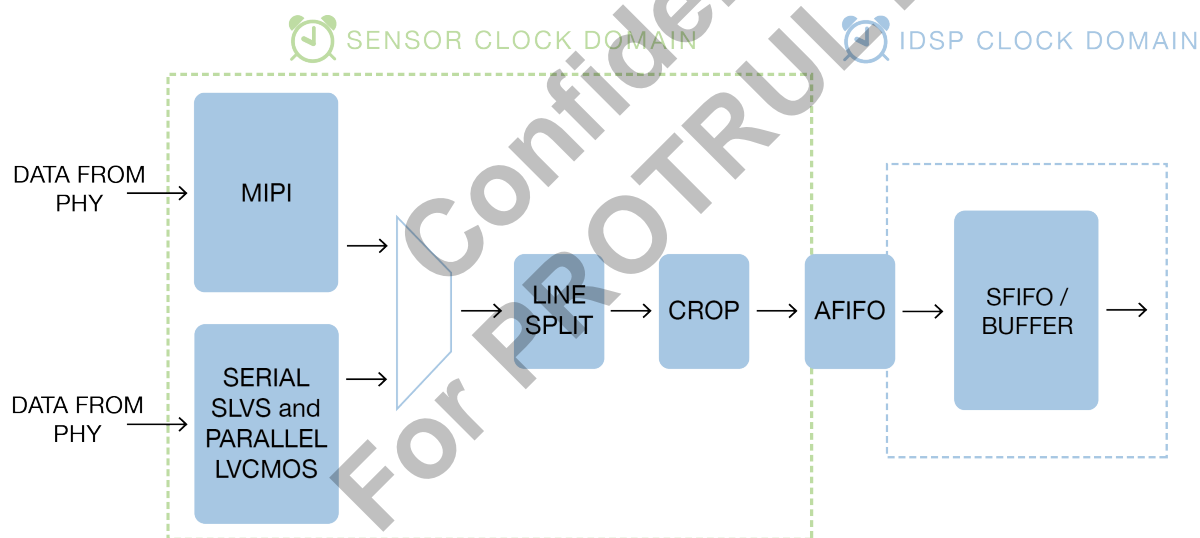


Figure 2-1. VIN Interface: Basic Input Pipeline for B5Nd.

The features of the B5Nd input interface are provided below.

- Two channels of input
- Three input modes:
 - **Serializer-Deserializer (SERDES) Input Mode:** Two SERDES inputs from B5F chips
 - **Sensor Input Mode:** Two channels of 4-lane SLVS/MIPI sensor input, or two channels of 12-bit LVCMOS sensor input
 - **SERDES / Sensor Mixed Mode:** Either of the two channels can be configured to support SERDES; one channel can be configured to support LVCMOS input
 - Note that all sensors must be the same type, and must be configured identically.
 - B5Nd performs all sensor synchronization.
 - Each input mode supports:
 - Up to 1080p60 per input
 - Master (external) sync generation
- Flexible sync detection can handle a variety of sync code protocols and formats:
 - Support for 2- and 4-lane interleaving / striping of sync codes
- Pixel Reordering module allows programmable sequencing of the YUV (Y, Cb, Cr) components into the desired output order:
 - Support for RGB format included

2.3 Video Output Formatter (VOUTF) Interface

The B5Nd video output formatter (VOUTF) is capable of outputting two-channel video via 10-lane SLVS. The B5Nd video output stream is transmitted to the VIN module of the main Ambarella SoC.

The following image shows a logic block diagram for the B5Nd VOUTF interface.

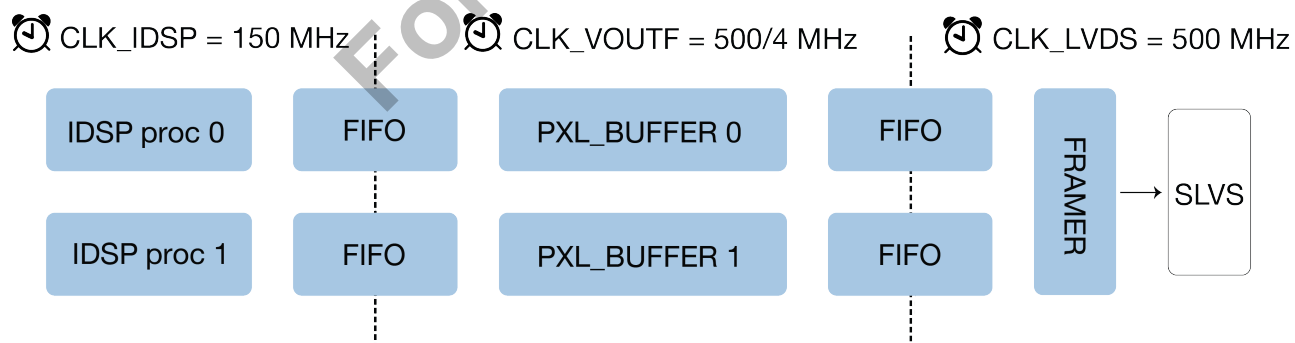


Figure 2-2. VOUTF Interface: Logic Block Diagram.

The features of the B5Nd VOUTF interface are as follows:

- Two full-HD channels of output through 10-lane SLVS (14-bit/pixel)
 - Up to 3.5 Gbps (2x1080p60)
 - Output channel format: SLVS protocol (maximum 10-lane)
- Two packing modes for multi-channel operations:
 - Line concatenating mode
 - Line interleaving mode
- Embedded pattern generator with programmable values
- Configurable border support for each channel in line-concatenating mode.

2.4 IDCS Bridge Module

The IDCS module is an I2C / IDC slave device that serves as a bridge between the B5Nd internal bus and the Ambarella DSP. Features of the IDCS module include:

- Three operational modes:
 - Standard mode: up to 100 kb/s data transfer rate
 - Fast mode: up to 400 kb/s data transfer rate
 - High-speed (Hs) mode: up to 3.4 Mb/s data transfer rate
- Minimum clock frequency: 1.34 MHz in standard mode

2.5 SSI Host Interface

The B5Nd chip provides a SSI host interface module, a slave interface which receives sensor input frames and transfers them into a AHB master signal. Features of the SSI host interface include:

- Support for 8-bit data frames
- Support for **scph** = 0, indicating that the serial clock toggles in the middle of the first data bit, and **scpol** = 0, indicating a low inactive state.

3. PINS

3.1 Overview of the B5Nd Pins

This chapter details the external pins for the B5Nd co-processor. Please refer to Chapter 7 for a complete pin list according to ball-map location.

3.2 Pin Tables

The pins for the B5Nd chip are classified according to interface as follows:

- (Section 3.2.1) Input Pins
- (Section 3.2.2) Video Output Pins
- (Section 3.2.3) I2C / IDC Pins
- (Section 3.2.4) SSI / SPI Pins
- (Section 3.2.5) GPIO Pins
- (Section 3.2.6) System Pins
- (Section 3.2.7) Power, Ground and PLL Pins

Each pin table below provides the functional pin name, location, pin direction, pad type, and a brief description.

3.2.1 Input Pins

B5Nd input pins can be categorized according to the specific two-channel configuration selected:

- (Section 3.2.1.1) Input: SERDES + SERDES
- (Section 3.2.1.2) Input: SLVS/MIPI Sensor + SLVS/MIPI Sensor
- (Section 3.2.1.3) Input: LVCMOS Sensor + LVCMOS Sensor
- (Section 3.2.1.4) Input: LVCMOS Sensor + SERDES

3.2.1.1 Input: SERDES + SERDES

Name	Location	Dir	Type	Description
DN_[00:02]	P8, N7, P5	I	Sub-LVDS	Sub-LVDS data
DN_[10:12]	P13, N12, P10			
DP_[00:02]	N8, P7, N5	I	Sub-LVDS	
DP_[10:12]	P14, P12, N10			
MPHY_VDDA25_[L]	M10, M11, M12	S	Analog Supply	SERDES PHY analog power
MPHY_VDDA12_[L]	M6, M7, M8, M9	S	Analog Supply	
MPHY_VDDAIO_[L]	K10, K9	S	Analog Supply	
MPHY_VSSA25	K5, K6, K7, K8	G	Analog Ground	SERDES PHY analog ground

Table 3-1. Video Input Interface Pins: SERDES/SERDES Dual-Channel.

Notes:

1. VIN pins **DP_32**, **DN_32**, and **DSIP_3**—which are unused in this dual-channel configuration—should be pulled-down with a 10 K-Ohm resistor.
2. Other VIN pins which are unused in this dual-channel configuration should be tied to ground.

3.2.1.2 Input: SLVS/MIPI Sensor + SLVS/MIPI Sensor

Name	Location	Dir	Type	Description
CLK_SI	C5	I/O	CMOS	Sensor master clock output
DN_[00:02]	P8, N7, P5	I	MIPI / SLVS	Sensor data Both single and double data rates supported.
DN_[10:12]	P13, N12, P10		MIPI / SLVS	
DP_[00:02]	N8, P7, N5	I	MIPI / SLVS	
DP_[10:12]	P14, P12, N10		MIPI / SLVS	
DSIN_[0:1]	P4, P9	I	MIPI / SLVS	
DSIP_[0:1]	N4, N9	I	MIPI / SLVS	
HSYNC[0:1]	M4, A6	O	CMOS	Video input master HSync
SPCLKN_[0:1]	P6, P11, N1, K1	I	MIPI/ SLVS	Video / sensor input clock
SPCLKP_[0:1]	N6, N11, N2, K2	I	MIPI/ SLVS	
VSYNC[0:1]	J3, A9	O	CMOS	Video input master VSync
MPHY_VDDA25_[L]	M10, M11, M12	S	Analog Supply	VIN analog power
MPHY_VDDA12_[L]	M6, M7, M8, M9	S	Analog Supply	
MPHY_VDDAIO_[L]	K10, K9	S	Analog Supply	
MPHY_VSSA25	K5, K6, K7, K8	G	Analog Ground	VIN analog ground

Table 3-2. Video Input Interface Pins: SLVS-MIPI/SLVS-MIPI Dual-Channel.

Notes:

1. VIN pins **DP_32**, **DN_32**, and **DSIP_3**—which are unused in this dual-channel configuration—should be pulled-down with a 10 K-Ohm resistor.
2. Other VIN pins which are unused in this dual-channel configuration should be tied to ground.

3.2.1.3 Input: LVCMOS Sensor + LVCMOS Sensor

Name	Location	Dir	Type	Description
CLK_SI	C5	I/O	CMOS	Sensor master clock output
DN_[00:02]	P8, N7, P5	I	LVCMOS	Sensor data Both single and double data rates supported.
DN_[10:11]	P13, N12			
DN_[20:22]	P3, P1, M1			
DN_[30:31]	L1, G1			
DP_[00:02]	N8, P7, N5	I	LVCMOS	
DP_[10:11]	P14, P12			
DP_[20:22]	N3, P2, M2			
DP_[30:31]	L2, G2			
DSIP_0	N4	I	LVCMOS	
DSIN_0	P4			
DSIP_2	H2			
DSIN_2	H1			
DN_12	P10	O	CMOS	HSync
DP_12	N10	O	CMOS	VSync
DSIP_1	N9	O	CMOS	Field
DN_32	J1	O	CMOS	HSync
DP_32	J2	O	CMOS	VSync
DSIP_3	F2	O	CMOS	Field
HSYNC[0:1]	M4, A6	O	CMOS	Video input master HSync
SPCLKP_0 SPCLKP_2	N6, N2	I	LVCMOS	Video / sensor input clock
VSYNC[0:1]	J3, A9	O	CMOS	Video input master VSynC
MPHY_VDDA25_[L]	M10, M11, M12	S	Analog Supply	VIN analog power
MPHY_VDDA12_[L]	M6, M7, M8, M9	S	Analog Supply	
MPHY_VDDAIO_[L]	K10, K9	S	Analog Supply	
MPHY_VSSA25	K5, K6, K7, K8	G	Analog Ground	VIN analog ground

Table 3-3. Video Input Interface Pins: LVCMOS/LVCMOS Dual-Channel.

Notes:

1. VIN pins which are unused in this dual-channel configuration should be tied to ground.

3.2.1.4 Input: LVCMOS Sensor + SERDES

Name	Location	Dir	Type	Description
CLK_SI	C5	I/O	CMOS	Sensor master clock output
DN_[00:02]	P8, N7, P5	I	LVCMOS	Sensor data Both single and double data rates supported.
DN_[10:11]	P13, N12			
DP_[00:02]	N8, P7, N5	I	LVCMOS	
DP_[10:11]	P14, P12			
DSIP_0	N4	I	LVCMOS	
DSIN_0	P4			
DN_[20:22]	P3, P1, M1	I	LVDS	LVDS data
DP_[20:22]	N3, P2, M2	I	LVDS	LVDS data
DN_12	P10	O	CMOS	HSync
DP_12	N10	O	CMOS	VSynC
DSIP_1	N9	O	CMOS	Field
HSYNC[0:1]	M4, A6	O	CMOS	Video input master HSync
SPCLKP_0	N6	I	LVCMOS	Video / sensor input clock
VSYN[0:1]	J3, A9	O	CMOS	Video input master VSynC
MPHY_VDDA25_[L]	M10, M11, M12	S	Analog Supply	VIN analog power
MPHY_VDDA12_[L]	M6, M7, M8, M9	S	Analog Supply	
MPHY_VDDAIO_[L]	K10, K9	S	Analog Supply	
MPHY_VSSA25	K5, K6, K7, K8	G	Analog Ground	VIN analog ground

Table 3-4. Video Input Interface Pins: LVCMOS/SERDES Dual-Channel.

Notes:

1. VIN pins **DP_32**, **DN_32**, and **DSIP_3**—which are unused in this dual-channel configuration—should be pulled-down with a 10 K-Ohm resistor.
2. Other VIN pins which are unused in this dual-channel configuration should be tied to ground.

3.2.2 Video Output Pins

Pin Name	Pin Number	Dir	Type	Description
LVDS_N_[0:9]	A12, A13, C14, G14, J14, K14, B14, H14, M14, N14	O	SLVS	Video data output
LVDS_P_[0:9]	B12, A14, C13, G13, J13, K13, B13, H13, M13, N13	O	SLVS	
LVDS_CKN	E14	O	SLVS	Video output clock
LVDS_CKP	E13	O	SLVS	
LVDS_VDDA12_[L]	K12, L12	S	Analog Supply	VOUT analog power
LVDS_VDDA25_[L]	D12, E12, F12, G12	S	Analog Supply	
LVDS_AVSS	E10, F10, G10, H12, J12	G	Analog Ground	VOUT analog ground

Table 3-5. Video Output Interface Pins.

Note:

- Pins **CKN_[0:3]** and **CKP_[0:3]** are serializer outputs.

3.2.3 I2C / IDC Pins

Pin Name	Pin Number	Dir	Type	Description
I2C0_SCL	C7	I/O	CMOS	Camera module interface
I2C0_SDA	C6	I/O	CMOS	
I2C1_SCL0	E2	I/O	CMOS	Sensor configuration interface
I2C1_SCL1	B8	I/O	CMOS	
I2C1_SDA0	D1	I/O	CMOS	
I2C1_SDA1	A7	I/O	CMOS	

Table 3-6. I2C / IDC Interface Pins.

3.2.4 SSI / SPI Pins

Pin Name	Pin Number	Dir	Type	Description
SPI_CLK	A1	I/O	CMOS	Sensor configuration interface
SPI_EN0	B3	I/O	CMOS	Sensor configuration interface
SPI_MISO	B2	I/O	CMOS	Sensor configuration interface
SPI_MOSI	B7	I/O	CMOS	Sensor configuration interface
CFG_SPI_CLK	A8	I/O	CMOS	SSI host interface
CFG_SPI_EN	C10	I/O	CMOS	SSI host interface
CFG_SPI_MISO	E1	I/O	CMOS	SSI host interface
CFG_SPI_MOSI	D3	I/O	CMOS	SSI host interface

Table 3-7. SSI / SPI Pins.

3.2.5 GPIO Pins

GPIO	Pin Name	Multiplexed Function		
		First	Second	Third
0	I2C1_SCL0	i2c1_scl0	spi_en1	pwm_ls_tx_out0
1	I2C1_SDA0	i2c1_sda0	spi_en2	pwm_ls_tx_out1
2	I2C1_SCL1	i2c1_scl1	spi_en3	pwm_ls_tx_out2
3	I2C1_SDA1	i2c1_sda1		pwm_ls_tx_out3
4	SPI_CLK	spi_clk	i2c1_scl2	uart_ahbm_clk
5	SPI_EN0	spi_en0	i2c1_sda2	
6	SPI_MOSI	spi_mosi	i2c1_scl3	
7	SPI_MISO	spi_miso	i2c1_sda3	
8	I2C0_SCL	i2c0_scl	uart_ahbm_rx	
9	I2C0_SDA	i2c0_sda	uart_ahbm_tx	
10	VSYNCO	vin_vsync0	irq	
11	HSYNCO	vin_hsync0	por_l_brdcst	
12	VSYNC1	vin_vsync1		
13	HSYNC1	vin_hsync1		
14	Reserved			
15	Reserved			
16	Reserved			
17	Reserved			
18	B5F_0_RST_L	por_l_brdcst		
19	B5F_1_RST_L	por_l_brdcst		
20	Reserved			
21	Reserved			

GPIO	Pin Name	Multiplexed Function		
		First	Second	Third
22	GPIO_0			
23	GPIO_1			
24	GPIO_2			
25	GPIO_3			
26	GPIO_4			
27	GPIO_5	pll_obsrv_core		
28	GPIO_6	pll_obsrv_phy		
29	GPIO_7	pll_obsrv_sensor		
30	GPIO_8			
31	GPIO_9			

Table 3-8. General Purpose Input / Output Pins.

Confidential
For PROTRULY Only

3.2.6 System Pins

Name	Location	Dir	Description
PACKAGE_ID	G3	I	Package identification
REPEATER_MODE	A3	I	Repeater mode control
CLK_SI	C5	O	Sensor reference clock
CLK_REF_SEL	C4	I	Clock reference selection
POR_L	B5	I	Power-on reset pin (active low)
TEST_MODE	C8	I	0 - Normal mode 1 - Test mode
IRQ	F3	O	Interrupt request to host
XIN	D2	I	24-MHz or 48-MHz crystal or crystal oscillator input
XOUT	C1	O	

Table 3-9. System Pins.

3.2.7 Power, Ground and PLL Pins

Name	Location	Dir	Type	Description
VDDI	H10, J10, J7, J8, J9	S	Digital Supply	Digital input power supply
VDDA10_PLL	E7, E8	S	Analog Supply	PLL analog power supply
MPHY_VDDA12	M6, M7, M8, M9	S	Analog Supply	MIPI PHY analog power supply
LVDS_VDDA12	K12, L12	S	Analog Supply	LVDS analog power supply
LVDS_VDDA25	D12, E12, F12, G12	S	Analog Supply	LVDS analog power supply
MPHY_VDDA25	M10, M11, M12	S	Analog Supply	MIPI PHY analog power supply
VDDA25_PLL	E5, E6	S	Digital Supply	PLL analog power supply
MPHY_VDDAIO	K10, K9	S	Analog Supply	MIPI PHY analog power supply
VDDO	F5, G5, G6, H5, J5	S	Digital Supply	Digital output power supply
VSSI	E9, F9, G9, H8, H9	G	Digital Ground	Digital input ground
VSSO	F8, G7, G8, H6, H7, J6	G	Digital Ground	Digital output ground
LVDS_AVSS	E10, F10, G10, H12, J12	G	Analog Ground	LVDS analog ground

Name	Location	Dir	Type	Description
MPHY_VSSA25	K5, K6, K7, K8	G	Analog Ground	MIPI PHY analog ground
VSSA_PLL	F6, F7	G	Analog Ground	PLL analog ground

Table 3-10. Power, Ground and PLL Pins.

Confidential
For PROTRULY Only

4. ELECTRICAL CHARACTERISTICS

4.1 Overview of the Electrical Characteristics

This chapter provides information regarding the electrical characteristics of the B5Nd co-processor. The chapter is organized as follows:

- (Section 4.2) Absolute Ratings
- (Section 4.3) Recommended Operating Conditions
- (Section 4.4) Fail-Safe Pins
- (Section 4.5) Video Signal Waveforms and Timing

Note that the electrical details provided in this chapter are preliminary estimates. Please contact an Ambarella representative for current electrical specifications.

4.2 Absolute Ratings

The following table provides absolute ratings for the nominal analog / digital voltages in [Section 4.3.1](#).

Parameter	Minimum	Maximum
Analog supply voltage (3.3 V)	-0.3 V	3.6 V
Digital supply voltage (3.3 V)	-0.3 V	3.6 V
Analog supply voltage (1.3 V)	-0.3 V	1.35 V
Digital supply voltage (1.3 V)	-0.3 V	1.35 V
Digital I/O range (V)	-0.3 V	3.6 V
Analog I/O range (V)	-0.3 V	3.6 V
Operating temperature (case) (°C)	-20 °C	+85 °C

Table 4-1. Absolute Ratings.

Note:

This Ambarella part will support a full range of operation at the case temperature specified above, provided that the customer's PCB design, manufacturing processes, and power supply design are equal to those of the Ambarella reference hardware platform in terms of quality. All other components used during system design are also required to operate successfully at the case temperature range specified above to guarantee proper overall system operation.

The operating temperature range for the B5Nd chip has not been finalized, and is subject to change.

4.3 Recommended Operating Conditions

Recommended operating conditions are provided for the following:

- (Section 4.3.1) Power Rails DC
- (Section 4.3.2) Digital I/O
- (Section 4.3.3) Serial Sensor / MIPI / SLVS I/O Specification
- (Section 4.3.4) Parallel LVCMOS I/O Specification

4.3.1 Power Rails DC

Parameter	Comments	Minimum	Typical	Maximum	Ripple
VDDI		1.25 V	1.3 V	1.35 V	2%
VDDO	VDDIO ranges from 1.8 V to 3.3 V	VDDIO - 0.1 V	VDDIO	VDDIO + 0.1 V	2%
LVDS_VDDA12		1.25 V	1.3 V	1.35 V	2%
MPHY_VDDA12		1.25 V	1.3 V	1.35 V	2%
VDDA10_PLL		1.25 V	1.3 V	1.35 V	2%
MPHY_VDDAIO	MIPI Mode	1.25 V	1.3 V	1.35 V	2%
	Other: VDD_VIN ranges from 1.8 V to 2.5 V	VDD_VIN - 0.1 V	VDD_VIN	VDD_VIN + 0.1 V	2%
LVDS_VDDA25		2.25 V	2.5 V	2.75 V	2%
MPHY_VDDA25		2.25 V	2.5 V	2.75 V	2%
VDDA25_PLL		2.25 V	2.5 V	2.75 V	2%

Table 4-2. Power Rails DC Characteristics (Subject to Change).

Note:

- The DC characteristics shown above are subject to change.

4.3.2 Digital I/O

Parameter	Comments	Minimum	Typical	Maximum
VIL	Input Low Voltage	-0.3 V		0.7 V
VIH	Input High Voltage	2.0 V		3.6 V
VOL	Output Low Voltage			0.4 V
VOH	Output High Voltage	2.4 V		

Table 4-3. Digital I/O Characteristics.

4.3.3 Serial Sensor / MIPI / SLVS I/O Specification

Parameter	Comments	Minimum	Typical	Maximum
V_{CM}	Common mode input voltage	0.5 V	0.9 V	1.3 V
V_{THL}	Receiver input low threshold	-25 mV		
V_{thh}	Receiver input high threshold			+ 25 mV

Table 4-4. Serial Sensor I/O Specification.

4.3.4 Parallel LVCMOS I/O Specification

Parameter	Comments	Minimum	Typical	Maximum
VIL				0.6 V
VIH		1.62 V		

Table 4-5. Parallel LVCMOS I/O Specification.

4.4 Fail-Safe Pins

All B5Nd CMOS pins are fail-safe and can have active signals at or below 3.6 V when the B5Nd is powered down.

4.5 Video Signal Waveforms and Timing

This section contains B5Nd analog video waveform diagrams for reference purposes. Please ensure that the analog video output from the system board meets desired/standard specifications. The section is organized as follows:

- (Section 4.5.1) Video Input (VIN) Timing: LVCMOS Mode
- (Section 4.5.2) Video Input (VIN) Timing: MIPI / SLVS Mode
- (Section 4.5.3) Video Output (VOUT) Timing

4.5.1 Video Input (VIN) Timing: LVCMOS Mode

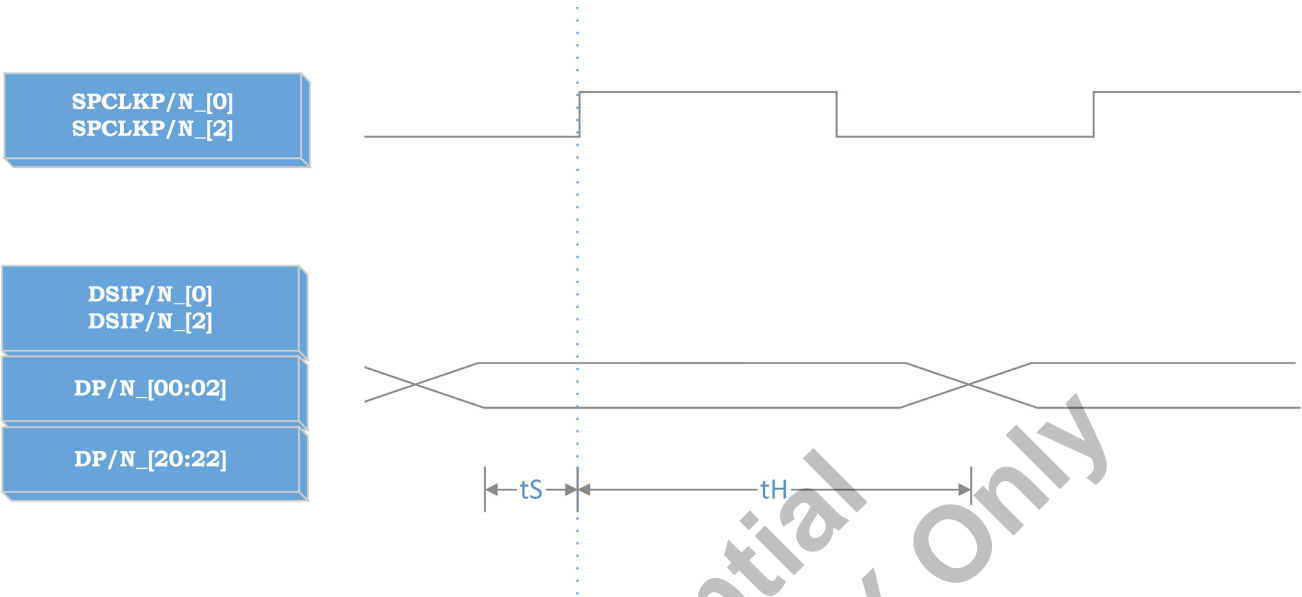


Figure 4-1. Video Input Timing: LVCMOS Mode.

Parameter	Setup (tS)	Hold (tH)	Comment
Data: DSIP/N_0 DSIP/N_2 DP/N_[00:02] DP/N_[20:22]	2 ns	2 ns	Note that LVCMOS mode is supported by VIN0 and VIN2 only.

Table 4-6. LVCMOS Video Input Timing Setup/Hold With Respect to SPCLKP/N_0, SPCLKP/N_2.

4.5.2 Video Input (VIN) Timing: MIPI / SLVS Mode

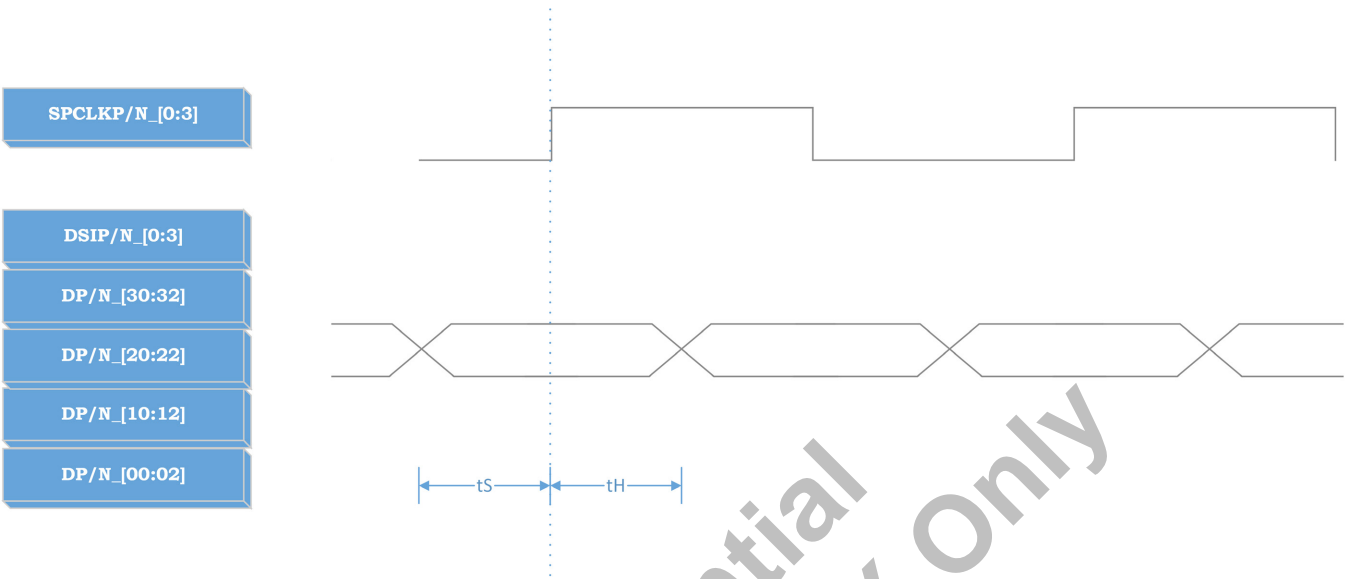


Figure 4-2. Video Input Timing: SLVS / MIPI Mode.

Parameter	Setup (tS)	Hold (tH)	Comment
Data: DSIP/N_[0:3] DP/N_[30:32] DP/N_[20:22] DP/N_[10:12] DP/N_[00:02]	150 ps	150 ps	

Table 4-7. SLVS / MIPI Video Input Timing Setup/Hold With Respect to **SPCLKP/N_[0:3]**.

4.5.3 Video Output (VOUT) Timing

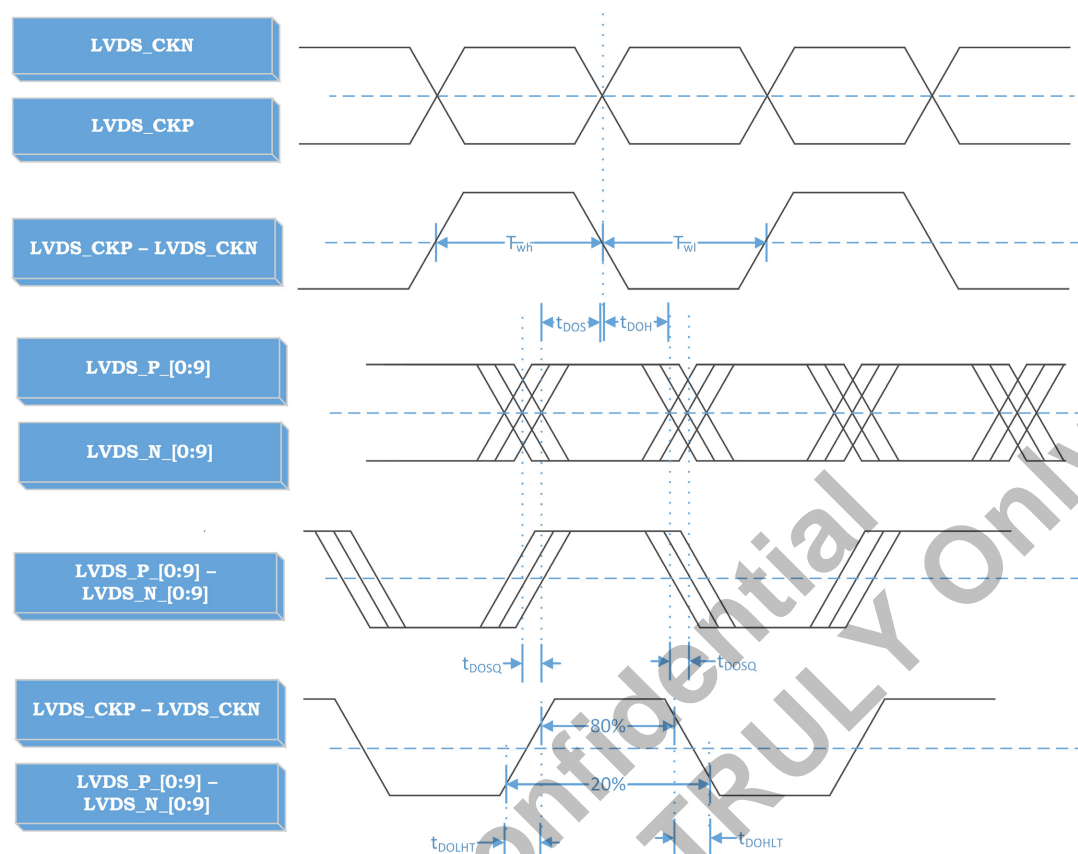


Figure 4-3. Video Output Timing.

Item	Symbol	Min.	Typ.	Max.	Unit	Comments
DO skew time (including jitter)	t_{DOSQ}			361	ps	Data rate 350 MHz DDR
DO setup time	t_{DOS}	350			ps	Data rate 350 MHz DDR
DO hold time	t_{DOH}	350			ps	Data rate 350 MHz DDR
DO rise time	t_{DOLHT}		500		ps	Simulated value with load capacitance (4 pF)
DO fall time	t_{DOHLT}		500		ps	Simulated value with load capacitance (4 pF)
DCK duty cycle	D_{DCDCK}	45	50	55	%	
DCK pulse width	$T_{wh} T_{wl}$	1100			ps	Including period jitter

Table 4-8. Video Output Timing Values.

5. PACKAGE

The B5Nd chip has a 168-pin TFBGA package (10 mm x 10 mm).

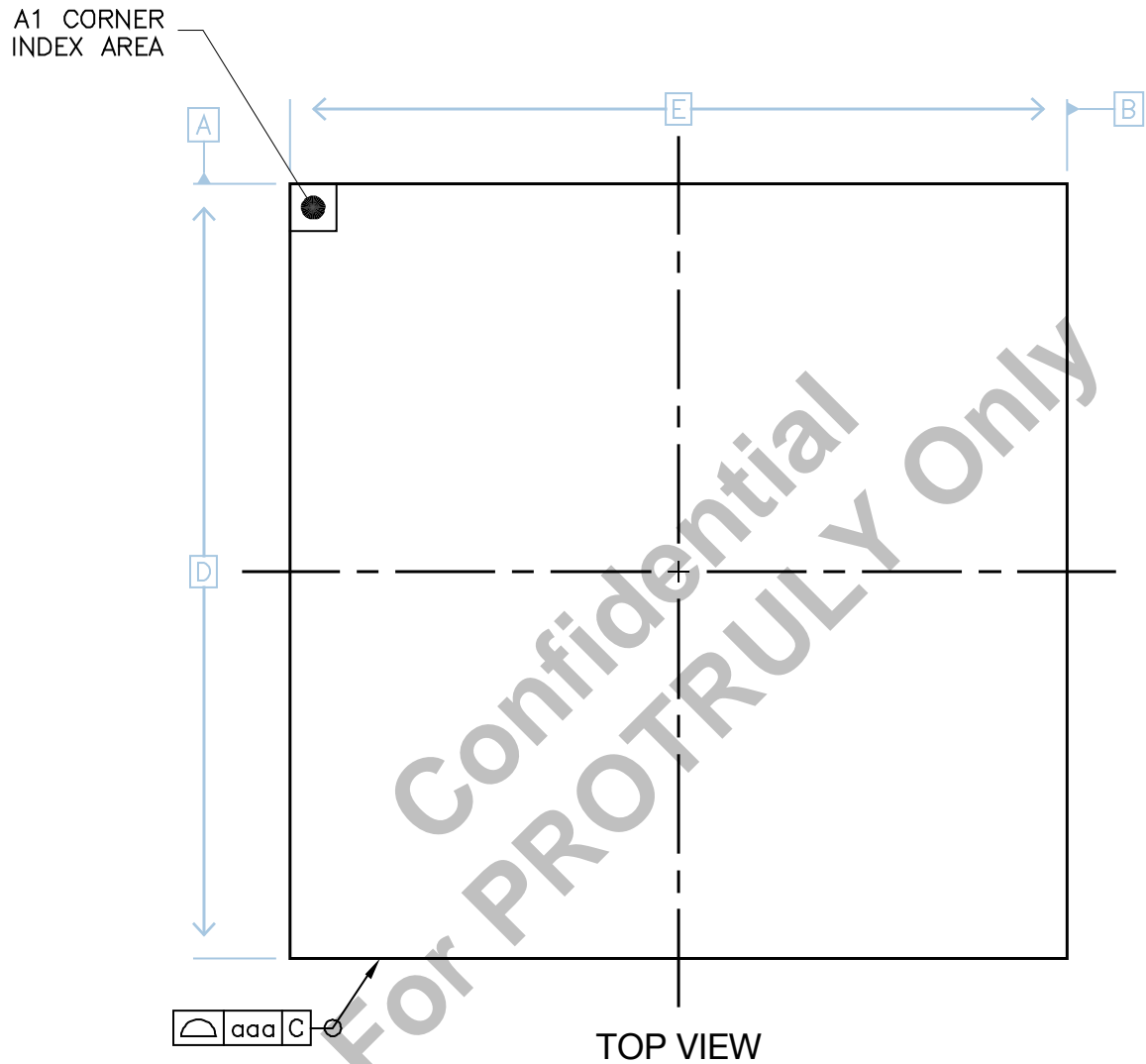


Figure 5-1. Top View of the B5Nd Package.

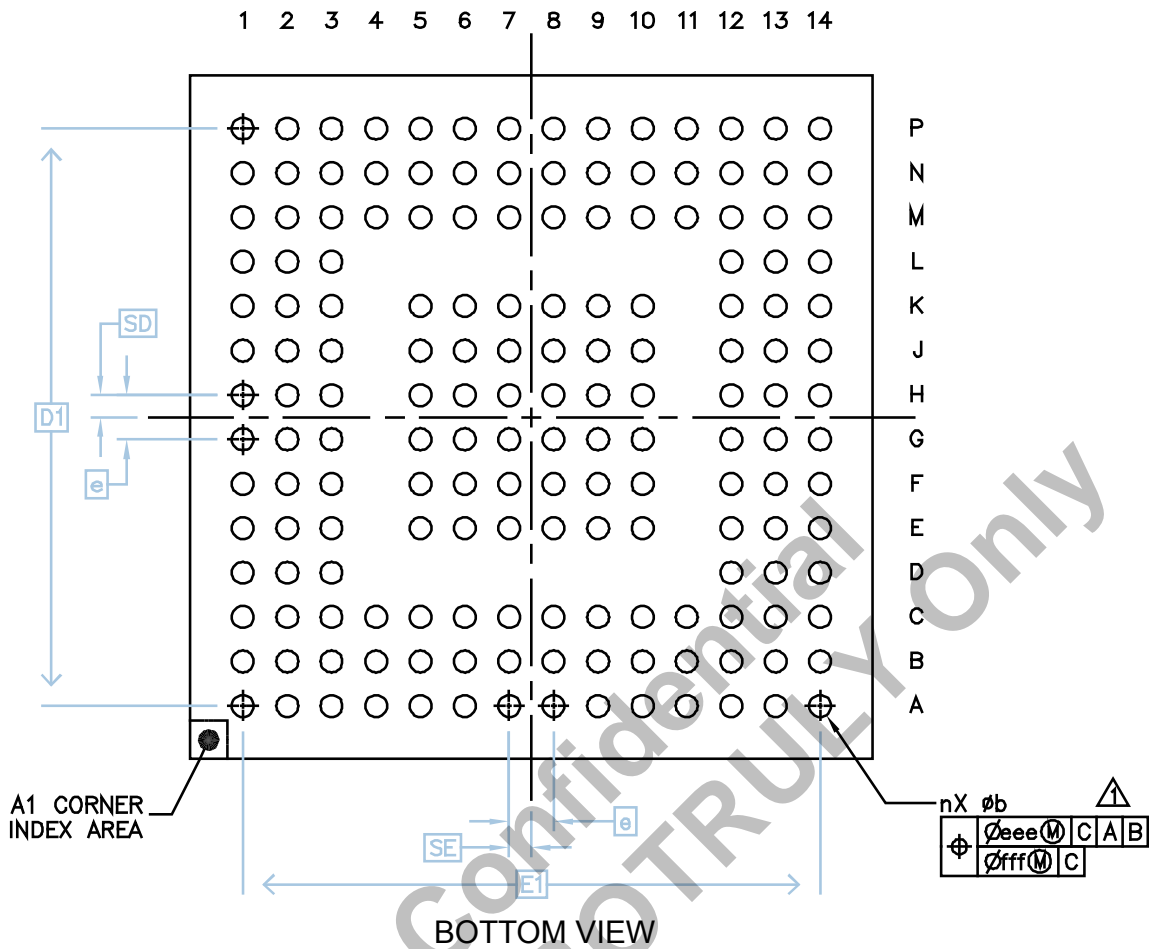


Figure 5-2. Bottom View of the B5Nd Package.

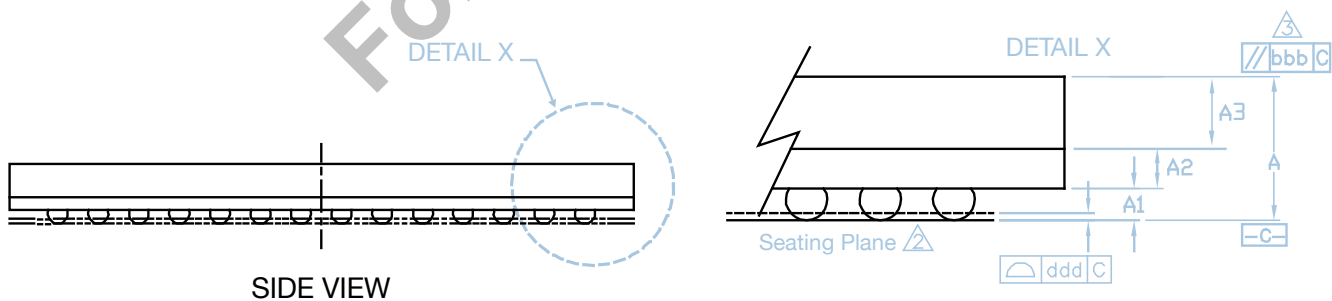


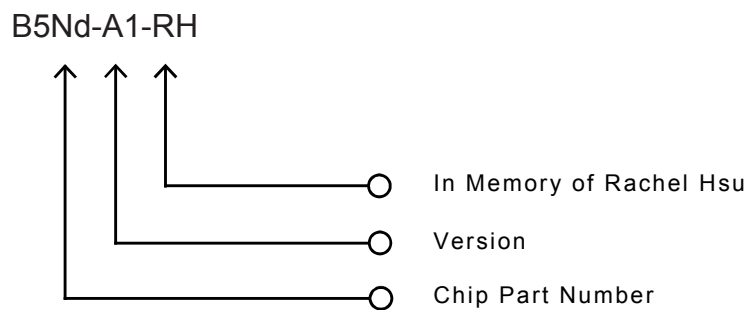
Figure 5-3. Side View with Seating Plane for the B5Nd Package.

Description		Symbol	Minimum	Nominal	Maximum
Total thickness		A			1.1
Stand off		A1	0.16		0.26
Substrate thickness		A2		0.21 REF	
Mold thickness		A3		0.54 REF	
Body size	X	D		10 BSC	
	Y	E		10 BSC	
Ball diameter				0.3	
Ball opening				0.275	
Ball width		b	0.27		0.37
Ball pitch		e		0.65 BSC	
Ball count		n		168	
Edge ball center to center		D1		8.45 BSC	
		E1		8.45 BSC	
Body center to contact ball		SD		0.325 BSC	
		SE		0.325 BSC	
Package edge tolerance		aaa		0.1	
Mold flatness		bbb		0.1	
Coplanarity		ddd		0.08	
Ball offset (package)		eee		0.15	
Ball offset (ball)		fff		0.08	

Table 5-1. Dimensions of the B5Nd Package (Millimeters).

6. CONTACT AND ORDER INFORMATION

All chips in the B5 series are Lead-Free, Halogen-Free and RoHS compliant.



For complete Ambarella contact information, please visit www.ambarella.com.

7. PIN LIST AND MAPPING TABLE

This chapter provides a list of the 168 external pins according to their location on the B5Nd chip. The figure below indicates the orientation of the pins by column (numbers) and row (letters).

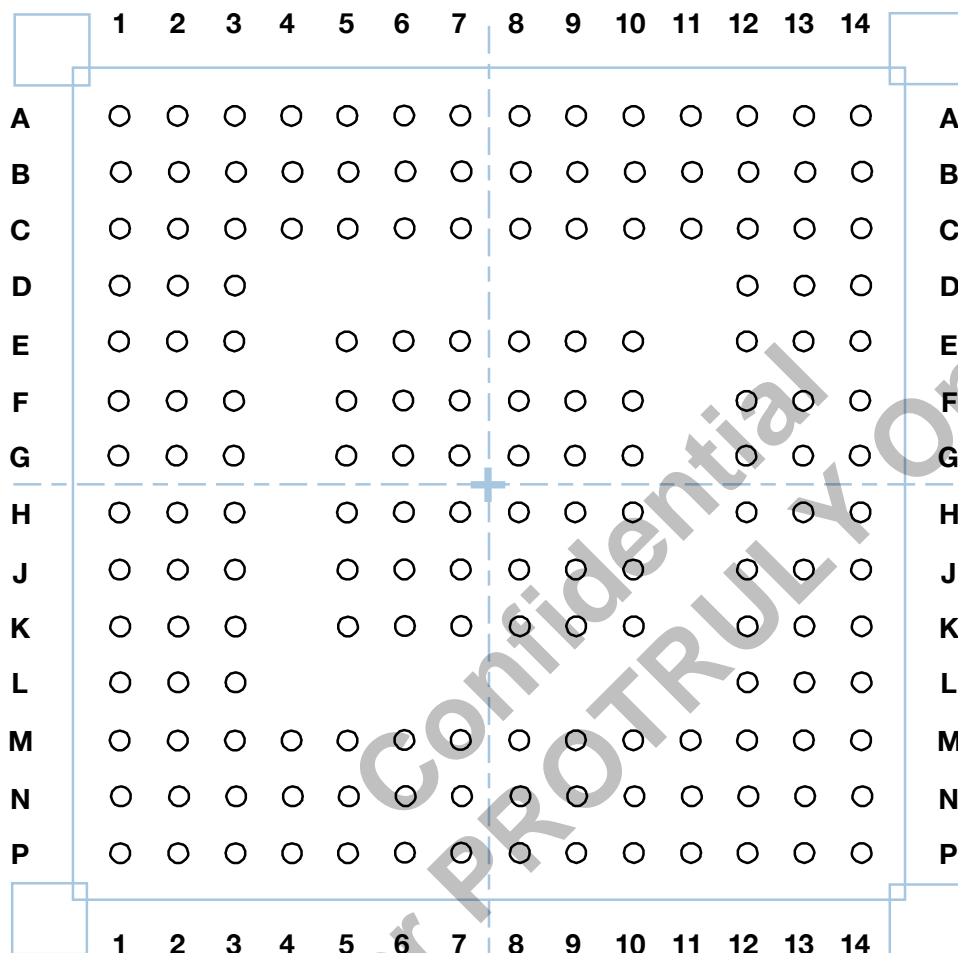


Figure 7-1. Pin Map for the B5Nd Chip.

The following table lists all of the external pins on the B5Nd chip in alphabetic order by map location. Each entry provides the pin name as it appears on the ball map, the location of the pin on the map and on schematics, the functional group, and multiplexed functionality detail if applicable.

Loc.	Pin Name	Group	Multiplexed Functions			
			First	Second	Third	GPIO
A1	SPI_CLK	Sensor Config	spi_clk	i2c1_scl2	uart_ahbm_clk	4
A2	B5F_1_RST_L	Power / Reset	por_l_brdcst			19

Loc.	Pin Name	Group	Multiplexed Functions			
			First	Second	Third	GPIO
A3	REPEATER_MODE	System				
A4	B5F_0_RST_L	Power / Reset	por_l_brdcst			18
A5	Reserved	Sensor				17
A6	HSYNC1	Sensor	vin_hsync1			13
A7	I2C1_SDA1	Sensor Config	i2c1_sda1		pwm_ls_tx_out3	3
A8	CFG_SPI_CLK	DSP Con-fig				
A9	VSNC1	Sensor	vin_vsync1			12
A10	GPIO_8	Board Control				30
A11	CKN_0	LVDS				
A12	LVDS_N_0	LVDS				
A13	LVDS_N_1	LVDS				
A14	LVDS_P_1	LVDS				
B1	Reserved	Power / Reset	por_l_brdcst			21
B2	SPI_MISO	Sensor Config	spi_miso	i2c1_sda3		7
B3	SPI_EN0	Sensor Config	spi_en0	i2c1_sda2		5
B4	Reserved	Sensor				16
B5	POR_L	System				
B6	Reserved	Sensor				15
B7	SPI_MOSI	Sensor Config	spi_mosi	i2c1_scl3		6
B8	I2C1_SCL1	Sensor Config	i2c1_scl1	spi_en3	pwm_ls_tx_out2	2
B9	GPIO_5	Board Control	pll_obsrv_core			27
B10	GPIO_9	Board Control				31
B11	CKP_0	LVDS				
B12	LVDS_P_0	LVDS				
B13	LVDS_P_6	LVDS				
B14	LVDS_N_6	LVDS				
C1	XOUT	System				
C2	Reserved	Power / Reset				20
C3	Reserved	Sensor				14
C4	CLK_REF_SEL	System				
C5	CLK_SI	System				
C6	I2C0_SDA	Camera Interface	i2c0_sda	uart_ahbm_tx		9

Loc.	Pin Name	Group	Multiplexed Functions			
			First	Second	Third	GPIO
C7	I2C0_SCL	Camera Interface	i2c0_scl	uart_ahbm_rx		8
C8	TEST_MODE	System				
C9	GPIO_0	Board Control				22
C10	CFG_SPI_EN	DSP Con-fig				
C11	GPIO_7	Board Control	pll_obsrv_sensor			29
C12	GPIO_6	Board Control	pll_obsrv_phy			28
C13	LVDS_P_2	LVDS				
C14	LVDS_N_2	LVDS				
D1	I2C1_SDA0	Sensor Config	i2c1_sda0	spi_en2	pwm_ls_tx_out1	1
D2	XIN	System				
D3	CFG_SPI_MOSI	DSP Con-fig				
D12	LVDS_VDDA25_D12	Power				
D13	CKP_1	LVDS				
D14	CKN_1	LVDS				
E1	CFG_SPI_MISO	DSP Con-fig				
E2	I2C1_SCL0	Sensor Config	i2c1_scl0	spi_en1	pwm_ls_tx_out0	0
E3	REXT	Band Gap				
E5	VDDA25_PLL_E5	Power				
E6	VDDA25_PLL_E6	Power				
E7	VDDA10_PLL_E7	Power				
E8	VDDA10_PLL_E8	Power				
E9	VSSI_E9	Power				
E10	LVDS_AVSS	Power				
E12	LVDS_VDDA25_E12	Power				
E13	LVDS_CKP	LVDS				
E14	LVDS_CKN	LVDS				
F1	DSIN_3	MIPI PHY				
F2	DSIP_3	MIPI PHY				
F3	IRQ	IRQ				
F5	VDDO_F5	Power				
F6	VSSA_PLL_F6	Power				
F7	VSSA_PLL_F7	Power				
F8	VSSO_F8	Power				
F9	VSSI_F9	Power				
F10	LVDS_AVSS_F10	Power				

Loc.	Pin Name	Group	Multiplexed Functions			
			First	Second	Third	GPIO
F12	LVDS_VDDA25_F12	Power				
F13	CKP_2	LVDS				
F14	CKN_2	LVDS				
G1	DN_31	MIPI PHY				
G2	DP_31	MIPI PHY				
G3	PACKAGE_ID	System				
G5	VDDO_G5	Power				
G6	VDDO_G6	Power				
G7	VSSO_G7	Power				
G8	VSSO_G8	Power				
G9	VSSI_G9	Power				
G10	LVDS_AVSS_G10	Power				
G12	LVDS_VDDA25_G12	Power				
G13	LVDS_P_3	LVDS				
G14	LVDS_N_3	LVDS				
H1	DSIN_2	MIPI PHY				
H2	DSIP_2	MIPI PHY				
H3	EFUSE_VQPS	EFUSE				
H5	VDDO_H5	Power				
H6	VSSO_H6	Power				
H7	VSSO_H7	Power				
H8	VSSI_H8	Power				
H9	VSSI_H9	Power				
H10	VDDI_H10	Power				
H12	LVDS_AVSS_H12	Power				
H13	LVDS_P_7	LVDS				
H14	LVDS_N_7	LVDS				
J1	DN_32	MIPI PHY				
J2	DP_32	MIPI PHY				
J3	VSYNCO	Sensor	vin_vsync0	irq		10
J5	VDDO_J5	Power				
J6	VSSO_J6	Power				
J7	VDDI_J7	Power				
J8	VDDI_J8	Power				
J9	VDDI_J9	Power				
J10	VDDI_J10	Power				
J12	LVDS_AVSS_J12	Power				
J13	LVDS_P_4	LVDS				
J14	LVDS_N_4	LVDS				
K1	SPCLKN_3	MIPI PHY				
K2	SPCLKP_3	MIPI PHY				
K3	GPIO_3	Board Control				25



Loc.	Pin Name	Group	Multiplexed Functions			
			First	Second	Third	GPIO
K5	MPHY_VSSA25_K5	Power				
K6	MPHY_VSSA25_K6	Power				
K7	MPHY_VSSA25_K7	Power				
K8	MPHY_VSSA25_K8	Power				
K9	MPHY_VDDAIO_K9	Power				
K10	MPHY_VDDAIO_K10	Power				
K12	LVDS_VDDA12_K12	Power				
K13	LVDS_P_5	LVDS				
K14	LVDS_N_5	LVDS				
L1	DN_30	MIPI PHY				
L2	DP_30	MIPI PHY				
L3	GPIO_2	Board Control				24
L12	LVDS_VDDA12_L12	Power				
L13	CKP_3	LVDS				
L14	CKN_3	LVDS				
M1	DN_22	MIPI PHY				
M2	DP_22	MIPI PHY				
M3	GPIO_1	Board Control				23
M4	HSYNC0	Sensor	vin_hsync0	por_l_brdcst		11
M5	GPIO_4	Board Control				26
M6	MPHY_VDDA12_M6	Power				
M7	MPHY_VDDA12_M7	Power				
M8	MPHY_VDDA12_M8	Power				
M9	MPHY_VDDA12_M9	Power				
M10	MPHY_VDDA25_M10	Power				
M11	MPHY_VDDA25_M11	Power				
M12	MPHY_VDDA25_M12	Power				
M13	LVDS_P_8	LVDS				
M14	LVDS_N_8	LVDS				
N1	SPCLKN_2	MIPI PHY				
N2	SPCLKP_2	MIPI PHY				
N3	DP_20	MIPI PHY				

Loc.	Pin Name	Group	Multiplexed Functions			
			First	Second	Third	GPIO
N4	DSIP_0	MIPI PHY				
N5	DP_02	MIPI PHY				
N6	SPCLKP_0	MIPI PHY				
N7	DN_01	MIPI PHY				
N8	DP_00	MIPI PHY				
N9	DSIP_1	MIPI PHY				
N10	DP_12	MIPI PHY				
N11	SPCLKP_1	MIPI PHY				
N12	DN_11	MIPI PHY				
N13	LVDS_P_9	LVDS				
N14	LVDS_N_9	LVDS				
P1	DN_21	MIPI PHY				
P2	DP_21	MIPI PHY				
P3	DN_20	MIPI PHY				
P4	DSIN_0	MIPI PHY				
P5	DN_02	MIPI PHY				
P6	SPCLKN_0	MIPI PHY				
P7	DP_01	MIPI PHY				
P8	DN_00	MIPI PHY				
P9	DSIN_1	MIPI PHY				
P10	DN_12	MIPI PHY				
P11	SPCLKN_1	MIPI PHY				
P12	DP_11	MIPI PHY				
P13	DN_10	MIPI PHY				
P14	DP_10	MIPI PHY				

Table 7-1. Pin List and Mapping Table for the B5Nd Chip.

8. IMPORTANT NOTICE

All Ambarella design specifications, datasheets, drawings, files, and other documents (together and separately, “materials”) are provided on an “as is” basis, and Ambarella makes no warranties, expressed, implied, statutory, or otherwise with respect to the materials, and expressly disclaims all implied warranties of noninfringement, merchantability, and fitness for a particular purpose. The information contained herein is believed to be accurate and reliable. However, Ambarella assumes no responsibility for the consequences of use of such information.

Ambarella Incorporated reserves the right to correct, modify, enhance, improve, and otherwise change its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

All products are sold subject to Ambarella’s terms and conditions of sale supplied at the time of order acknowledgment. Ambarella warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with its standard warranty. Testing and other quality control techniques are used to the extent Ambarella deems necessary to support this warranty.

Ambarella assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using Ambarella components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

Ambarella does not warrant or represent that any license, either expressed or implied, is granted under any Ambarella patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which Ambarella products or services are used. Information published by Ambarella regarding third-party products or services does not constitute a license from Ambarella to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Ambarella under the patents or other intellectual property of Ambarella.

Reproduction of information from Ambarella documents is not permissible without prior approval from Ambarella.

Ambarella products are not authorized for use in safety-critical applications (such as life support) where a failure of the product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Customers acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of Ambarella products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by Ambarella. Further, Customers must fully indemnify Ambarella and its representatives against any damages arising out of the use of Ambarella products in such safety-critical applications.

Ambarella products are neither designed nor intended for use in military/aerospace applications or environments. Customers acknowledge and agree that any such use of Ambarella products is solely at the Customer’s risk, and they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

9. TYPOGRAPHICAL CONVENTIONS

This document provides technical detail using a set of consistent typographical conventions to help the user differentiate key concepts at a glance.

Conventions include:

Example	Description
AmbaGuiGen, DirectUSB Save, File > Save Power, Reset, Home	Software names GUI commands and command sequences Computer / Hardware buttons
Flash_IO_control da, status, enable	Register names and register fields. For example, Flash_IO_control is the register for global control of Flash I/O, and bit 17 (da) is used for DMA acknowledgement.
GPIO81, CLK_AU	Hardware external pins
VIL, VIH, VOL, VOH	Hardware pin parameters
INT_O, RXDATA_I	Hardware pin signals
amb_performance_t amb_operating_mode_t amb_set_operating_mode()	API details (e.g., functions, structures, and type definitions)
/usr/local/bin success = amb_set_operating_ mode (amb_hal_base_address, & operating_mode)	User entries into software dialogues and GUI windows File names and paths Command line scripting and Code

Table 9-1. *Typographical Conventions for Technical Documents.*

Additional Ambarella typographical conventions include:

- Acronyms are given in UPPER CASE using the default font (e.g., AHB, ARM11 and DDRIO).
- Names of Ambarella documents and publicly available standards, specifications, and databooks appear in *italic* type.

10. REVISION HISTORY

NOTE: Page/chapter numbers for previous drafts may differ from those in the current version.

Version	Date	Comments
1.0	14 Feb 2014	New B5 Part
1.1	25 Apr 2014	Update electrical characteristics
1.2	22 Oct 2014	Update throughput specification
1.3	24 Sep 2015	Update operating temperature range to -20 C ~ +85 C

Confidential
For PROTRULY Only