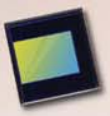
OmniVision



datasheet

PRELIMINARY SPECIFICATION

1/3" color CMOS 4 megapixel (2688 x 1520) image sensor
with improved OmniBSI-2™ technology

OV4689

color CMOS 4 megapixel (2688 x 1520) image sensor with OmniBSI-2™ technology

datasheet (CSP5)
PRELIMINARY SPECIFICATION

version 1.2
september 2013

To learn more about OmniVision Technologies, visit www.ovt.com.
OmniVision Technologies is publicly traded on NASDAQ under the symbol OVTI.

applications

- IP cameras
- sports cameras
- automotive

ordering information

- **OV04689-H67A** (color, lead-free)
  67-pin CSP5

features

- automatic black level calibration (ABLC)
- programmable controls for frame rate, mirror and flip, cropping, and windowing
- static defective pixel canceling
- supports output formats: 10-bit RAW RGB (MIPI)
- supports horizontal and vertical subsampling
- supports images sizes: 4Mpixel, 3Mpixel, EIS1080p, 1080p, EIS720p
- fast mode switching
- support 2x2 binning, 4x4 binning, re-sampling filter
- standard serial SCCB interface
- up to 4-lane MIPI serial output interface
- embedded 4K bits one-time programmable (OTP) memory for part identification, etc (see **sidebar note**)
- two on-chip phase lock loops (PLLs)
- programmable I/O drive capability
- built-in temperature sensor

note Only1.5K bits of OTP is available for customer's use.

key specifications (typical)

- **active array size:** 2688 x 1520
- **power supply:**
  core: 1.1 ~ 1.3V
  analog: 2.6 ~ 3.0V
  I/O: 1.7 ~ 3.0V
- **power requirements:**
  active: 163 mA (261 mW)
  standby: 1 mA
  XSHUTDOWN: <10 µA
- **temperature range:**
  operating: -30°C to +85°C junction temperature (see **table 7-2**)
  stable image: 0°C to +60°C junction temperature (see **table 7-2**)
- **output formats:** 10-bit RAW
- **lens size:** 1/3"
- **input clock frequency:** 6~64 MHz
- **lens chief ray angle:** 0°
- **max S/N ratio:** 38.3 dB
- **dynamic range:** 64.6 dB @ 1x gain
- **maximum image transfer rate:**
  2688x1520: 90 fps (see **table 2-1**)
  1280x720: 180 fps (see **table 2-1**)
  1920x1080: 120 fps (see **table 2-1**)
  672x380: 330 fps (see **table 2-1**)
- **sensitivity:** 1900 mV/Lux-sec
- **scan mode:** progressive
- **maximum exposure interval:** 1548 $\times T_{ROW}$
- **pixel size:** 2 µm x 2 µm
- **dark current:** 4mV/sec @ 60°C junction temperature
- **image area:** 5440 µm x 3072 µm
- **package dimensions:** 6630 µm x 5830 µm

note Higher junction temperature degrades image quality

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1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pin numbers for the OV4689 image sensor. The package information is shown in section 8.

table 1-1 signal descriptions (sheet 1 of 3)

pin number	signal name	pin type	description
A1	NC	–	no connect
A2	DVDD	power	power for digital circuit
A3	AVDD	power	power for analog circuit
A4	DOVDD	power	power for I/O circuit
A5	ATEST0	reference	analog reference test output
A6	DVDD	power	power for digital circuit
A7	IL_PWM	I/O	no connect in system
A8	AVDD	power	power for analog circuit
A9	NC	–	no connect
B1	AGND	ground	ground for analog circuit
B2	DOGND	ground	ground for digital circuit
B3	DOGND	ground	ground for digital circuit
B4	AVDD	power	power for analog circuit
B5	XSHUTDOWN	input	reset and power down (active low with internal pull down resistor)
B6	DOGND	ground	ground for digital circuit
B7	PVDD	power	power for analog circuit
B8	DVDD	power	power for digital circuit
B9	DVDD	power	power for digital circuit
C1	AVDD	power	power for analog circuit
C2	VH	reference	internal analog reference
C3	VN	reference	internal analog reference
C4	DVDD	power	power for digital circuit
C5	PWDNB	input	power down (active low with internal pull up resistor)
C6	NC	–	no connect
C7	GPIO	I/O	general purpose input/output

table 1-1 signal descriptions (sheet 2 of 3)

pin number	signal name	pin type	description
C8	AGND	ground	ground for analog circuit
C9	DOGND	ground	ground for digital circuit
D1	NC	–	no connect
D9	NC	–	no connect
E1	DVDD	power	power for digital circuit
E9	FREX	I/O	frame exposure control
F1	DOGND	ground	ground for digital circuit
F2	MDP0	I/O	MIPI TX data lane 0 positive output
F3	MDN0	I/O	MIPI TX data lane 0 negative output
F4	MDP1	I/O	MIPI TX data lane 1 positive output
F5	MDN1	I/O	MIPI TX data lane 1 negative output
F6	DOVDD	power	power for I/O circuit
F7	STROBE	I/O	strobe control
F8	TM	input	test mode (active high with internal pull down resistor)
F9	FSIN	I/O	frame sync I/O
G1	AGND	ground	ground for analog circuit
G2	MDP2	I/O	MIPI TX data lane 2 positive output
G3	EVDD	power	power for MIPI circuit (connect to DVDD)
G4	EVDD	power	power for MIPI circuit (connect to DVDD)
G5	EGND	ground	ground for MIPI circuit
G6	SIOC	input	SCCB input clock
G7	DOVDD	power	power for I/O circuit
G8	HREF	I/O	HREF output
G9	DOGND	ground	ground for digital circuit
H1	AVDD	power	power for analog circuit
H2	MDN2	I/O	MIPI TX data lane 2 negative output
H3	EGND	ground	ground for MIPI circuit
H4	MCP	I/O	MIPI TX clock lane positive output
H5	MDN3	I/O	MIPI TX data lane 3 negative output
H6	DOGND	ground	ground for digital circuit

table 1-1 signal descriptions (sheet 3 of 3)

pin number	signal name	pin type	description
H7	SIOD	I/O	SCCB data I/O
H8	VSYNC	I/O	VSYNC output
H9	DVDD	power	power for digital circuit
J1	NC	–	no connect
J2	EGND	ground	ground for MIPI circuit
J3	PVDD	power	power for analog circuit
J4	MCN	I/O	MIPI TX clock lane negative output
J5	MDP3	I/O	MIPI TX data lane 3 positive output
J6	DVDD	power	power for digital circuit
J7	EXTCLK	input	system input clock
J8	SID	input	SCCB address selection 0: Select ID1 when SID = 0 or ID2 when SID = 1 1: Select ID2 when SID = 0 or ID1 when SID = 1
J9	NC	–	no connect

table 1-2 configuration under various conditions (sheet 1 of 2)

pin	signal name	RESET[a]	after RESET release[b]	software standby[c]	hardware standby[d]
B5	XSHUTDOWN	input	input	input	input
C5	PWDNB	input	input	input	input
C7	GPIO	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
E9	FREX	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
F2	MDP0	high-z	high	high by default (configurable)	high by default (configurable)
F3	MDN0	high-z	high	high by default (configurable)	high by default (configurable)
F4	MDP1	high-z	high	high by default (configurable)	high by default (configurable)
F5	MDN1	high-z	high	high by default (configurable)	high by default (configurable)
F7	STROBE	low	low	low by default	low by default

table 1-2 configuration under various conditions (sheet 2 of 2)

pin	signal name	RESET[a]	after RESET release[b]	software standby[c]	hardware standby[d]
F8	TM	input	input	input	input
F9	FSIN	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
G2	MDP2	high-z	high	high by default (configurable)	high by default (configurable)
G6	SIOC	high-z	input	input	high-z
G8	HREF	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
H2	MDN2	high-z	high	high by default (configurable)	high by default (configurable)
H4	MCP	high-z	high	high by default (configurable)	high by default (configurable)
H5	MDN3	high-z	high	high by default (configurable)	high by default (configurable)
H7	SIOD	open drain	I/O	I/O	open drain
H8	VSYNC	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
J4	MCN	high-z	high	high by default (configurable)	high by default (configurable)
J5	MDP3	high-z	high	high by default (configurable)	high by default (configurable)
J7	EXTCLK	high-z	input	input	high-z
J8	SID	input	input	input	input

a. XSHUTDOWN = 0
b. XSHUTDOWN from 0 to 1
c. sensor set to sleep from streaming mode
d. sensor set to hardware standby from streaming mode by pulling PWDNB = 0

figure 1-1 pin diagram

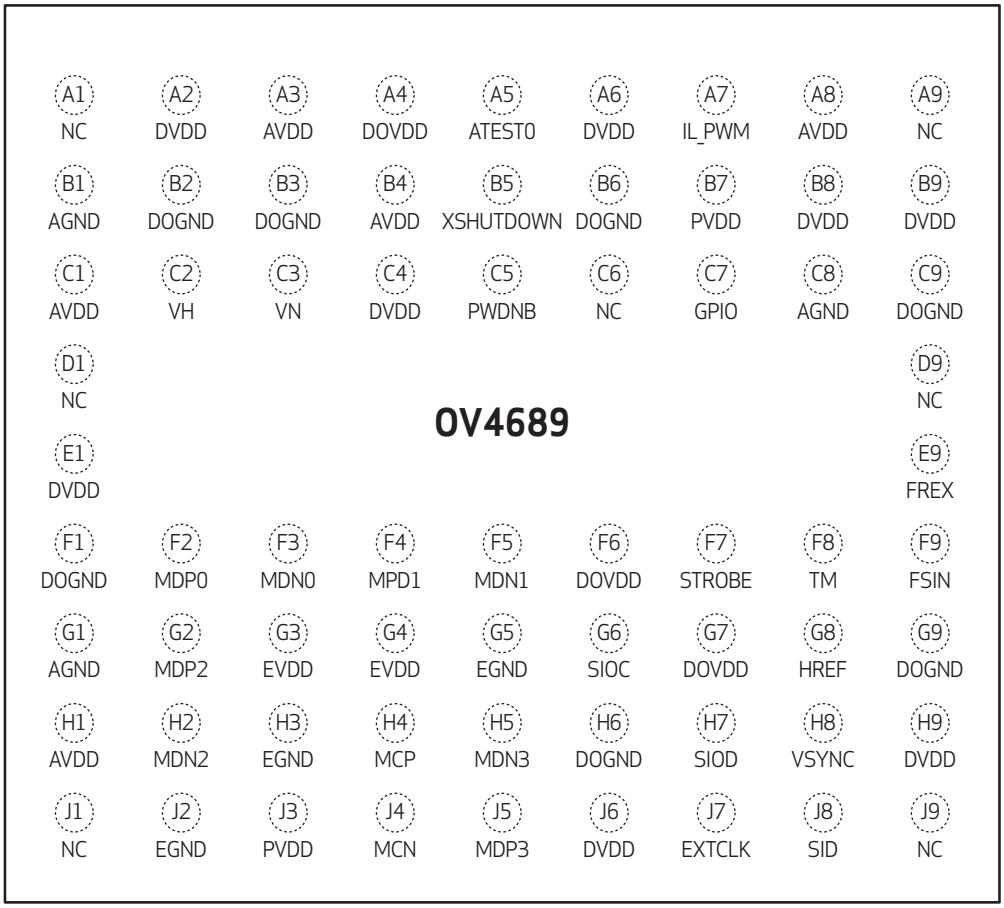

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table 1-3 pad symbol and equivalent circuit (sheet 1 of 2)

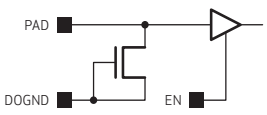
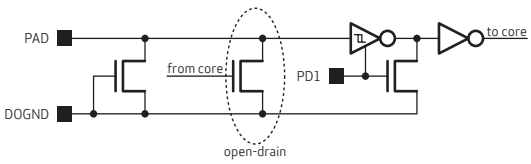
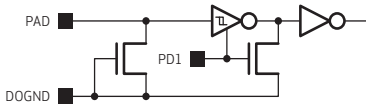
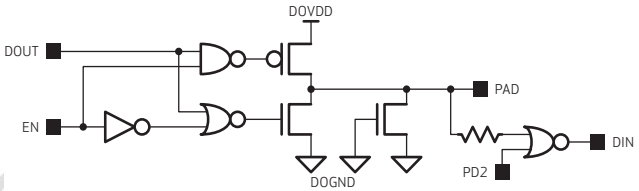
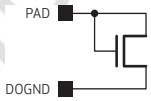
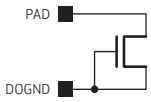
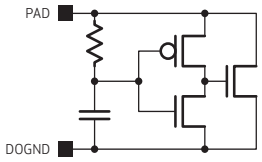
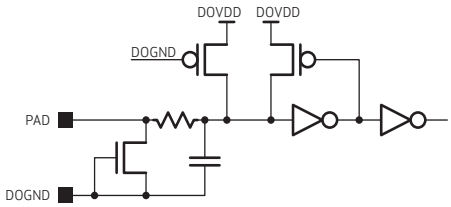
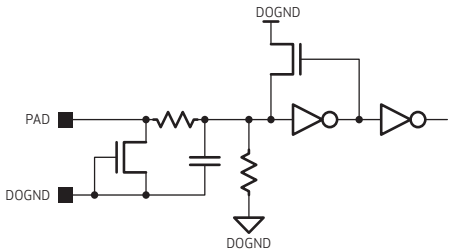
symbol	equivalent circuit
EXTCLK	
SIOD	

table 1-3 pad symbol and equivalent circuit (sheet 2 of 2)

symbol	equivalent circuit
SIOC	
VSYNC, STROBE, FREX, FSIN, GPIO	
VN, VH	
MDP3, MDP2, MDP1, MDP0, MDN3, MDN2, MDN1, MDN0, MCP, MCN, EGND, AGND, DOGND	
AVDD, EVDD, DVDD, DOVDD, PVDD	
PWDNB	
XSHUTDOWN, SID, TM	

2 system level description

2.1 overview

The OV4689 color image sensor is a high performance, 4 megapixel RAW image sensor that delivers 2688x1520 at 90 fps using OmniBSI-2™ pixel technology. Users can program image resolution, frame rate, image quality parameters and camera functions are controlled using the industry standard serial camera control bus (SCCB).

The OV4689 provides various kinds of HDR modes to increase dynamic range as well as maintain higher frame rate.

All required image processing functions are programmable through the SCCB interface. In addition, OmniVision image sensors utilize proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, etc., to produce a clean, fully stable, color image.

2.2 architecture

The OV4689 sensor core generates streaming pixel data at a constant frame rate. **figure 2-1** shows the functional block diagram of the OV4689 image sensor.

The timing generator outputs clocks to access the rows of the imaging array, pre charging and sampling the rows of the array sequentially. In the time between pre charging and sampling a row, the charge in the pixels decreases with exposure to incident light. This is the exposure time in rolling shutter architecture.

The exposure time is controlled by adjusting the time interval between pre charging and sampling. After the data of the pixels in the row has been sampled, it is processed through analog circuitry to correct the offset and multiply the data with corresponding gain. Following analog processing is the ADC which outputs up to 10-bit data for each pixel in the array.

figure 2-1 OV4689 block diagram

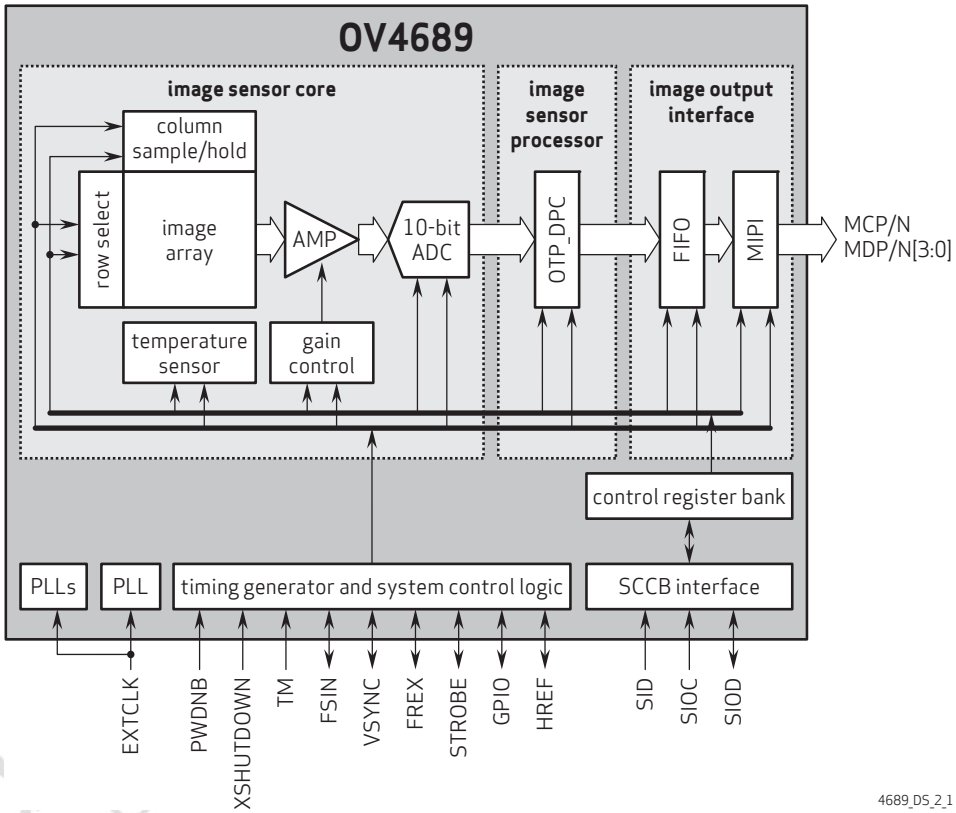
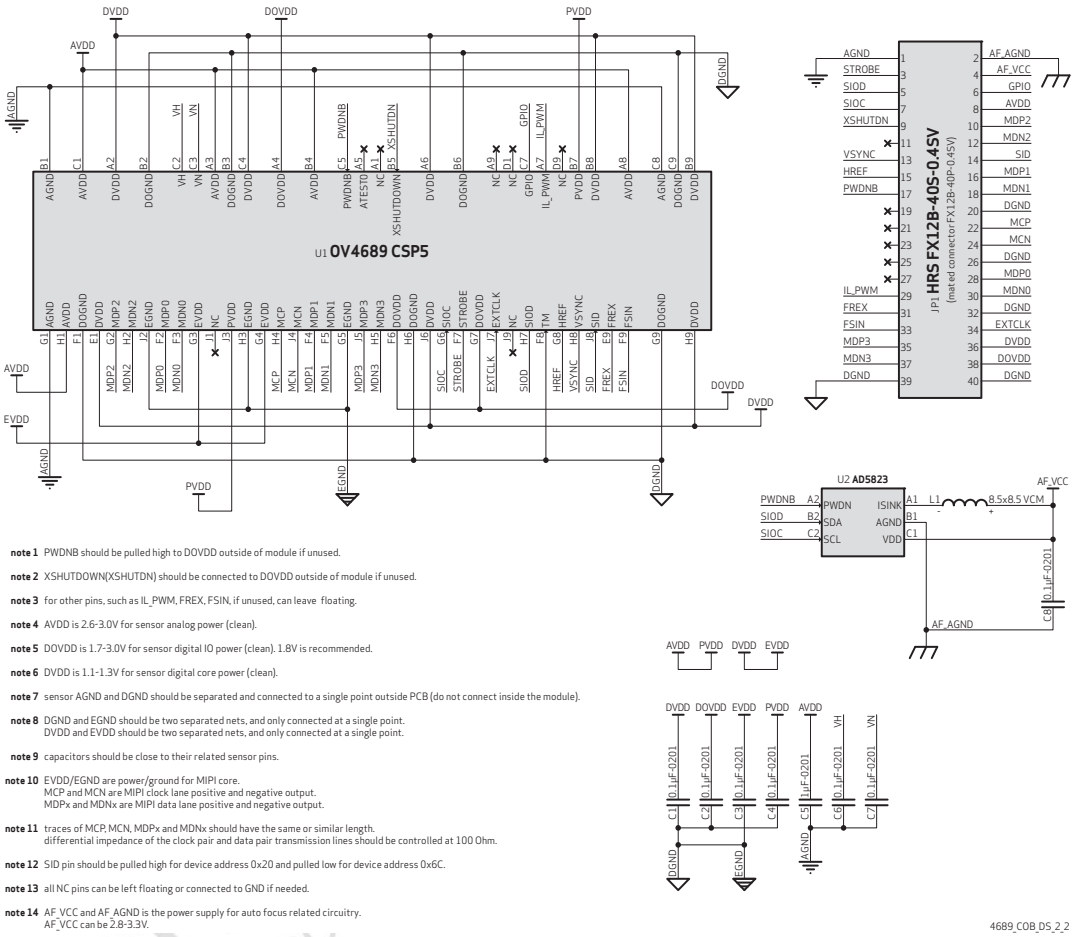


figure 2-2 reference schematic



note 1 PWDNB should be pulled high to DOVDD outside of module if unused.

note 2 XSHUTDOWN(XSHUTDN) should be connected to DOVDD outside of module if unused.

note 3 for other pins, such as IL_PWM, FREX, FSIN, if unused, can leave floating.

note 4 AVDD is 2.6-3.0V for sensor analog power (clean).

note 5 DOVDD is 1.7-3.0V for sensor digital IO power (clean). 1.8V is recommended.

note 6 DVDD is 1.1-1.3V for sensor digital core power (clean).

note 7 sensor AGND and DGND should be separated and connected to a single point outside PCB (do not connect inside the module).

note 8 DGND and EGND should be two separated nets, and only connected at a single point.
DVDD and EVDD should be two separated nets, and only connected at a single point.

note 9 capacitors should be close to their related sensor pins.

note 10 EVDD/EGND are power/ground for MIPI core.
MCP and MCN are MIPI clock lane positive and negative output.
MDPx and MDNx are MIPI data lane positive and negative output.

note 11 traces of MCP, MCN, MDPx and MDNx should have the same or similar length.
differential impedance of the clock pair and data pair transmission lines should be controlled at 100 Ohm.

note 12 SID pin should be pulled high for device address 0x20 and pulled low for device address 0x6C.

note 13 all NC pins can be left floating or connected to GND if needed.

note 14 AF_VCC and AF_AGND is the power supply for auto focus related circuitry.
AF_VCC can be 2.8-3.3V.

4689_COB_DS_2.2

2.3 format and frame

The OV4689 supports RAW RGB output with one/two/four lane MIPI interface.

table 2-1 non HDR mode frame rate

resolution	10-bit output	10-bit output MIPI 4 lanes	methodology
2688x1520	90 fps	1000 Mbps/lane	full
1280x720	180 fps	1000 Mbps/lane	2x2 binning or 2:1 skipping
1920x1080	120 fps	1000 Mbps/lane	cropping
672x380	330 fps	1000 Mbps/lane	4x4 binning or 4:1 skipping

table 2-2 staggered HDR mode frame rate

resolution	10-bit output	10-bit output MIPI 4 lanes	methodology
2688 x 1520 staggered 2	45 fps	1000 Mbps/lane	full
1280x720 staggered 2	90 fps	1000 Mbps/lane	2x2 binning or 2:1 skipping
2688 x 1520 staggered 3	30 fps	1000 Mbps/lane	full
1280x720 staggered 3	60 fps	1000 Mbps/lane	2x2 binning or 2:1 skipping

2.4 I/O control

The OV4689 can configure its I/O pad as an input or output. For the output signal, it follows one of two paths either from the data path or from register control.

table 2-3 I/O control registers

function	register	description
output drive capability control	0x3011	Bit[6:5]: I/O pin drive capability 00: 1x 01: 2x 10: 3x 11: 4x
HREF I/O control	0x3002	Bit[6]: HREF output enable 0: input 1: output
HREF output select	0x3010	Bit[6]: enable HREF as GPIO controlled by register
HREF output value	0x300D	Bit[6]: register control HREF output
GPIO I/O control	0x3002	Bit[0]: GPIO0 output enable 0: input 1: output
GPIO output select	0x3010	Bit[0]: enable GPIO as GPIO controlled by register
GPIO output value	0x300D	Bit[0]: register control GPIO output
VSYNC I/O control	0x3002	Bit[7]: VSYNC output enable 0: input 1: output
VSYNC output select	0x3010	Bit[7]: enable VSYNC as GPIO controlled by register
VSYNC output value	0x300D	Bit[7]: register control VSYNC output

2.5 MIPI interface

The OV4689 supports a MIPI interface of up to 4-lanes. The MIPI interface can be configured for 1/2/3/4-lane.

2.6 power management

Based on the system power configuration (RESETB, PWDN control), the power up sequence will be different. OmniVision recommends cutting off all power supplies, including the external DVDD, when the sensor is not in use.

2.6.1 power up sequence

To avoid any glitch from a strong external noise source, OmniVision recommends controlling XSHUTDOWN or PWDNB by GPIO and tie the other pin to DOVDD.

Whether or not XSHUTDOWN is controlled by GPIO, the XSHUTDOWN rising cannot occur before AVDD, and DOVDD.

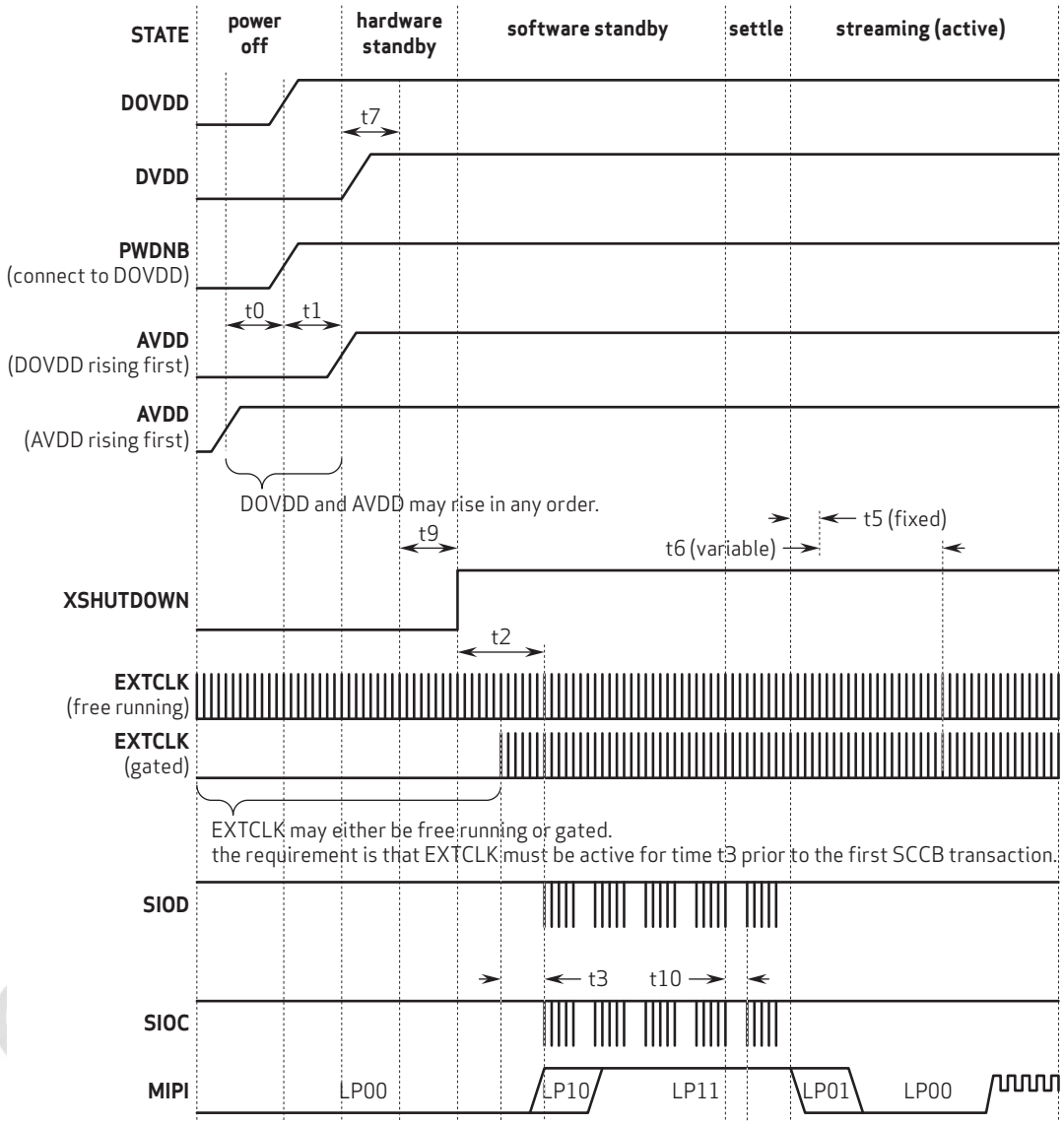
table 2-4 power up sequence

case	XSHUTDOWN	PWDNB	power up sequence requirement
1	GPIO	DOVDD	Refer to **figure 2-3** 1. DOVDD rising must occur before DVDD rising 2. AVDD rising can occur before or after DOVDD rising 3. AVDD must occur before DVDD 4. XSHUTDOWN rising must occur after AVDD, DOVDD and DVDD are stable
2	DOVDD	GPIO	Refer to **figure 2-4** 1. AVDD rising occurs before DOVDD rising 2. DOVDD rising occurs before DVDD 3. PWDNB rising occurs after DVDD rising

table 2-5 power up sequence timing constraints

constraint	label	min	max	unit
AVDD rising – DOVDD rising	t0	0	∞	ns
DOVDD rising – AVDD rising	t1			ns
XSHUTDOWN rising – first SCCB transaction	t2	8192		EXTCLK cycles
minimum number of EXTCLK cycles prior to the first SCCB transaction	t3	8192		EXTCLK cycles
entering streaming mode – first frame start sequence (fixed part)	t5		10	ms
entering streaming mode – first frame start sequence (variable part)	t6	delay is the exposure time value		lines
AVDD or DOVDD, whichever is last – DVDD	t7	0	∞	ns
DVDD – PWDNB rising	t8	0	∞	ns
DVDD – XSHUTDOWN rising	t9	0	∞	ns
power up settle down - from streaming enable to analog stable	t10	10		ms

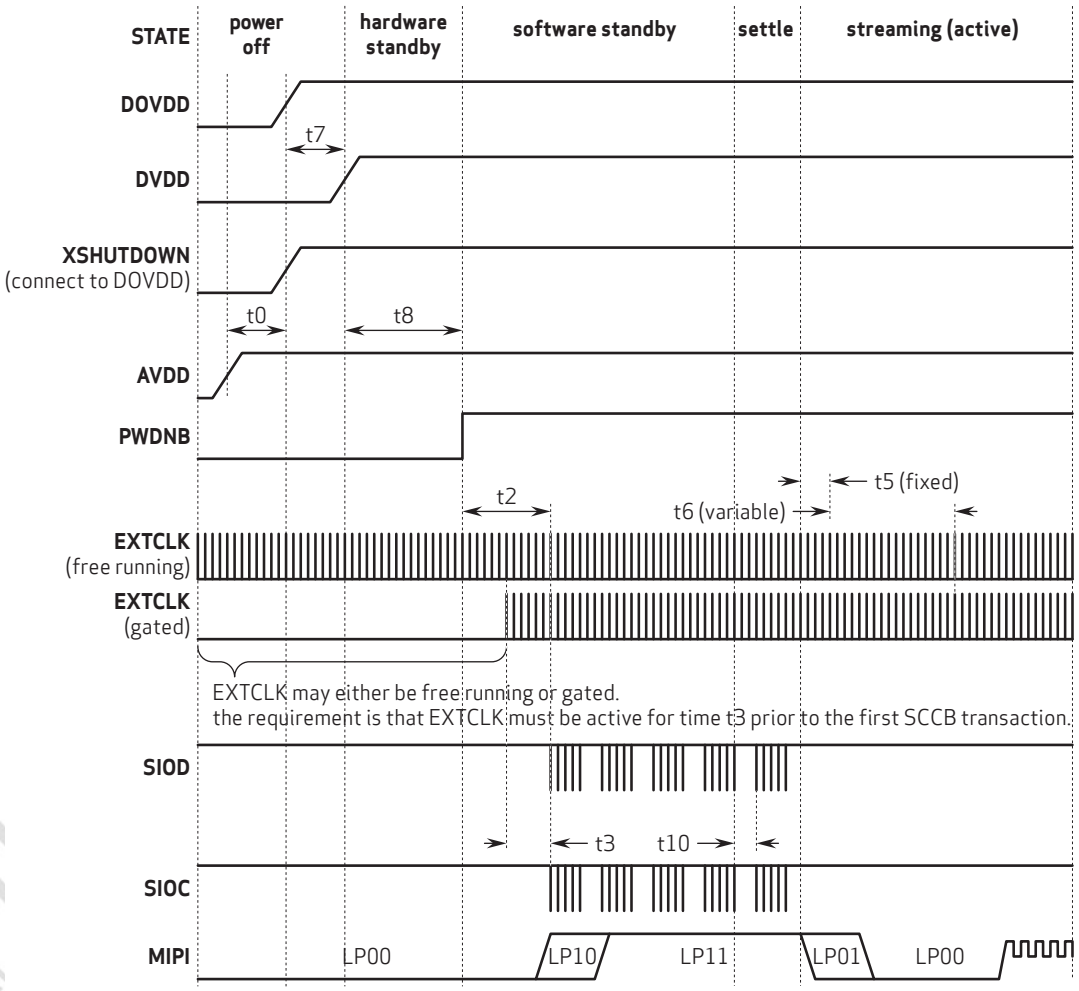
figure 2-3 power up sequence (case 1)



note 1 t10 two registers access the settle period check with local OmniVision FAE for further information

4689_DS_2_3

figure 2-4 power up sequence (case 2)



note 1 t10 few registers need to be loaded after software wakeup, check with local OmniVision FAE for further information

4689_DS_2_4

2.6.2 power down sequence

The digital and analog supply voltages can be powered down in any order (e.g. DOVDD, then AVDD or AVDD, then DOVDD). Similar to the power up sequence, the EXTCLK input clock may be either gated or continuous. If the SCCB command to exit streaming is received while a frame of MIPI data is being output, then the sensor must wait to the MIPI frame end code before entering software standby mode.

If the SCCB command to exit streaming mode is received during the inter frame time, then the sensor must enter software standby mode immediately.

table 2-6 power down sequence

case	XSHUTDOWN	PWDNB	power down sequence requirement
1	GPIO	DOVDD	Refer to **figure 2-6** 1. software standby recommended 2. pull XSHUTDOWN low for minimum power consumption 3. cut off DVDD 4. pull AVDD and DOVDD low in any order
2	DOVDD	GPIO	Refer to **figure 2-7** 1. software standby is needed 2. pull PWDNB low for low power consumption 3. cut off DVDD 4. pull DOVDD low (XSHUTDOWN connected to DOVDD) 5. pull AVDD low

table 2-7 power down sequence timing constraints

constraint	label	min	max	unit
enter software standby SCCB command device in software standby mode	t0	when a frame of MIPI data is output, wait for the MIPI end code before entering the software for standby; otherwise, enter the software standby mode immediately		
minimum of EXTCLK cycles after the last SCCB transaction or MIPI frame end	t1	512		EXTCLK cycles
last SCCB transaction or MIPI frame end, XSHUTDOWN falling	t2	512		EXTCLK cycles
XSHUTDOWN falling – AVDD falling or DOVDD falling whichever is first	t3	0.0		ns
AVDD falling – DOVDD falling	t4	AVDD and DOVDD may fall in any order, the falling separation can vary from 0 ns to infinity		ns
DOVDD falling – AVDD falling	t5			ns
PWDNB falling – DOVDD falling	t6	0.0		ns
XSHUTDOWN falling – DVDD falling	t7	0.0		ns
DVDD falling – AVDD falling or DOVDD falling whichever is first	t8	0.0		ns
PWDNB falling – DVDD falling	t9	0.0		ns

2.6.2.1 software standby

```
6C  0100  00    ;set sensor to sleep mode
delay 1 frame
6C  301A  F9
6C  4805  03
```

2.6.2.2 sensor wakeup from sleep mode

```
6C  0100  01    ;set sensor to streaming mode
6C  301A  F9
delay 10ms
6C  301A  F1
6C  4805  00
6C  301A  F0
```

figure 2-5 software standby sequence

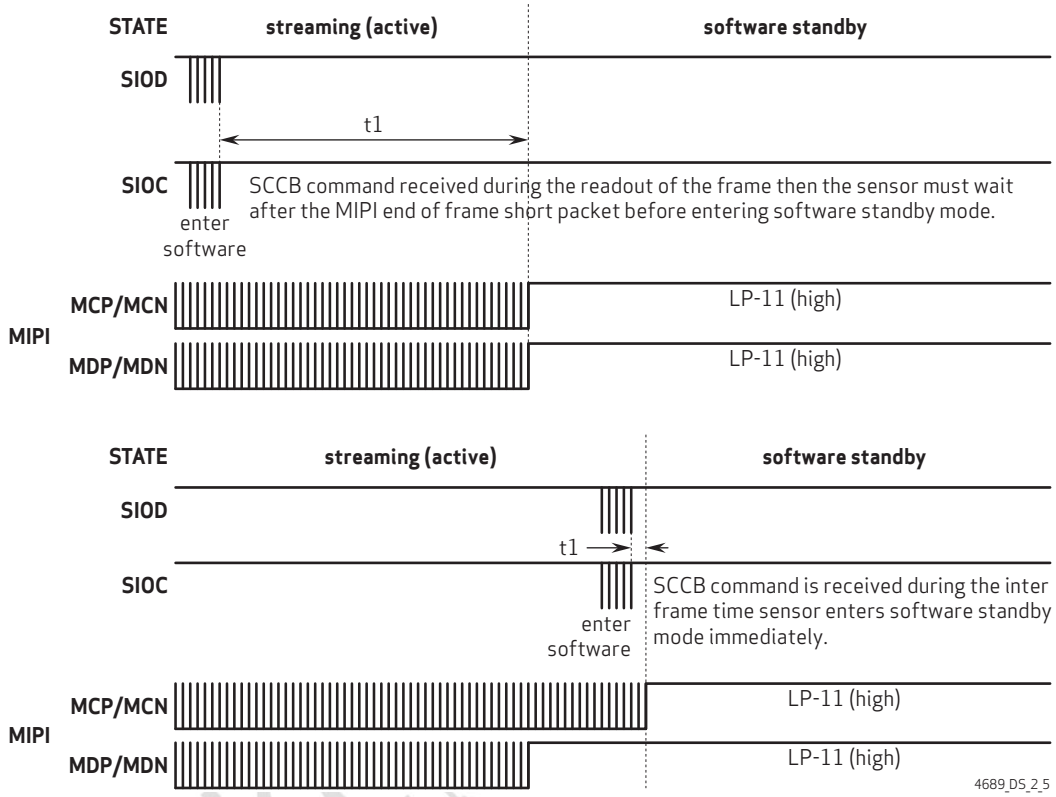


figure 2-6 power down sequence (case 1)

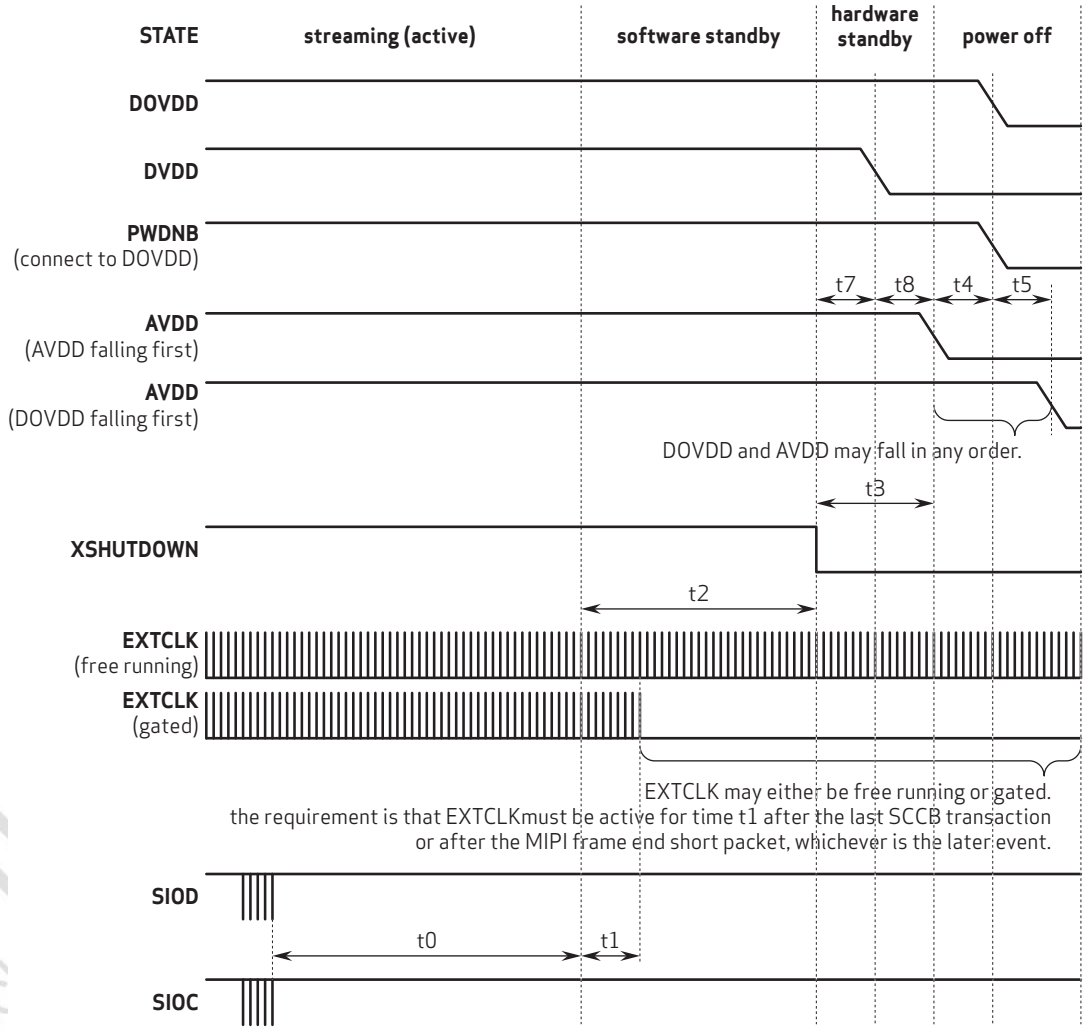
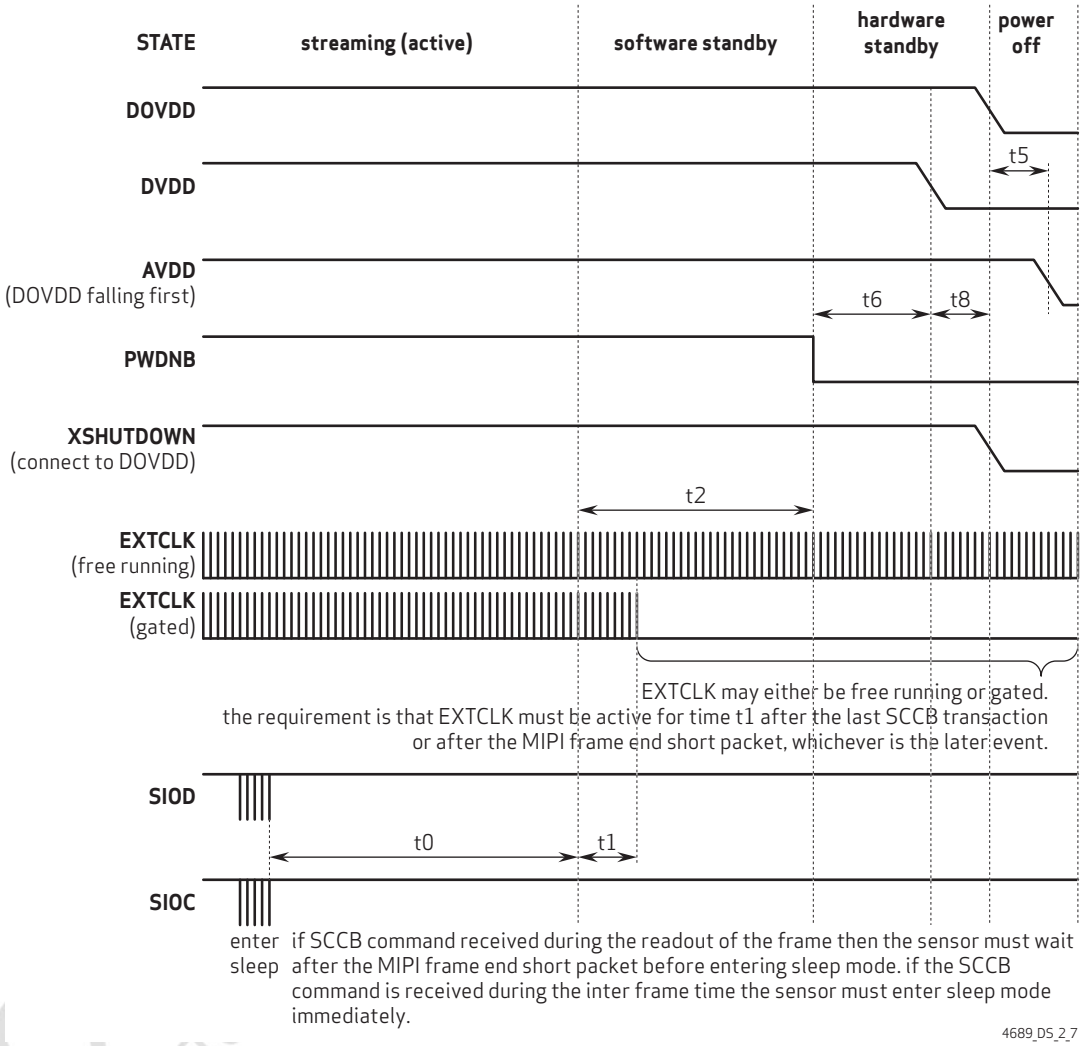


figure 2-7 power down sequence (case 2)



2.7 reset

The whole chip will be reset during power up.

2.7.1 power ON reset

In this sensor a power on reset is generated after the core power becomes stable.

2.7.2 software reset

When register 0x0103[0] is configured as 1, all registers are reset to default value.

2.8 hardware and software standby

Two suspend modes are available for the OV4689:

- hardware standby
- software standby

2.8.1 hardware standby

To initiate hardware standby mode, the XSHUTDOWN or PWDNB pin must be tied to low. When this occurs, the OV4689 internal device clock is halted even when the external clock source is still clocking and all internal counters are reset.

With "PWDNB" control, the sensor register setting can be maintained and the sensor is in low power consumption mode. With "XSHUTDOWN" mode the sensor is in power cut mode, no register settings are kept and the sensor is in minimum power consumption.

2.8.2 software standby

When the software standby (0x0100[0]) control is enabled through the SCCB interface, all function blocks are in standby mode except the SCCB slave.

table 2-8 hardware and standby description

mode	description
hardware standby with PWDNB	1. enabled by pulling PWDNB low 2. input clock is gated by PWDNB, no SCCB communication 3. register values are maintained 4. power down all blocks and regulator 5. low power consumption 6. GPIO can be configured as high/low/tri-state
hardware standby with XSHUTDOWN	1. enabled by pulling XSHUTDOWN low 2. power down all blocks 3. register values are reset to default values 4. no SCCB communication 5. minimum power consumption
software standby	1. default mode after power on reset 2. power down all blocks except SCCB and regulator 3. register values are maintained 4. SCCB communication is available 5. low power consumption 6. GPIO can be configured as high/low/tri-state

2.9 system clock control

2.9.1 PLL1

The PLL1 generates a default 126 MHz pixel clock and 1008MHz MIPI serial clock from a 6~64 MHz input clock. The VCO range is from 600 MHz to 1200 MHz. A programmable clock is provided to generate different frequencies.

2.9.2 PLL2

The PLL2 generates a default 120 MHz system clock from a 6~64 MHz input clock. The VCO range is from 600 MHz to 1200 MHz. A programmable clock divider is provided to generate different frequencies.

figure 2-8 PLL structure

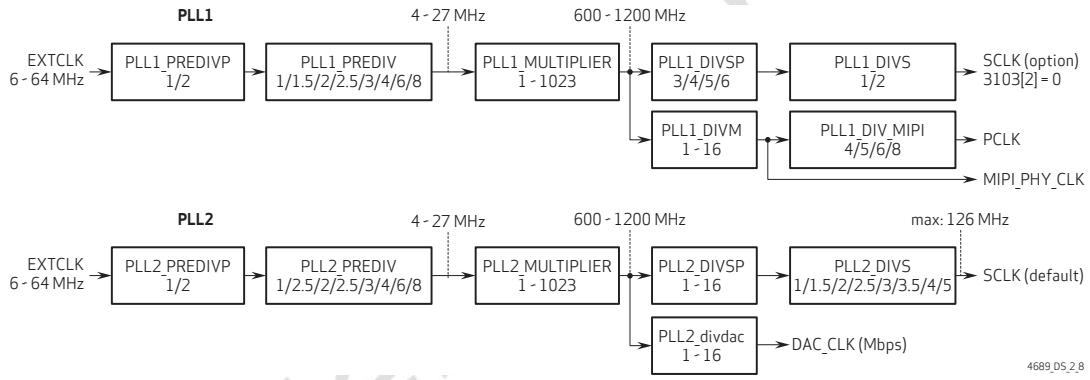


table 2-9 PLL speed limitation

parameter	value
PLL1_multiplier input	4~27 MHz
PLL1_multiplier output	600~1200 MHz
PLL2_multiplier input	4~27 MHz
PLL2_multiplier output	600~1200 MHz
SCLK	10~126 MHz
PCLK	10~150 MHz
DAC	360~378 MHz

table 2-10 PLL registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x0300	PLL_CTRL_0	0x00	RW	Bit[2:0]: pll1_prediv 000: /1 001: /1.5 010: /2 011: /2.5 100: /3 101: /4 110: /6 111: /8
0x0301	PLL_CTRL_1	0x00	RW	Bit[1:0]: pll1_multiplier[9:8]
0x0302	PLL_CTRL_2	0x2A	RW	Bit[7:0]: pll1_multiplier[7:0]
0x0303	PLL_CTRL_3	0x00	RW	Bit[3:0]: pll1_divm 0000: /1 0001: /2 0010: /3 0011: /4 0100: /5 0101: /6 0110: /7 0111: /8 1000: /9 1001: /10 1010: /11 1011: /12 1100: /13 1101: /14 1110: /15 1111: /16
0x0304	PLL_CTRL_4	0x03	RW	Bit[1:0]: pll1_div_mipi 00: /4 01: /5 10: /6 11: /8
0x0305	PLL_CTRL_5	0x01	RW	Bit[1:0]: pll1_divsp 00: /3 01: /4 10: /5 11: /6
0x0306	PLL_CTRL_6	0x01	RW	Bit[0]: pll1_div_s 0: /1 1: /2
0x0308	PLL_CTRL_8	0x00	RW	Bit[0]: pll1_bypass
0x0309	PLL_CTRL_9	0x01	RW	Bit[2:0]: pll1_cp

table 2-10 PLL registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x030A	PLL_CTRL_A	0x00	RW	Bit[0]: pll1_predivp 0: /1 1: /2
0x030B	PLL_CTRL_B	0x00	RW	Bit[2:0]: pll2_prediv 000: 1 001: 1.5 010: 2 011: 2.5 100: 3 101: 4 110: 6 111: 8
0x030C	PLL_CTRL_C	0x00	RW	Bit[1:0]: pll2_multiplier[9:8]
0x030D	PLL_CTRL_D	0x1E	RW	Bit[7:0]: pll2_multiplier[7:0]
0x030E	PLL_CTRL_E	0x04	RW	Bit[2:0]: pll2_divs 000: 1 001: 1.5 010: 2 011: 2.5 100: 3 101: 3.5 110: 4 111: 5
0x030F	PLL_CTRL_F	0x01	RW	Bit[3:0]: pll2_divsp 0000: /1 0001: /2 0010: /3 0011: /4 0100: /5 0101: /6 0110: /7 0111: /8 1000: /9 1001: /10 1010: /11 1011: /12 1100: /13 1101: /14 1110: /15 1111: /16
0x0310	PLL_CTRL_10	0x01	RW	Bit[2:0]: pll2_r_cp
0x0311	PLL_CTRL_11	0x00	RW	Bit[0]: pll2_predivp 0: /1 1: /2

table 2-10 PLL registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x0312	PLL_CTRL_12	0x01	RW	Bit[4]: pll2_bypass Bit[3:0]: pll2_divdac 0000: /1 0001: /2 0010: /3 0011: /4 0100: /5 0101: /6 0110: /7 0111: /8 1000: /9 1001: /10 1010: /11 1011: /12 1100: /13 1101: /14 1110: /15 1111: /16
0x031B	PLL_CTRL_1B	0x00	RW	Bit[0]: pll1_rst
0x031C	PLL_CTRL_1C	0x00	RW	Bit[0]: pll2_rst
0x031F	PLL_CTRL_1F	0x00	RW	Bit[1:0]: lvds_bit_sel 00: Bit[8] Others: Bit[10]

table 2-11 sample PLL configuration (sheet 1 of 2)

control name	address	input clock (EXTCLK)		
		64 MHz	24 MHz	6 MHz
PLL1_PREDIVP	0x030A[0]	0x0	0x0	0x0
PLL1_PREDIV	0x0300[2:0]	0x7	0x0	0x0
PLL1_MULTIPLIER	{0x0301[1:0], 0x0302[7:0]}	0x7E	0x2A	0xA8
PLL1_DIV_MIPI	0x0304[1:0]	0x3	0x3	0x3
PLL1_DIVM	0x0303[3:0]	0x0	0x0	0x0
PLL1_DIVSP	0x0305[1:0]	0x1	0x1	0x1
PLL1_DIVS	0x0306[0]	0x1	0x1	0x1
PLL2_PREDIVP	0x0311[0]	0x0	0x0	0x0
PLL2_PREDIV	0x030B[2:0]	0x5	0x0	0x0

table 2-11 sample PLL configuration (sheet 2 of 2)

control name	address	input clock (EXTCLK)		
		64 MHz	24 MHz	6 MHz
PLL2_MULTIPLIER	{0x030C[1:0], 0x030D[7:0]}	0x2D	0x1E	0x78
PLL2_DIVSP	0x030F[3:0]	0x1	0x1	0x1
PLL2_DIVS	0x030E[2:0]	0x4	0x4	0x4
SCLK	–	120 MHz	120 MHz	120 MHz
MIPI_SCLK	–	1008 MHz	1008 MHz	1008 MHz
MIPI_PCLK	–	126 MHz	126 MHz	126 MHz

2.10 serial camera control bus (SCCB) interface

The Serial Camera Control Bus (SCCB) interface controls the image sensor operation. Refer to the *OmniVision Technologies Serial Camera Control Bus (SCCB) Specification* for detailed usage of the serial control port.

In the OV4689, the SCCB ID is controlled by the SID pin. If SID is low, the sensor's SCCB address comes from register 0x3004 which has a default value of 0x6C. If SID is high, the sensor's SCCB address comes from register 0x3012 which has a default value of 0x20.

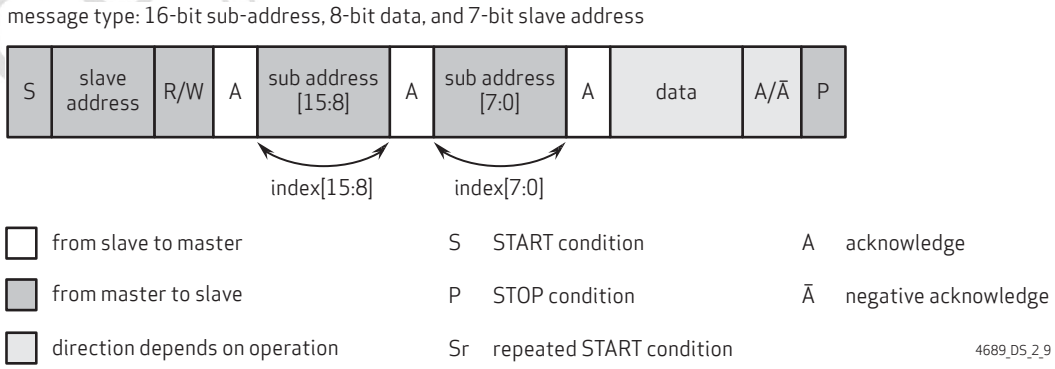
2.10.1 data transfer protocol

The data transfer of the OV4689 follows the SCCB protocol.

2.10.2 message format

The OV4689 supports the message format shown in **figure 2-9**. The repeated START (Sr) condition is not shown in **figure 2-10**, but is shown in **figure 2-11** and **figure 2-12**.

figure 2-9 message type



2.10.3 read / write operation

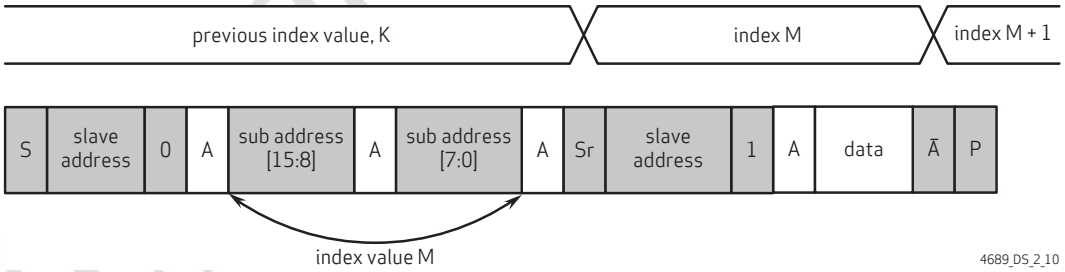
The OV4689 supports four different read operations and two different write operations:

- a single read from random locations
- a sequential read from random locations
- a single read from current location
- a sequential read from current location
- single write to random locations
- sequential write starting from random location

The sub-address in the sensor automatically increases by one after each read/write operation.

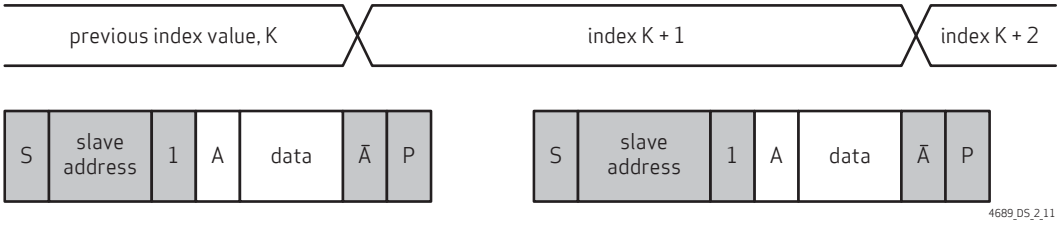
In a single read from random locations, the master does a dummy write operation to desired sub-address, issues a repeated start condition and then addresses the camera again with a read operation. After acknowledging its slave address, the camera starts to output data onto the SIOD line as shown in **figure 2-10**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-10 SCCB single read from random location



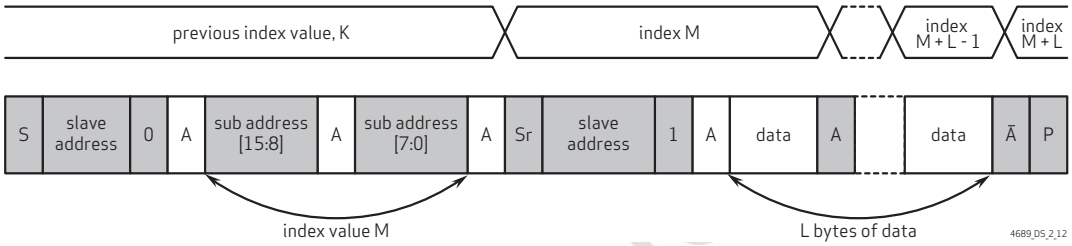
If the host addresses the camera with read operation directly without the dummy write operation, the camera responds by setting the data from last used sub-address to the SIOD line as shown in **figure 2-11**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-11 SCCB single read from current location



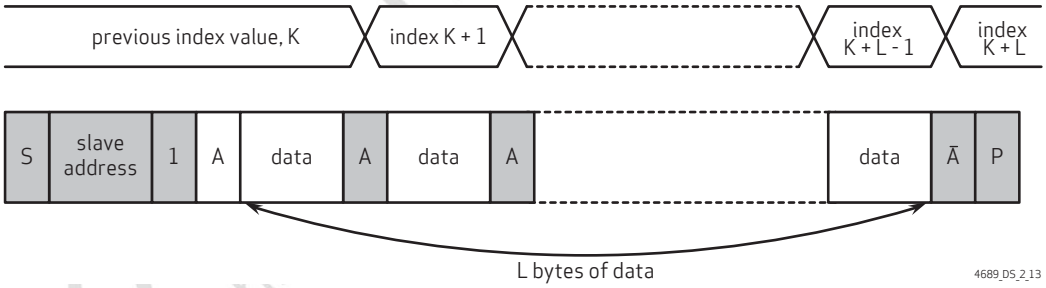
The sequential read from a random location is illustrated in **figure 2-12**. The master does a dummy write to the desired sub-address, issues a repeated start condition after acknowledge from slave and addresses the slave again with read operation. If a master issues an acknowledge after receiving data, it acts as a signal to the slave that the read operation shall continue from the next sub-address. When master has read the last data byte, it issues a negative acknowledge and stop condition.

figure 2-12 SCCB sequential read from random location



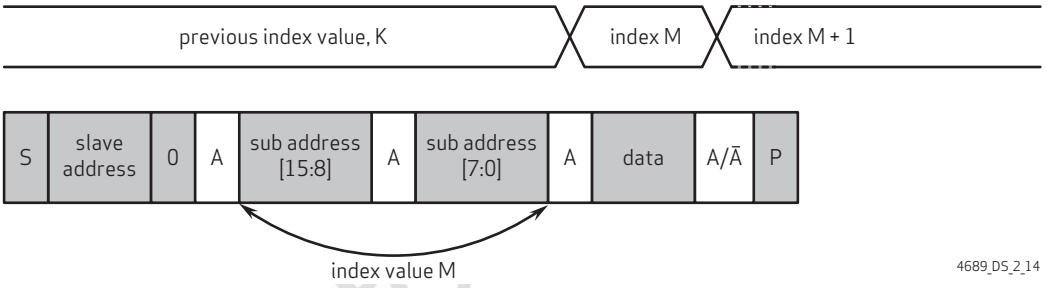
The sequential read from current location is similar to a sequential read from a random location. The only exception is that there is no dummy write operation, as shown in **figure 2-13**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-13 SCCB sequential read from current location



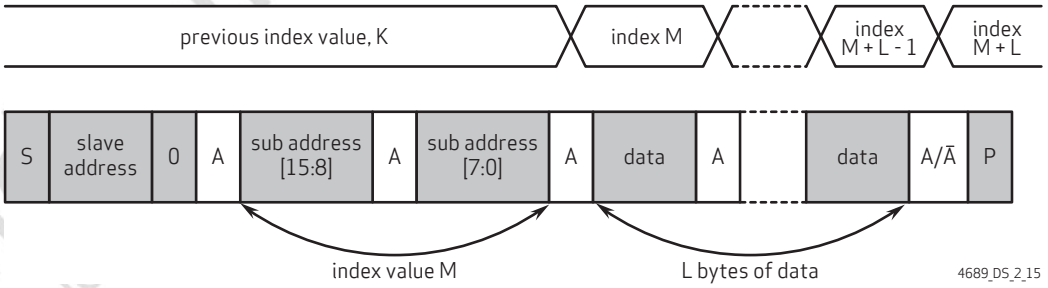
The write operation to a random location is illustrated in **figure 2-14**. The master issues a write operation to the slave, sets the sub-address and data correspondingly after the slave has acknowledged. The write operation is terminated with a stop condition from the master.

figure 2-14 SCCB single write to random location



The sequential write is illustrated in **figure 2-15**. The slave automatically increments the sub-address after each data byte. The sequential write operation is terminated with stop condition from the master.

figure 2-15 SCCB sequential write to random location



2.10.4 SCCB timing

figure 2-16 SCCB interface timing

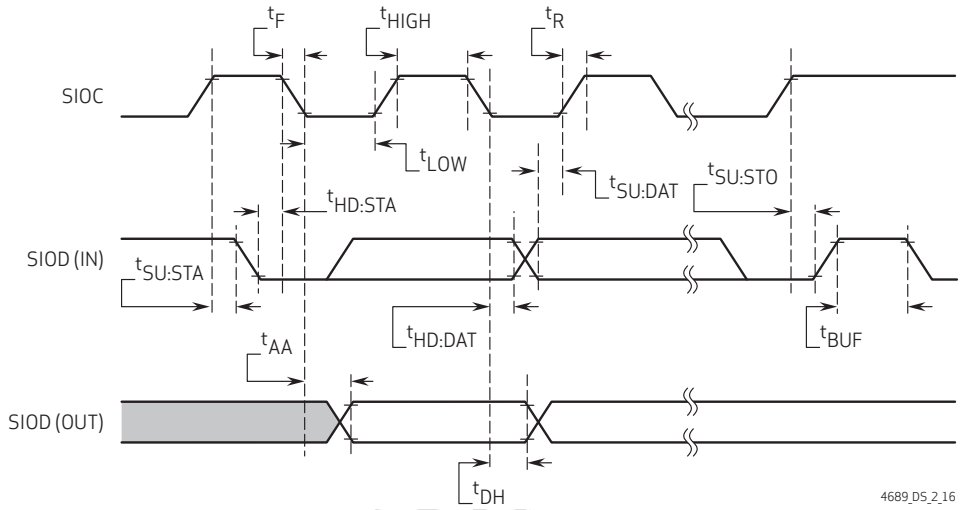


table 2-12 SCCB interface timing specifications[ab]

symbol	parameter	min	typ	max	unit
f_{SIOC}	clock frequency			400	kHz
t_{LOW}	clock low period	1.3			µs
t_{HIGH}	clock high period	0.6			µs
t_{AA}	SIOC low to data out valid	0.1		0.9	µs
t_{BUF}	bus free time before new start	1.3			µs
$t_{HD:STA}$	start condition hold time	0.6			µs
$t_{SU:STA}$	start condition setup time	0.6			µs
$t_{HD:DAT}$	data in hold time	0			µs
$t_{SU:DAT}$	data in setup time	0.1			µs
$t_{SU:STO}$	stop condition setup time	0.6			µs
t_R, t_F	SCCB rise/fall times			0.3	µs
t_{DH}	data out hold time	0.05			µs

a. SCCB timing is based on 400kHz mode

b. timing measurement shown at the beginning of the rising edge and/or of the falling edge signifies 30%, timing measurement shown in the middle of the rising/falling edge signifies 50%, timing measurement shown at the beginning of the rising edge and/or of the falling edge signifies 70%

2.11 group write

Group write is supported in order to update a group of registers in the same frame. These registers are guaranteed to be written prior to the internal latch at the frame boundary.

The OV4689 supports up to four groups. These groups share 1024x8 bits or 1024 bytes and the size of each group is programmable by adjusting the start address.

table 2-13 context switching control (sheet 1 of 2)

address	register name	default value	R/W	description
0x3208	GROUP ACCESS	0x00	RW	Group Access Bit[7:4]: Group control 0000: Group hold start 0001: Group hold end 1010: Group delay launch 1110: Group quick launch Others: Debug mode Bit[3:0]: Group ID 0000: Group bank 0, default start from address 0x00 0001: Group bank 1, default start from address 0x40 0010: Group bank 2, default start from address 0x80 0011: Group bank 3, default start from address 0xB0 Others: Debug mode
0x3209	GRP0_PERIOD	0x00	RW	Bit[6:5]: Switch back group Bit[4:0]: Number of frames to stay in group 0
0x320A	GRP1_PERIOD	0x00	RW	Frames For Staying in Second Group (can be Group 1-3) 0 Means Always Stay in Second Group
0x320B	GRP_SWCTRL	0x01	RW	Bit[7]: Auto switch Bit[3]: group_switch_repeat_enable Enable the first group (group 0) and second group repeatable switch Bit[2]: context_enable Enable to switch from second group back to first group (group 0) automatically Bit[1:0]: Second group selection 00: group 0 01: group 1 10: group 2 11: group 3
0x320D	GRP_ACT	–	R	Indicates Which Group is Active

table 2-13 context switching control (sheet 2 of 2)

address	register name	default value	R/W	description
0x320E	FRAME_CNT_GRP0	–	R	Frame Count Group 0
0x320F	FRAME_CNT_GRP1	–	R	Frame Count Group 1

2.12 hold

After the groups are configured, users can perform a hold operation to store register settings into the SRAM of each group. The hold of each group starts and ends with the control register 0x3208. The lower 4 bits of register 0x3208 control which group to access, and the upper 4 bits control the start (0x0: hold start) and end (0x1: hold end) of the hold operation.

The example setting below shows the sequence to hold group 0:

```
6C  3208  00    group 0 hold start
6C  3800  11    first register into group 0
6C  3911  22    second register into group 0
6C  3208  10    group 0 hold end
```

2.13 launch

After the contents of each group are defined in the hold operation, all registers belonging to each group are stored in SRAM, and ready to be written into target registers (i.e., the launch of that group).

There are five launch modes as described section **section 2.13.1** to **section 2.13.5**.

2.13.1 launch mode 1 - quick manual launch

Manual launch is enabled by setting the register 0x320B to 0.

Quick manual launch is achieved by writing to control register 0x3208. The value written into this register is 0xEX, the upper 4 bits (0xE) are the quick launch command and the lower 4 bits (0xX) are the group number. For example, if users want to launch group 0, they just write the value 0xE0 to 0x3208, then the contents of group 0 will be written to the target registers immediately after the sensor gets this command through the SCCB. Below is an example setting.

```
6C  320B  00    manual launch on
6C  3208  E0    quick launch group 0
```

2.13.2 launch mode 2 - delay manual launch

Delay manual launch is achieved by writing to the register 0x3208. The value written into this register is 0xAX, where the upper 4 bits (0xA) are the delay launch command and the lower 4 bits (0xX) are the group number. For example, if users want to launch group 1, they just write the value 0xA1 to 0x3208, then the contents of group 1 will be written to the target registers. The difference with mode 1 is that the writing will wait for some internally defined time spot in vertical blanking, thus delayed. Below is an example setting.

```
6C  320B  00    manual launch on
6C  3208  A1    delay launch group 1
```

2.13.3 launch mode 3 - quick auto launch

Quick auto launch works like the mode 1, the difference is it will return to a specified group automatically. This is controlled by the register 0x3209, where bit[6:5] controls which group to return and bit[4:0] controls how many frames to stay before returning. The auto launch enable bit is the 0x320B[7]. The operation can be better understood with an example setting:

```
6C  3209  44    Bit[6:5]: 2, return to group 2, Bit[4:0]: 4: stay 4 frames
6C  320B  80    auto launch on
6C  3208  E0    quick launch group 0
```

In this example, sensor will quick launch group 0, stay at group 0 for 4 frames, then return to group 2 after that.

2.13.4 launch mode 4: delay auto launch

Delay auto launch works like mode 2 in the delay launch part and like the mode 3 in the return part.

The operation can be better understood with an example setting:

```
6C  3209  44    Bit[6:5]: 2, return to group 2, Bit[4:0]: 4: stay 4 frames
6C  320B  80    auto launch on
6C  3208  A0    delay launch group 0
```

In this example, sensor will delay launch group 0, stay at group 0 for 4 frames, then return to group 2 after that.

2.13.5 launch mode 5: repeat launch

Repeat launch is controlled by registers 0x3209, 0x320A, and 0x320B. In this mode, the launch is repeated automatically between the first group (must be group 0) and the second group (can be either one of groups 1-3, which is specified by register 0x320B[1:0]). The register 0x3209 defines how many frames remain at group 0, and register 0x320A defines how many frames remain at the second group.

The operation can be better understood with an example setting:

```
6C  3209  02    Bit[7:0]: 2, stay 2 frames in group 0
6C  320A  03    Bit[7]: 3, stay 3 frames in the second group
6C  320B  0E    Bit[3:2]: 3, repeat launch on, Bit[1:0]: 2, second group select:
                group 2
6C  3208  A0    always use a0 for repeat launch
```

In this example, sensor will delay launch group 0, stay at group 0 for 2 frames, then switch to group 2 for 3 frames, then back to group 0 for 2 frames, group 2 for 3 frames and so on.

Below is another example to apply launch mode 2 (delay manual launch) first, sensor stays at group 2 for an indefinite number of frames, then apply launch mode 5 (repeat launch). The sensor will switch to group 0 for 2 frames, then group 2 for 3 frames, and so on.

```
6C  320B  00    manual launch on
6C  3208  A2    delay launch group 2 stay at group 2 for indefinite frames
6C  3209  02    Bit[7:0]: 2, stay 2 frames in group 0
6C  320A  03    Bit[7:0]: 3, stay 3 frames in the second group
6C  320B  0E    Bit3:2]: 3, repeat launch on, Bit[1:0]: 2, second group select:
                group 2
6C  3208  A0    always use A0 for repeat launch
```

Switch to group 0 for 2 frames, then group 2 for 3 frames, and so on.

3 block level description

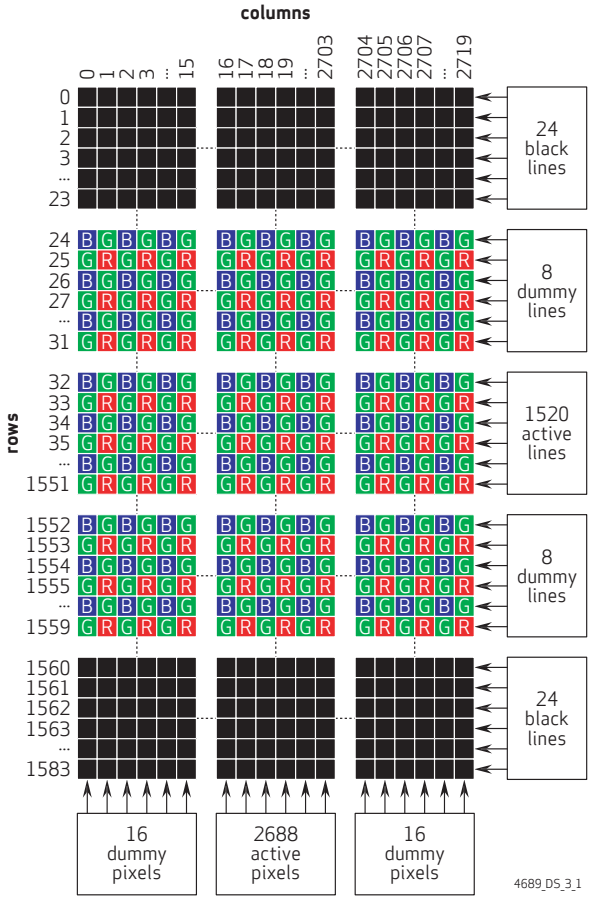
3.1 pixel array structure

The OV4689 sensor has an image array of 2720 columns by 1584 rows (4,308,480 pixels). **figure 3-1** shows a cross-section of the image sensor array.

The color filters are arranged in a Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 4,308,480 pixels, 4,177,920 (2720x1536) are active pixels and can be output. The other pixels are used for black level calibration and interpolation. The center 2688x1520 pixels is suggested to be output from the whole active pixel array. The backend processor can use the boundary pixels for additional processing.

The sensor array design is based on a field integration readout system with line-by-line transfer and an electronic shutter with a synchronous pixel readout scheme.

figure 3-1 sensor array region color filter layout



3.2 subsampling

The OV4689 supports a binning mode to provide a lower resolution output while maintaining the field of view. With binning mode ON, the voltage levels of adjacent pixels (of the same color) are averaged before being sent to the ADC. The OV4689 supports 2x2 binning, and 4x4 binning which is illustrated in **figure 3-2** and **figure 3-2**, where the voltage levels of two horizontal (2x1) adjacent same-color pixels are averaged.

figure 3-2 example of 2x2 binning

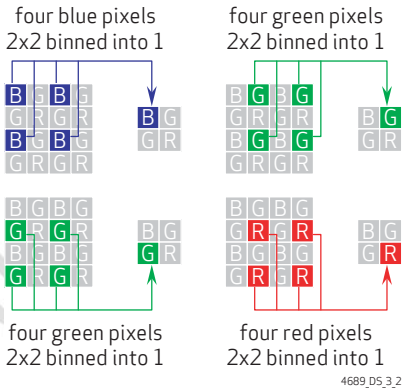


figure 3-3 example of 4x4 binning

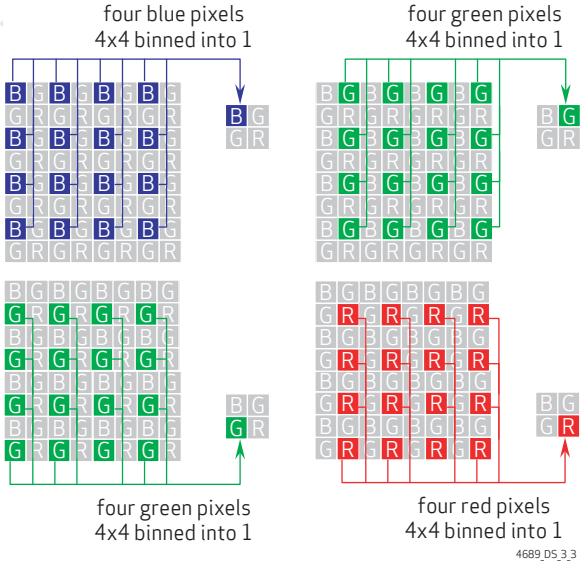


table 3-1 binning-related registers

address	register name	default value	R/W	description
0x3820	TIMING_FORMAT1	0x10	RW	Bit[0]: Vertical binning
0x3821	TIMING_FORMAT2	0x08	RW	Bit[0]: Horizontal binning

3.3 analog amplifier

When the column sample/hold circuit has sampled one row of pixels, the pixel data will shift out one-by-one into an analog amplifier.

3.4 10-bit A/D converters

The balanced signal is then digitized by the on-chip 10-bit ADC.

4 image sensor core digital functions

4.1 mirror and flip

The OV4689 provides mirror and flip readout modes, which respectively reverse the sensor data readout order horizontally and vertically (see **figure 4-1**).

figure 4-1 mirror and flip samples

original image | mirrored image | flipped image | mirrored and flipped image

4689_DS_4_1

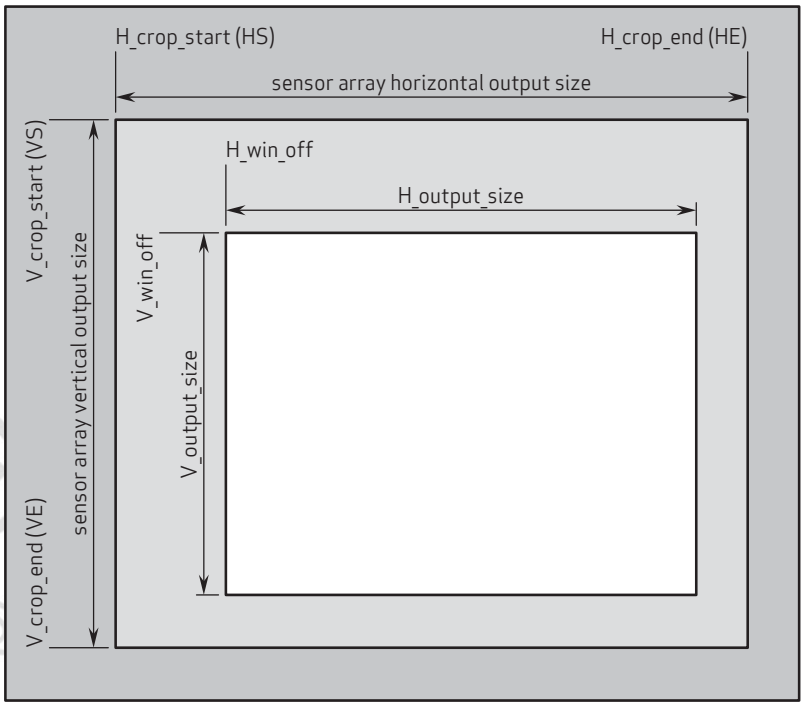
table 4-1 mirror and flip registers

address	register name	default value	R/W	description
0x3820	FORMAT1	0x00	RW	Timing Control Register Bit[2]: Digital vertical flip enable 0: Normal 1: Vertical flip Bit[1]: Array vertical flip enable 0: Normal 1: Vertical flip
0x3821	FORMAT2	0x00	RW	Timing Control Register Bit[2]: Digital horizontal mirror enable 0: Normal 1: Horizontal mirror Bit[1]: Array horizontal mirror enable 0: Normal 1: Horizontal mirror

4.2 image cropping and windowing

An image cropping area is defined by four parameters, horizontal_crop_start (HS), horizontal_crop_end (HE), vertical_crop_start (VS), and vertical_crop_end (VE). By properly setting the parameters, any portion within the sensor array size can output as a visible area. Windowing is achieved by masking off the pixels outside of this cropping window using H_win_off and V_win_off parameters (see **figure 4-2**); thus, the original timing is not affected.

figure 4-2 image cropping and windowing



4689_DS_4_2

table 4-2 image cropping and windowing control functions (sheet 1 of 2)

address	register name	default value	R/W	description
0x3800	H_CROP_START	0x00	RW	Bit[4:0]: Horizontal crop start address[12:8]
0x3801	H_CROP_START	0x20	RW	Bit[7:0]: Horizontal crop start address[7:0]
0x3802	V_CROP_START	0x00	RW	Bit[3:0]: Vertical crop start address[11:8]
0x3803	V_CROP_START	0x0C	RW	Bit[7:0]: Vertical crop start address[7:0]
0x3804	H_CROP_END	0x12	RW	Bit[4:0]: Horizontal crop end address[12:8]

table 4-2 image cropping and windowing control functions (sheet 2 of 2)

address	register name	default value	R/W	description
0x3805	H_CROP_END	0x3F	RW	Bit[7:0]: Horizontal crop end address[7:0]
0x3806	V_CROP_END	0x0D	RW	Bit[3:0]: Vertical crop end address[11:8]
0x3807	V_CROP_END	0x8C	RW	Bit[7:0]: Vertical crop end address[7:0]
0x3808	H_OURPUT_SIZE	0x12	RW	Bit[4:0]: Horizontal output size[12:8]
0x3809	H_OUTPUT_SIZE	0x00	RW	Bit[7:0]: Horizontal output size[7:0]
0x380A	V_OURPUT_SIZE	0x0D	RW	Bit[3:0]: Vertical output size[11:8]
0x380B	V_OUTPUT_SIZE	0x80	RW	Bit[7:0]: Vertical output size[7:0]
0x380C	TIMING_HTS	0x05	RW	Bit[6:0]: Horizontal total size[14:8]
0x380D	TIMING_HTS	0xF8	RW	Bit[7:0]: Horizontal total size[7:0]
0x380E	TIMING_VTS	0x0D	RW	Bit[6:0]: Vertical total size[14:8]
0x380F	TIMING_VTS	0xA4	RW	Bit[7:0]: Vertical total size[7:0]
0x3810	H_WIN_OFF	0x00	RW	Bit[3:0]: Horizontal windowing offset[11:8]
0x3811	H_WIN_OFF	0x01	RW	Bit[7:0]: Horizontal windowing offset[7:0]
0x3812	V_WIN_OFF	0x00	RW	Bit[3:0]: Vertical windowing offset[11:8]
0x3813	V_WIN_OFF	0x00	RW	Bit[7:0]: Vertical windowing offset[7:0]
0x3814	H_INC_ODD	0x01	RW	Bit[4:0]: Horizontal sub-sample odd increase number
0x3815	H_INC_EVEN	0x01	RW	Bit[4:0]: Horizontal sub-sample even increase number
0x382A	V_INC_ODD	0x01	RW	Bit[4:0]: Vertical sub-sample odd increase number
0x382B	V_INC_EVEN	0x01	RW	Bit[4:0]: Vertical sub-sample even increase number

4.3 test pattern

For testing purposes, the OV4689 offers three types of test patterns: color bar, square and random data. The OV4689 also offers two digital effects: transparent effect and rolling bar effect. The output type of digital test pattern is controlled by the test_pattern_type register (0x5040[3:2]). The digital test pattern function is controlled by register 0x5040[7].

4.3.1 color bar

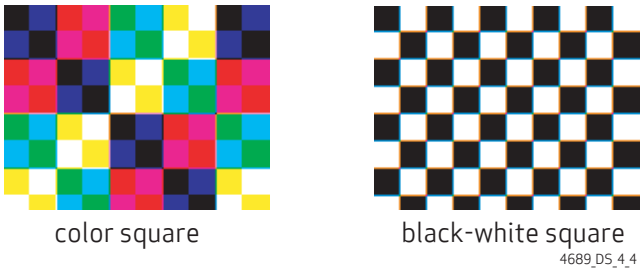
There are four types of color bars (see **figure 4-3**) which are switched by bar-style in register 0x5040[3:2].

figure 4-3 color bar types

4.3.2 square

There are two types of squares: color square and black-white square (see **figure 4-4**). The squ_bw register (0x5040[4]) determines which type of square will be output.

figure 4-4 color, black and white square bars



4.3.3 random data

There are two types of random data test patterns: frame-changing and frame-fixed random data.

4.3.4 transparent effect

The transparent effect is enabled by transparent_en register (0x5040[5]). If this register is set, the transparent test pattern will be displayed. The image in **figure 4-5** is an example which shows a transparent color bar image.

figure 4-5 transparent effect

4689_DS_4_5

4.3.5 rolling bar effect

The rolling bar is set by rolling_bar_en register (0x5040[6]). If it is set, a inverted-color rolling bar will roll from up to down. The image in **figure 4-6** is an example which shows a rolling bar on color bar image.

figure 4-6 rolling bar effect

4689_DS_4_6

table 4-3 test pattern registers

address	register name	default value	R/W	description
0x5040	PRE CTRL00	0x00	RW	Bit[7]: Test pattern enable 0: Disable test function 1: Enable test function Bit[6]: Rolling bar enable 0: Disable 1: Enable Bit[5]: Transparent enable 0: Disable 1: Enable Bit[4]: Square mode 0: Color square 1: Black-white square Bit[3:2]: Color bar style 00: Standard color bar 01: Top-bottom darker color bar 10: Right-left darker color bar 11: Bottom-top darker color bar Bit[1:0]: Test pattern mode 00: Color bar 01: Random data 10: Square 11: Black image
0x5041	PRE CTRL01	0x41	RW	Bit[6]: Window cut enable 0: Do not cut the redundant pixels 1: Cut the redundant pixels Bit[4]: Same seed enable When set, the seed used to generate the random data are same which is set in seed register Bit[3:0]: Seed Seed used in generating random data

4.4 gain and exposure control

The OV4689 does not support auto exposure control (AEC) or auto gain control (AGC). Both exposure time and gain are set manually. The related registers are listed in **table 4-4**.

table 4-4 gain/exposure control registers[a] (sheet 1 of 2)

address	register name	default value	R/W	description
0x3500	EXPO	0x00	RW	Bit[3:0]: Expo[19:16]
0x3501	EXPO	0x02	RW	Bit[7:0]: Expo[15:8]
0x3502	EXPO	0x00	RW	Bit[7:0]: Expo[7:0] Low 4 bits are fraction bits
0x3503	AEC MANUAL	0x00	RW	AEC Manual Mode Control Bit[6]: Digital fraction gain delay option 0: Delay 1 frame 1: No delay 1 frame Bit[5]: Gain change delay option 0: Delay 1 frame 1: No delay 1 frame Bit[4]: Gain delay option 0: Delay 1 frame 1: No delay 1 frame Bit[2]: Gain man as sensor gain 0: Gain input as real gain format 1: gain input as sensor gain format Bit[1]: Exposure delay option 0: Delay 1 frame 1: No delay 1 frame Bit[0]: Exposure change delay option 0: Delay 1 frame 1: No delay 1 frame
0x3507	AEC LONG GAIN	0x00	RW	Long Gain Bit[1:0]: Long gain[17:16]
0x3508	AEC LONG GAIN	0x00	RW	Long Gain Bit[7:0]: Long gain[15:8]
0x3509	AEC LONG GAIN	0x80	RW	Long Gain Bit[7:0]: Long gain[7:0] Low 7 bits are fraction bits
0x350A	AEC MIDDLE EXPO	0x00	RW	Middle Exposure Bit[3:0]: Middle exposure[19:16]
0x350B	AEC MIDDLE EXPO	0x01	RW	Middle Exposure Bit[7:0]: Middle exposure[15:8]

note
For optimal performance, maximum exposure should be 200ms. For more details, contact your local OmniVision FAE.

table 4-4 gain/exposure control registers[a] (sheet 2 of 2)

address	register name	default value	R/W	description
0x350C	AEC MIDDLE EXPO	0x00	RW	Middle Exposure Bit[7:0]: Middle exposure[7:0] Low 4 bits are fraction bits
0x350D	AEC MIDDLE GAIN	0x00	RW	Middle Gain Bit[1:0]: Middle gain[17:16]
0x350E	AEC MIDDLE GAIN	0x00	RW	Middle Gain Bit[7:0]: Middle gain[15:8]
0x350F	AEC MIDDLE GAIN	0x80	RW	Middle Gain Bit[7:0]: Middle gain[7:0] Low 7 bits are fraction bits
0x3510	AEC SHORT EXPO	0x00	RW	Short Exposure Bit[3:0]: Short exposure[19:16]
0x3511	AEC SHORT EXPO	0x00	RW	Short Exposure Bit[7:0]: Short exposure[15:8]
0x3512	AEC SHORT EXPO	0x80	RW	Short Exposure Bit[7:0]: Short exposure[7:0] Low 4 bits are fraction bits
0x3513	AEC SHORT GAIN	0x00	RW	Short Gain Bit[1:0]: Short gain[17:16]
0x3514	AEC SHORT GAIN	0x00	RW	Short Gain Bit[7:0]: Short gain[15:8]
0x3515	AEC SHORT GAIN	0x80	RW	Short Gain Bit[7:0]: Short gain[7:0] Low 7 bits are fraction bits

a. for the gain formula, please contact your local OmniVision FAE

4.5 high dynamic range (HDR) mode

HDR mode increases image dynamic range by capturing multiple exposures of a similar scene and then combining them into one single image. The OV4689 supports three kinds of HDR mode:

- sequential HDR
- staggered HDR

table 4-5 timing control

address	register name	default value	R/W	description
0x3829	FORMAT	0x00	RW	Bit[3]: hdr_lite_enable

4.5.1 sequential HDR

The OV4689 supports up to five different exposure/gain sets for sequential HDR.

In 3-set sequential HDR mode, long/medium/short exposure frames are interlaced as shown in **figure 4-7**. A backend chip will take two consecutive frames and combine them into one HDR frame.

figure 4-7 sequential HDR mode

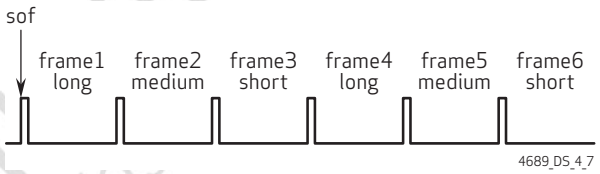


table 4-6 timing control

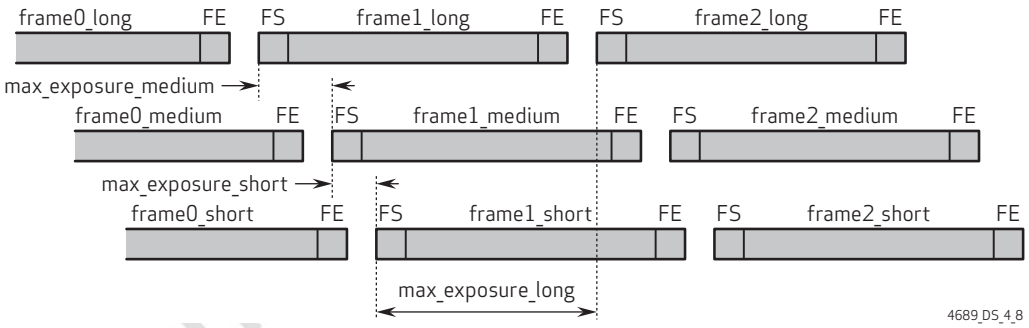
address	register name	default value	R/W	description
0x3846	TIMING_REG_36	0x08	RW	Bit[2:0]: Sequential HDR number

4.5.2 staggered HDR

In staggered HDR mode, long/medium/short exposure frames are overlapping with each other. This reduces the timing delay between different exposure frames, which will combine into one HDR frame. It also reduces the frame/line buffer needed for the backend chip. **figure 4-8** and **figure 4-9** illustrate the frame timing for 3-set staggered HDR. The OV4689 supports 2-set/3-set staggered HDR mode.

The OV4689 uses MIPI virtual channel to differentiate different exposure frames. Long/medium/short frame uses MIPI virtual channel vc0/vc1/vc2, respectively, so that different exposure frames will not be mixed up at the MIPI receiver side.

figure 4-8 staggered HDR with virtual channel



The OV4689 also supports different exposure transfers without MIPI virtual channel, which is controlled by register 0x3837.

figure 4-9 staggered HDR without virtual channel

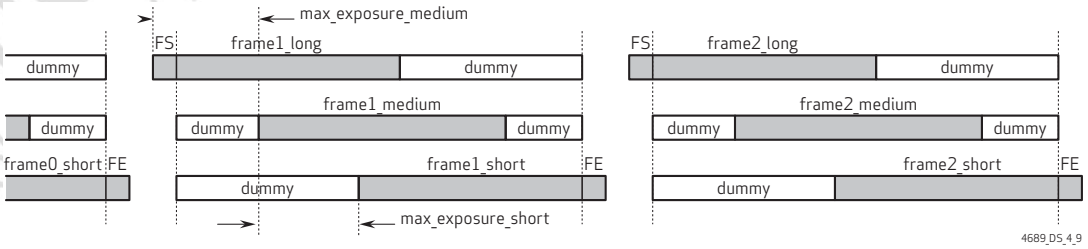


table 4-7 timing control

address	register name	default value	R/W	description
0x3837	TIMING_REG_37	0x00	RW	Bit[7]: stg_vc_man_en Bit[5:4]: vc_l Bit[3:2]: vc_m Bit[1:0]: vc_s
0x3841	TIMING_REG_41	0x02	RW	Bit[0]: Staggered HDR enable

4.5.3 average luminance (YAVG)

Exposure time control is based on a frame brightness average value. The OV4689 supports the average image luminance calculation. By properly setting X_start, Y_start, and window_width and window_height as shown in transparent effect, a 4x4 grid average window is defined. It will automatically divide the window into 4x4 zones. The average value is the weighted average of the 16 sections. **table 4-8** lists the corresponding registers.

figure 4-10 average-based window definition

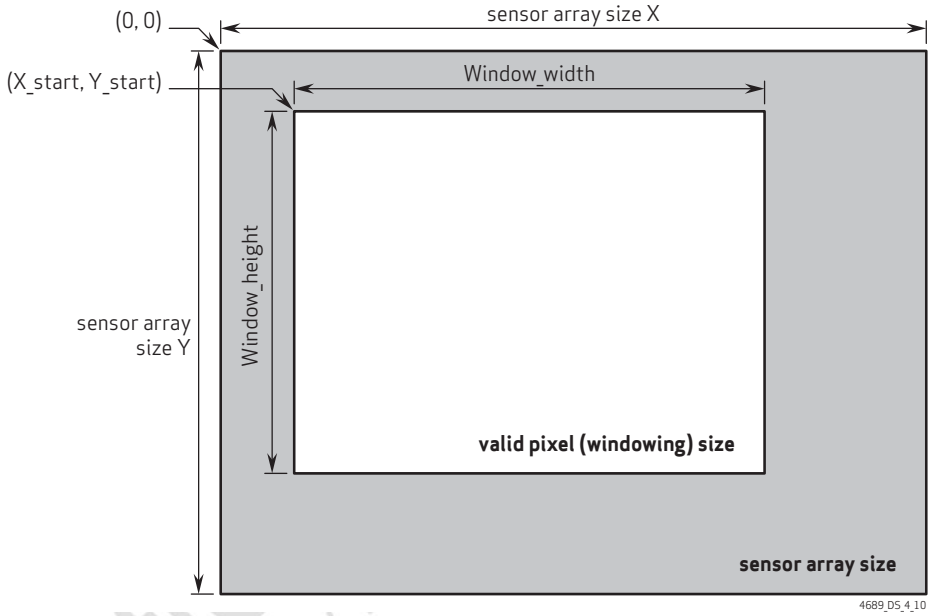


table 4-8 AVG registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5680	AVG CTRL00	0x00	RW	Bit[4:0]: X_start_avg[12:8]
0x5681	AVG CTRL01	0x00	RW	Bit[7:0]: X_start_avg[7:0]
0x5682	AVG CTRL02	0x00	RW	Bit[3:0]: Y_start_avg[11:8]
0x5683	AVG CTRL03	0x00	RW	Bit[7:0]: Y_start_avg[7:0]
0x5684	AVG CTRL04	0x11	RW	Bit[4:0]: Window_width_avg[12:8]
0x5685	AVG CTRL05	0x00	RW	Bit[7:0]: Window_width_avg[7:0]
0x5686	AVG CTRL06	0x09	RW	Bit[3:0]: Window_height_avg[11:8]
0x5687	AVG CTRL07	0xA0	RW	Bit[7:0]: Window_height_avg[7:0]

table 4-8 AVG registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5688	AVG CTRL08	0x11	RW	Bit[7:4]: Weight01 Bit[3:0]: Weight00
0x5689	AVG CTRL09	0x11	RW	Bit[7:4]: Weight03 Bit[3:0]: Weight02
0x568A	AVG CTRL0A	0x11	RW	Bit[7:4]: Weight11 Bit[3:0]: Weight10
0x568B	AVG CTRL0B	0x11	RW	Bit[7:4]: Weight13 Bit[3:0]: Weight12
0x568C	AVG CTRL0C	0x11	RW	Bit[7:4]: Weight21 Bit[3:0]: Weight20
0x568D	AVG CTRL0D	0x11	RW	Bit[7:4]: Weight23 Bit[3:0]: Weight22
0x568E	AVG CTRL0E	0x11	RW	Bit[7:4]: Weight31 Bit[3:0]: Weight30
0x568F	AVG CTRL0F	0x11	RW	Bit[7:4]: Weight33 Bit[3:0]: Weight32
0x5690	AVG CTRL10	0x02	RW	Bit[1]: Sum option 0: Sum=(4×B+9×G×2+10×R)/8 1: Sum=B+G×2+R Bit[0]: Sub-window function enable 0: Use whole output window for average 1: Use registers 0x5680~0x5687 to define window for average
0x5693	AVG ROREG2	–	R	Bit[7:0]: AVG High 8 bits of whole image AVG output

4.5.4 black level calibration (BLC)

The pixel array contains several optically shielded (black) lines and optically shielded (black) pixels on the right side. These lines and columns are used as reference for black level calibration. The main functions of the BLC are:

- adjusting all normal pixel values based on the values of the black levels
- applying multiplication to all pixel values based on digital gain

Black level adjustments can be made with registers 0x4000, 0x4004, and 0x4005.

table 4-9 BLC registers

address	register name	default value	R/W	description
0x4000	BLC CTRL00	0xF1	RW	Bit[7]: Offset out of range triggers BLC enable Bit[6]: Format change triggers BLC enable Bit[5]: Gain change triggers BLC enable Bit[4]: Exposure change triggers BLC enable Bit[3]: Manually trigger BLC signal Its rising edge will triggers BLC Bit[2]: BLC freeze function enable When set, BLC will be frozen and the offsets will keep the pre-frame values Bit[1]: BLC always triggered enable When set, the BLC will be triggered every frame unless the 0x4000[2] is enabled.
0x4004	BLC CTRL04	0x00	RW	Bit[7:0]: Target[15:8] High bits of BLC target
0x4005	BLC CTRL05	0x40	RW	Bit[7:0]: Target[7:0] Low bits of BLC target

4.6 one time programmable (OTP) memory

The OV4689 supports a maximum of 512 bytes of one-time programmable (OTP) memory to store chip identification and manufacturing information, which can be used to update the sensor's default setting and can be controlled through the SCCB (see **table 4-10**).

Registers 0x7000~0x710F and 0x71CB~0x71FF are reserved for use by OmniVision only. Registers 0x7110~0x71CA are available for use by customers.

4.6.1 OTP other functions

OTP loading data can be triggered when power up or writing 0x01 to register 0x3D81. Power up loading data is controlled by register 0x3D85[2], by default it is off. Auto mode and manual mode can be chosen by setting register 0x3D84[6] to 0 and 1, respectively, and by default, it is in auto mode. In auto mode, all data in the OTP will be loaded to the OTP buffer; while in manual mode, part of the data which is defined by the start address ({0x3D88,0x3D89}) and the end address ({0x3D8A,0x3D8B}) of the OTP will be loaded to the OTP buffer.

The OTP memory access conditions are based on typical conditions, sensor wakeup, 2.6~3.0V AVDD, 1.2V DVDD, and 120 MHz system clock.

OTP access requires special timing. In order for OTP access to work with default settings, SCLK should be between 114~126MHz.

To use OTP memory under different operating conditions, please contact your local OmniVision FAE.

table 4-10 OTP control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x7000~ 0x71FF	OTP_SRAM	0x00	RW	Bit[7:0]: OTP buffer
0x3D80	OTP_PROGRAM_CTRL	0x00	RW	Bit[7]: OTP_wr_busy Bit[0]: OTP_program_enable
0x3D81	OTP_LOAD_CTRL	0x00	RW	Bit[7]: OTP_rd_busy Bit[5]: OTP_bist_error Bit[4]: OTP_bist_done Bit[0]: OTP_load_enable
0x3D84	OTP_MODE_CTRL	0x00	RW	Bit[7]: Program disable 1: Disable Bit[6]: Mode select 0: Auto mode 1: Manual mode

table 4-10 OTP control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3D85	OTP_REG85	0x13	RW	Bit[5]: OTP_bist_select 0: Compare with SRAM 1: Compare with zero Bit[4]: OTP_bist_enable Bit[2]: OTP power up load data enable Bit[1]: OTP power up load setting enable Bit[0]: OTP write register load setting enable
0x3D88	OTP_START_ADDRESS	0x00	RW	OTP Start High Address for Manual Mode
0x3D89	OTP_START_ADDRESS	0x00	RW	OTP Start Low Address for Manual Mode
0x3D8A	OTP_END_ADDRESS	0x00	RW	OTP End High Address For Manual Mode
0x3D8B	OTP_END_ADDRESS	0x00	RW	OTP End Low Address For Manual Mode
0x3D8C	OTP_SETTING_STT_ADDRESS	0x00	RW	OTP Start High Address For Load Setting
0x3D8D	OTP_SETTING_STT_ADDRESS	0x00	RW	OTP Start Low Address For Load Setting

4.7 temperature sensor

TheOV4689 supports an on-chip temperature sensor that covers -64~192°C with an average range of 5°C. It can be controlled through the SCCB interface (see **table 4-11**).

Before reading the temperature, the temperature sensor should be triggered by a 0 to 1 transition of register 0x4D12[0]. There is a 64°C offset in the readout value. The junction temperature can be calculated by converting the readout value from hex to decimal and minus 64.

table 4-11 temperature sensor functions

address	register name	R/W	description
0x4D12	TPM TRIGGER	RW	Bit[0]: Temperature sensor trigger
0x4D13	TPM READ	RW	Bit[0]: Temperature readout

4.8 strobe flash and frame exposure

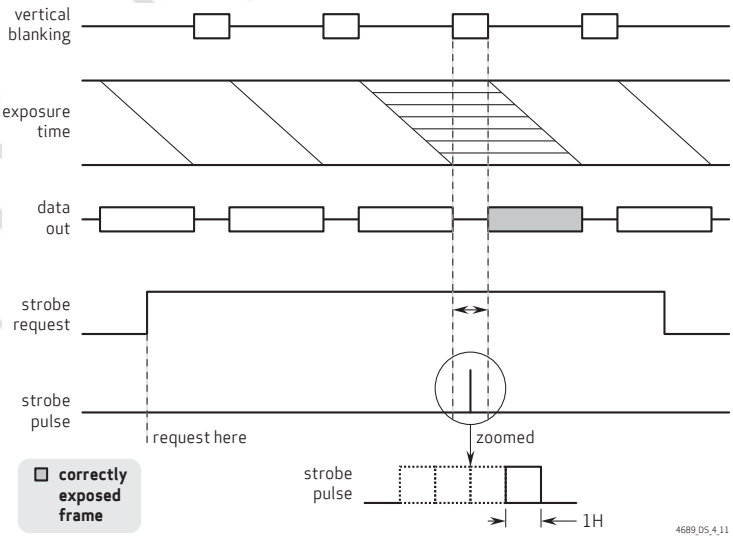
4.8.1 strobe flash control

The strobe signal is programmable using register 0x3B00[1:0]. It supports both LED and Xenon modes. The polarity of the pulse can be changed. The strobe signal is enabled (turned high/low depending on the pulse's polarity) by requesting the signal via the SCCB interface using register bit 0x3B00[7]. Flash modules are triggered by the rising edge by default or by the falling edge if the signal polarity is changed. it supports the following flashing modes: xenon flash control, LED mode 1, LED mode 2 and LED mode 3.

4.8.1.1 xenon flash control

After a strobe request is submitted, the strobe pulse will be activated at the beginning of the third frame (see figure 4-11). The third frame will be correctly exposed. The pulse width can be changed in Xenon mode between 1H and 4H using register 0x3B00[5:4], where H is one row period.

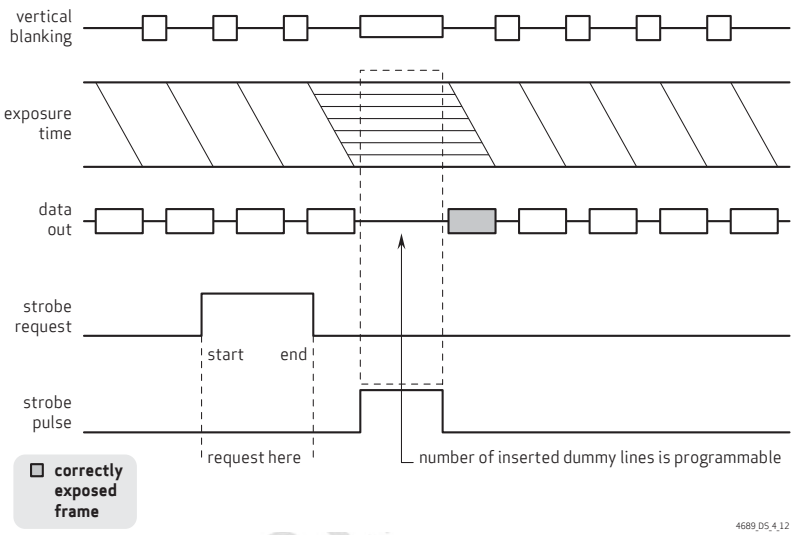
figure 4-11 xenon flash mode



4.8.1.2 LED 1/LED 2

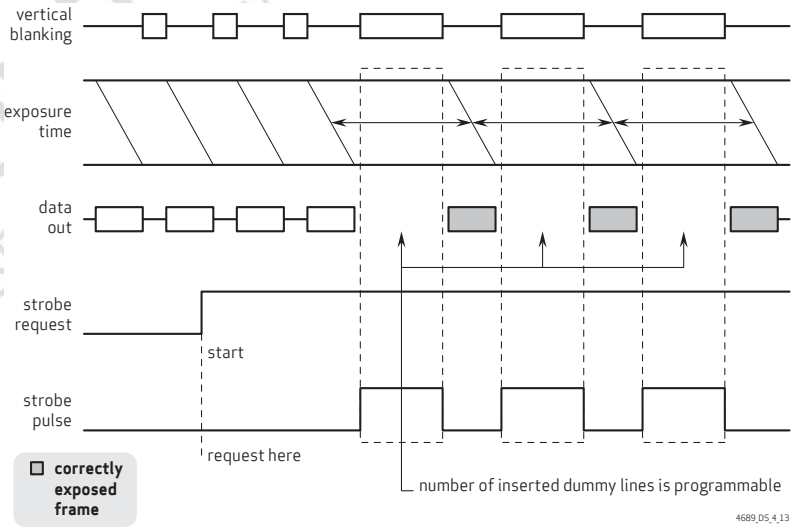
In LED 1/LED 2 mode, the strobe signal stays active until the strobe end request is sent (see LED 1 mode).

figure 4-12 LED 1/ LED 2 single frame mode



The strobe width is controlled by (0x3B02, 0x3B03), unit is now period. The strobe pulse will be activated at the beginning of the third frame.

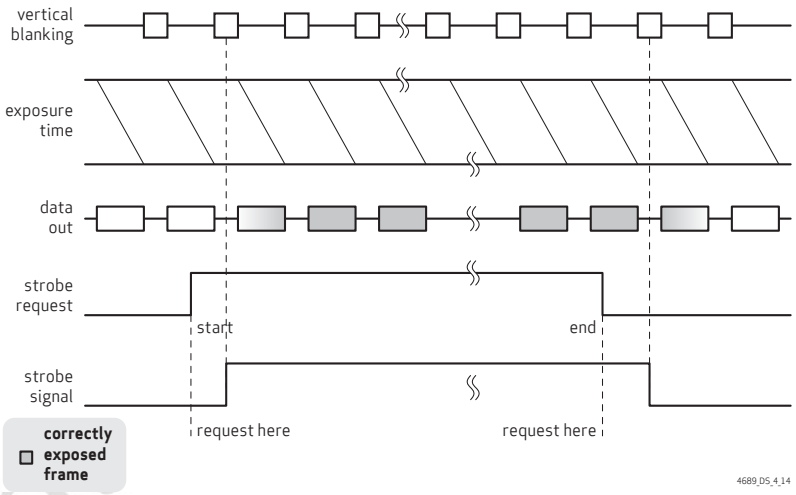
figure 4-13 LED1/LED2 multi-frame mode



4.8.1.3 LED 3 mode

In LED 3 mode, the strobe signal will be activated at the beginning of the first frame and the pulse start point can be selected from SOF or EOF controlled by 0x3B04[3]. The strobe signal stays active until the strobe end request is sent (see **figure 4-14**).

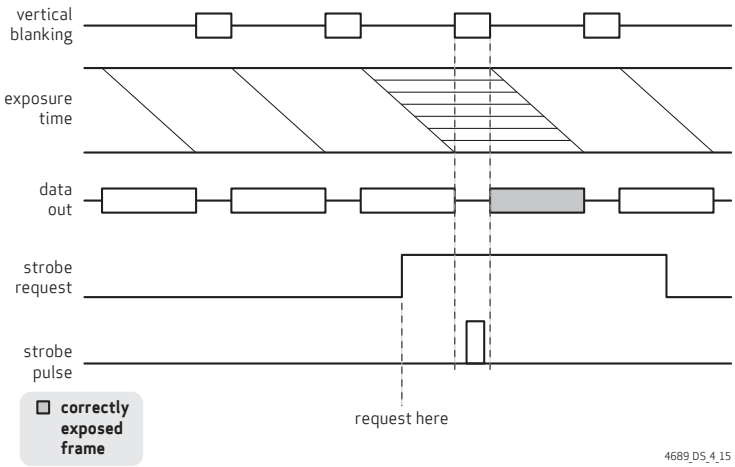
figure 4-14 LED 3 mode



4.8.1.4 LED 4 mode

In LED 4 mode, the strobe signal width is controlled by register 0x3B05. Strobe width = 128 × (2^0x3B05[1:0]) × (0x3B05[7:2] + 1) × sclk_period. The strobe width cannot be longer than v-blanking period. The pulse start point can be selected from SOF or EOF which is controlled by 0x3B04[3], and strobe timing delay can be controlled by 0x3B04[1:0]. The repeat trigger is supported by setting 0x3B04[4] to be 1.

figure 4-15 LED 4 mode



4.8.2 frame exposure (FREX) mode

In FREX mode, all pixels in the frame start integration at the same time, rather than integrating row by row. After a user-defined exposure time, the mechanical shutter should be closed, preventing further integration, and then the image begins to read out. After the readout finishes, the shutter opens again and the sensor resumes normal mode, waiting for the next FREX request.

The OV4689 supports two modes of FREX (see **figure 4-16** and **figure 4-17**):

figure 4-16 FREX mode 1

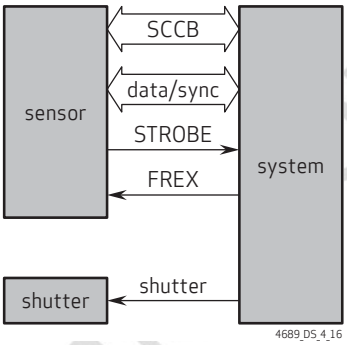
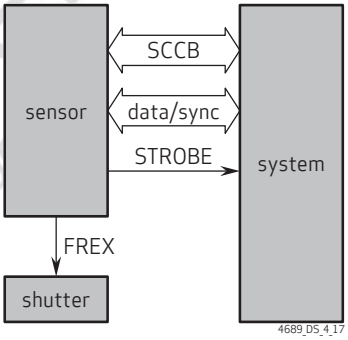


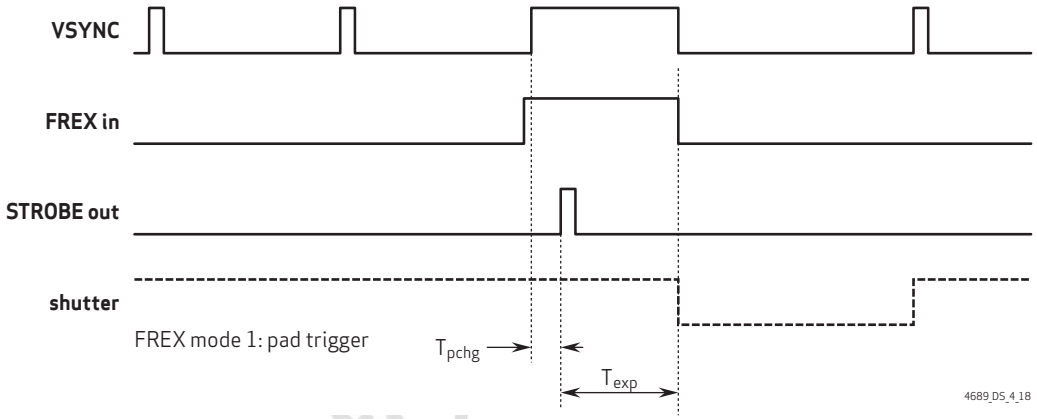
figure 4-17 FREX mode 2



In mode 1, the FREX pin is configured as an input while it is configured as an output in mode 2. In both mode 1 and mode 2, the strobe output is irrelevant with the rolling strobe function. When in rolling shutter mode, the strobe function and this FREX/shutter control function do not work at the same time.

The timing diagram for mode 1 is shown in **figure 4-18**.

figure 4-18 FREX mode 1 timing diagram



In mode 1, the host asserts FREX at any time in preview mode (mechanical shutter is open at this time). The sensor will trigger STROBE to indicate the start of exposure time. Exposure time is calculated from the STROBE rising edge to when the mechanical shutter closes. The host will control when to close the mechanical shutter (shutter delay is handled by the host). The host can re-open the shutter after receiving the entire image data or the next VSYNC signal.

The timing diagrams for mode 2 are shown in **figure 4-19** and **figure 4-20**.

figure 4-19 FREX mode 2 (shutter delay = 0) timing diagram

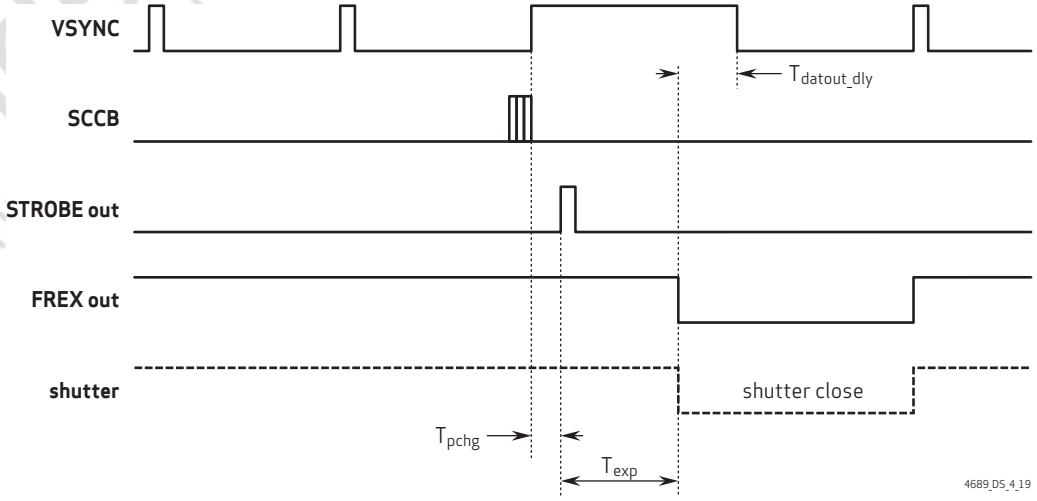
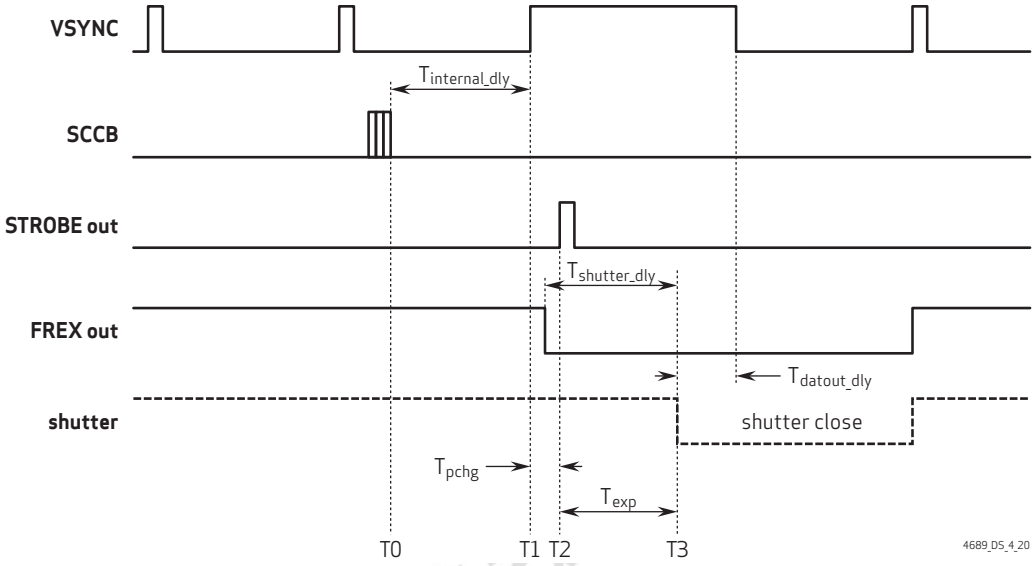


figure 4-20 FREX mode 2 (shutter delay > 0) timing diagram



Before using mode 2, the host needs to program exposure time (registers 0x37C5, 0x37C6, 0x37C7), shutter delay (registers 0x37CC, 0x37CD), strobe width (registers 0x37C9, 0x37CA, 0x37CB), and data output delay. The host triggers this mode by SCCB at any time in preview mode (mechanical shutter is open at this time). The sensor can either start frame exposure right away (since the current data packet is broken, the receiver may get a packet error) or wait for the current frame to finish (controlled by register 0x37DF[0]). If there is no STROBE delay, the sensor will trigger STROBE to indicate the start of exposure time. Exposure time is calculated from STROBE rising edge to when the mechanical shutter closes. Otherwise, the STROBE signal will be sent out even before the sensor begins to pre-charge. The host can control the sensor to start sending image data after a certain delay (registers 0x37D0, 0x37D1) after FREX goes low. The host can re-open the shutter after receiving the entire image data or the next VSYNC signal.

See **table 4-12** for FREX strobe control functions.

table 4-12 FREX strobe control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3B00	STROBE CTRL	0x00	RW	Bit[7]: Strobe ON/OFF Bit[6]: Strobe polarity 0: Active high 1: Active low Bit[5:4]: width_in_xenon Bit[2:0]: Mode 000: Xenon 001: LED1 010: LED2 011: LED3 100: LED4
0x3B02	STROBE H	0x00	RW	Dummy Lines Added at Strobe Mode, MSB
0x3B03	STROBE L	0x00	RW	Dummy Lines Added at Strobe Mode, LSB
0x3B04	STROBE CTRL	0x00	RW	Bit[3]: start_point_selection Bit[2]: Strobe repeat enable Bit[1:0]: Strobe latency 00: Strobe generated at next frame 01: Strobe generated 2 frames later 10: Strobe generated 3 frames later 11: Strobe generated 4 frames later
0x3B05	STROBE WIDTH	0x00	RW	Bit[7:2]: Strobe pulse width step Bit[1:0]: Strobe pulse width gain strobe_pulse_width = 128 × (2^gain) × (step+1) × Tsclk
0x37C5	FREX REG5	0x00	RW	Bit[7:0]: Frame exposure[23:16] MSB of frame exposure time in mode 2 Exposure time in units of 128 system clock cycles
0x37C6	FREX REG6	0x00	RW	Bit[7:0]: Frame exposure[15:8] Middle byte of frame exposure time in mode 2
0x37C7	FREX REG7	0x08	RW	Bit[7:0]: Frame exposure[7:0] LSB of frame exposure time in mode 2
0x37C9	FREX REG9	0x00	RW	Bit[3:0]: Strobe width[19:16] MSB of strobe width in mode 2. Strobe width in units of 1 system clock cycle.
0x37CA	FREX REGA	0x06	RW	Bit[7:0]: Strobe width[15:8] Middle byte of strobe width in mode 2
0x37CB	FREX REGB	0x00	RW	Bit[7:0]: Strobe width[7:0] LSB of strobe width in mode 2

table 4-12 FREX strobe control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x37CC	FREX REGC	0x00	RW	Bit[4:0]: Shutter dly[12:8] MSB of shutter delay in mode 2. Shutter delay is in units of 128 system clock cycles.
0x37CD	FREX REGD	0x44	RW	Bit[7:0]: Shutter dly[7:0] LSB of shutter delay in mode 2
0x37CE	FREX REGE	0x1F	RW	Bit[7:0]: FREX precharge width[15:8] MSB of sensor precharge in mode 2 Sensor precharge is in units of 1 system clock cycle.
0x37CF	FREX REGF	0x40	RW	Bit[7:0]: FREX precharge width[7:0] LSB of sensor precharge in mode 2
0x37D0	FREX REG10	0x00	RW	Bit[7:0]: Readout delay[15:8] MSB of readout delay time in mode 2 Readout delay time is in units of 128 system clock cycles.
0x37D1	FREX REG11	0x01	RW	Bit[7:0]: Readout delay[7:0] LSB of readout delay time in mode 2
0x37D2	FREX_REG12	0x00	RW	Bit[4:0]: Strobe delay[12:8] MSB of strobe delay time Strobe delay time is in units of 1 system clock cycles
0x37D3	FREX_REG13	0x00	RW	Bit[7:0]: Strobe delay[7:0] LSB of strobe delay time
0x37DE	FREX REG1E	0x01	RW	Bit[0]: FREX SCCB request repeat trigger selection 0: SOF 1: EOF

table 4-12 FREX strobe control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x37DF	FREX REG1F	0x04	RW	Bit[7]: FREX SCCB request (self-clearing) Bit[5]: frex_strobe_out_sel 0: Strobe for rolling mode 1: Strobe for frame mode Bit[4]: FREX nopchg Bit[3]: FREX strobe polarity 0: Active high 1: Active low Bit[2]: FREX shutter polarity Bit[1]: FREX pad input enable 0: Frame mode is triggered by register 1: Frame mode is triggered by FREX pad Bit[0]: No latch at SOF for FREX SCCB request 0: Trigger frame mode in SOF 1: Trigger frame mode immediately

4.8.2.1 exposure time control

Registers: r_frame_exp = {0x37C5, 0x37C6, 0x37C7}, 24 bits, 1 step = 128 clock cycles.

Minimum exposure time: 0x37C5 = 0x00, 0x37C6 = 0x00, 0x37C7 = 0x00.
If OV4689 works at 120 MHz, the minimum exposure time is 0 and minimum step is 1.067 µs.

Maximum exposure time: 0x37C5 = 0xFF, 0x37C6 = 0xFF, 0x37C7 = 0xFF.
If OV4689 works at 120 MHz, the maximum exposure time is 13.98 sec.

4.8.2.2 shutter delay control

Registers: r_shutter_dly = {0x37CC[4:0], 0x37CD[7:0]}, 13 bits, 1 step = 128 clock cycles.

Minimum shutter delay time: 0x37CC = 0x00, 0x37CD = 0x00.

Minimum step is 1.067 µs.

Maximum shutter delay time: 0x37CC = 0x1F, 0x37CD = 0xFF.
If OV4689 works at 120 MHz, the maximum shutter delay time is 8.74 ms.

4.8.2.3 sensor pre charge control

Registers: r_frex_pchg = {0x37CE[7:0], 0x37CF[7:0]}, 16 bits, 1 step = 1 system clock cycle.

These registers affect sensor performance. It is for internal use and not recommended for customer to change.

4.8.2.4 strobe control

Registers: r_strobe_width = {0x37C9[3:0], 0x37CA[7:0], 0x37CB[7:0]}, 20 bits, 1 step = 1 clock cycle.

These registers control the strobe signal output width.

Register: r_strobe_dky = {0x37D2[4:0], 0x7D3[7:0]}, 13 bits, 1 step - 1 clock cycle. These registers control the delay between strobe to shutter.

5 image sensor processor digital functions

5.1 DSP top

Two functions of DSP top are to integrate all sub-modules and to create necessary control signals.

table 5-1 DSP top registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5000	ISP CTRL0	0xF3	RW	Bit[7]: Digital gain enable 0: Disable 1: Enable Bit[6]: Bin enable 0: Disable 1: Enable Bit[5]: OTP enable 0: Disable 1: Enable Bit[4]: WB gain enable 0: Disable 1: Enable Bit[1]: Average enable Bit[0]: ISP enable
0x5001	ISP CTRL1	0x11	RW	Bit[7]: New_stg_hdr_en Bit[6]: New_stg_EOF_en Bit[4]: ISP EOF select Bit[3]: ISP SOF select Bit[0]: BLC 0: Disable 1: Enable
0x5002	ISP CTRL2	0x85	RW	Bit[7]: ISP RAW enable 0: Disable 1: Enable Bit[3]: WB bias manual enable 0: Disable 1: Enable Bit[2]: WB bias on Bit[1]: Digital gain bias manual enable Bit[0]: Digital gain bias on
0x5003	ISP CTRL03	0x10	RW	Bias Manual
0x500A	ISP CTRL0A	0x00	RW	Bit[7:0]: X address end address
0x500B	ISP CTRL0B	0x00	RW	Bit[7:0]: Y address end address
0x500C	ISP CTRL0C	0x04	RW	Bit[3:0]: Long WB R gain[11:8]
0x500D	ISP CTRL0D	0x00	RW	Bit[7:0]: Long WB R gain[7:0]

table 5-1 DSP top registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x500E	ISP CTRL0E	0x04	RW	Bit[3:0]: Long WB G gain[11:8]
0x500F	ISP CTRL0F	0x00	RW	Bit[7:0]: Long WB G gain[7:0]
0x5010	ISP CTRL10	0x04	RW	Bit[3:0]: Long WB B gain[11:8]
0x5011	ISP CTRL11	0x00	RW	Bit[7:0]: Long WB B gain[7:0]
0x5012	ISP CTRL 12	0x04	RW	Bit[3:0]: Middle WB R gain[11:8]
0x5013	ISP CTRL 13	0x00	RW	Bit[7:0]: Middle WB R gain[7:0]
0x5014	ISP CTRL 14	0x04	RW	Bit[3:0]: Middle WB G gain[11:8]
0x5015	ISP CTRL 15	0x00	RW	Bit[7:0]: Middle WB G gain[7:0]
0x5016	ISP CTRL 16	0x04	RW	Bit[3:0]: Middle WB B gain[11:8]
0x5017	ISP CTRL 17	0x00	RW	Bit[7:0]: Middle WB B gain[7:0]
0x5018	ISP CTRL 18	0x04	RW	Bit[3:0]: Short WB R gain[11:8]
0x5019	ISP CTRL 19	0x00	RW	Bit[7:0]: Short WB R gain[7:0]
0x501A	ISP CTRL 1A	0x04	RW	Bit[3:0]: Short WB G gain[11:8]
0x501B	ISP CTRL 1B	0x00	RW	Bit[7:0]: Short WB G gain[7:0]
0x501C	ISP CTRL 1C	0x04	RW	Bit[3:0]: Short WB B gain[11:8]
0x501D	ISP CTRL 1D	0x00	RW	Bit[7:0]: Short WB B gain[7:0]
0x502A	ISP CTRL 2A	0x00	RW	Bit[0]: Long add offset[8]
0x502B	ISP CTRL 2B	0x00	RW	Bit[7:0]: Long add offset[7:0]
0x502C	ISP CTRL 2C	0x00	RW	Bit[0]: Middle add offset[8]
0x502D	ISP CTRL 2D	0x00	RW	Bit[7:0]: Middle add offset[7:0]
0x502E	ISP CTRL 2E	0x00	RW	Bit[0]: Short add offset[8]
0x502F	ISP CTRL 2F	0x00	RW	Bit[7:0]: Short add offset[7:0]
0x5031	ISP CTRL 31	0x20	RW	Bit[5]: Bin mode select Bit[4]: Bypass SOF Bit[3]: Long/short reverse WB gain Bit[2]: Long/short reverse digital gain Bit[1]: Debug mode

5.2 DSP_pre

The main purposes of the DSP_pre module include:

- adjust HREF, valid, RBlue signals and data
- create color bar image
- determine the sizes of input image by removing redundant data
- create control signals

table 5-2 pre_ISP registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5040	PRE ISP TEST CTRL	0x00	RW	Bit[7]: test_enable Bit[6]: Rolling enable Rolling bar in test mode Bit[5]: Transparent image + normal image enable Bit[4]: Square black white enable Bit[3:2]: color_bar style 00: Horizontal bar 01: Vertical bar 10: Horizontal fading bar 11: Vertical fading bar Bit[1:0]: Test selection 00: Color bar 01: Random data 10: Square black white 11: Black
0x5041	PRE ISP WIN	0x41	RW	Bit[6]: Window cut enable Bit[5]: ISP test, low bits to 0 Bit[4]: Random, random data reset Bit[3:0]: Random seed
0x5048	PRE ISP X OFF	0x00	RW	Bit[7:0]: X manual offset[15:8]
0x5049	PRE ISP X OFF	0x00	RW	Bit[7:0]: X manual offset[7:0]
0x504A	PRE ISP Y OFF	0x00	RW	Bit[7:0]: Y manual offset15:8]
0x504B	PRE ISP Y OFF	0x00	RW	Bit[7:0]: Y manual offset[7:0]
0x5050~ 0x5051	DEBUG MODE	–	–	Debug Mode
0x504C	PRE ISP PIX NUM	–	R	Bit[7:0]: pixel_number_h[15:8]
0x504D	PRE ISP PIX NUM	–	R	Bit[7:0]: pixel_number_l[7:0]
0x504E	PRE ISP LN NUM	–	R	Bit[7:0]: line_number_h[15:8]
0x504F	PRE ISP LN NUM	–	R	Bit[7:0]: line_number_l[7:0]

table 5-2 pre_ISP registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5057	PRE ISP XY INC	–	R	Bit[7:4]: x_odd_inc Bit[3:0]: y_odd_inc
0x5058	PRE ISP X OFF R	–	R	Bit[7:0]: x_offset[15:8]
0x5059	PRE ISP X OFF R	–	R	Bit[7:0]: x_offset[7:0]
0x505A	PRE ISP Y OFF R	–	R	Bit[7:0]: y_offset[15:8]
0x505B	PRE ISP Y OFF R	–	R	Bit[7:0]: y_offset[7:0]
0x505C	PRE ISP WIN X OFF	–	R	Bit[7:0]: win_x_offset[15:8]
0x505D	PRE ISP WIN X OFF	–	R	Bit[7:0]: win_x_offset[7:0]
0x505E	PRE ISP WIN Y OFF	–	R	Bit[7:0]: win_y_offset[15:8]
0x505F	PRE ISP WIN Y OFF	–	R	Bit[7:0]: win_y_offset[7:0]
0x5060	PRE ISP WIN X OUT	–	R	Bit[7:0]: win_x_output_h size[15:8]
0x5061	PRE ISP WIN X OUT	–	R	Bit[7:0]: win_x_output_l size[7:0]
0x5062	PRE ISP WIN Y OUT	–	R	Bit[7:0]: win_y_output_h size[15:8]
0x5063	PRE ISP WIN Y OUT	–	R	Bit[7:0]: win_y_output_l size[7:0]
0x5064	PRE ISP SKIP	–	R	Bit[5:4]: x_skip Bit[1:0]: y_skip
0x5065	PRE ISP CTRL 25	–	R	Bit[7:4]: X even inc Bit[3:0]: Y even inc
0x5066	PRE ISP CTRL 26	–	R	Bit[3]: X odd inc[4] Bit[2]: Y odd inc[4] Bit[1]: X even inc[4] Bit[0]: Y even inc[4]
0x5067	PRE ISP CTRL 27	–	R	Bit[2:0]: Y cut top offset[10:8]
0x5068	PRE ISP CTRL 28	–	R	Bit[7:0]: Y cut top offset[7:0]
0x5069	PRE ISP CTRL 29	–	R	Bit[2:0]: Y cut bottom offset[10:8]
0x506A	PRE ISP CTRL 2A	–	R	Bit[7:0]: Y cut bottom offset[7:0]
0x506B	PRE ISP CTRL 2B	0x06	RW	Bit[2:0]: Y address fullsize[10:8]
0x506C	PRE ISP CTRL 2C	0x00	RW	Bit[7:0]: Y address fullsize[7:0]

5.3 OTP for cluster cancellation

table 5-3 OTP for cluster cancellation registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5000	ISP CTRL0	0xF3	RW	Bit[5]: OTP enable 0: Disable 1: Enable
0x5500	OTP DPC START	0x00	RW	Bit[0]: OTP start address[8]
0x5501	OTP DPC START	0x00	RW	Bit[7:0]: OTP start address[7:0]
0x5502	OTP DPC END	0x01	RW	Bit[0]: OTP end address[8]
0x5503	OTP DPC END	0xFF	RW	Bit[7:0]: OTP end address[7:0]
0x5505	OTP DPC CTRL 05	0x6C	RW	Bit[6:5]: Recover method select 00: Left 1 neighbor pixel on same channel 01: Minimum of left 2 neighbor pixels 10: Maximum of left and right 1 neighbor pixels 11: Maximum between the minimum of left 2 neighbor pixels and the minimum of right 2 neighbor pixels Bit[4]: Recover with fixed pattern Bit[3]: Fixed pattern mode 0: 0x00 1: 0xFF Bit[1]: Sensor exposure constrain enable Bit[0]: Sensor gain constrain enable
0x5506	OTP DPC EXPO CONSTRAINT L	0x00	RW	Bit[7:0]: OTP expo constrain long[15:8]
0x5507	OTP DPC EXPO CONSTRAINT L	0x00	RW	Bit[7:0]: OTP expo constrain long[7:0]
0x5508	OTP DPC GAIN CONSTRAINT L	0x07	RW	OTP Gain Constrain Long
0x5509	OTP DPC THRE L	0x08	RW	OTP Threshold Long
0x5524	OTP EXPO CONSTRAIN M	0x00	RW	Bit[7:0]: OTP expo constrain middle[15:8]
0x5525	OTP EXPO CONSTRAIN M	0x00	RW	Bit[7:0]: OTP expo constrain middle[7:0]
0x5526	OTP GAIN CONSTRAIN M	0x07	RW	OTP Gain Constrain Middle

table 5-3 OTP for cluster cancellation registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5527	OTP THRE MS	0x88	RW	Bit[7:4]: OTP threshold middle Bit[3:0]: OTP threshold short
0x5528	OTP EXPO CONSTRAIN S	0x00	RW	Bit[7:0]: OTP expo constrain short[15:8]
0x5529	OTP EXPO CONSTRAIN S	0x00	RW	Bit[7:0]: OTP expo constrain short[7:0]
0x552A	OTP GAIN CONSTRAIN S	0x07	RW	OTP Gain Constrain Short

5.4 window control (WINC)

The main purpose of the WINC module is to make the image size to be real size by removing offset.

table 5-4 WINC registers

address	register name	default value	R/W	description
0x5980	WIN XSTART_OFF	0x00	RW	Bit[4:0]: X start offset[12:8]
0x5981	WIN XSTART_OFF	0x00	RW	Bit[7:0]: X start offset[7:0]
0x5982	WIN YSTART_OFF	0x00	RW	Bit[3:0]: Y start offset[11:8]
0x5983	WIN YSTART_OFF	0x00	RW	Bit[7:0]: Y start offset[7:0]
0x5984	WIN WIDTH	0x0A	RW	Bit[4:0]: Window width[12:8]
0x5985	WIN WIDTH	0x80	RW	Bit[7:0]: Window width[7:0]
0x5986	WIN HEIGHT	0x05	RW	Bit[3:0]: Window height[11:8]
0x5987	WIN HEIGHT	0xF0	RW	Bit[7:0]: Window height[7:0]
0x5988	WIN MAN	0x00	RW	Bit[0]: Window size manual 0: Disable 1: Enable
0x5989	WIN PX_CNT	–	R	Bit[4:0]: Pixel counter[12:8]
0x598A	WIN PX_CNT	–	R	Bit[7:0]: Pixel counter[7:0]
0x598B	WIN LN_CNT	–	R	Bit[3:0]: Line counter[11:8]
0x598C	WIN LN_CNT	–	R	Bit[7:0]: Line counter[7:0]

5.5 manual white balance (MWB)

The MWB provides digital gain for R,G and B channels. Each channel gain is 12-bit. 0x400 is 1x gain.

table 5-5 MWB registers

address	register name	default value	R/W	description
0x500C	ISP CTRL0C	0x04	RW	Bit[3:0]: Long WB R gain[11:8]
0x500D	ISP CTRL0D	0x00	RW	Bit[7:0]: Long WB R gain[7:0]
0x500E	ISP CTRL0E	0x04	RW	Bit[3:0]: Long WB G gain[11:8]
0x500F	ISP CTRL0F	0x00	RW	Bit[7:0]: Long WB G gain[7:0]
0x5010	ISP CTRL10	0x04	RW	Bit[3:0]: Long WB B gain[11:8]
0x5011	ISP CTRL11	0x00	RW	Bit[7:0]: Long WB B gain[7:0]
0x5012	ISP CTRL 12	0x04	RW	Bit[3:0]: Middle WB R gain[11:8]
0x5013	ISP CTRL 13	0x00	RW	Bit[7:0]: Middle WB R gain[7:0]
0x5014	ISP CTRL 14	0x04	RW	Bit[3:0]: Middle WB G gain[11:8]
0x5015	ISP CTRL 15	0x00	RW	Bit[7:0]: Middle WB G gain[7:0]
0x5016	ISP CTRL 16	0x04	RW	Bit[3:0]: Middle WB B gain[11:8]
0x5017	ISP CTRL 17	0x00	RW	Bit[7:0]: Middle WB B gain[7:0]
0x5018	ISP CTRL 18	0x04	RW	Bit[3:0]: Short WB R gain[11:8]
0x5019	ISP CTRL 19	0x00	RW	Bit[7:0]: Short WB R gain[7:0]
0x501A	ISP CTRL 1A	0x04	RW	Bit[3:0]: Short WB G gain[11:8]
0x501B	ISP CTRL 1B	0x00	RW	Bit[7:0]: Short WB G gain[7:0]
0x501C	ISP CTRL 1C	0x04	RW	Bit[3:0]: Short WB B gain[11:8]
0x501D	ISP CTRL 1D	0x00	RW	Bit[7:0]: Short WB B gain[7:0]

5.6 AVG

The main function of the AVG module is to calculate the luminance average using special filters.

table 5-6 AVG control registers

address	register name	default value	R/W	description
0x5680	AVG X START	0x00	RW	Bit[3:0]: X start offset[11:8]
0x5681	AVG X START	0x00	RW	Bit[7:0]: X start offset[7:0]
0x5682	AVG Y START	0x00	RW	Bit[3:0]: Y start offset[11:8]
0x5683	AVG Y START	0x00	RW	Bit[7:0]: Y start offset[7:0]
0x5684	AVG WIN WIDTH	0x0A	RW	Bit[3:0]: Window width[11:8]
0x5685	AVG WIN WIDTH	0x80	RW	Bit[7:0]: Window width[7:0]
0x5686	AVG WIN HEIGHT	0x05	RW	Bit[3:0]: Window height[11:8]
0x5687	AVG WIN HEIGHT	0xF0	RW	Bit[7:0]: Window height[7:0]
0x5688	AVG WT 0	0x11	RW	Bit[7:4]: Weight of zone 01 Bit[3:0]: Weight of zone 00
0x5689	AVG WT 1	0x11	RW	Bit[7:4]: Weight of zone 03 Bit[3:0]: Weight of zone 02
0x568A	AVG WT 2	0x11	RW	Bit[7:4]: Weight of zone 11 Bit[3:0]: Weight of zone 10
0x568B	AVG WT 3	0x11	RW	Bit[7:4]: Weight of zone 13 Bit[3:0]: Weight of zone 12
0x568C	AVG WT 4	0x11	RW	Bit[7:4]: Weight of zone 21 Bit[3:0]: Weight of zone 20
0x568D	AVG WT 5	0x11	RW	Bit[7:4]: Weight of zone 23 Bit[3:0]: Weight of zone 22
0x568E	AVG WT 6	0x11	RW	Bit[7:4]: Weight of zone 31 Bit[3:0]: Weight of zone 30
0x568F	AVG WT 7	0x11	RW	Bit[7:4]: Weight of zone 33 Bit[3:0]: Weight of zone 32
0x5690	AVG MANUAL CTRL	0x02	RW	Bit[1]: Average option 0: Sum=(4*B+9*G*2+10*R) /8 1: Sum=B+G*2+R Bit[0]: Average size manual 0: Disable 1: Enable
0x5693	AVG READOUT	–	R	Bit[7:0]: High 8-bit of average output

6 register tables

The following tables provide descriptions of the device control registers contained in the OV4689. For all register enable/disable bits, ENABLE = 1 and DISABLE = 0. The device slave addresses are 0x6C for write and 0x6D for read (when SID=1, 0x20 for write and 0x21 for read).

6.1 PLL control [0x0300 - 0x031F]

table 6-1 PLL registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x0300	PLL_CTRL_0	0x00	RW	Bit[7:3]: Debug mode Bit[2:0]: pll1_pre_div
0x0301	PLL_CTRL_1	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: pll1_multiplier[9:8]
0x0302	PLL_CTRL_2	0x2A	RW	Bit[7:0]: pll1_multiplier[7:0]
0x0303	PLL_CTRL_3	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: pll1_divm Divider = /(1+ pll1_divm) (range from /1~16)
0x0304	PLL_CTRL_4	0x03	RW	Bit[7:2]: Debug mode Bit[1:0]: pll1_div_mipi 00: /4 01: /5 10: /6 11: /8
0x0305	PLL_CTRL_5	0x01	RW	Bit[7:2]: Debug mode Bit[1:0]: pll1_div_sp 00: /3 01: /4 10: /5 11: /6
0x0306	PLL_CTRL_6	0x01	RW	Bit[7:1]: Debug mode Bit[0]: pll1_div_s 0: /1 1: /2
0x0307	DEBUG MODE	–	–	Debug Mode
0x0308	PLL_CTRL_8	0x00	RW	Bit[7:1]: Debug mode Bit[0]: pll1_bypass
0x0309	PLL_CTRL_9	0x01	RW	Bit[7:3]: Debug mode Bit[2:0]: pll1_cp

table 6-1 PLL registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x030A	PLL_CTRL_A	0x00	RW	Bit[7:1]: Debug mode Bit[0]: pll1_predivp 0: /1 1: /2
0x030B	PLL_CTRL_B	0x00	RW	Bit[7:3]: Debug mode Bit[2:0]: pll2_pre_div 000: /1 001: /1.5 010: /2 011: /2.5 100: /3 101: /4 110: /6 111: /8
0x030C	PLL_CTRL_C	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: pll2_multiplier[9:8]
0x030D	PLL_CTRL_D	0x1E	RW	Bit[7:0]: pll2_multiplier[7:0]
0x030E	PLL_CTRL_E	0x04	RW	Bit[7:3]: Debug mode Bit[2:0]: pll2_rdivs 000: /1 001: /1.5 010: /2 011: /2.5 100: /3 101: /3.5 110: /4 111: /5
0x030F	PLL_CTRL_F	0x01	RW	Bit[7:4]: Debug mode Bit[3:0]: pll2_divsp Divider = /(1+ pll2_divsp) (range from /1~16)
0x0310	PLL_CTRL_10	0x01	RW	Bit[7:3]: Debug mode Bit[2:0]: pll2_cp
0x0311	PLL_CTRL_11	0x00	RW	Bit[7:1]: Debug mode Bit[0]: pll2_bypass
0x0312	PLL_CTRL_12	0x01	RW	Bit[7:4]: Debug mode Bit[3:0]: pll2_divdac Divider = /(1+ pll2_divdac) (range from /1~16)
0x031B	PLL_CTRL_1B	0x00	RW	Bit[7:1]: Debug mode Bit[0]: pll1_rst
0x031C	PLL_CTRL_1C	0x00	RW	Bit[7:1]: Debug mode Bit[0]: pll2_rst

table 6-1 PLL registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x031E	DEBUG MODE	–	–	Debug Mode
0x031F	PLL_CTRL_1F	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: lvds_bit_sel 00: Bit[8] Others: Bit[10]

6.2 system control (SC) [0x0100 - 0x303F]

table 6-2 SC registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x0100	SC_CTRL0100	0x00	RW	Bit[7:1]: Debug mode Bit[0]: software_standby 0: software_standby 1: streaming
0x0103	SC_CTRL0103	0x00	RW	Bit[7:1]: Debug mode Bit[0]: software_reset
0x3000	SC_CMMN_PAD_OEN0	0x00	RW	Bit[7:6]: Not used Bit[5]: FSIN output enable 0: Input 1: Output Bit[4:0]: Debug mode
0x3001	DEBUG MODE	–	–	Debug Mode
0x3002	SC_CMMN_PAD_OEN2	0x20	RW	Bit[7]: VSYNC output enable 0: Input 1: Output Bit[6]: HREF output enable 0: Input 1: Output Bit[5]: Debug mode Bit[4]: FREX output enable 0: Input 1: Output Bit[3:1]: Debug mode Bit[0]: GPIO0 output enable 0: Input 1: Output
0x3004	SCCB ID	0x6C	RW	SCCB Slave ID1

table 6-2 SC registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x3005	SC_CMMN_CLKRST5	0xF0	RW	Bit[7:6]: Debug mode Bit[5]: Enable SRC clock Bit[4]: Enable sync FIFO clock Bit[3:2]: Debug mode Bit[1]: Reset SRC Bit[0]: Reset sync FIFO
0x3006	CMMN_SCCB_ID2	0x42	RW	SCCB Slave ID, Sensor Unique ID Not related to SID control
0x3007	CORE_CTRL2	0x38	RW	Bit[7]: pll12_dacclk_sel Bit[6]: r_fc_byp Bit[5]: ispin_array_addr_sel Bit[4:0]: Debug mode
0x3008	SC_CMMN_PAD_OUT0	0x00	RW	Register Control Output Pad Output as GPIO (works only when related bits in register 0x300E are set to 1) Bit[7:0]: Debug mode
0x3009	DEBUG MODE	–	–	Debug Mode
0x300A	SC_CMMN_CHIP_ID	0x46	R	Chip ID High
0x300B	SC_CMMN_CHIP_ID	0x88	R	Chip ID Low
0x300D	SC_CMMN_PAD_OUT2	0x00	RW	Register Control Output Pad Output as GPIO (works only when related bits in register 0x3010 are set to 1) Bit[7]: Register control VSYNC output Bit[6]: Register control HREF output Bit[5]: Not used Bit[4]: Register control FREX output Bit[3]: Register control STROBE output Bit[2]: Register control SIOD output Bit[1]: Register control IL_PWM output Bit[0]: Register control GPIO output
0x300E~ 0x300F	DEBUG MODE	–	–	Debug Mode

table 6-2 SC registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x3010	SC_CMMN_PAD_SEL2	0x00	RW	Enable Pad as GPIO Controlled by Registers (0: pad by data path control; 1: pad as GPIO controlled by register) Bit[7]: Enable VSYNC as GPIO controlled by register Bit[6]: Enable HREF as GPIO controlled by register Bit[5]: Enable sif_sda as GPIO controlled by register Bit[4]: Enable FREX as GPIO controlled by register Bit[3]: Enable STROBE as GPIO controlled by register Bit[2]: Enable sccb_sda as GPIO controlled by register Bit[1:0]: Debug mode
0x3011	SC_CMMN_PAD_PK	0x00	RW	Bit[7]: Not used Bit[6:5]: pad_driving_strength 00: 1x 01: 2x 10: 3x 11: 4x Bit[2]: fsin_pad_enb Bit[1]: frex_pad_enb Bit[0]: Not used
0x3012	SCCB_SECOND_ID	0x20	RW	SCCB Slave ID2
0x3016	SC_CMMN_MIPI_PK	0x08	RW	Not Used
0x3017	SC_CMMN_MIPI_PK	0x10	RW	Not Used
0x3018	SC_CMMN_MIPI_SC_CTRL	0x72	RW	Bit[7:5] MIPI lane mode 000: 1-lane mode 001: 2-lane mode 011: 4-lane mode Others: Not allowed Bit[4]: Debug mode Bit[3]: Not used Bit[2]: pd_mipi_manual Bit[1]: Reset MIPI PHY when sleep Bit[0]: Auto disable MIPI lane when sleep

table 6-2 SC registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x3019	SC_CMMN_MIPI_SC_CTRL	0x00	RW	Bit[7:4]: Debug mode Bit[3]: Manual lane disable 1: Disable MIPI lane 3 Bit[2]: Manual lane disable 1: Disable MIPI lane 2 Bit[1]: Manual lane disable 1: Disable MIPI lane 1 Bit[0]: Manual lane disable 1: Disable MIPI lane 0
0x301A	SC_CMMN_CLKRST0	0xF0	RW	Bit[7]: Enable emb clock Bit[6]: Enable strobe clock Bit[5]: Debug mode Bit[4]: Enable timing control clock Bit[3]: mipi_phy_rst_manual Bit[2]: Reset strobe block Bit[1]: Reset analog control block Bit[0]: Reset timing control block
0x301B	SC_CMMN_CLKRST1	0xF0	RW	Bit[7]: Enable BLC clock Bit[6]: Enable ISP clock Bit[5]: Enable AVG clock Bit[4]: Enable VFIFO clock Bit[3]: Reset BLC Bit[2]: Reset ISP Bit[1]: Reset TESTMOD Bit[0]: Reset VFIFO
0x301C	SC_CMMN_CLKRST2	0xF0	RW	Bit[7]: Debug mode Bit[6]: Enable MIPI clock Bit[5]: Debug mode Bit[4]: Enable OTP clock Bit[3]: Debug mode Bit[2]: Reset MIPI Bit[1]: Debug mode Bit[0]: Reset OTP
0x301D	SC_CMMN_CLKRST3	0xF0	RW	Bit[7]: Debug mode Bit[6]: Enable group control clock Bit[5]: Enable BIST clock Bit[4:3]: Debug mode Bit[2]: Reset group control Bit[1]: Reset BIST Bit[0]: Debug mode

table 6-2 SC registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x301E	SC_CMMN_CLKRST4	0xF0	RW	Bit[7]: Debug mode Bit[6]: pclk_lvds Bit[5]: pclk_vfifo Bit[4]: pclk_mipi Bit[3]: Debug Bit[2]: rst_lvds Bit[1]: rst_emb Bit[0]: Debug mode
0x301F	SC_CMMN_CLKRST5	0x00	RW	Reset Each Module Before Entering into FREX Mode Bit[7]: Reset AEC Bit[6]: Reset SRC/BLC/SYNC_FIFO Bit[5]: Reset ISP Bit[4]: Debug mode Bit[3]: Reset MIPI Bit[2]: Reset VFIFO Bit[1]: Reset TESTMOD Bit[0]: Reset MIPI_PHY
0x3020	SC_CMMN_CLOCK_ SEL	0x93	RW	Bit[7]: Clock switch control 0: Switch to pad clock 1: Switch to PLL clock Bit[6:4]: Debug mode Bit[3]: pclk_sel 0: Select pll_pclk_i 1: Select pll_pclk_d2 Bit[2:0]: Debug mode
0x3021	SC_CMMN_MISC_ CTRL	0x63	RW	Bit[7]: Debug mode Bit[6]: Sleep no latch enable Bit[5]: fst_stby_ctr 0: Software standby enter at v_blk 1: Software standby enter at l_blk Bit[4:1]: Debug mode Bit[0]: cen_global_o for all SRAM
0x3022	SC_CMMN_MIPI_SC_ CTRL	0x01	RW	Bit[7:4]: Debug mode Bit[3]: Enable LVDS mode Bit[2]: MIPI clock lane1 disable manual Bit[1]: MIPI clock lane0 disable manual Bit[0]: Enable power down MIPI when sleep
0x302A	SC_CMMN_SUB_ID	–	R	Bit[7:4]: Process Bit[3:0]: Version

table 6-2 SC registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x3030	SC_CMMN_CLK_INV	0x00	RW	Bit[7:6]: Debug mode Bit[5]: Reverse SCLK Bit[4]: Reverse PCLK Bit[3:0]: Debug mode
0x3031	SC_CMMN_BIT_SEL	0x0A	RW	Bit[7:5]: Debug mode Bit[4:0]: mipi_bit_sel 01000: 8-bit mode 01010: 10-bit mode 01100: 12-bit mode Others: Not allowed
0x3032	SC_CMMN_CORE_CTRL0	0x00	RW	Bit[7]: isp_sof_in_opt Bit[6]: Debug mode Bit[5]: array_hskip_man_en Bit[4]: sram_bin_man_en Bit[3]: sram_hbin_man Bit[2:0]: array_hskip_man[3:1]
0x3034~ 0x3036	DEBUG MODE	–	–	Debug Mode
0x3037	SID CTRL	0x00	RW	Bit[7:1]: Debug mode Bit[0]: r_sid 0: Select ID1 when SID = 0 or ID2 when SID = 1 1: Select ID2 when SID = 0 or ID1 when SID = 1
0x3038~ 0x303D	DEBUG MODE	–	–	Debug Mode
0x303F	SCCB_ID_CTRL	0x00	RW	Bit[7:1]: Debug mode Bit[0]: Enable programmable ID1 and ID2 0: ID1 fix = 0x6C ID2 fix = 0x20 1: ID1 from register 0x3004 ID2 from register 0x3012

6.3 SCCB control [0x3100 - 0x3106]

table 6-3 SCCB registers

address	register name	default value	R/W	description
0x3100~ 0x3106	DEBUG MODE	–	–	Debug Mode

6.4 group hold [0x3200 - 0x320F]

table 6-4 group hold registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3200	GROUP ADR0	0x00	RW	Group0 Start Address in SRAM, Actual Address is {0x3200[5:0], 0x0}
0x3201	GROUP ADR1	0x10	RW	Group1 Start Address in SRAM, Actual Address is {0x3201[5:0], 0x0}
0x3202	GROUP ADR2	0x20	RW	Group2 Start Address in SRAM, Actual Address is {0x3202[5:0], 0x0}
0x3203	GROUP ADR3	0x30	RW	Group3 Start Address in SRAM, Actual Address is {0x3203[5:0], 0x0}
0x3204	GROUP LEN0	–	R	Length of Group0
0x3205	GROUP LEN1	–	R	Length of Group1
0x3206	GROUP LEN2	–	R	Length of Group2
0x3207	GROUP LEN3	–	R	Length of Group3
0x3208	GROUP ACCESS	–	W	Bit[7:4]: group_ctrl 0000: Group hold start 0001: Group hold end 1010: Group launch 1110: Fast group launch Others: Debug mode Bit[3:0]: Group ID 0000: Group bank 0 0001: Group bank 1 0010: Group bank 2 0011: Group bank 3 Others: Debug mode
0x3209	GROUP0 PERIOD	0x00	RW	Bit[7]: Debug mode Bit[6:5]: Switch back group Bit[4:0]: Number of frames to stay in group 0
0x320A	GROUP1 PERIOD	0x00	RW	Number of Frames to Stay in Group 1
0x320B	GRP_SW_CTRL	0x01	RW	Bit[7]: Auto switch enable Bit[6:5]: Debug mode Bit[4]: frame_cnt_trig Bit[3]: group_switch_repeat Enable the first group (group 0) and second group repeatable switch Bit[2]: context_en Enable the switch from second group back to first group (group 0) Bit[1:0]: Second group select

table 6-4 group hold registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x320C	SRAM TEST	0x0A	RW	Bit[7:5]: Debug mode Bit[4]: Group hold SRAM test enable Bit[3:0]: Group hold SRAM RM[3:0]
0x320D	GRP_ACT	–	R	Active Group Indicator
0x320E	FM_CNT_GRP0	–	R	Group 0 Frame Count
0x320F	FM_CNT_GRP1	–	R	Group 1 Frame Count

6.5 ASRAM control [0x3300 - 0x3318]

table 6-5 ASRAM control registers

address	register name	default value	R/W	description
0x3300~ 0x3318	ASRAM TEST	–	–	ASRAM Control Registers

6.6 ADC and analog control [0x3600 - 0x364C]

table 6-6 ADC and analog control registers

address	register name	default value	R/W	description
0x3600~ 0x364C	ANALOG CTRL	–	–	Analog Control Registers

6.7 sensor control [0x3700 - 0x379A]

table 6-7 sensor control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3700~ 0x375F	SENSOR CTRL	–	–	Sensor Timing Control Registers

table 6-7 sensor control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3760	SENSOR CTRL60	0x00	RW	Max Medium Exposure Time in Staggered HDR Mode MSB (works only when 0x3764[0] = 1)
0x3761	SENSOR CTRL61	0x00	RW	Max Medium Exposure Time in Staggered HDR Mode LSB (works only when 0x3764[0] = 1)
0x3762	SENSOR CTRL62	0x00	RW	Max Short Exposure Time in Staggered HDR Mode MSB (works only when 0x3764[0] = 1)
0x3763	SENSOR CTRL63	0x00	RW	Max Short Exposure Time in Staggered HDR Mode LSB (works only when 0x3764[0] = 1)
0x3764	SENSOR CTRL64	0x00	RW	Bit[0]: Stagger HDR mode output timing manual control enable
0x3765~ 0x379C	SENSOR CTRL	–	–	Sensor Timing Control Registers

6.8 FREX control [0x37C5 - 0x37DF]

table 6-8 FREX control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x37C5	FREX_REG5	0x00	RW	Bit[7:0]: Frame exposure[23:16] MSB of frame exposure time in mode 2. Exposure time in units of 128 system clock cycles
0x37C6	FREX_REG6	0x00	RW	Bit[7:0]: Frame exposure[15:8] Middle byte of frame exposure time in mode 2
0x37C7	FREX_REG7	0x08	RW	Bit[7:0]: Frame exposure[7:0] LSB of frame exposure time in mode 2
0x37C8	DEBUG MODE	–	–	Debug Mode
0x37C9	FREX_REG9	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: Strobe width[19:16] MSB of strobe width in mode 2. Strobe width in units of 1 system clock cycle.
0x37CA	FREX_REGA	0x06	RW	Bit[7:0]: Strobe width[15:8] Middle byte of strobe width in mode 2
0x37CB	FREX_REGB	0x00	RW	Bit[7:0]: Strobe width[7:0] LSB of strobe width in mode 2

table 6-8 FREX control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x37CC	FREX_REGC	0x00	RW	Bit[7:5]: Debug mode Bit[4:0]: Shutter dly[12:8] MSB of shutter delay in mode 2. Shutter delay is in units of 128 system clock cycles.
0x37CD	FREX_REGD	0x44	RW	Bit[7:0]: Shutter dly[7:0] LSB of shutter delay in mode 2
0x37CE	FREX_REGE	0x1F	RW	Bit[7:0]: FREX precharge width[15:8] MSB of sensor precharge in mode 2. Sensor precharge is in units of 1 system clock cycle.
0x37CF	FREX_REGF	0x40	RW	Bit[7:0]: FREX precharge width[7:0] LSB of sensor precharge in mode 2
0x37D0	FREX_REG10	0x00	RW	Bit[7:0]: Readout delay[15:8] MSB of readout delay time in mode 2. Readout delay time is in units of 128 system clock cycles.
0x37D1	FREX_REG11	0x01	RW	Bit[7:0]: Readout delay[7:0] LSB of readout delay time in mode 2
0x37D2	FREX_REG12	0x00	RW	Bit[7:5]: Debug mode Bit[4:0]: Strobe delay[12:8] Unit is system clock
0x37D3	FREX_REG13	0x00	RW	Bit[7:0]: Strobe delay[7:0]
0x37D4~ 0x37D6	DEBUG MODE	–	–	Debug Mode
0x37DE	FREX_REG1E	0x01	RW	Bit[7:1]: Debug mode Bit[0]: FREX SCCB request repeat trigger selection 0: SOF 1: EOF

table 6-8 FREX control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x37DF	FREX_REG1F	0x04	RW	Bit[7]: FREX SCCB request (self-clearing) Bit[6]: Debug mode Bit[5]: frex_strobe_out_sel 0: Strobe for rolling mode 1: Strobe for frame mode Bit[4]: FREX nopchg Bit[3]: FREX strobe polarity 0: Active high 1: Active low Bit[2]: FREX shutter polarity Bit[1]: FREX pad input enable 0: Frame mode is triggered by register 1: Frame mode is triggered by FREX pad Bit[0]: No latch at SOF for FREX SCCB request 0: Trigger frame mode in SOF 1: Trigger frame mode immediately

6.9 timing control [0x3800 - 0x3847]

table 6-9 timing control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x3800	H_CROP_START	0x00	RW	Bit[7:5]: Debug mode Bit[4:0]: Horizontal crop start address[12:8]
0x3801	H_CROP_START	0x00	RW	Bit[7:0]: Horizontal crop start address[7:0]
0x3802	V_CROP_START	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: Vertical crop start address[11:8]
0x3803	V_CROP_START	0x04	RW	Bit[7:0]: Vertical crop start address[7:0]
0x3804	H_CROP_END	0x0A	RW	Bit[7:5]: Debug mode Bit[4:0]: Horizontal crop end address[12:8]
0x3805	H_CROP_END	0x9F	RW	Bit[7:0]: Horizontal crop end address[7:0]
0x3806	V_CROP_END	0x05	RW	Bit[7:4]: Debug mode Bit[3:0]: Vertical crop end address[11:8]
0x3807	V_CROP_END	0xFB	RW	Bit[7:0]: Vertical crop end address[7:0]
0x3808	H_OURPUT_SIZE	0x0A	RW	Bit[7:5]: Debug mode Bit[4:0]: Horizontal output size[12:8]

table 6-9 timing control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x3809	H_OUTPUT_SIZE	0x80	RW	Bit[7:0]: Horizontal output size[7:0]
0x380A	V_OURPUT_SIZE	0x05	RW	Bit[7:4]: Debug mode Bit[3:0]: Vertical output size[11:8]
0x380B	V_OUTPUT_SIZE	0xF0	RW	Bit[7:0]: Vertical output size[7:0]
0x380C	TIMING_HTS	0x03	RW	Bit[7]: Debug mode Bit[6:0]: Horizontal total size[14:8]
0x380D	TIMING_HTS	0x5C	RW	Bit[7:0]: Horizontal total size[7:0]
0x380E	TIMING_VTS	0x06	RW	Bit[7]: Debug mode Bit[6:0]: Vertical total size[14:8]
0x380F	TIMING_VTS	0x10	RW	Bit[7:0]: Vertical total size[7:0]
0x3810	H_WIN_OFF	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: Horizontal windowing offset[11:8]
0x3811	H_WIN_OFF	0x10	RW	Bit[7:0]: Horizontal windowing offset[7:0]
0x3812	V_WIN_OFF	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: Vertical windowing offset[11:8]
0x3813	V_WIN_OFF	0x02	RW	Bit[7:0]: Vertical windowing offset[7:0]
0x3814	H_INC_ODD	0x01	RW	Bit[7:5]: Debug mode Bit[4:0]: Horizontal sub-sample odd increase number
0x3815	H_INC_EVEN	0x01	RW	Bit[7:5]: Debug mode Bit[4:0]: Horizontal sub-sample even increase number
0x3816	VSYNC_START_H	0x00	RW	Bit[7:0]: Timing control VSYNC start point[15:8]
0x3817	VSYNC_START_L	0x00	RW	Bit[7:0]: Timing control VSYNC start point[7:0]
0x3818	VSYNC_END_H	0x00	RW	Bit[7:0]: Timing control VSYNC end point[15:8]
0x3819	VSYNC_END_L	0x00	RW	Bit[7:0]: Timing control VSYNC end point[7:0]
0x381A	VTS_EXP_DIFF	0x04	RW	Bit[7:0]: Difference between VTS and exposure

table 6-9 timing control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x3820	FORMAT	0x00	RW	Timing Control Register Bit[7:4]: Debug mode Bit[3]: bypass_isp Bit[2]: Digital vertical flip enable 0: Normal 1: Vertical flip Bit[1]: Array vertical flip enable 0: Normal 1: Vertical flip Bit[0]: Vbin
0x3821	FORMAT	0x00	RW	Bit[7:3]: Debug mode Bit[2]: Digital horizontal mirror enable 0: Normal 1: Horizontal mirror Bit[1]: Array horizontal mirror enable 0: Normal 1: Horizontal mirror Bit[0]: Not used
0x3822	TIMING_REG22	0x88	RW	Bit[7:5]: zero_line_num /2 Bit[4:0]: blc_line_num /2
0x3823	TIMING_REG23	0x00	RW	Bit[7]: ext_vs_re Bit[6]: ext_vs_en Bit[5:0]: Debug mode
0x3824	CS_RST_FSIN	0x00	RW	Bit[7:0]: CS reset value at vs_ext[15:8]
0x3825	CS_RST_FSIN	0x20	RW	Bit[7:0]: CS reset value at vs_ext[7:0]
0x3826	R_RST_FSIN	0x00	RW	Bit[7:0]: R reset value at vs_ext[15:8]
0x3827	R_RST_FSIN	0x04	RW	Bit[7:0]: R reset value at vs_ext[7:0]
0x3828	TIMING_REG28	0x00	RW	Bit[7]: ext_hs_re Bit[6]: ext_hs_en Bit[5]: Debug mode Bit[4]: hts_inc_en at slave mode Bit[3:0]: Debug mode
0x3829	FORMAT	0x00	RW	Bit[7:4]: Debug mode Bit[3]: hdr_lite_en Bit[2:0]: Not used
0x382A	V_INC_ODD	0x01	RW	Bit[7:5]: Debug mode Bit[4:0]: Vertical sub-sample odd increase number
0x382B	V_INC_EVEN	0x01	RW	Bit[7:5]: Debug mode Bit[4:0]: Vertical sub-sample even increase number
0x382C	BLC_COL_ST	0x00	RW	Bit[7:0]: Black column start address

table 6-9 timing control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x382D	BLC_COL_END	0x7F	RW	Bit[7:0]: Black column end address
0x3830	BLC_NUM_OPTION	0x04	RW	Bit[7:5]: blc_adj Bit[4:0]: blc_use_num /2
0x3831	BLC_NUM_MAN	0x00	RW	Bit[7:6]: Debug mode Bit[5]: Manually set BLC num enable Bit[4:0]: blc_num_man /2
0x3832	FRACTIONAL_HTS	0x00	RW	Bit[7:0]: Fractional HTS in slave mode[15:8]
0x3833	FRACTIONAL_HTS	0x00	RW	Bit[7:0]: Fractional HTS in slave mode[7:0]
0x3834	EXT_DIV_FACTORS	0x01	RW	Bit[7:4]: ext_vs_div Bit[3:0]: ext_hs_div
0x3835	DEBUG MODE	–	–	Debug Mode
0x3836	TIMING_REG_36	0x01	RW	Bit[7:5]: Debug mode Bit[4:0]: r_zline_use_num/2
0x3837	TIMING_REG_37	0x00	RW	Bit[7]: stg_vc_man_en Bit[6]: Not used Bit[5:4]: vc_l Bit[3:2]: vc_m Bit[1:0]: vc_s
0x3841	TIMING_REG_41	0x02	RW	Bit[7:5]: Debug mode Bit[4]: r_sdg_hdr_num Bit[3:2]: Debug mode Bit[1]: r_rcnt_fix Bit[0]: r_stg_hdr_en
0x3846	TIMING_REG_46	0x08	RW	Bit[7:5]: Debug mode Bit[4]: r_seq_hdr_sw_opt Bit[3]: fcnt_trig_rst_en Bit[2:0]: r_seq_hdr_num
0x3847	DEBUG MODE	–	–	Debug Mode

6.10 strobe [0x3B00 - 0x3B05]

table 6-10 strobe control registers

address	register name	default value	R/W	description
0x3B00	STROBE CTRL	0x00	RW	Bit[7]: Strobe ON/OFF Bit[6]: Strobe polarity 0: Active high 1: Active low Bit[5:4]: width_in_xenon Bit[2:0]: Mode 000: Xenon 001: LED1 010: LED2 011: LED3 100: LED4
0x3B02	STROBE DMY H	0x00	RW	Dummy Lines Added at Strobe Mode, MSB
0x3B03	STROBE DMY L	0x00	RW	Dummy Lines Added at Strobe Mode, LSB
0x3B04	STROBE CTRL	0x00	RW	Bit[7:4]: Debug mode Bit[3]: start_point_sel Bit[2]: Strobe repeat enable Bit[1:0]: Strobe latency 00: Strobe generated at next frame 01: Strobe generated 2 frames later 10: Strobe generated 3 frames later 11: Strobe generated 4 frames later
0x3B05	STROBE WIDTH	0x00	RW	Bit[7:2]: Strobe pulse width step Bit[1:0]: Strobe pulse width gain strobe_pulse_width = 128×(2^gain)×(step+1)×Tsclk

6.11 PSRAM control [0x3F00 - 0x3F0A]

table 6-11 PSRAM control registers

address	register name	default value	R/W	description
0x3F00~ 0x3F0A	PSRAM CTRL	–	–	PSRAM Control Registers

6.12 ADC sync control [0x4500 - 0x4503]

table 6-12 ADC sync control registers

address	register name	default value	R/W	description
0x4500~ 0x4503	ADC_SYNC_CTRL	–	–	ADC Sync Control

6.13 test mode [0x8000 - 0x8008]

table 6-13 test mode registers

address	register name	default value	R/W	description
0x8000	TEST CTRL1	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: fix_pattern_B[11:8]
0x8001	TEST CTRL2	0x00	RW	Bit[7:0]: fix_pattern_B[7:0]
0x8002	TEST CTRL3	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: fix_pattern_Gb[11:8]
0x8003	TEST CTRL4	0x00	RW	Bit[7:0]: fix_pattern_Gb[7:0]
0x8004	TEST CTRL5	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: fix_pattern_Gr[11:8]
0x8005	TEST CTRL6	0x00	RW	Bit[7:0]: fix_pattern_Gr[7:0]
0x8006	TEST CTRL7	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: fix_pattern_R[11:8]
0x8007	TEST CTRL8	0x00	RW	Bit[7:0]: fix_pattern_R[7:0]
0x8008	TEST CTRL9	0x00	RW	Bit[7:2]: Debug mode Bit[1]: PN9 enable Bit[0]: Fix pattern enable

6.14 OTP control [0x3D80 - 0x3D8D]

table 6-14 OTP control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3D80	OTP_PROGRAM_CTRL	0x00	RW	Bit[7]: OTP_wr_busy Bit[6:1]: Debug mode Bit[0]: OTP_program_enable
0x3D81	OTP_LOA_CTRL	0x00	RW	Bit[7]: OTP_rd_busy Bit[6]: Debug mode Bit[5]: OTP_bist_error Bit[4]: OTP_bist_done Bit[3:1]: Debug mode Bit[0]: OTP_load_enable
0x3D82	OTP_PGM_PULSE	0x55	RW	Program Strobe Pulse Width Unit: 8×system clock period
0x3D83	OTP_LOAD_PULSE	0x08	RW	Load Strobe Pulse Width Unit: system clock period
0x3D84	OTP_MODE_CTRL	0x00	RW	Bit[7]: Program disable 0: Enable 1: Disable Bit[6]: Mode select 0: Auto mode 1: Manual mode Bit[5:0]: Debug mode
0x3D85	OTP_REG85	0x10	RW	Bit[7:6]: Debug mode Bit[5]: OTP_bist_select 0: Compare with SRAM 1: Compare with zero Bit[4]: OTP_bist_enable Bit[3]: Debug mode Bit[2]: OTP power up load data enable Bit[1]: OTP power up load setting enable Bit[0]: OTP write register load setting enable
0x3D86	SRAM_TEST_SIGNALS	0x02	RW	Bit[7:3]: Debug mode Bit[2]: r_test Bit[1:0]: r_rm
0x3D87	OTP_PS2CS	0x0A	RW	OTP PS to CSB Delay Unit: system clock period
0x3D88	OTP_START_ADDRESS	0x00	RW	OTP Start High Address for Manual Mode
0x3D89	OTP_START_ADDRESS	0x00	RW	OTP Start Low Address for Manual Mode

table 6-14 OTP control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3D8A	OTP_EN_ADDRESS	0x00	RW	OTP End High Address for Manual Mode
0x3D8B	OTP_END_ADDRESS	0x00	RW	OTP End Low Address for Manual Mode
0x3D8C	OTP_SETTING_STT_ ADDRESS	0x00	RW	OTP Start High Address for Load Setting
0x3D8D	OTP_SETTING_STT_ ADDRESS	0x00	RW	OTP Start Low Address for Load Setting

6.15 frame control [0x4200 - 0x4203]

table 6-15 frame control registers

address	register name	default value	R/W	description
0x4200	FRAME CTRL0	0x00	RW	Bit[7:3]: Debug mode Bit[2]: fcnt_eof_sel Bit[1]: fcnt_mask_dis Bit[0]: fcnt_reset
0x4201	FRAME ON NUMBER	0x00	RW	Bit[3:0]: Frame on number
0x4202	FRAME OFF NUMBER	0x00	RW	Bit[3:0]: Frame off number
0x4203	FRAME CTRL1	0x00	RW	Bit[7:6]: Debug mode Bit[5]: data_mask_dis Bit[4]: valid_mask_dis Bit[3]: href_mask_dis Bit[2]: eof_mask_dis Bit[1]: sof_mask_dis Bit[0]: all_mask_dis

6.16 ISPFC [0x4240 - 0x4243]

table 6-16 ISPFC registers

address	register name	default value	R/W	description
0x4240	FRAME CTRL0	0x00	RW	Bit[7:3]: Debug mode Bit[2]: fcnt_eof_sel Bit[1]: fcnt_mask_dis Bit[0]: fcnt_reset
0x4241	FRAME ON NUMBER	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: Frame on number
0x4242	FRAME OFF NUMBER	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: Frame off number
0x4243	FRAME CTRL1	0x00	RW	Bit[7:6]: Debug mode Bit[5]: data_mask_dis Bit[4]: valid_mask_dis Bit[3]: href_mask_dis Bit[2]: eof_mask_dis Bit[1]: sof_mask_dis Bit[0]: all_mask_dis

6.17 format clip [0x4302 - 0x4307]

table 6-17 format clip registers

address	register name	default value	R/W	description
0x4302	CLIPPING MAX	0xFF	RW	Bit[7:0]: Clipping max[15:8]
0x4303	CLIPPING MAX	0xFF	RW	Bit[7:0]: Clipping max[7:0]
0x4304	CLIPPING MIN	0x00	RW	Bit[7:0]: Clipping min[15:8]
0x4305	CLIPPING MIN	0x00	RW	Bit[7:0]: Clipping min[7:0]
0x4306	DPCM_CTRL	0x00	RW	Bit[7:3]: Debug mode Bit[2]: vfifo_pix_swap Bit[1]: dpcm_en Bit[0]: vfifo_rblue 0: First is red line 1: First is blue line
0x4307	MIPI DT16	0x2E	RW	Bit[7:0]: Debug mode
0x4308	EMBED CTRL	0x02	RW	Bit[7:1]: Debug mode Bit[0]: embed_en

6.18 VFIFO [0x4600 - 0x4603]

table 6-18 VFIFO registers

address	register name	default value	R/W	description
0x4600	VFIFO_CTRL_00	0x00	RW	Bit[7:0]: r_vfifo_read_start[15:8]
0x4601	VFIFO_CTRL_01	0x04	RW	Bit[7:0]: r_vfifo_read_start[7:0]
0x4602~ 0x4603	DEBUG MODE	–	–	Debug Mode

6.19 MIPI top [0x4800 - 0x484F]

table 6-19 MIPI top registers (sheet 1 of 9)

address	register name	default value	R/W	description
0x4800	MIPI CTRL 00	0x04	RW	MIPI Control 00 Bit[7]: mipi_hs_only 1: MIPI always in high speed mode Bit[6]: Debug mode Bit[5]: Clock lane gate enable 0: Clock lane is free running 1: Gate clock lane when no packet to transmit Bit[4]: Line sync enable 0: Do not send line short packet for each line 1: Send line short packet for each line Bit[3]: r_frame_act_all1 Bit[2:0]: Debug mode

table 6-19 MIPI top registers (sheet 2 of 9)

address	register name	default value	R/W	description
0x4801	MIPI CTRL 01	0x00	RW	MIPI Control 01 Bit[7]: Debug mode Bit[6]: Short packet data type manual enable 1: Use dt_spkt as short packet data Bit[5]: first_bit Change clk_lane first bit 0: Output 0x05 1: Output 0xAA Bit[4]: PH bit order for ECC 0: {DI[7:0],WC[7:0], WC[15:8]} 1: {DI[0:7],WC[0:7], WC[8:15]} Bit[3:2]: Debug mode Bit[1]: LPX select for pclk domain 0: Auto calculate t_lpx_p, unit pclk2x cycle 1: Use lpx_p_min[7:0] Bit[0]: Debug mode

table 6-19 MIPI top registers (sheet 3 of 9)

address	register name	default value	R/W	description
0x4802	MIPI CTRL 02	0x00	RW	MIPI Control 02 Bit[7]: hs_prepare_sel 0: Auto calculate T_hs_prepare, unit pclk2x 1: Use hs_prepare_min_o[7:0] Bit[6]: clk_prepare_sel 0: Auto calculate T_clk_prepare, unit pclk2x 1: Use clk_prepare_min_o[7:0] Bit[5]: clk_post_sel 0: Auto calculate T_clk_post, unit pclk2x 1: Use clk_post_min_o[7:0] Bit[4]: clk_trail_sel 0: Auto calculate T_clk_trail, unit pclk2x 1: Use clk_trail_min_o[7:0] Bit[3]: hs_exit_sel 0: Auto calculate T_hs_exit, unit pclk2x 1: Use hs_exit_min_o[7:0] Bit[2]: hs_zero_sel 0: Auto calculate T_hs_zero, unit pclk2x 1: Use hs_zero_min_o[7:0] Bit[1]: hs_trail_sel 0: Auto calculate T_hs_trail, unit pclk2x 1: Use hs_trail.min_o[7:0] Bit[0]: clk_zero_sel 0: Auto calculate T_clk_zero, unit pclk2x 1: Use clk_zero_min_o[7:0]
0x4803	MIPI CTRL 03	0x00	RW	MIPI Control 03 Bit[7:4]: Debug mode Bit[3]: manual_ofset_o t_period manual offset Bit[2]: r_manual_half2one t_period half to 1 Bit[1:0]: Debug mode
0x4804	MIPI CTRL 04	0x04	RW	MIPI Control 04 Bit[7:4]: man_lane_num Bit[3]: lane_num_manual_enable Bit[2]: lane4_6b_en 1: Support 4,7,8-lane 6-bit Bit[1:0]: Debug mode

table 6-19 MIPI top registers (sheet 4 of 9)

address	register name	default value	R/W	description
0x4805	MIPI CTRL 05	0x00	RW	MIPI Control 05 Bit[7:4]: Debug mode Bit[3]: lpda_retime_manu_o Bit[2]: lpda_retime_sel_o 1: Manual Bit[1]: lpck_retime_manu_o Bit[0]: lpck_retime_sel_o 1: Manual
0x4806	MIPI REG R/W CTRL	0x10	RW	Bit[7:4]: Debug mode Bit[3]: mipi_remote_rst Bit[2]: mipi_susp Bit[1]: smia_lane_ch_en Bit[0]: tx_lsb_first
0x4807	SW T LPX	0x03	RW	Bit[7:4]: Debug mode Bit[3:0]: ul_tx_lpx
0x4808	WKUP DLY	0x0A	RW	Bit[7:0]: Mark1 wake-up delay/2^10
0x4810	MIPI MAX FRAME COUNT	0xFF	RW	High Byte of Maximum Frame Count of Frame Sync Short Packet
0x4811	MIPI MAX FRAME COUNT	0xFF	RW	Low Byte of Maximum Frame Count of Frame Sync Short Packet
0x4813	MIPI CTRL13	0x00	RW	MIPI Control 13 Bit[7:4]: Debug mode Bit[3]: Select HDR virtual channel enable 0: Select manual Input VC 1: Select HDR VC Bit[2]: vc_sel Input VC or register VC Bit[1:0]: VC Virtual channel of MIPI
0x4814	MIPI CTRL14	0x2A	RW	MIPI Control 14 Bit[7]: Debug mode Bit[6]: lpkt_dt_sel 0: Use mipi_dt 1: Use dt_man_o as long packet data Bit[5:0]: Data type in manual mode

table 6-19 MIPI top registers (sheet 5 of 9)

address	register name	default value	R/W	description
0x4815	MIPI_DT_SPKT	0x00	RW	Bit[7]: Debug mode Bit[6]: pclk_inv 0: Use falling edge of mipi_pclk_o to generate MIPI bus to PHY 1: Use rising edge of mipi_pclk_o to generate MIPI bus to PHY Bit[5:0]: Manual data type for short packet
0x4816	EMB_DT_SEL	0x52	RW	emb_dt_sel Bit[7]: Debug mode Bit[6]: emb_line_sel 1: Use emb_dt as data in first emb_line_nu bit[5:0]: emb_dt Manual set embedded data type
0x4818	HS_ZERO_MIN	0x00	RW	High Byte of Minimum Value for hs_zero, unit ns
0x4819	HS_ZERO_MIN	0x70	RW	Low Byte of Minimum Value for hs_zero, unit ns hs_zero_real = hs_zero_min_o + Tui*ui_hs_zero_min_o
0x481A	HS_TRAIL_MIN	0x00	RW	High Byte of Minimum Value for hs_trail, unit ns
0x481B	HS_TRAIL_MIN	0x3C	RW	Low Byte of Minimum Value for hs_trail, unit ns hs_trail_real = hs_trail_min_o + Tui*ui_hs_trail_min_o
0x481C	CLK_ZERO_MIN	0x01	RW	High Byte of Minimum Value for clk_zero, unit ns
0x481D	CLK_ZERO_MIN	0x06	RW	Low Byte of Minimum Value for clk_zero, unit ns clk_zero_real = clk_zero_min_o + Tui*ui_clk_zero_min_o
0x481E	CLK_PREPARE_MAX	0x5F	RW	Maximum Value for clk_prepare, unit ns clk_prepare_max
0x481F	CLK_PREPARE_MIN	0x36	RW	Minimum Value for clk_prepare clk_prepare_real = clk_prepare_min_o + Tui*ui_clk_prepare_min_o
0x4820	CLK_POST_MIN	0x00	RW	High Byte of Minimum Value for clk_post, unit ns Bit[7:2]: Debug mode Bit[1:0]: clk_post_min[9:8]
0x4821	CLK_POST_MIN	0x3C	RW	Low Byte of Minimum Value for clk_post, unit ns clk_post_real = clk_post_min_o + Tui*ui_clk_post_min_o

table 6-19 MIPI top registers (sheet 6 of 9)

address	register name	default value	R/W	description
0x4822	CLK_TRAIL_MIN	0x00	RW	High Byte of Minimum Value for clk_trail, unit ns Bit[7:2]: Debug mode Bit[1:0]: clk_trail_min[9:8]
0x4823	CLK_TRAIL_MIN	0x3C	RW	Low Byte of Minimum Value for clk_trail, unit ns clk_trail_real = clk_trail_min_o + Tui*ui_clk_trail_min_o
0x4824	LPX_P_MIN	0x00	RW	High Byte of Minimum Value for lpx_p, unit ns Bit[7:2]: Debug mode Bit[1:0]: lpx_p_min[9:8]
0x4825	LPX_P_MIN	0x32	RW	Low Byte of Minimum Value for lpx_p, unit ns lpx_p_real = lpx_p_min_o + Tui*ui_lpx_p_min_o
0x4826	HS_PREPARE_MIN	0x28	RW	Minimum Value for hs_prepare, unit ns hs_prepare_min
0x4827	HS_PREPARE_MAX	0x55	RW	Maximum Value for hs_prepare hs_prepare_real = hs_prepare_min_o + Tui*ui_hs_prepare_min_o
0x4828	HS_EXIT_MIN	0x00	RW	High byte of Minimum value for hs_exit, unit ns Bit[7:2]: Debug mode Bit[1:0]: hs_exit_min[9:8]
0x4829	HS_EXIT_MIN	0x64	RW	Low Byte of Minimum value for hs_exit, unit ns hs_exit_real = hs_exit_min_o + Tui*ui_hs_exit_min_o
0x482A	UI_HS_ZERO_MIN	0x06	RW	Minimum UI Value for hs_zero, unit UI
0x482B	UI_HS_TRAIL_MIN	0x04	RW	Minimum UI Value for hs_trail, unit UI
0x482C	UI_CLK_ZERO_MIN	0x00	RW	Minimum UI Value for clk_zero, unit UI
0x482D	UI_CLK_PREPARE	0x00	RW	ui_clk_prepare_min_ctrl Bit[7:4]: Debug mode Bit[3:0]: ui_clk_prepare_min Minimum UI value of clk_prepare, unit UI
0x482E	UI_CLK_POST_MIN	0x34	RW	Minimum UI Value of clk_post, unit UI
0x482F	UI_CLK_TRAIL_MIN	0x00	RW	Minimum UI Value of clk_trail, unit UI
0x4830	UI_LPX_P_MIN	0x00	RW	Minimum UI Value of lpx_p, unit UI

table 6-19 MIPI top registers (sheet 7 of 9)

address	register name	default value	R/W	description
0x4831	UI_HS_PREPARE_MIN	0x6C	RW	ui_hs_prepare Bit[7:4]: ui_hs_prepare_max Maximum UI value of hs_prepare, unit UI Bit[3:0]: ui_hs_prepare_min Minimum UI value of hs_prepare, unit UI
0x4832	UI_HS_EXIT_MIN	0x00	RW	Minimum UI Value of hs_exit, unit UI
0x4833	MIPI_PKT_ST_SIZE	0x08	RW	Bit[7:6]: Debug mode Bit[5:0]: mipi_pkt_start_size
0x4836	GLB_MODE_SEL	0x00	RW	glb_mode_sel Bit[7:1]: Debug mode Bit[0]: smia_cal_en 0: Use period to calculate 1: Use SMIA bit rate to calculate
0x4837	PCLK_PERIOD	0x08	RW	Period of pclk2x, pclk_div = 1, and 1-bit decimal
0x4838	MIPI_LP_GPIO0	0x00	RW	Bit[7]: lp_sel0 0: Auto generate mipi_lp_dir0_o 1: Use lp_dir_man0 to be mipi_lp_dir0_o Bit[6]: lp_dir_man0 0: Input 1: Output Bit[5]: lp_p0_o Bit[4]: lp_n0_o Bit[3]: lp_sel1 0: Auto generate mipi_lp_dir1_o 1: Use lp_dir_man1 to be mipi_lp_dir1_o Bit[2]: lp_dir_man1 0: Input 1: Output Bit[1]: lp_p1_o Bit[0]: lp_n1_o

table 6-19 MIPI top registers (sheet 8 of 9)

address	register name	default value	R/W	description
0x4839	MIPI_LP_GPIO1	0x00	RW	Bit[7]: lp_sel2 0: Auto generate mipi_lp_dir2_o 1: Use lp_dir_man2 to be mipi_lp_dir2_o Bit[6]: lp_dir_man2 0: Input 1: Output Bit[5]: lp_p2_o Bit[4]: lp_n2_o Bit[3]: lp_sel3 0: Auto generate mipi_lp_dir3_o 1: Use lp_dir_man3 to be mipi_lp_dir3_o Bit[2]: lp_dir_man3 0: Input 1: Output Bit[1]: lp_p3_o Bit[0]: lp_n3_o
0x483C	MIPI_CTRL3C	0x42	RW	Bit[7:4]: Debug mode Bit[3:0]: t_clk_pre Unit: pclk2x cycle
0x483D	MIPI_LP_GPIO4	0x00	RW	Bit[7]: lp_ck_sel0 0: Auto generate mipi_ck_lp_dir0_o 1: Use lp_ck_dir_man0 to be mipi_ck_lp_dir0_o Bit[6]: lp_ck_dir_man0 0: Input 1: Output Bit[5]: lp_ck_p0_o Bit[4]: lp_ck_n0_o Bit[3]: lp_ck_sel1 0: Auto generate mipi_ck_lp_dir1_o 1: Use lp_ck_dir_man1 to be mipi_ck_lp_dir1_o Bit[2]: lp_ck_dir_man1 0: Input 1: Output Bit[1]: lp_ck_p1_o Bit[0]: lp_ck_n1_o

table 6-19 MIPI top registers (sheet 9 of 9)

address	register name	default value	R/W	description
0x484A	SEL_MIPI_CTRL4A	0x07	RW	Bit[7:6]: Debug mode Bit[5]: slp_lp_pon_man_o Set for power up Bit[3]: slp_lp_pon_da Bit[3]: slp_lp_pon_ck Bit[2]: mipi_slp_man_st MIPI bus status manual control enable in sleep mode Bit[1]: clk_lane_state Bit[0]: data_lane_state
0x484B	SMIA_OPTION	0x07	RW	Bit[7:3]: Debug mode Bit[2]: line_st_sel_o 0: Line start after HREF 1: Line start after fifo_st Bit[1]: clk_start_sel_o 0: Clock start after SOF 1: Clock start after reset Bit[0]: sof_sel_o 0: Frame start after HREF starts 1: Frame start after SOF
0x484C	SEL_MIPI_CTRL4C	0x02	RW	Bit[7]: Debug mode Bit[6]: SMIA fcnt_i select Bit[5]: prbs_enable Bit[4]: MIPI high speed only test mode enable Bit[3]: Set frame count to inactive mode (keep 0) Bit[2:0]: Debug mode
0x484D	TEST_PATTEN_DATA	0xB6	RW	Data Lane Test Pattern Register
0x484E	FE_DLY	0x10	RW	Last Packet to Frame End Delay/2
0x484F	TEST_PATTEN_CK_DATA	0x55	RW	clk_test_patten_reg

6.20 temperature monitor [04D00x - 0x4D23]

table 6-20 temperature monitor registers

address	register name	default value	R/W	description
0x4D00	TPM_CTRL_00	0x05	RW	Bit[7:0]: Tpm slope[15:8]
0x4D01	TPM_CTRL_01	0x19	RW	Bit[7:0]: Tpm slope[7:0]
0x4D02	TPM_CTRL_02	0xFD	RW	Bit[7:0]: Tpm offset[31:24]
0x4D03	TPM_CTRL_03	0xD1	RW	Bit[7:0]: Tpm offset[23:16]
0x4D04	TPM_CTRL_04	0xFF	RW	Bit[7:0]: Tpm offset[15:8]
0x4D05	TPM_CTRL_05	0xFF	RW	Bit[7:0]: Tpm offset[7:0]
0x4D06~ 0x4D23	TPM_CTRL	–	–	Debug Registers

6.21 AEC PK [0x3500 - 0x352B]

table 6-21 AEC/AGC registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x3500	AEC LONG EXPO	0x00	RW	Long Exposure Bit[7:4]: Not used Bit[3:0]: Long exposure[19:16]
0x3501	AEC LONG EXPO	0x02	RW	Long Exposure Bit[7:0]: Long exposure[15:8]
0x3502	AEC LONG EXPO	0x00	RW	Long Exposure Bit[7:0]: Long exposure[7:0] Low 4 bits are fraction bits and should be all 0's

table 6-21 AEC/AGC registers (sheet 2 of 5)

address	register name	default value	R/W	description
0x3503	AEC MANUAL	0x00	RW	AEC Manual Mode Control Bit[7]: Debug mode Bit[6]: Digital fraction gain delay option Always the same with 0x3503[4] 0: Delay 1 frame 1: No delay 1 frame Bit[5]: Gain change delay option Always the same with 0x3503[4] 0: Delay 1 frame 1: No delay 1 frame Bit[4]: Gain delay option 0: Delay 1 frame 1: No delay 1 frame Bit[3]: Not used Bit[2]: Gain man as sensor gain 0: Gain input ({0x3508,0x3509}) as real gain format 1: Gain input ({0x3508,0x3509}) as sensor gain format Bit[1]: Exposure delay option Always 0 to make sure OTP_DPC catches the correct exposure value 0: Delay 1 frame 1: No delay 1 frame Bit[0]: Exposure change delay option Always 0 0: Delay 1 frame 1: No delay 1 frame
0x3504~ 0x3506	DEBUG MODE	–	–	Debug Mode
0x3507	AEC LONG GAIN	0x00	RW	Long gain Bit[7:2]: Debug mode Bit[1:0]: Long gain[17:16]
0x3508	AEC LONG GAIN	0x00	RW	Long gain Bit[7:0]: Long gain[15:8]
0x3509	AEC LONG GAIN	0x80	RW	Long gain Bit[7:0]: Long gain[7:0] Low 7 bits are fraction bits
0x350A	AEC MIDDLE EXPO	0x00	RW	Middle Exposure Bit[7:4]: Not used Bit[3:0]: Middle exposure[19:16]

table 6-21 AEC/AGC registers (sheet 3 of 5)

address	register name	default value	R/W	description
0x350B	AEC MIDDLE EXPO	0x01	RW	Middle Exposure Bit[7:0]: Middle exposure[15:8]
0x350C	AEC MIDDLE EXPO	0x00	RW	Middle Exposure Bit[7:0]: Middle exposure[7:0] Low 4 bits are fraction bits and should be all 0's
0x350D	AEC MIDDLE GAIN	0x00	RW	Middle gain Bit[7:2]: Not used Bit[1:0]: Middle gain[17:16]
0x350E	AEC MIDDLE GAIN	0x00	RW	Middle Gain Bit[7:0]: Middle gain[15:8]
0x350F	AEC MIDDLE GAIN	0x80	RW	Middle Gain Bit[7:0]: Middle gain[7:0] Low 7 bits are fraction bits
0x3510	AEC SHORT EXPO	0x00	RW	Short Exposure Bit[7:4]: Not used Bit[3:0]: Short exposure[19:16]
0x3511	AEC SHORT EXPO	0x00	RW	Short Exposure Bit[7:0]: Short exposure[15:8]
0x3512	AEC SHORT EXPO	0x80	RW	Short Exposure Bit[7:0]: Short exposure[7:0] Low 4 bits are fraction bits and should be all 0's
0x3513	AEC SHORT GAIN	0x00	RW	Short Gain Bit[7:2]: Not used Bit[1:0]: Short gain[17:16]
0x3514	AEC SHORT GAIN	0x00	RW	Short Gain Bit[7:0]: Short gain[15:8]
0x3515	AEC SHORT GAIN	0x80	RW	Short Gain Bit[7:0]: Short gain[7:0] Low 7 bits are fraction bits
0x3516	AEC 4 EXPO	0x00	RW	Fourth Exposure Bit[7:4]: Not used Bit[3:0]: Fourth exposure[19:16]
0x3517	AEC 4 EXPO	0x02	RW	Fourth Exposure Bit[7:0]: Fourth exposure[15:8]
0x3518	AEC 4 EXPO	0x00	RW	Fourth Exposure Bit[7:0]: Fourth exposure[7:0] Low 4 bits are fraction bits and should be all 0's

table 6-21 AEC/AGC registers (sheet 4 of 5)

address	register name	default value	R/W	description
0x3519	AEC 4 GAIN	0x00	RW	Fourth Gain Bit[7:2]: Not used Bit[1:0]: Fourth gain[17:16]
0x351A	AEC 4 GAIN	0x00	RW	Fourth Gain Bit[7:0]: Fourth gain[15:8]
0x351B	AEC 4 GAIN	0x80	RW	Fourth Gain Bit[7:0]: Fourth gain[7:0] Low 7 bits are fraction bits
0x351C	AEC 5 EXPO	0x00	RW	Fifth Exposure Bit[7:4]: Not used Bit[3:0]: Fifth exposure[19:16]
0x351D	AEC 5 EXPO	0x02	RW	Fifth Exposure Bit[7:0]: Fifth exposure[15:8]
0x351E	AEC 5 EXPO	0x00	RW	Fifth Exposure Bit[7:0]: Fifth exposure[7:0] Low 4 bits are fraction bits and should be all 0's
0x351F	AEC 5 GAIN	0x00	RW	Fifth Gain Bit[7:2]: Not used Bit[1:0]: Fifth gain[17:16]
0x3520	AEC 5 GAIN	0x00	RW	Fifth Gain Bit[7:0]: Fifth gain[15:8]
0x3521	AEC 5 GAIN	0x80	RW	Fifth Gain Bit[7:0]: Fifth gain[7:0] Low 7 bits are fraction bits
0x3522	DIG GAIN FRAC MIDDLE	0x04	RW	Bit[7:1]: Not used Bit[6:0]: Middle digital fraction gain[14:8] Low 11 bits are fraction bits Valid when 0x3503[2]=1'b1
0x3523	DIG GAIN FRAC MIDDLE	0x00	RW	Bit[7:0]: Middle digital fraction gain[7:0] Valid when 0x3503[2]=1'b1
0x3524	DIG GAIN FRAC SHORT	0x04	RW	Bit[7:1]: Not used Bit[6:0]: Short digital fraction gain[14:8] Low 11 bits are fraction bits Valid when 0x3503[2]=1'b1
0x3525	DIG GAIN FRAC SHORT	0x00	RW	Bit[7:0]: Short digital fraction gain[7:0] Valid when 0x3503[2]=1'b1

table 6-21 AEC/AGC registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x3526	DIG GAIN FRAC 4	0x04	RW	Bit[7:1]: Not used Bit[6:0]: Fourth digital fraction gain[14:8] Low 11 bits are fraction bits Valid when 0x3503[2]=1'b1
0x3527	DIG GAIN FRAC 4	0x00	RW	Bit[7:0]: Fourth digital fraction gain[7:0] Valid when 0x3503[2]=1'b1
0x3528	DIG GAIN FRAC 5	0x04	RW	Bit[7:1]: Not used Bit[6:0]: Fifth digital fraction gain[14:8] Low 11 bits are fraction bits Valid when 0x3503[2]=1'b1
0x3529	DIG GAIN FRAC 5	0x00	RW	Bit[7:0]: Fifth digital fraction gain[7:0] Valid when 0x3503[2]=1'b1
0x352A	DIG GAIN FRAC LONG	0x04	RW	Bit[7:1]: Not used Bit[6:0]: Long digital fraction gain[14:8] Low 11 bits are fraction bits Valid when 0x3503[2]=1'b1
0x352B	DIG GAIN FRAC LONG	0x00	RW	Bit[7:0]: Long digital fraction gain[7:0] Valid when 0x3503[2]=1'b1

6.22 BLC [0x4000 - 0x4033]

table 6-22 BLC registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x4000	BLC CTRL00	0xF1	RW	Bit[7]: Outrange_trig_en Offset out of range trigger function enable signal 0: Disable 1: Enable Bit[6]: format_chg_en Format change triggers function enable signal 0: Disable 1: Enable Bit[5]: gain_chg_en Gain change triggers function enable signal 0: Disable 1: Enable Bit[4]: exp_chg_en Exposure changes trigger function enable signal 0: Disable 1: Enable Bit[3]: manual_trig Manually trigger signal Rising edge triggers BLC Bit[2]: freeze_en BLC freeze function enable signal When set, BLC will freeze Offsets will maintain the pre-frame values Bit[1]: always_do BLC always trigger signal When set, BLC triggers every frame unless the freeze_en is enabled Bit[0]: Debug mode
0x4001~ 0x4002	DEBUG MODE	–	–	Debug Mode
0x4003	BLC CTRL03	0x14	RW	Bit[7:0]: Black line_num Black line number used to calculate the offsets
0x4004	BLC CTRL04	0x00	RW	Bit[7:0]: Target[15:8] BLC target
0x4005	BLC CTRL05	0x40	RW	Bit[7:0]: Target[7:0] BLC target in 12-bit domain

table 6-22 BLC registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x4006	BLC CTRL06	0x1F	RW	Bit[7:0]: format_chg_fn Frame number for format change trigger
0x4007	BLC CTRL07	0x1F	RW	Bit[7:0]: reset_trig_fn Frame number for reset trigger
0x4008	BLC CTRL08	0x01	RW	Bit[7:0]: manual_trig_fn Frame number for manual trigger
0x4009~ 0x400B	DEBUG MODE	–	–	Debug Mode
0x400C	BLC CTRL0C	0x00	RW	Bit[7:0]: offset_trig_thresh[13:6] (works only when register 0x4000[7] = 1) Threshold for offset trigger When line_current_offset - blc_line_offset| > offset_trig_thresh, BLC update will be set.
0x400D	BLC CTRL0D	0x20	RW	Bit[7:2]: offset_trig_thresh[5:0] Bit[1:0]: Debug mode
0x400E	BLC CTRL0E	0x00	RW	Bit[7:0]: bypass_offset[15:8] Offset for BLC bypass
0x400F	BLC CTRL0F	0x00	RW	Bit[7:0]: bypass_offset[7:0] Offset for BLC bypass
0x4010	DEBUG MODE	–	–	Debug Mode
0x4011	BLC CTRL11	0x00	RW	Bit[7:6]: Debug mode Bit[5]: offset_man_same When it is enabled, the manual offsets will be same. They are all defined by manual_offset00({0x4012,0x4013}) Bit[4]: offset_man_en When it is enabled, the offsets will be defined manually with registers manual_offset00 ~ manual_offset11 (0x4012~0x4019) Bit[3:1]: Debug mode Bit[0]: Black_line_out_en 0: Black line pixels will not be output 1: Black line pixels will be output
0x4012	BLC CTRL12	0x00	RW	Bit[7:0]: manual_offset00[15:8] Manual offset for normal even-line and even-column pixels
0x4013	BLC CTRL13	0x00	RW	Bit[7:0]: manual_offset00[7:0]

table 6-22 BLC registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x4014	BLC CTRL14	0x00	RW	Bit[7:0]: manual_offset01[15:8] Manual offset for normal even-line and odd-column pixels
0x4015	BLC CTRL15	0x00	RW	Bit[7:0]: manual_offset01[7:0]
0x4016	BLC CTRL16	0x00	RW	Bit[7:0]: manual_offset10[15:8] Manual offset for normal odd-line and even-column pixels
0x4017	BLC CTRL17	0x00	RW	Bit[7:0]: manual_offset10[7:0]
0x4018	BLC CTRL18	0x00	RW	Bit[7:0]: manual_offset11[15:8] Manual offset for normal odd-line and odd-column pixels
0x4019	BLC CTRL19	0x00	RW	Bit[7:0]: manual_offset11[7:0]
0x401A~ 0x401F	DEBUG MODE	–	–	Debug Mode
0x4020	ANCHOR LEFT START	0x02	RW	Bit[7:4]: Debug mode Bit[3:0]: Anchor left start[11:8]
0x4021	ANCHOR LEFT START	0x40	RW	Bit[7:0]: Anchor left start[7:0]
0x4022	ANCHOR LEFT END	0x03	RW	Bit[7:4]: Debug mode Bit[3:0]: Anchor left end[11:8]
0x4023	ANCHOR LEFT END	0x3F	RW	Bit[7:0]: Anchor left end[7:0]
0x4024	ANCHOR RIGHT START	0x07	RW	Bit[7:4]: Debug mode Bit[3:0]: Anchor right start[11:8]
0x4025	ANCHOR RIGHT START	0xC0	RW	Bit[7:0]: Anchor right start[7:0]
0x4026	ANCHOR RIGHT END	0x08	RW	Bit[7:4]: Debug mode Bit[3:0]: Anchor right end[11:8]
0x4027	ANCHOR RIGHT END	0xBF	RW	Bit[7:0]: Anchor right end[7:0]
0x4028	TOP ZLINE ST	0x00	RW	Top Zline Start
0x4029	TOP ZLINE NUM	0x02	RW	Top Zline Number
0x402A	TOP BLKLINE ST	0x06	RW	Top Blkline Start
0x402B	TOP BLKLINE NUM	0x04	RW	Top Blkline Number
0x402C	BOT ZLINE ST	0x02	RW	Bot Zline Start

table 6-22 BLC registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x402D	BOT ZLINE NUM	0x02	RW	Bot Zline Number
0x402E	BOT BLKLINE ST	0x0E	RW	Bot Blkline Start
0x402F	BOT BLKLINE NUM	0x04	RW	Bot Blkline Number
0x4030	DCBLC K1	0x01	RW	Bit[7:4]: Debug mode Bit[3:0]: DCBLC k1[11:8]
0x4031	DCBLC K1	0x00	RW	Bit[7:0]: DCBLC k1[7:0]
0x4032	DCBLC K2	0x01	RW	Bit[7:4]: Debug mode Bit[3:0]: DCBLC k2[11:8]
0x4033	DCBLC K2	0x00	RW	Bit[7:0]: DCBLC k2[7:0]

6.23 ISP top [0x5000 - 0x5033]

table 6-23 ISP top registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5000	ISP CTRL0	0xF3	RW	Bit[7]: Digital gain enable 0: Disable 1: Enable Bit[6]: Bin enable 0: Disable 1: Enable Bit[5]: OTP enable 0: Disable 1: Enable Bit[4]: WB gain enable 0: Disable 1: Enable Bit[3:2]: Debug mode Bit[1]: Average enable Bit[0]: ISP enable

table 6-23 ISP top registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5001	ISP CTRL1	0x11	RW	Bit[7]: New_stg_hdr_en Bit[6]: New_stg_EOF_en Bit[5]: Debug mode Bit[4]: ISP EOF select Bit[3]: ISP SOF select Bit[2]: Debug mode Bit[0]: BLC 0: Disable 1: Enable
0x5002	ISP CTRL2	0x85	RW	Bit[7]: ISP RAW enable 0: Disable 1: Enable Bit[6:4]: Debug mode Bit[3]: WB bias man enable 0: Disable 1: Enable Bit[2]: WB bias on Bit[1]: Digital gain bias man enable Bit[0]: Digital gain bias on
0x5003	ISP CTRL03	0x10	RW	Bias Manual
0x5004~ 0x500B	DEBUG MODE	–	–	Debug Mode
0x500C	ISP CTRL0C	0x04	RW	Bit[7:4]: Debug mode Bit[3:0]: Long WB R gain[11:8]
0x500D	ISP CTRL0D	0x00	RW	Bit[7:0]: Long WB R gain[7:0]
0x500E	ISP CTRL0E	0x04	RW	Bit[7:4]: Debug mode Bit[3:0]: Long WB G gain[11:8]
0x500F	ISP CTRL0F	0x00	RW	Bit[7:0]: Long WB G gain[7:0]
0x5010	ISP CTRL10	0x04	RW	Bit[7:4]: Debug mode Bit[3:0]: Long WB B gain[11:8]
0x5011	ISP CTRL11	0x00	RW	Bit[7:0]: Long WB B gain[7:0]
0x5012	ISP CTRL 12	0x04	RW	Bit[7:4]: Debug mode Bit[3:0]: Middle WB R gain[11:8]
0x5013	ISP CTRL 13	0x00	RW	Bit[7:0]: Middle WB R gain[7:0]
0x5014	ISP CTRL 14	0x04	RW	Bit[7:4]: Debug mode Bit[3:0]: Middle WB G gain[11:8]
0x5015	ISP CTRL 15	0x00	RW	Bit[7:0]: Middle WB G gain[7:0]
0x5016	ISP CTRL 16	0x04	RW	Bit[7:4]: Debug mode Bit[3:0]: Middle WB B gain[11:8]
0x5017	ISP CTRL 17	0x00	RW	Bit[7:0]: Middle WB B gain[7:0]

table 6-23 ISP top registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x5018	ISP CTRL 18	0x04	RW	Bit[7:4]: Debug mode Bit[3:0]: Short WB R gain[11:8]
0x5019	ISP CTRL 19	0x00	RW	Bit[7:0]: Short WB R gain[7:0]
0x501A	ISP CTRL 1A	0x04	RW	Bit[7:4]: Debug mode Bit[3:0]: Short WB G gain[11:8]
0x501B	ISP CTRL 1B	0x00	RW	Bit[7:0]: Short WB G gain[7:0]
0x501C	ISP CTRL 1C	0x04	RW	Bit[7:4]: Debug mode Bit[3:0]: Short WB B gain[11:8]
0x501D	ISP CTRL 1D	0x00	RW	Bit[7:0]: Short WB B gain[7:0]
0x501E~ 0x5030	DEBUG MODE	–	–	Debug Mode
0x5031	ISP CTRL 31	0x20	RW	Bit[5]: Bin mode select Bit[4]: Bypass SOF Bit[3]: Long/short reverse WB gain Bit[2]: Long/short reverse digital gain Bit[1:0]: Debug mode
0x5032~ 0x5033	DEBUG MODE	–	–	Debug Mode

6.24 pre_ISP control [0x5040 - 0x506C]

table 6-24 pre_ISP control registers

address	register name	default value	R/W	description
0x5040	PRE ISP TEST CTRL	0x00	RW	Bit[7]: test_enable Bit[6]: Rolling enable Rolling bar in test mode Bit[5]: Transparent image + normal image enable Bit[4]: square black white enable Bit[3:2]: color_bar style 00: Horizontal bar 01: Vertical bar 10: Horizontal fading bar 11: Vertical fading bar Bit[1:0]: Test selection 00: Color bar 01: Random data 10: Square black white 11: Black
0x5041	PRE ISP WIN	0x41	RW	Bit[7]: Not used Bit[6]: Window cut enable Bit[5]: ISP test, low bits to 0 Bit[4]: Random, random data reset Bit[3:0]: Random seed
0x5042~ 0x5047	DEBUG MODE	–	–	Debug Mode
0x5048	PRE ISP X OFF	0x00	RW	Bit[7:0]: X manual offset[15:8]
0x5049	PRE ISP X OFF	0x00	RW	Bit[7:0]: X manual offset[7:0]
0x504A	PRE ISP Y OFF	0x00	RW	Bit[7:0]: Y manual offset15:8]
0x504B	PRE ISP Y OFF	0x00	RW	Bit[7:0]: Y manual offset[7:0]
0x504C~ 0x506C	DEBUG MODE	–	–	Debug Mode

6.25 binning control [0x5301 - 0x530F]

table 6-25 binning control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5301	BIN CTRL 01	0x00	RW	Bit[7:5]: Debug mode Bit[4]: Enable manual input filter coefficients Bit[3:0]: Debug mode
0x5302	BIN CTRL 02	0x23	RW	Bit[7:6]: Debug mode Bit[5:4]: First row number of output BG rows BIt[3]: Debug mode Bit[2:0]: First row number of output GR rows
0x5303	BIN CTRL 03	0x22	RW	Bit[7]: Debug mode Bit[6:4]: Step between two output rows BIt[3]: Debug mode Bit[2:0]: Shift number of row calculation
0x5304	BIN CTRL 04	0x40	RW	Bit[7:4]: B row filter coefficient 0 BIt[3]: Debug mode Bit[2:0]: B row filter coefficient 1
0x5305	BIN CTRL 05	0x31	RW	Bit[7:4]: R row filter coefficient 0 BIt[3]: Debug mode Bit[2:0]: R row filter coefficient 1
0x5306	BIN CTRL 06	0x23	RW	Bit[7:6]: Debug mode Bit[5:4]: First column number of output B columns BIt[3]: Debug mode Bit[2:0]: First column number of output R columns
0x5307	BIN CTRL 07	0x54	RW	Bit[7]: Enable column filter with two coefficients Bit[6:4]: Shift number of column calculation Bit[3:0]: Step between two output columns
0x5308	BIN CTRL 08	0x03	RW	Bit[7:3]: Debug mode Bit[2:0]: B column filter coefficient 0[2:0]
0x5309	BIN CTRL 09	0x19	RW	Bit[7:0]: B column filter coefficient 1[7:0]
0x530A	BIN CTRL 0A	0x09	RW	Bit[7]: Debug mode Bit[6:0]: B column filter coefficient 2[6:0]
0x530B	BIN CTRL 0B	0x01	RW	Bit[7:4]: Debug mode Bit[3:0]: B column filter coefficient 3[3:0]
0x530C	BIN CTRL 0C	0x01	RW	Bit[7:3]: Debug mode Bit[2:0]: R column filter coefficient 0[2:0]
0x530D	BIN CTRL 0D	0x09	RW	Bit[7:0]: R column filter coefficient 1[7:0]

table 6-25 binning control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x530E	BIN CTRL 0E	0x19	RW	Bit[7]: Debug mode Bit[6:0]: R column filter coefficient 2[6:0]
0x530F	BIN CTRL 0F	0x03	RW	Bit[7:4]: Debug mode Bit[3:0]: R column filter coefficient 3[3:0]

6.26 OTP_DPC control [0x5000 - 0x552A]

table 6-26 OTP_DPC control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5000	ISP CTRL0	0xF3	RW	Bit[7:6]: Debug mode Bit[5]: OTP enable 0: Disable 1: Enable
0x5500	OTP DPC START	0x00	RW	Bit[7:1]: Debug mode Bit[0]: OTP start address[8]
0x5501	OTP DPC START	0x00	RW	Bit[7:0]: OTP start address[7:0]
0x5502	OTP DPC END	0x01	RW	Bit[7:1]: Debug mode Bit[0]: OTP end address[8]
0x5503	OTP DPC END	0xFF	RW	Bit[7:0]: OTP end address[7:0]
0x5505	OTP DPC CTRL 05	0x6C	RW	Bit[7]: Debug mode Bit[6:5]: Recover method select 00: Left 1 neighbor pixel on same channel 01: Minimum of left 2 neighbor pixels 10: Maximum of left and right 1 neighbor pixels 11: Maximum between the minimum of left 2 neighbor pixels and the minimum of right 2 neighbor pixels Bit[4]: Recover with fixed pattern Bit[3]: Fixed pattern mode 0: 0x00 1: 0xFF Bit[1]: Sensor exposure constrain enable Bit[0]: Sensor gain constrain enable

table 6-26 OTP_DPC control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5506	OTP DPC EXPO CONSTRAINT L	0x00	RW	Bit[7:0]: OTP exposure constrain long[15:8]
0x5507	OTP DPC EXPO CONSTRAINT L	0x00	RW	Bit[7:0]: OTP exposure constrain long[7:0]
0x5508	OTP DPC GAIN CONSTRAINT L	0x07	RW	OTP Gain Constrain Long
0x5509	OTP DPC THRE L	0x08	RW	OTP Threshold Long
0x5524	OTP EXPO CONSTRAIN M	0x00	RW	Bit[7:0]: OTP exposure constrain middle[15:8]
0x5525	OTP EXPO CONSTRAIN M	0x00	RW	Bit[7:0]: OTP exposure constrain middle[7:0]
0x5526	OTP GAIN CONSTRAIN M	0x07	RW	OTP Gain Constrain Middle
0x5527	OTP THRE MS	0x88	RW	Bit[7:4]: OTP threshold middle Bit[3:0]: OTP threshold short
0x5528	OTP EXPO CONSTRAIN S	0x00	RW	Bit[7:0]: OTP exposure constrain short[15:8]
0x5529	OTP EXPO CONSTRAIN S	0x00	RW	Bit[7:0]: OTP exposure constrain short[7:0]
0x552A	OTP GAIN CONSTRAIN S	0x07	RW	OTP Gain Constrain Short

6.27 windowing (WIN) control [0x5980 - 0x598C]

table 6-27 WIN control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5980	WIN XSTART_OFF	0x00	RW	Bit[7:5]: Debug mode Bit[4:0]: X start offset[12:8]
0x5981	WIN XSTART_OFF	0x00	RW	Bit[7:0]: X start offset[7:0]
0x5982	WIN YSTART_OFF	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: Y start offset[11:8]
0x5983	WIN YSTART_OFF	0x00	RW	Bit[7:0]: Y start offset[7:0]
0x5984	WIN WIDTH	0x0A	RW	Bit[7:5]: Debug mode Bit[4:0]: Window width[12:8]

table 6-27 WIN control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5985	WIN WIDTH	0x80	RW	Bit[7:0]: Window width[7:0]
0x5986	WIN HEIGHT	0x05	RW	Bit[7:4]: Debug mode Bit[3:0]: Window height[11:8]
0x5987	WIN HEIGHT	0xF0	RW	Bit[7:0]: Window height[7:0]
0x5988	WIN MAN	0x00	RW	Bit[7:1]: Debug mode Bit[0]: Window size manual 0: Disable 1: Enable
0x5989~ 0x598C	DEBUG MODE	–	–	Debug Mode

6.28 average (AVG) control [0x5680 - 0x5693]

table 6-28 AVG control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5680	AVG X START	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: X start offset[11:8] Valid when 0x5690[0]=1
0x5681	AVG X START	0x00	RW	Bit[7:0]: X start offset[7:0] Valid when 0x5690[0]=1
0x5682	AVG Y START	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: Y start offset[11:8] Valid when 0x5690[0]=1
0x5683	AVG Y START	0x00	RW	Bit[7:0]: Y start offset[7:0] Valid when 0x5690[0]=1
0x5684	AVG WIN WIDTH	0x0A	RW	Bit[7:4]: Debug mode Bit[3:0]: Window width[11:8] Valid when 0x5690[0]=1
0x5685	AVG WIN WIDTH	0x80	RW	Bit[7:0]: Window width[7:0] Valid when 0x5690[0]=1
0x5686	AVG WIN HEIGHT	0x05	RW	Bit[7:4]: Debug mode Bit[3:0]: Window height[11:8] Valid when 0x5690[0]=1
0x5687	AVG WIN HEIGHT	0xF0	RW	Bit[7:0]: Window height[7:0] Valid when 0x5690[0]=1

table 6-28 AVG control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5688	AVG WT 0	0x11	RW	Bit[7:4]: Weight of zone 01 Bit[3:0]: Weight of zone 00
0x5689	AVG WT 1	0x11	RW	Bit[7:4]: Weight of zone 03 Bit[3:0]: Weight of zone 02
0x568A	AVG WT 2	0x11	RW	Bit[7:4]: Weight of zone 11 Bit[3:0]: Weight of zone 10
0x568B	AVG WT 3	0x11	RW	Bit[7:4]: Weight of zone 13 Bit[3:0]: Weight of zone 12
0x568C	AVG WT 4	0x11	RW	Bit[7:4]: Weight of zone 21 Bit[3:0]: Weight of zone 20
0x568D	AVG WT 5	0x11	RW	Bit[7:4]: Weight of zone 23 Bit[3:0]: Weight of zone 22
0x568E	AVG WT 6	0x11	RW	Bit[7:4]: Weight of zone 31 Bit[3:0]: Weight of zone 30
0x568F	AVG WT 7	0x11	RW	Bit[7:4]: Weight of zone 33 Bit[3:0]: Weight of zone 32
0x5690	AVG MANUAL CTRL	0x02	RW	Bit[7:2]: Debug mode Bit[1]: Average option 0: Sum = (4×B+9×G×2+10×R)/8 1: Sum = B+G×2+R Bit[0]: Average size manual 0: Disable 1: Enable
0x5691	AVG WT SUM READOUT	–	R	Bit[7:0]: Average weight sum
0x5692	AVG SCCB DONE	–	R	Average Calculated Indicating Signal for SCCB Read
0x5693	AVG READOUT	–	R	Bit[7:0]: High 8-bit of average output

7 operating specifications

7.1 absolute maximum ratings

table 7-1 absolute maximum ratings

parameter		absolute maximum rating[a]
ambient storage temperature		-40°C to +125°C
supply voltage (with respect to ground)	V_{DD-A}	4.5V
	V_{DD-D}	3V
	V_{DD-IO}	4.5V
electro-static discharge (ESD)	human body model	2000V
	machine model	200V
all input/output voltages (with respect to ground)		-0.3V to V_{DD-IO} + 1V
I/O current on any input or output pin		± 200 mA
peak solder temperature (10 second dwell time)		245°C

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

7.2 functional temperature

table 7-2 functional temperature

parameter	range
operating temperature (for applications up to 90fps)[a]	-30°C to +85°C junction temperature
stable image temperature[b]	0°C to +60°C junction temperature

a. sensor functions but image quality may be noticeably different at temperatures outside of stable image range

b. image quality remains stable throughout this temperature range

7.3 DC characteristics

table 7-3 DC characteristics (-30°C < T_J < 85°C)

symbol	parameter	min	typ	max[a]	unit
supply					
V_{DD-A}	supply voltage (analog)	2.6	2.8	3.0	V
V_{DD-IO}	supply voltage (digital I/O)	1.7	1.8	3.0	V
V_{DD-D}	supply voltage (digital core for 4-lane MIPI up to 1000 Mbps/lane)	1.1	1.2	1.3	V
I_{DD-A}	active (operating) current[b]		40	45	mA
I_{DD-IO}			3	7	mA
I_{DD-D}			120	150	mA
I_{DD-A}	standby (SCCB) current[c]		10	20	µA
I_{DD-IO}			50	70	µA
I_{DD-D}			1	20	mA
I_{DD-A}	standby (PWDN) current[c]		10	20	µA
I_{DD-IO}			20	30	µA
I_{DD-D}			0.2	20	mA
I_{DD-A}	standby (XSHUTDOWN) current[c]		0.3	2	µA
I_{DD-IO}			0.3	2	µA
I_{DD-D}			2	8	µA
digital inputs (typical conditions: AVDD = 2.8V, DVDD = 1.2V, DOVDD = 1.8V)					
V_{IL}	input voltage LOW			V_{DD-IO} x 0.3	V
V_{IH}	input voltage HIGH	V_{DD-IO} x 0.7			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	V_{DD-IO} x 0.9			V
V_{OL}	output voltage LOW			V_{DD-IO} x 0.1	V

table 7-3 DC characteristics (-30°C < T_J < 85°C)

symbol	parameter	min	typ	max[a]	unit
serial interface inputs					
V_{IL}[d]	SIOC and SIOD	-0.5	0	0.54	V
V_{IH}	SIOC and SIOD	1.28	1.8	3.0	V

a. maximum active current is measured under typical supply voltage

b. DVDD is provided by external regulator for lower power consumption. DVDD and EVDD are tied together. DOVDD = 1.8V

c. standby current is measured at room temperature with external clock off

d. based on DOVDD = 1.8V

7.4 timing characteristics

table 7-4 timing characteristics

symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{OSC}	frequency (EXTCLK)[a]	6	24	64	MHz
t_r, t_f	clock input rise/fall time			(see footnote [b])	ns
	clock input duty cycle	45	50	55	%

a. for input clock range 6~64MHz, the OV4689 can tolerate input clock period jitter up to 600ps peak-to-peak

b. for clock input rise/fall time, the max is 27% whole clock period

8 mechanical specifications

8.1 physical specifications

figure 8-1 package specifications

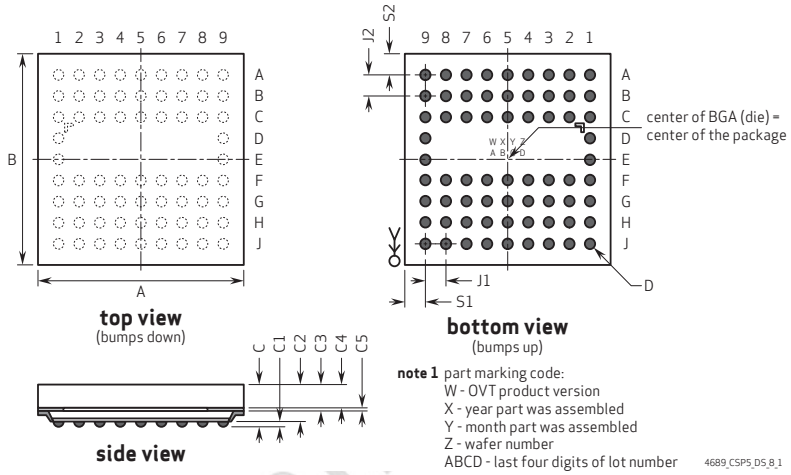


table 8-1 package dimensions

parameter	symbol	min	typ	max	unit
package body dimension x	A	6605	6630	6655	µm
package body dimension y	B	5805	5830	5855	µm
package height	C	680	740	800	µm
ball height	C1	100	130	160	µm
package body thickness	C2	575	610	645	µm
thickness from top glass surface to wafer	C3	425	445	465	µm
glass thickness	C4	385	400	415	µm
air gap between sensor and glass	C5	41	45	49	µm
ball diameter	D	220	250	280	µm
total ball count	N		67 (7 NC)		
pins pitch x-axis	J1		710		µm
pins pitch y-axis	J2		580		µm
edge-to-pin center distance along x	S1	465	475	505	µm
edge-to-pin center distance along y	S2	585	595	625	µm

8.2 IR reflow specifications

note
The OV4689 uses a lead-free package.

figure 8-2 IR reflow ramp rate requirements

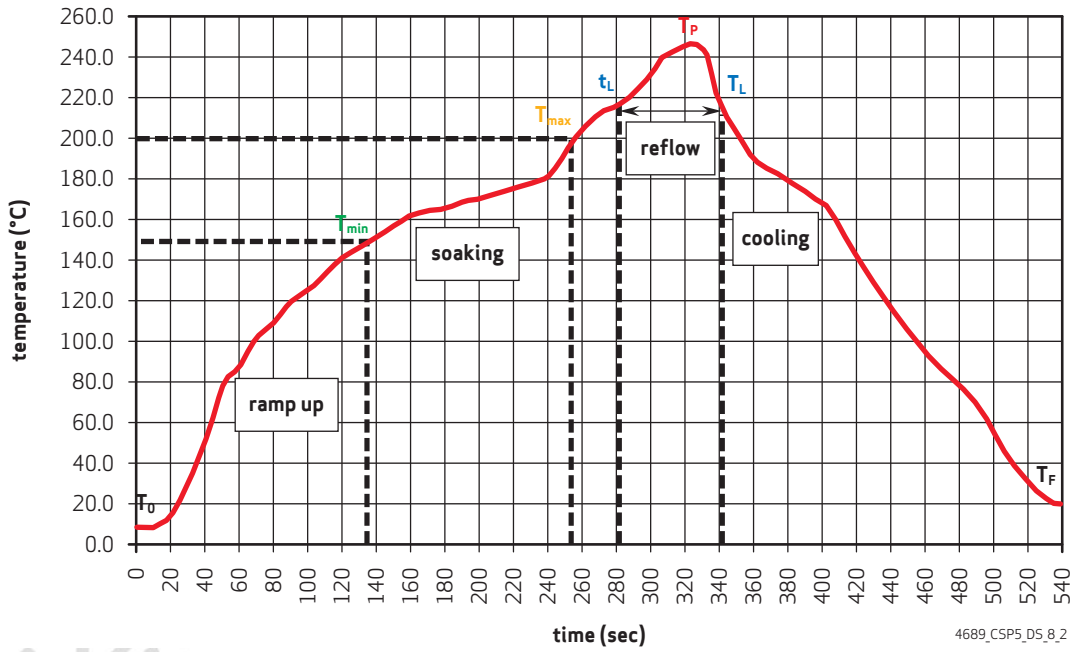


table 8-2 reflow conditions[ab]

zone	description	exposure
ramp up A (T_0 to T_{min})	heating from room temperature to 150°C	temperature slope ≤ 3°C per second
soaking	heating from 150°C to 200°C	90 ~ 150 seconds
ramp up B (t_L to T_p)	heating from 217°C to 245°C	temperature slope ≤ 3°C per second
peak temperature	maximum temperature in SMT	245°C +0/-5°C (duration max 30sec)
reflow (t_L to T_L)	temperature higher than 217°C	30 ~ 120 seconds
ramp down A (T_p to T_L)	cooling down from 245°C to 217°C	temperature slope ≤ 3°C per second
ramp down B (T_L to T_f)	cooling down from 217°C to room temperature	temperature slope ≤ 2°C per second
T_0 to T_p	room temperature to peak temperature	≤ 8 minutes

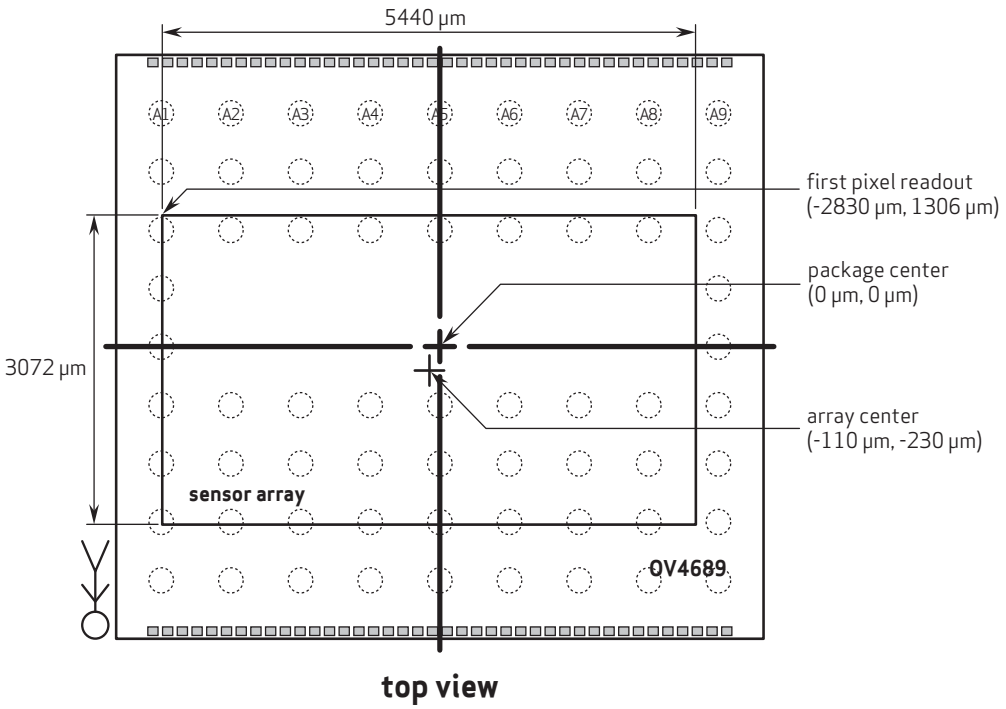
a. maximum number of reflow cycles =3

b. N2 gas reflow or control O2 gas PPM<500 as recommendation

9 optical specifications

9.1 sensor array center

figure 9-1 sensor array center



top view

note 1 this drawing is not to scale and is for reference only.

note 2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pin A1 oriented down on the PCB.

4689_CSP5_DS_9_1

revision history

version 1.0 04.18.2013

- initial release

version 1.1 07.25.2013

- changed title of figure 4-8 to "staggered HDR with virtual channel"
- added figure 4-9, staggered HDR without virtual channel

version 1.2 09.18.2013

- in table 5-1, added bit description for 0x5001[7] and 0x5001[6]
- in table 6-7, added descriptions for registers 0x3760~0x3764
- in table 6-23, changed description for 0x5001[7] from Debug mode to New_stg_hdr_en and changed description for 0x5001[6] from Debug mode to New_stg_EOF_en

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