A12A55 Chip Datasheet - Preliminary

SUMMARY DESCRIPTION

The A12A55 is an integrated system-on-a-chip (SoC) platform for single- and multi-channel automotive video camera solutions.

A12A55 chips provide a 792-MHz ARM Cortex-A9 CPU and an advanced digital signal processing (DSP) subsystem with a 64-Mpixel image sensor pipeline (ISP) and a high-definition (HD) H.264 codec engine.

KEY FEATURES

- Embedded ARM Cortex-A9 792-MHz CPU
- More than 480 MPixel/s processing rate
  - 64-MPixel maximum resolution
- Fish-eye lens dewarping and barrel distortion correction
- Advanced motion-compensated 3D noise reduction (MCTF)
- Advanced dynamic range (WDR and HDR) engine
- H.264 BP/MP/HP Level 5.1 and MJPEG codecs
- Encode performance up to 4Mp30 (in a single-channel configuration) or 3Mp30+2Mp30 (in a dual-channel configuration)
- Two input channels with multiple serial input modes
- 114 General Purpose Input/Output (GPIO) short-height pins
- 404-pin LFBGA package (15 mm x 15 mm)
- 28-nm CMOS Low Power (LP) technology

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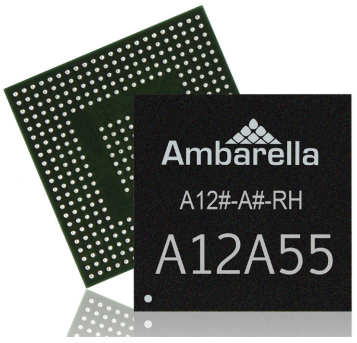


1. OVERVIEW

This preliminary datasheet for the A12A55 processor from Ambarella begins with a brief introduction to the chip (Section 1.1) and a summary of key features (Section 1.2). Chapter 2 describes the A12A55 peripheral interfaces. For pin details and electrical characteristics refer to Chapter 3 and Chapter 4, respectively. See Chapter 5 for package information and Chapter 6 for Ambarella contact and ordering details.

Please note that the chip features described in this datasheet are subject to change. Details that have not been entirely finalized (e.g., encoding specifics) are provided using conservative estimates (i.e., final encoding performance is expected to meet or exceed the estimate provided). Please contact an Ambarella representative for additional information.

1.1 Introduction

The A12A55 is an integrated system-on-a-chip (SoC) platform for single- and multi-channel automotive video camera solutions. A12A55 chips provide a single-core Cortex-A9 ARM CPU and an advanced digital signal processing (DSP) subsystem with a 64-Mpixel image sensor pipeline (ISP) and a high-definition (HD) H.264 codec engine. A functional block diagram of the A12A55 SoC is provided below.

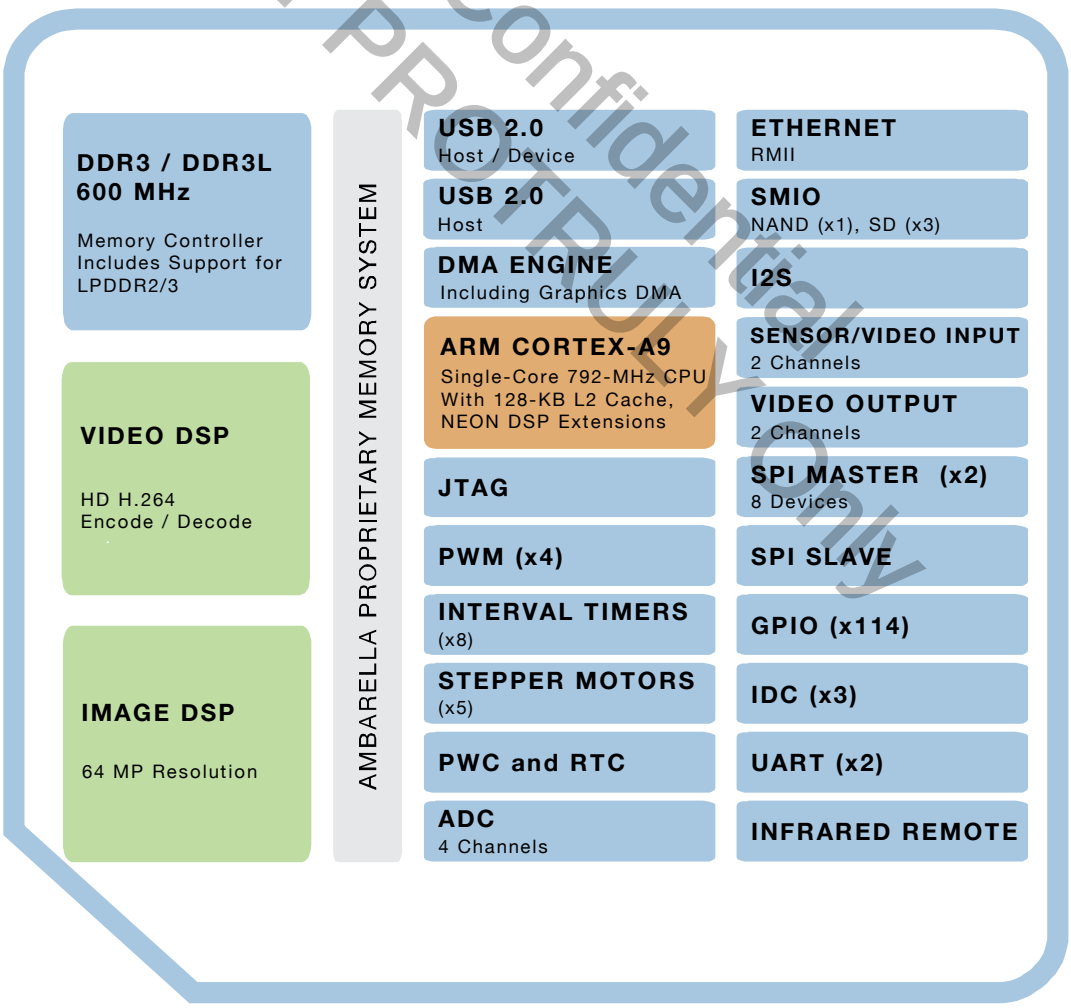


Figure 1-1. A12A55 Overview: Functional Block Diagram of the A12A55 SoC.

The Ambarella A12A55 chip enables the capture of up to 4Mp30-resolution (single-channel) or 3Mp30+2Mp30-resolution (dual-channel) video for automotive applications.

The A12A55 chip can be used in a variety of configurations depending on specific application needs:

- **Single-channel camera systems**
- **Standalone dual-channel camera systems**
  - Two local sensors generate two distinct inputs to the A12A55 SoC (Figure 1-2)

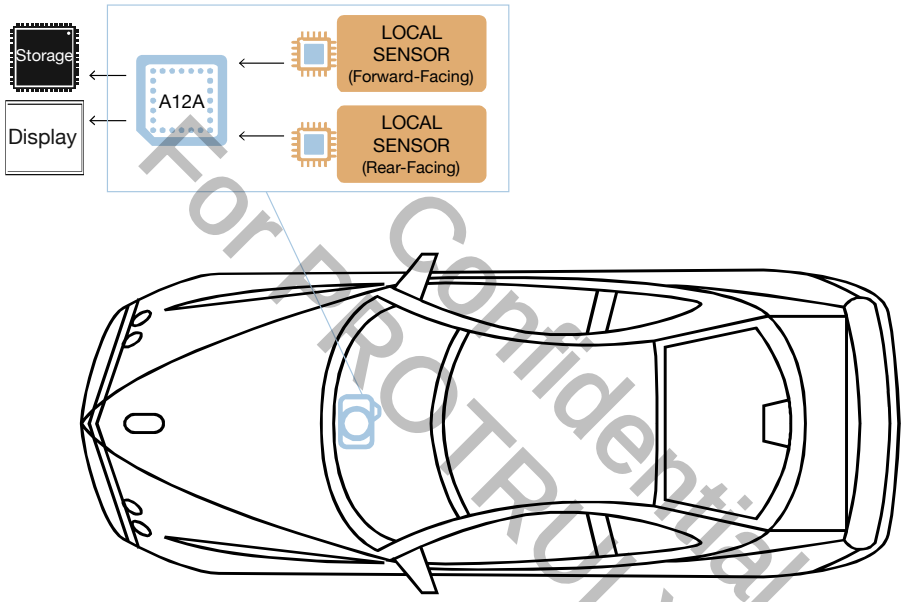


Figure 1-2. A12A55 *Automotive Video Camera Application: Two-Channel Standalone with Two Local Sensors.*

- **Ambarella B5-equipped camera systems**
  - Two possible configurations:
    1. Two remote sensor inputs are sent to the A12A55 SoC via the Ambarella B5F (serializer) and B5Nd (de-serializer) companion chips (Figure 1-3)
       - Sensor inputs are routed through the Ambarella B5F serializer chip to the B5Nd de-serializer chip via a USB cable (up to 7.5 m) or an HDMI cable (up to 10 m)
       - Note that both sensors must be the same type, and must be configured identically.
    2. Inputs from both a local sensor and a remote sensor are sent to the A12A55 SoC (Figure 1-4)
       - The remote sensor input is routed through the Ambarella B5F serializer chip to the B5Nd de-serializer chip via a USB cable (up to 7.5 m) or an HDMI cable (up to 10 m)
       - Note that this configuration allows the use of different sensor types (e.g., HD-capable and Full-HD-capable).

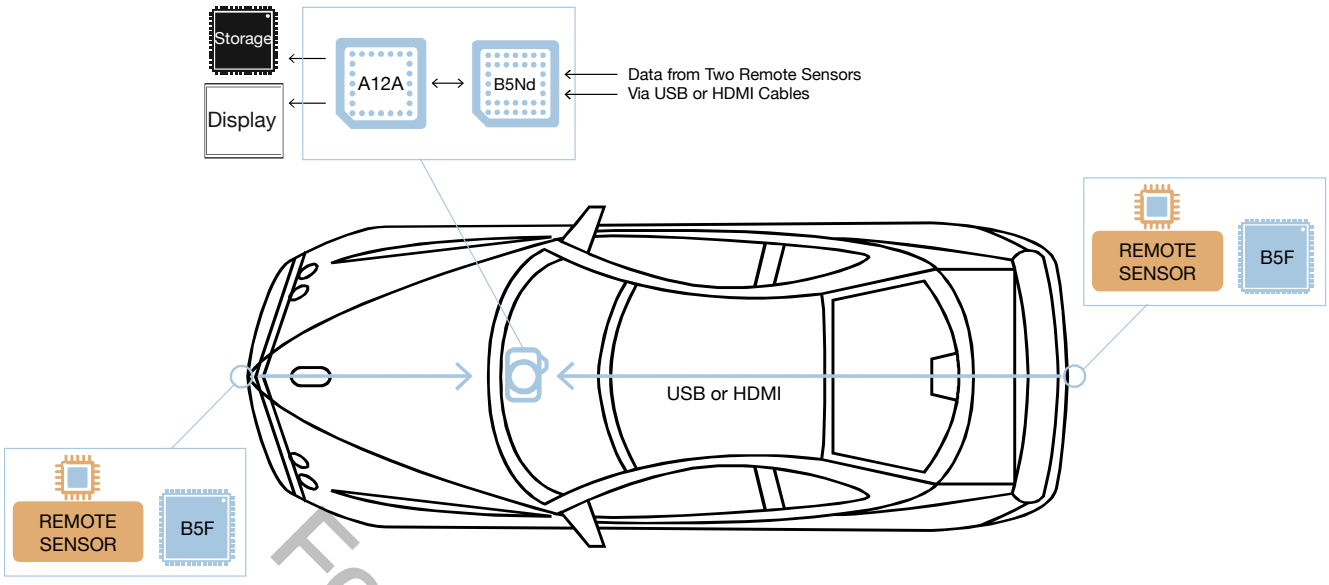


Figure 1-3. A12A55 *Automotive Camera Application: Dual Remote Sensor Configuration (B5-Equipped).*

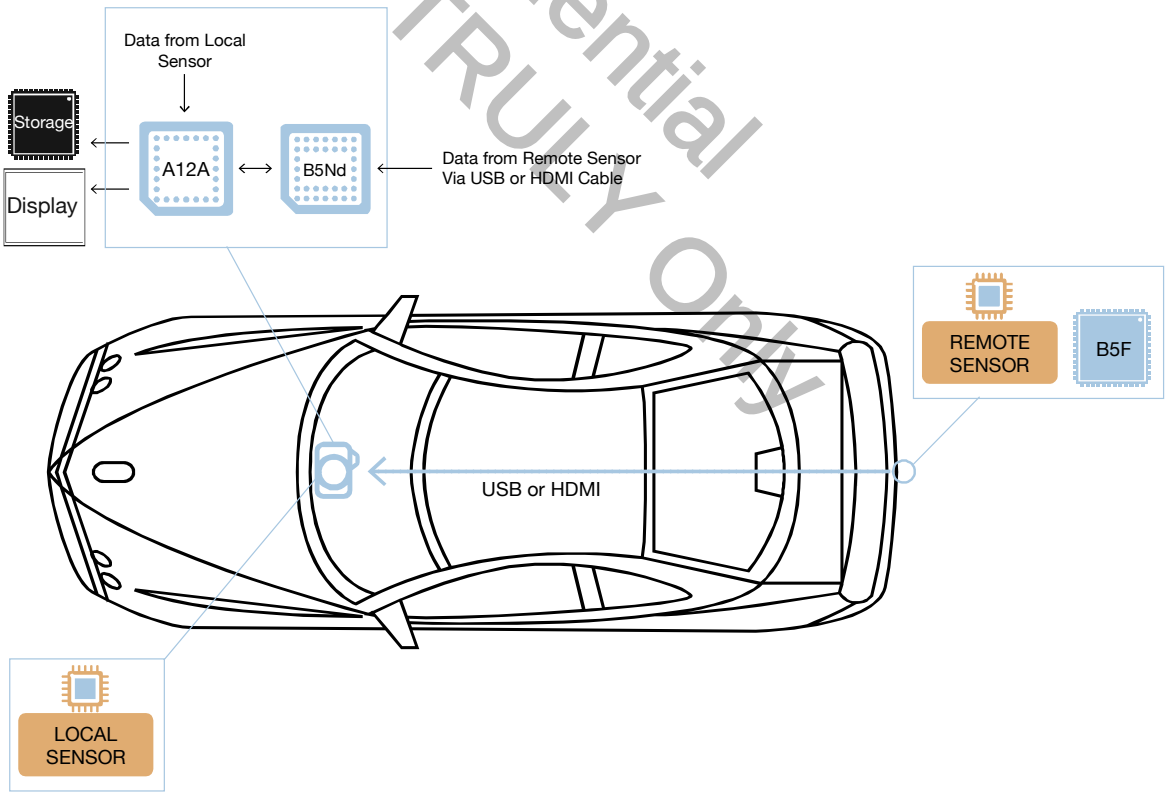


Figure 1-4. A12A55 *Automotive Camera Application: Local / Remote Sensor Configuration (B5-Equipped).*

The A12A55 SoC provides a glueless interface to Serial Sub-LVDS, HiSPi, and MIPI interfaces, as well as parallel connections to popular CMOS image sensors. The ISP offers advanced image-processing features, including improved high dynamic range (HDR) processing with multi-exposure fusion, wide dynamic range (WDR) local contrast enhancement, 3D motion-compensated noise reduction (MCTF), edge enhancement, 3A, image stabilization, and dewarping.

The H.264 codec engine delivers versatile encoding up to 4Mp30 total performance in a single-channel configuration. The high-efficiency H.264 encoder implements progressive refresh for low-latency operations, as well as advanced Main and High-Profile functions for the highest-quality and lowest possible bitrate. These functions include bidirectional prediction (B-frames), large motion-estimation search range, and macroblock-level quantization. Ambarella builds in flexibility with a multi-streaming function, allowing on-the-fly start/stop as well as the adjustment of the bitrate, frame rate, and GOP of each individual stream. The A12A55 WiFi module supports fast-action capture with loop recording, remote view finders, and remote control by handheld devices.

A 792-MHz ARM Cortex-A9 CPU with NEON DSP extensions and floating point support is available for implementing full-featured user applications.

The A12 family is fabricated using low-power 28-nm CMOS technology and integrates advanced power-saving modes, such as utilizing DSP-subsystem memory resources to reduce external memory bandwidth and total camera system power requirements.

1.2 Feature List

Features of the A12A55 chip include:

- Embedded single-core ARM Cortex-A9 CPU
  - Clock frequency up to 792-MHz
  - 32-KByte data / 32-KByte instruction cache
  - 128-KByte L2 cache
  - NEON SIMD engine
- DDR3 and DDR3L controller
  - Up to 600-MHz clock rate
  - 16-bit wide data bus
  - Maximum capacity of 8 Gbits (1 GByte)
  - Includes support for the LPDDR2 and LPDDR3 low-power DDR interfaces
- Image pipeline
  - More than 480 MPixel/s processing rate
  - 64-MPixel maximum resolution
  - Fish-eye lens dewarping and barrel distortion correction
  - Black level correction
  - Dynamic and static defect pixel cluster correction
  - CFA crosstalk and fixed-pattern noise reduction
  - RGB Bayer demosaicing
  - Lens shading

- 3D LUT color transform with gamma
- Advanced motion-compensated sharpening
- Advanced dynamic range (WDR and HDR) engine with multi-exposure fusion and motion artifact reduction
- Per-pixel local exposure dynamic range enhancement
- Tone mapping and global tone-curve adjustment
- Chromatic aberration correction
- Flexible APIs and image-tuning tools
- Adjustable 3A; exposure, white balance and focus control (AE/AWB/AF)
- Day/Night and DC/P iris control
- Crop, mirror, flip, 90°/270° rotation
- Image stabilization with rolling shutter compensation

- Video engine
  - H.264 BP/MP/HP Level 5.1 and MJPEG codecs
  - Maximum encode performance:
    - 4Mp30 in a single-channel configuration
    - 3Mp30+2Mp30 in a dual-channel configuration
    - 1280x720p60
  - Advanced H.264 compression tools
    - I, IP, IBP modes (M=1,2,3,4…; IP, IBP, IBBP, IBBBP…)
    - High Profile with B-frames and hierarchical GOP
    - Up to three reference frames
  - Flexible rate control
    - CBR, VBR and Constant QP with max bitrate control
    - Macroblock-level adaptive quantization
  - 3D noise reduction (MCTF)
- Sensor/Video Input (VIN) interfaces
  - Two input channels with multiple input modes
    - Primary channel supports up to 8-lane SLVS / HiSPi input and up to 4-lane MIPI input
    - Secondary channel supports up to 2-lane SLVS / HiSPi / MIPI input
    - In SVLS mode the two input channels may be combined to support a single 10-lane SLVS / HiSPi sensor
    - Support for 14-bit parallel and LVCMOS sensors
  - Support for popular CMOS sensors: Sony, ON Semiconductor, Panasonic, OmniVision
  - Two clocking options (PLL-generated GCLK_VIN or SLVS bit clock)
  - 16-bit CCIR.601 video input with external sync signals
  - 8-bit, 10-bit, 12-bit or 14-bit BT.656-style video input with embedded sync codes including full-data-range support

- Video Output (VOUT) interfaces
  - Two logical channels to drive three video output ports
    - One logical channel drives HDMI or analog
    - One logical channel drives digital
  - Support for RGBA and YUVA OSD
  - Video DAC for 480i/576i composite PAL/NTSC output
  - BT.656-style embedded sync YUV output (8-bit or 16-bit mode)
  - HDMI 1.4b output with Consumer Electronics Control (CEC) and on-chip PHY
- AHB Bus DMA controller
  - Memory-to-memory transfers including support for transfers between memory and peripherals
  - Programmable transfer count up to 4 MB
  - DMA scatter/gather via chained descriptor list in memory with DMA control information source
- Dedicated DMA co-processor for graphics and image operations
  - Offers linear copy, 2-D copy, composite, and alpha-blend image operations
  - Supports 4- to 32-bit pixel formats
- I2S digital audio interface (stereo)
  - Audio record/playback
- Ethernet MAC controller
  - IEEE 802.3 compliant with full- and half-duplex (IEEE 802.3x flow-control) and Jumbo frames
  - IEEE 802.1Q VLAN tag detection
  - Checksum off-load for received IP and TCP/UDP packets
  - Dedicated pins for RMII or MII interface
  - FIFO (2 KB / 2 KB) and DMA support
- Two USB 2.0 interfaces
  - One host port and one additional port configurable as host or device, each with built-in PHY
- Flexible Storage Media Input / Output (SMIO) interface
  - NAND Flash controller
    - Up to 8-Gbit device, 512-Byte and 2-KByte page sizes
    - 8-bit flash chip data bus
    - 4-bit and 8-bit SLC with ECC hardware and read-confirm support
    - BCH error correction and increased spare area available
  - Two SD controllers (SD0, SD1)
    - SD0:
      - SDIO v3.0, SD, SDHC, SDXC, MMC and eMMC operation with boot support and UHS-I speed
    - SD1:
      - SDIO v3.0, SD, SDHC, SDXC, MMC and eMMC operation
    - 32-GByte maximum capacity for SDHC SD Card

  - 2-TByte maximum capacity for SDXC SD Card
  - 1-bit, 4-bit and 8-bit SD modes, CRC7 for command and CRC16 for data integrity
  - 1-bit, 4-bit SDIO modes
- Multiple boot options
  - NOR-SPI, NAND Flash, USB and eMMC
- Vector interrupt controller including VIC CPU-offload functionality
- SSI / SPI controller interfaces
  - Two SSI / SPI masters with DMA support for up to eight device enables
  - One dedicated SSI / SPI slave port to connect to an external system master
- Two-wire serial Inter-Integrated Circuit (I2C / IDC) interfaces (x3)
  - Configurable IDC buses (x2)
  - One IDC bus dedicated for use with HDMI
- UART interfaces (x2)
  - DMA support
  - One interface supports flow control
- Up to 96 General Purpose Input/Output (GPIO) pins with individual pull-up/down control
- ADC (four channels) with high/low threshold interrupt generation and 12-bit resolution
- Built-in power controller for power-up/down sequencing
- Real Time Clock (RTC)
- Interval timing with eight general-purpose timers configurable as external event counters
- Watchdog timer
- Stepper motor interface (five channels) with four-channel Micro-Stepper interface
- Pulse Width Modulators (PWM) (x4)
- JTAG In-Circuit Emulator (ICE) interface for debugging
- 404-pin, 0.65-pitch LFBGA package (15 mm x 15 mm)
- 28-nm CMOS Low Power (LP) technology
- Operating temperature from -20 C to +85 C

2. INTERFACES

2.1 Overview

This section summarizes the peripheral interfaces for the A12A55 chip as follows:

2.2 SDRAM Interface

The A12A55 chip includes a synchronous DRAM interface, enabling high data-access rates in response to pipe-lined commands. The features of the A12A55 SDRAM interface include:

- Frequencies up to 600 MHz
- Support for DDR3 and DDR3L operations
- Support for the LPDDR2/3 low-power DDR interface
- Programmable I/O strength
- 16-bit data bus

Please contact an Ambarella representative to select a qualified Ambarella-approved DDR component.

2.3 Video Input (VIN) Interface

The A12A55 chip supports two input channels, each with multiple serial and parallel input modes. The features of the A12A55 VIN interface include:

- Support for up to 8-lane SLVS / HiSPi input and up to 4-lane MIPI CSI input in the primary channel
- Up to 2-lane SLVS / HiSPi / MIPI inputs in the secondary channel
    - Note that the secondary VIN interface may not be supported in software. Please contact Ambarella for more information about the use of the secondary VIN channel.
- Support for a single 10-lane SLVS / HiSPi sensor when the two input channels are combined
- Support for 14-bit parallel and LVCMOS sensors
- 16-bit CCIR.601 video input with external sync signals
- 8-bit, 10-bit, 12-bit or 14-bit BT.656-style video input with embedded sync codes including full-data-range support

The following table summarizes the A12A55-supported input data formats, as well as their associated data ports and link types/speeds.

Data Format	Link Type/Speed	Port Selection
YUV (YCbCr)	> 74.25 MHz ≤ 150 MHz	External LVCMOS YUV (YCbCr)
Sensor Data	LVCMOS ≤ 150 MHz	Parallel LVCMOS
Sensor Data	SLVS ≤ 700 Mbps	Serial SLVS
Sensor Data	MIPI ≤ 1 Gbps	Serial MIPI CSI

Table 2-1. Video Input Port Selection.

The A12A55 VIN module is part of the DSP cluster. Like other modules in the DSP cluster it is configured using a set of APIs. Please contact an Ambarella representative for information regarding VIN module configuration for a specific sensor.

2.3.1 Input Modes

The A12A55 chip supports the following input modes:

- (Section 2.3.1.1) Input Mode: External YUV Source
- (Section 2.3.1.2) Input Mode: Bayer Data Parallel Input LVCMOS
- (Section 2.3.1.3) Input Mode: Serial SLVS
- (Section 2.3.1.4) Input Mode: MIPI Camera Serial Interface (CSI)

2.3.1.1 Input Mode: External YUV Source

- Port: External LVCMOS YUV
- Pixel clock: **SPCLK_LVDS_P_0**
- Pixel data [7:0]: **SD_LVDS_P_[7:0]** (8-bit and 16-bit modes)
- Pixel data [15:8]: **SD_LVDS_N_[7:0]** (16-bit mode)
- HSync: **SPCLK_LVDS_N_0**
- VSync: **SPCLK_LVDS_N_1**
- SField: **SPCLK_LVDS_P_1**

2.3.1.2 Input Mode: Bayer Data Parallel Input LVCMOS

- Port: Parallel LVCMOS
- Pixel clock: **SPCLK_LVDS_P_0**
- Pixel data [7:0] (single-ended): **SD_LVDS_P_[7:0]**
- Pixel data [13:8] (single-ended): **SD_LVDS_N_[5:0]**
- HSync: **SPCLK_LVDS_N_0** (Slave Mode - Input is received from the video / sensor device)
  SHSYNC (Master Mode - the A12A55 video input unit drives the sync operation)
- VSync: **SPCLK_LVDS_N_1** (Slave Mode)
  SVSYNC (Master Mode)
- SField: **SPCLK_LVDS_P_1**

2.3.1.3 Input Mode: Serial SLVS

- Port: Serial SLVS
- For every four serial lanes, there should be one sync clock
- Includes support for one, two, four, or eight serial lanes
- Connect the input clock to **SPCLK_LVDS_P/N_[1:0]** as described in the table below. The skew between **SPCLK_LVDS_P/N_[1:0]** must be less than 600 ps.
- Connect the input data to **SD_LVDS_P/N_[7:0]** as described in the table below
- If only one clock is used then connect it to **SPCLK_LVDS_P/N_0**

Number of Data Lanes Used	Mapping	
	Clock	Data Lanes
2	**SPCLK_LVDS_P/N_0**	**SD_LVDS_P/N_[1:0]**
4	**SPCLK_LVDS_P/N_0**	**SD_LVDS_P/N_[3:0]**
8 (except as below*)	**SPCLK_LVDS_P/N_0**	**SD_LVDS_P/N_[3:0]**
	SPCLK_LVDS_P/N_1	**SD_LVDS_P/N_[7:4]**
*Sensors with only one CLK	**SPCLK_LVDS_P/N_0**	**SD_LVDS_P/N_[7:0]**

Table 2-2. SLVS: Sensor Input Port Clock Mapping for the SLVS Interface.

Note

1. The skew between **SPCLK_LVDS_P/N_[0:1]** must be maintained at less than 600 ps.

2.3.1.4 Input Mode: MIPI Camera Serial Interface (CSI)

- Port: Serial MIPI CSI
- Capability: Up to 4-lane MIPI CSI interface to compatible sensors
- Data Formats: Raw-8, Raw-10, Raw-12, Raw-14, YUV-422-8, and Generic-8
- Connect clock to **SPCLK_LVDS_P/N_0**
- Connect data lanes to **SD_LVDS_P/N_[3:0]**

2.4 Video Output (VOUT) Interfaces

The A12A55 Video Output (VOUT) interface supports a total of three output ports using two logical video channels.

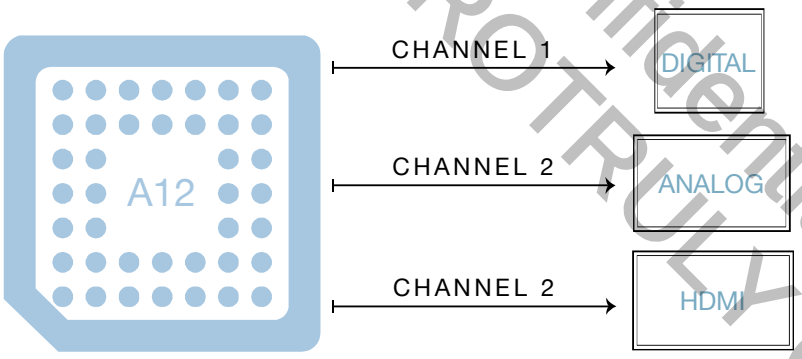


Figure 2-1. A12A55 Video Output Channels and Ports.

One VOUT channel is capable of driving digital output to RGB LCD panels, while the second VOUT channel drives either analog composite output or HDMI output to the on-chip HDMI transmitter (Tx) unit. The A12A55 chip supports simultaneous 1080i and 480i output rates.

2.4.1 Analog Video Output

The A12A55 video digital-to-analog converter (DAC) can drive standard-definition 480i/576i composite video outputs. Refer to the "*A12 Hardware Programming Reference Manual*" for VOUT register programming details.

2.4.2 Digital Video Output

The A12A55 chip supports several digital video output modes including 8-bit or 16-bit {CbY, CrY}, LCD-RGB, CCIR.601, and BT.656-style as described in the tables below.

Refer to the "*A12 Hardware Programming Reference Manual*" for VOUT register programming information.

Bits	Mapped To Signal	Notes
VD0_OUT[15:8]	Unused	
VD0_OUT[7:0]	Interleaved R,G,B	**VD0_OUT[7]** is MSB

Table 2-3. Digital RGB Mode (Video Output Modes 0/1/2 for 3-bit Output to the LCD).

Bits	Mapped To Signal	Notes
VD0_OUT[15:11]	Upper 5 bits of the Red channel	**VD0_OUT[15]** is the MSB
VD0_OUT[10:5]	Upper 6 bits of the Green channel	**VD0_OUT[10]** is the MSB
VD0_OUT[4:0]	Upper 5 bits of the Blue channel	**VD0_OUT[4]** is the MSB

Table 2-4. 5:6:5 RGB Mode (Video Output Mode 3 for 16-bit RGB Output to the LCD).

Bits	Mapped To Signal	Notes
VD0_OUT[15:8]	Unused	
VD0_OUT[7:0]	Interleaved Cb,Y,Cr,Y . . .	Output data rate is 13.5 MHz Clock rate is 27 MHz

Table 2-5. 656-Style YCbCr Mode (Video Output Mode 4 for D1 - 480i and 576 - Resolution).

Bits	Mapped To Signal	Notes
VD0_OUT[15:8]	Interleaved Cb,Cr	**VD0_OUT[15]** is the MSB
VD0_OUT[7:0]	Y	**VD0_OUT[7]** is the MSB

Table 2-6. 16-bit 656-Style YCbCr Mode (Video Output Mode 4) and 16-bit 601-YCbCr Mode (Video Output Mode 5).

Table 2-5 and Table 2-6 correspond to 4:2:2 output format.

2.4.3 HDMI Output

The A12A55 chip includes an embedded HDMI 1.4b transmitter that provides three lanes of transition-minimized differential signaling (TMDS) data and one clock lane. The features of the A12A55 HDMI interface include:

- Consumer Electronics Control (CEC) support, allowing command and control of up to 15 CEC-enabled devices
- An additional two-wire bus (IDC2) for secure key transfer (see Section 2.10)

Refer to the "*A12 Hardware Programming Reference Manual*" for VOUT register programming details.

2.5 I2S Audio Interface

The A12A55 chip provides an Integrated Interchip Sound (I2S) controller for two-channel audio support. Features of the I2S interface include:

- Support for audio using an external analog-to-digital converter (ADC)
- I2S host interface support
- All data lanes are clocked by the same clock signal

Refer to the "*A12 Hardware Programming Reference Manual*" for I2S register programming details.

2.6 Ethernet Interface

The A12A55 Ethernet interface enables a host to transmit and receive data in compliance with the "*IEEE 802.3-2002 Standard for Ethernet Based LANs".* Features include:

- Supports 10/100-Mbps data transfer rates with IEEE 802.3-compliant RMII and MII interfaces to communicate with an external Fast Ethernet PHY
- Supports both full-duplex and half-duplex operation
- MDIO Master interface (optional) for PHY device configuration and management
- A second 25-MHz clock pin for Ethernet PHY

2.7 USB Interfaces

The A12A55 SoC includes two USB 2.0 high-speed interfaces: one USB host and one USB host/device. The host interface (USB1) is configured as a master port, while the device interface (USB0) can be configured to operate in either master or slave mode. Features of the A12A55 USB interfaces include:

- One USB host and one configurable USB host/device, each with a built-in PHY
- USB power-on boot mode

Refer to the "*A12 Hardware Programming Reference Manual*" for USB register programming information.

2.8 Smart Media Input/Output (SMIO) Interface

The A12A55 chip provides Smart Media Input/Output (SMIO) pins as a flexible storage-media interface for NAND Flash and SD controllers. Features of the A12A55 SMIO interface include:

- NAND Flash controller
    - Up to 8-Gbit device, 512-Byte and 2-KByte page sizes

  - 8-bit flash chip data bus
  - 4-bit and 8-bit single-level cell (SLC) memory with error-correcting code (ECC) hardware and read-confirm support

- Three SD controllers (SD0, SD1, SD2)
  - SD0:
    - SDIO v3.0, SD, SDHC, SDXC, MMC and eMMC operation with boot support and UHS-I speed
  - SD1:
    - SDIO v3.0, SD, SDHC, SDXC, MMC and eMMC operation
  - SD2:
    - SDIO v1.0, SD, SDHC, SDXC, MMC and eMMC operation
  - 32-GByte maximum capacity for SDHC SD Card
  - 2-TByte maximum capacity for SDXC SD Card
  - 1-bit, 4-bit and 8-bit SD modes, cyclic redundancy check 7 (CRC-7) for command, and cyclic redundancy check 16 (CRC-16) for data integrity
- Power-on NAND Flash and eMMC boot modes

Refer to the "*A12 Hardware Programming Reference Manual*" for SMIO register programming details.

Controller	Capacity			UHS-1	MMC / eMMC	Boot Support	SDIO (1.0 or 3.0)
	SD	SDHC	SDXC				
SD0	√	√	√	√	√	√	3.0
SD1	√	√	√		√		3.0
SD2	√	√	√		√		1.0

Table 2-7. Supported SD Modes; Where √ = Supported.

2.9 SSI / SPI Interface

The A12A55 chip provides two Synchronous Serial Interface (SSI) / Serial Peripheral Interface (SPI) masters and one dedicated SSI / SPI slave for full-duplex data transmission support. Features of the A12A55 SSI / SPI interface include:

- SSI / SPI master control with DMA support for up to eight slave devices
- Dedicated SSI / SPI slave port for connection to an external system master
- SPI-NOR, SPI-EEPROM boot support included with DMA support

Refer to the "*A12 Hardware Programming Reference Manual*" for register programming information.

Master	Number of Device Enables	Device Enable Pins	SSI/SPI Function	Default Polarity[1]
SSI0	4	**SSI0EN0**	ssi0_en0 Device Enable	Active Low
		SSI0EN1	ssi0_en1 Device Enable	Active Low
		SC_E0	ssi0_en2 Device Enable	Active Low
		TIMER2	ssi0_en3 Device Enable	Active Low
SSI1	4	**ENET_RXD_0** or **SC_A3**	ssi1_en0 Device Enable	Active Low
		ENET_RXD_1 or **SC_B0**	ssi1_en1 Device Enable	Active Low
		ENET_RX_ER or **SC_B1**	ssi1_en2 Device Enable	Active Low
		ENET_CRS_DV or **SC_B2**	ssi1_en3 Device Enable	Active Low

Table 2-8. A12A55 SSI / SPI Master with Device Enable Detail.

Note:

1. Each SSI / SPI device-enable has programmable polarity; i.e., the polarity can be assigned to meet peripheral requirements without external glue logic.

2.10 IDC / I2C Interface

The A12A55 SoC includes three Inter-Integrated Circuit (IDC / I2C) interfaces to provide bidirectional data communication between the chip and its peripheral devices. Features of the A12A55 IDC / I2C interfaces include:

- Two programmable I2C / IDC ports (IDC0 and IDC2)
- One I2C / IDC port dedicated for use with HDMI
- Protocol speeds up to 400 Kbps
- Support for single-master mode

Refer to the "*A12 Hardware Programming Reference Manual*" for I2C / IDC register programming details.

2.11 UART Interface

The A12A55 chip includes two Universal Asynchronous Receiver / Transmitter (UART) ports. Features of the A12A55 UART interface include:

- Support for direct memory access (DMA) and hardware flow control in UART Port 1
- Debugging support in UART Port 0
- A maximum baud rate of 115.2 Kbps for UART0, based on per-port software settings

Refer to the "*A12 Hardware Programming Reference Manual*" for UART register programming.

2.12 InfraRed Remote Interface

The A12A55 chip provides one InfraRed (IR) receiver interface to enable remote control functionality. The A12A55 IR pin receives input signals from the IR module, and these signals are decoded through software programming. Refer to the "*A12 Hardware Programming Reference Manual*" for IR register programming information.

2.13 General Purpose Input/Output (GPIO) Interface

The A12A55 SoC includes 114 CMOS pins which can be programmed for multi-use General Purpose Input/Output (GPIO) functions. Features of the A12A55 GPIO interface include:

- Pins with reduced electrostatic discharge sensitivity, tested to the latest JEDEC standard (*Joint Standard for Component-Level Electrostatic Discharge Sensitivity Testing*)
- Multiplexing support, allowing GPIO pins to be assigned multiple functions that can be independently enabled via software
- Individual pull-up/down control
- Individual drive strength control

Refer to the "*A12 Hardware Programming Reference Manual*" for GPIO register programming details.

2.14 Analog-to-Digital Converter (ADC) Interface

The A12A55 chip provides multiple channels for analog-to-digital conversion (ADC). Features of the A12A55 ADC interface include:

- Four channels
- High/low threshold interrupt generation
- 12-bit resolution

Refer to the "*A12 Hardware Programming Reference Manual*" for ADC register programming information.

2.15 Power Controller (PWC) and Real Time Clock (RTC) Interfaces

To conserve power, the A12A55 system software optimizes clock and PLL frequencies according to operating mode. Peripheral clocks can be further optimized by the user through register programming. Refer to the "*A12 Hardware Programming Reference Manual*" for information regarding register programming with peripheral clocks.

Features of the power controller (PWC) and real-time clock (RTC) interfaces include:

- 32-bit embedded RTC maintained with one dedicated always-on power supply pin

- RTC provides current time, alarm set, and power-on and power-off sequence generation

Refer to the "*A12 Hardware Programming Reference Manual*" for PWC/RTC register programming details.

2.16 Stepper, Micro-Stepper, and Pulse Width Modulator (PWM) Interfaces

2.16.1 Stepper and Micro-Stepper Motor Controllers

The A12A55 chip supports five stepper motor controller channels, each of which can be used for independent motor control. The chip also provides four sets of micro-stepper interfaces.

Refer to the "*A12 Hardware Programming Reference Manual*" for stepper and micro-stepper register programming information.

2.16.2 Pulse Width Modulator (PWM)

The A12A55 chip provides four pulse width modulation interfaces (PWMB0/B1/C0/C1):

- The four PWM outputs are referred to as pwm_[0:3]. Functionally:
  - PWMB0 is associated with pwm_0
  - PWMB1 is associated with pwm_1
  - PWMC0 is associated with pwm_2
  - PWMC1 is associated with pwm_3
- Note that in addition to the PWM controller embedded in the stepper motor controller, the A12A55 external pin **VD_PWM** can also serve as a PWM controller.
- Selection of PWM functions is executed via software. pwm_[0:3] are typically used for motor control and are sourced to the video input clock **CLK_SI**.

Refer to the "*A12 Hardware Programming Reference Manual*" for PWM register programming details.

2.17 JTAG Interface

The A12A55 chip provides an interface for JTAG In-Circuit Emulator (ICE) debugging. Contact an Ambarella representative for more information regarding the JTAG interface.

3. PINS

3.1 Pins: Overview

The A12A55 SoC is equipped with 404 external physical pins including power balls, ground balls, and signal balls. This section provides pin details for the primary chip interfaces and functions.

- Refer to Section 4.4 for a list of fail-safe CMOS pins and their corresponding voltage thresholds.
- Refer to Chapter 7 for a complete list of pins sorted by their location on the A12A55 ball map.
- Refer to the "*A12 Hardware Programming Reference Manual*" for GPIO multi-function selection information.

3.2 Pins: Tables

This section lists the pins for each interface as follows:

For each pin listed, the following information is provided:

- Pin direction: (I) input, (O) output, (S) supply, (G) ground
- Pad type
- A brief description
- For complete multiplexing information, please refer to Section 3.2.12 and Chapter 7.

3.2.1 Pins: SDRAM

Name	Location	Dir	Type	Description
DDR_ADDR_[0:15]	A21, A22, B19, B21, B22, C21, C22, D21, D22, E19, E20, E21, E22, F21, F22, G21	O	SSTL18	Address for row address strobe (RAS) and column address strobe (CAS)
DDR_BA_[0:2]	D19, C20, F20	O	SSTL18	Bank address
DDR_CALIBR	A6	I/O	Analog	DDR3 - ZQ calibration LPDDR2 - NC
DDR_CAS	C18	O	SSTL18	Column address strobe (active low)
DDR_CK	B18	O	SSTL18	DRAM clock per SDRAM
DDR_CK_BAR	A18	O	SSTL18	**DDR_CK** and **DDR_CK_BAR** are differential clocks
DDR_CK_2	B20	O	SSTL18	DRAM clock per SDRAM (unused with 32-bit SDRAM)
DDR_CK_2_BAR	A20	O	SSTL18	**DDR_CK_2** and **DDR_CK_2_BAR** are differential clocks
DDR_CKE	A19	O	SSTL18	Clock enable
DDR_CS	F19	O	SSTL18	Chip select
DDR_CS_2	D20	O	SSTL18	
DDR_DM_[0:3]	A12, B15, B9, C10	O	SSTL18	Data write mask (1 bit per 8 data bits)
DDR_DQ_[0:31]	A14, A17, A7, B10, B12, B14, B17, B6, B7, C11, C12, C13, C14, C15, C16, C17, C6, C7, C8, C9, D10, D11, D13, D14, D15, D16, D17, D6, D7, D8, D9	I/O	SSTL18	Bi-directional data bus
DDR_DQS_[0:3]	B11, B13, B16, B8	I/O	SSTL18	Data strobe (1 bit per 8 data bits) Output with write data, center-aligned Input with read data, edge-aligned
DDR_DQS_BAR_[0:3]	A11, A13, A16, A8	I/O	SSTL18	**DDR_DQS_[N]** and **DDR_DQS_BAR_[N]** are differential signals
DDR_ODT	G19	O	SSTL18	SDRAM on-die termination control signal
DDR_RAS	D18	O	SSTL18	Row address strobe (active low)
DDR_RESET	G22	O	SSTL18	DDR3 - Asynchronous reset LPDDR2 - NC

Name	Location	Dir	Type	Description
DDR_WE	C19	O	SSTL18	Write enable (active low)
DDR_VDDQ_CKE	G20	S	Digital Supply	DDR power - clock enable Tied to internal pin DDR_CKEIN
DDR_VREF_[2:3]	A15, A9	I/O	SSTL18	Reference Voltage for SSTL18 pad (0.5***DDR_VDDQ**)
DDR_VDDQ_[L]	D12, E9, E10, E11, E12, E13, E14, E15, H8, H9, H10, H11, H12, H13, H14, H15	S	Digital Supply	DDR digital I/O power supply

Table 3-1. SDRAM Pins.

3.2.2 Pins: Sensor / Video Input

3.2.2.1 VIN Pins: Primary Sensor Interface

Name	Location	Dir	Type	Description
CLK_SI	N5	I/O	CMOS	Sensor master clock output
SD_LVDS_N_[0:9]	AA10, AA11, AA12, AA13, AA15, AA16, AA17, AA18, AA8, AA9	I	Sub-LVDS/ SLVS/ LVCMOS /MIPI	Sensor data Differential for sub-LVDS and MIPI Single-ended for LVCMOS mode. Termination resistor built in for sub-LVDS / SLVS mode. Both single and double data rates supported.
SD_LVDS_P_[0:9]	AB10, AB11, AB12, AB13, AB15, AB16, AB17, AB18, AB8, AB9	I	Sub-LVDS/ SLVS/ LVCMOS /MIPI	
SHSYNC	Y15	O	CMOS	H-Sync / H-Valid with Master mode configuration
SPCLK_LVDS_N_[0:2]	AA14, AA19, AA7	I	Sub-LVDS/ SLVS/ LVCMOS /MIPI	Sensor pixel clock Differential pairs for sub-LVDS and SLVS mode. **SPCLK_LVDS_P_0** is used for single-ended pixel clock with LVCMOS mode.
SPCLK_LVDS_P_[0:2]	AB14, AB19, AB7	I	Sub-LVDS/ SLVS/ LVCMOS /MIPI	
SVSYNC	Y16	I/O	CMOS	V-Sync / V-Valid with Master mode configuration
LVDS_VDDA18_[L]	W8, W9	S	Analog Supply	VIN analog power (common to primary and secondary sensors)
LVDS_VSSA_[L]	Y10, Y9	G	Analog Ground	VIN analog ground (common to primary and secondary sensors)

Table 3-2. Primary VIN Sensor Interface Pins.

Note:

1. When the secondary VIN interface is active, the primary VIN uses data lanes **SD_LVDS_N_[0:7]** and **SD_LVDS_P_[0:7]**. Note that the secondary VIN interface may not be supported in software. Please contact Ambarella for more information about the use of the secondary VIN channel.
2. If the primary VIN interface is in LVCMOS mode, the secondary VIN supports either a HiSPi/SLVS sensor or a MIPI sensor. If the secondary VIN uses a HiSPi/SLVS sensor, LVDS_VDDA11 can be either 1.8 V or 1.2 V. If the secondary VIN uses a MIPI sensor, LVDS_VDDA11 must be set to 1.2 V.

3.2.2.2 VIN Pins: Secondary Sensor Interface

Name	Location	Dir	Type	Description
SD_LVDS_N_[8:9]	AA8, AA9	I	SubLVDS/ SLVS/ MIPI	Sensor data Differential for sub-LVDS and MIPI Termination resistor built in for sub-LVDS / SLVS mode. Both single and double data rates supported.
SD_LVDS_P_[8:9]	AB8, AB9	I	SubLVDS/ SLVS/ MIPI	
SPCLK_LVDS_N_[2]	AA7	I	SubLVDS/ SLVS/ MIPI	Sensor pixel clock Differential pairs for sub-LVDS and SLVS mode.
SPCLK_LVDS_P_[2]	AB7	I	SubLVDS/ SLVS/ MIPI	

Table 3-3. Secondary VIN Sensor Interface Pins.

Note:

1. When the secondary VIN interface is active, the primary VIN uses data lanes **SD_LVDS_N_[0:7]** and **SD_LVDS_P_[0:7]**. Note that the secondary VIN interface may not be supported in software. Please contact Ambarella for more information about the use of the secondary VIN channel.

3.2.3 Pins: Video Output

This section covers video output Interface pins for Digital-to-Analog Conversion, Digital Video Output, and HDMI output.

3.2.3.1 VOUT Pins: Video Digital-to-Analog Conversion (DAC)

Name	Location	Dir	Type	Description
DAC_COMP	E1	I/O	Analog	Compensation pin
DAC_IO	F1	I/O	Analog	Composite CVBS output
DAC_RSET	G1	I/O	Analog	Reference resistor
DAC_VREFIN	E2	I/O	Analog	Voltage reference input

Name	Location	Dir	Type	Description
VDAC_VDDA18	E4	S	Analog Supply	Video DAC analog power supply
VDAC_VDDA33	F2	S	Analog Supply	Video DAC analog power supply
VDAC_VSSA	E3	G	Analog Ground	Video DAC analog ground

Table 3-4. Video DAC Pins.

3.2.3.2 VOUT Pins: Digital Video Output

Name	Location	Dir	Type	Description [1]
VD0_CLK	V18	I/O	CMOS	Video output clock
VD0_HSYNC	W17	I/O	CMOS	Video output HSync signal
VD0_HVLD	V22	I/O	CMOS	Video output data
VD0_OUT_0	U19	I/O	CMOS	Video output data
VD0_OUT_1	W18	I/O	CMOS	Video output data
VD0_OUT_2	W16	I/O	CMOS	Video output data
VD0_OUT_3	Y17	I/O	CMOS	Video output data
VD0_OUT_4	V16	I/O	CMOS	Video output data
VD0_OUT_5	Y18	I/O	CMOS	Video output data
VD0_OUT_6	Y20	I/O	CMOS	Video output data
VD0_OUT_7	V20	I/O	CMOS	Video output data
VD0_OUT_8	U18	I/O	CMOS	Video output data
VD0_OUT_9	V21	I/O	CMOS	Video output data
VD0_OUT_10	W20	I/O	CMOS	Video output data
VD0_OUT_11	U21	I/O	CMOS	Video output data
VD0_OUT_12	V19	I/O	CMOS	Video output data
VD0_OUT_13	V17	I/O	CMOS	Video output data
VD0_OUT_14	Y19	I/O	CMOS	Video output data
VD0_OUT_15	U22	I/O	CMOS	Video output data
VD0_VSYNC	W19	I/O	CMOS	Video output VSync signal

Table 3-5. Digital Video Output Pins.

Note:

1. A12A55 digital video output pins are used for power-on configuration (POC). For complete POC information, please refer to the "*A12 Hardware Programming Reference Manual*".

3.2.3.3 VOUT Pins: HDMI Output

Name	Location	Dir	Type	Description
CEC	W5	I/O	CMOS	Consumer Electronics Control (CEC) pin (3.3-V tolerance)

Name	Location	Dir	Type	Description
HDMI_CH0_M	M2	I/O	Analog	Transition-minimized differential signaling (TMDS) data out (open drain)
HDMI_CH0_P	M1			
HDMI_CH1_M	N2			
HDMI_CH1_P	N1			
HDMI_CH2_M	P2			
HDMI_CH2_P	P1			
HDMI_CLK_M	L2	I/O	Analog	Differential TMDS clock (open drain)
HDMI_CLK_P	L1	I/O	Analog	
HDMI_REXT	K1	I/O	Analog	Reference resistor - 10 KOhms (1% tolerance) (Required even if HDMI port is unused)
HPD	K2	I/O	CMOS	Hot-plug detect (3.3-V tolerance)
HDMI_AVDD25	L3	S	Analog Supply	HDMI analog power
HDMI_AVDDFLESD	L4	S	Analog Supply	HDMI analog power (Electrostatic Discharge)
HDMI_VDD10_[L]	M3, M4	S	Digital Supply	HDMI digital power
HDMI_VDDA_[L]	K4, J4		Analog Supply	HDMI analog power
HDMI_VSSA_[L]	J3, K3	G	Analog Ground	HDMI analog ground

Table 3-6. HDMI Output Pins.

3.2.4 Pins: I2S Digital Audio

Name	Location	Dir	Type	Description
CLK_AU	M5	O	CMOS	Master clock for external audio codec
I2S_CLK	U1	I/O	CMOS	I2S Controller audio bit clock
I2S_SI	W1	I	CMOS	I2S Controller serial data in
I2S_SO	V2	O	CMOS	I2S Controller serial data out
I2S_WS	V1	I/O	CMOS	I2S Controller word select

Table 3-7. I2S Controller Pins.

3.2.5 Pins: Ethernet Interface

Name	Location	Dir	Type	Description
ENET_REF_CLK	Y22	I/O	CMOS	Reference clock
ENET_CRS_DV	AA20	I/O	CMOS	Carrier sense
ENET_RXD_0	AB22	I/O	CMOS	Receive data
ENET_RXD_1	AA22	I/O	CMOS	
ENET_RX_ER	AB20	I/O	CMOS	Receive data error
ENET_TXD_0	AB21	I/O	CMOS	Transmit data
ENET_TXD_1	AA21	I/O	CMOS	

Name	Location	Dir	Type	Description
ENET_TXEN	Y21	I/O	CMOS	Transmit ready

Table 3-8. Ethernet Pins.

3.2.6 Pins: USB

Name	Location	Dir	Type	Description
GPIO_[1:2]	H3, G3	I/O	CMOS	USB EHCI overcurrent detect input [1, 2]
GPIO_[3:4]	G4, H4	I/O	CMOS	USB EHCI port power enable out [1, 2]
DETECT_VBUS	W6	I/O	CMOS	USB slave bus detect
USB0_DM	AA5	I/O	Analog	USB0 data. DP/DM are differential signals.
USB0_DP	AB5	I/O	Analog	
USB0_REXT	AA4	I/O	Analog	USB0 resistor
USB1_DM	AA6	I/O	Analog	USB1 data. DP/DM are differential signals.
USB1_DP	AB6	I/O	Analog	
USB1_REXT	Y6	I/O	Analog	USB1 resistor
USB_DVDD	AB4	S	Analog Supply	USB analog power supply
USB_VDDA18_[L]	AA3, AB3	S	Analog Supply	USB analog power supply
USB_VDDA33_[L]	Y4, Y5	S	Analog Supply	USB analog power supply
USB_VSSA_[L]	Y7, Y8	G	Analog Ground	USB analog ground

Table 3-9. USB Interface Pins.

Notes:

1. **GPIO1** (OVT0) / **GPIO3** (PWR0) internal are used for USB1
2. **GPIO2** (OVT1) / **GPIO4** (PWR1) internal are used for USB0

3.2.7 Pins: Smart Media Input/Output (SMIO)

- The Smart Media Input/Output (SMIO) pins are CMOS type and programmable input/output.
- SMIO pins are shared by controllers for NAND Flash (NAND) and SD / SDIO / SDHC / SDXC / MMC / eMMC (SD).
- SMIO pins use **SMIO_[N]** for the primary function name.

Name	GPIO	Loc.	NAND		SD		Description
			Function	Dir	Function	Dir	
SMIO_0	55	P22	nand_ce	O			NAND chip enable
SMIO_1	56	N22	nand_rb	I/O			NAND ready / busy
SMIO_2	57	H22			sd_clk	O	SD0 clock
SMIO_3	58	J22			sd_cmd	I/O	SD0 command
SMIO_4	59	M22			sd_cd	I/O	SD0 card detect
SMIO_5	60	K22			sd_wp	I/O	SD0 write protect
SMIO_6	61	R22	nand_re	O			NAND read enable
SMIO_7	62	R21	nand_we	O			NAND write enable
SMIO_8	63	T20	nand_ale	O			NAND address latch enable
SMIO_9	64	N21	nand_d[0]	I/O			NAND data
SMIO_10	65	M21	nand_d[1]	I/O			NAND data
SMIO_11	66	N20	nand_d[2]	I/O			NAND data
SMIO_12	67	M20	nand_d[3]	I/O			NAND data
SMIO_13	68	L20	nand_d[4]	I/O			NAND data
SMIO_14	69	L21	nand_d[5]	I/O			NAND data
SMIO_15	70	L22	nand_d[6]	I/O			NAND data
SMIO_16	71	P20	nand_d[7]	I/O			NAND data
SMIO_17	72	R20	nand_cle	O			NAND command latch enable
SMIO_18	73	P21			sd_d[0]	I/O	SD0 data
SMIO_19	74	K21			sd_d[1]	I/O	SD0 data
SMIO_20	75	J21			sd_d[2]	I/O	SD0 data
SMIO_21	76	H21			sd_d[3]	I/O	SD0 data
SMIO_22	77	J20			sd_d[4]	I/O	SD0 data
SMIO_23	78	K20			sd_d[5]	I/O	SD0 data
SMIO_24	79	L19			sd_d[6]	I/O	SD0 data
SMIO_25	80	H20			sd_d[7]	I/O	SD0 data
SMIO_26	81	M19			sdio_clk	O	SD1 clock
SMIO_27	82	N19			sdio_cmd	I/O	SD1 command
SMIO_28	83	P19			sdio_d[0]	I/O	SD1 data
SMIO_29	84	R19			sdio_d[1]	I/O	SD1 data
SMIO_30	85	T22			sdio_d[2]	I/O	SD1 data
SMIO_31	86	T21			sdio_d[3]	I/O	SD1 data
SMIO_32	87	U20			sdio_cd	I/O	SD1 card detect
SMIO_33	88	T19			sdio_wp	I/O	SD1 write protect
SC_A0	7	N3			sdxc_cmd	I/O	SD2 command
SC_A1	8	N4			sdxc_cd	I/O	SD2 card detect

Name	GPIO	Loc.	NAND		SD		Description
			Function	Dir	Function	Dir	
SC_A2	9	P3			sdxc_wp	I/O	SD2 write protect
SC_A3	10	P4			sdxc_d[0]	I/O	SD2 data
SC_B0	11	P5			sdxc_d[1]	I/O	SD2 data
SC_B1	12	R5			sdxc_d[2]	I/O	SD2 data
SC_B2	13	R4			sdxc_d[3]	I/O	SD2 data
SC_B3	14	T5			sdxc_d[4]	I/O	SD2 data
SC_C0	15	R2			sdxc_d[5]	I/O	SD2 data
SC_C1	16	R1			sdxc_d[6]	I/O	SD2 data
SC_C2	17	T1			sdxc_d[7]	I/O	SD2 data
SC_C3	18	T2			sdxc_CLK	O	SD2 clock
GPIO_0	0	J2			sd_hs_sel	I/O	SD0 high speed. Switch the SDXC power source from 1.8 V to 3.3 V.
WP	54	V5	nand_wp			I/O	NAND write protect

Table 3-10. Storage Media Interface Pins (SMIO) in NAND Flash and SD Modes.

3.2.8 Pins: SSI / SPI

Name	Location	Dir	Pad Type	Description
SSI0CLK	Y1	I/O	CMOS	ssi0 master port bit clock
SSI0EN0	AB1	O	CMOS	ssi0_en0 device enable
SSI0EN1	AA1	O	CMOS	ssi0_en1 device enable
SC_E0	R3	I/O	CMOS	ssi0_en2 device enable
TIMER2	U3	I/O	CMOS	ssi0_en3 device enable
ENET_RXD_0 or **SC_A3**	AB22, P4	I/O	CMOS	ssi1_en0 device enable
ENET_RXD_1 or **SC_B0**	AA22, P5	I/O	CMOS	ssi1_en1 device enable
ENET_RX_ER or **SC_B1**	AB20, R5	I/O	CMOS	ssi1_en2 device enable
ENET_CRS_DV or **SC_B2**	AA20, R4	I/O	CMOS	ssi1_en3 device enable
SSI0MISO	W2	I	CMOS	ssi0 master port data in
SSI0MOSI	Y2	O	CMOS	ssi0 master port data out

Table 3-11. SSI / SPI Interface Pins.

3.2.9 Pins: I2C / IDC

Name	Location	Dir	Pad Type	Description
IDCCLK	Y3	I/O	CMOS	First IDC serial port - clock
IDCDATA	W3	I/O	CMOS	First IDC serial port - data
IDC2CLK	AA2	I/O	CMOS	Second IDC serial port - clock Reserved for HDMI
IDC2DATA	AB2	I/O	CMOS	Second IDC serial port - data Reserved for HDMI
IDC3CLK	V4	I/O	CMOS	Third IDC serial port - clock
IDC3DATA	W4	I/O	CMOS	Third IDC serial port - data

Table 3-12. I2C / IDC Interface Pins.

3.2.10 Pins: UART

Name	Location	Dir	Pad Type	Description
UART0RX	V7	I	CMOS	UART Port 0 receive
UART0TX	W7	O	CMOS	UART Port 0 transmit
SC_D2	U5	I/O	CMOS	UART Port 1 flow control
SC_D3	U4	I/O	CMOS	UART Port 1 flow control
SC_D0	T3	I	CMOS	UART Port 1 receive
SC_D1	T4	O	CMOS	UART Port 1 transmit

Table 3-13. UART Interface Pins.

3.2.11 Pins: InfraRed Remote

Name	Location	Dir	Pad Type	Description
IR_IN	V6	I	CMOS	InfraRed input

Table 3-14. InfraRed Remote Interface Pins.

3.2.12 Pins: General Purpose Input/Output (GPIO)

The table below lists the General-Purpose Input/Output (GPIO) pins on the A12A55 chip. GPIO pins have multi-function capabilities and are CMOS-type programmable input/output. The function name that appears on the chip ball map is indicated in the **Pin Name** column. Refer to Chapter 7 for map locations. For complete function selection information, refer to the "A12 *Hardware Programming Reference Manual*".

GPIO	Pin Name	Multiplexed Function				
		First	Second	Third	Fourth	Fifth
0	**GPIO_0**	sd_hs_sel				
1	**GPIO_1**	ehci_app_prt_ovcurr0	uart_ahb_rx	ssis_sclk	sc_c0	
2	**GPIO_2**	ehci_app_prt_ovcurr1	uart_ahb_tx	ssis_rxd	sc_c1	
3	**GPIO_3**	ehci_prt_pwr_0	uart_ahb_cts_n	ssis_txd	sc_c2	
4	**GPIO_4**	ehci_prt_pwr_1	uart_ahb_rts_n	ssis_en	sc_c3	
5	**GPIO_5**	pwm_1	idsp_pip_iopad_master_hsync	vin_strig0	sc_d0	uart_ahb_cts_n
6	**GPIO_6**	pwm_2	idsp_pip_iopad_master_vsync	vin_strig1	sc_d1	uart_ahb_rts_n
7	**SC_A0**	sc_a0	ssi1_sclk	norspi_clk	pwm_0	sdxc_cmd
8	**SC_A1**	sc_a1	ssi1_txd	norspi_dq[0]	pwm_1	sdxc_cd
9	**SC_A2**	sc_a2	ssi1_rxd	norspi_dq[1]	pwm_2	sdxc_wp
10	**SC_A3**	sc_a3	ssi1_en0	norspi_dq[2]	pwm_3	sdxc_d[0]
11	**SC_B0**	sc_b0	ssi1_en1	norspi_dq[3]		sdxc_d[1]
12	**SC_B1**	sc_b1	ssi1_en2	norspi_en[0]	norspi_dq[2]	sdxc_d[2]
13	**SC_B2**	sc_b2	ssi1_en3	norspi_en[1]	norspi_dq[3]	sdxc_d[3]
14	**SC_B3**	sc_b3	pwm_3	norspi_en[2]		sdxc_d[4]
15	**SC_C0**	sc_c0	uart_ahb_rx	ssis_sclk		sdxc_d[5]
16	**SC_C1**	sc_c1	uart_ahb_tx	ssis_rxd	enet_crs	sdxc_d[6]
17	**SC_C2**	sc_c2	uart_ahb_cts_n	ssis_txd	enet_rxd_2	sdxc_d[7]
18	**SC_C3**	sc_c3	uart_ahb_rts_n	ssis_en	enet_rxd_3	sdxc_clk
19	**SC_D0**	sc_d0	uart_ahb_rx	ssis_sclk	enet_col	pwm_0
20	**SC_D1**	sc_d1	uart_ahb_tx	ssis_rxd	enet_tx_clk	pwm_1
21	**SC_D2**	sc_d2	uart_ahb_cts_n	ssis_txd	enet_tx_er	pwm_2
22	**SC_D3**	sc_d3	uart_ahb_rts_n	ssis_en	enet_txd_2	pwm_3
23	**SC_E0**	sc_e0	ssi0_en2	norspi_en[3]	enet_txd_3	pwm_1
24	**TIMER0**	tm11_clk			enet_2nd_ref_clk	
25	**TIMER1**	tm12_clk		idsp_pip_iopad_master_hsync	enet_mdc	
26	**TIMER2**	tm13_clk	ssi0_en3	idsp_pip_iopad_master_vsync	enet_mdio	
27	**IDCCLK**	idc0clk				
28	**IDCDATA**	idc0data				
29	**IDC2CLK**	idc1clk		norspi_dq[2]	norspi_en[2]	
30	**IDC2DATA**	idc1data		norspi_dq[3]	norspi_en[3]	
31	**IDC3CLK**	idc2clk	vin_strig0			
32	**IDC3DATA**	idc2data	vin_strig1			

GPIO	Pin Name	Multiplexed Function				
		First	Second	Third	Fourth	Fifth
33	IR_IN	ir_in				
34	SSI0CLK	ssi0_sclk	norspi_clk	uart_ahb_rx	ssis_sclk	
35	SSI0MOSI	ssi0_txd	norspi_dq[0]	uart_ahb_tx	ssis_rxd	
36	SSI0MISO	ssi0_rxd	norspi_dq[1]	uart_ahb_cts_n	ssis_txd	
37	SSI0EN0	ssi0_en0	norspi_en[0]	uart_ahb_rts_n	ssis_en	
38	SSI0EN1	ssi0_en1	norspi_en[1]			
39	UART0RX	uart0rx	uart_ahb_rx			
40	UART0TX	uart0tx	uart_ahb_tx			
41	I2S_CLK	i2s_clk				
42	I2S_SI	i2s_si				
43	I2S_SO	i2s_so				
44	I2S_WS	i2s_ws				
45	CLK_AU					
46	ENET_TXEN	enet_txen	sc_a0	enet_txen	ssi1_sclk	norspi_clk
47	ENET_TXD_0	enet_txd_0	sc_a1	enet_txd_0	ssi1_txd	norspi_dq[0]
48	ENET_TXD_1	enet_txd_1	sc_a2	enet_txd_1	ssi1_rxd	norspi_dq[1]
49	ENET_RXD_0	enet_rxd_0	sc_a3	enet_rxd_0	ssi1_en0	norspi_en[0]
50	ENET_RXD_1	enet_rxd_1	sc_b0	enet_rxd_1	ssi1_en1	norspi_en[1]
51	ENET_RX_ER	enet_rxer	sc_b1	enet_rxer	ssi1_en2	norspi_en[2]
52	ENET_CRS_DV	enet_crs_dv	sc_b2	enet_crs_dv	ssi1_en3	norspi_dq[2]
53	ENET_REF_CLK	enet_ref_clk	sc_b3	enet_rx_clk		norspi_dq[3]
54	WP		nand_wp			
55	SMIO_0		nand_ce	norspi_clk		
56	SMIO_1		nand_rb	norspi_dq[4]		
57	SMIO_2		sd_clk			
58	SMIO_3		sd_cmd			
59	SMIO_4		sd_cd			
60	SMIO_5		sd_wp			
61	SMIO_6		nand_re	norspi_dq[5]		
62	SMIO_7		nand_we	norspi_dq[6]		
63	SMIO_8		nand_ale	norspi_dq[7]		
64	SMIO_9		nand_d[0]	norspi_en[0]		
65	SMIO_10		nand_d[1]	norspi_en[1]		
66	SMIO_11		nand_d[2]	norspi_en[2]		
67	SMIO_12		nand_d[3]	norspi_en[3]		
68	SMIO_13		nand_d[4]	norspi_dq[0]		
69	SMIO_14		nand_d[5]	norspi_dq[1]		
70	SMIO_15		nand_d[6]	norspi_dq[2]		
71	SMIO_16		nand_d[7]	norspi_dq[3]		
72	SMIO_17		nand_cle			
73	SMIO_18		sd_d[0]			

GPIO	Pin Name	Multiplexed Function				
		First	Second	Third	Fourth	Fifth
74	**SMIO_19**		sd_d[1]			
75	**SMIO_20**		sd_d[2]			
76	**SMIO_21**		sd_d[3]			
77	**SMIO_22**		sd_d[4]		sc_c0	ssis_sclk
78	**SMIO_23**		sd_d[5]		sc_c1	ssis_rxd
79	**SMIO_24**		sd_d[6]		sc_c2	ssis_txd
80	**SMIO_25**		sd_d[7]		sc_c3	ssis_en
81	**SMIO_26**		sdio_clk			
82	**SMIO_27**		sdio_cmd			
83	**SMIO_28**		sdio_d[0]		sc_d0	ssis_sclk
84	**SMIO_29**		sdio_d[1]		sc_d1	ssis_rxd
85	**SMIO_30**		sdio_d[2]		sc_d2	ssis_txd
86	**SMIO_31**		sdio_d[3]		sc_d3	ssis_en
87	**SMIO_32**		sdio_cd			
88	**SMIO_33**		sdio_wp			
89	**HPD**	hdmitx_hpd				
90	**CEC**	hdmitx_cec	enet_2nd_ref_clk			
91	**SVSYNC**	vin_svsync	idsp_pip_iopad_master_hsync			
92	**SHSYNC**	vin_shsync	idsp_pip_iopad_master_vsync			
93	**VD0_OUT_0**	vd0_out[0]				
94	**VD0_OUT_1**	vd0_out[1]				
95	**VD0_OUT_2**	vd0_out[2]				
96	**VD0_OUT_3**	vd0_out[3]				
97	**VD0_OUT_4**	vd0_out[4]				
98	**VD0_OUT_5**	vd0_out[5]				
99	**VD0_OUT_6**	vd0_out[6]				
100	**VD0_OUT_7**	vd0_out[7]				
101	**VD0_OUT_8**	vd0_out[8]				
102	**VD0_OUT_9**	vd0_out[9]				
103	**VD0_OUT_10**	vd0_out[10]				
104	**VD0_OUT_11**	vd0_out[11]				
105	**VD0_OUT_12**	vd0_out[12]				
106	**VD0_OUT_13**	vd0_out[13]				
107	**VD0_OUT_14**	vd0_out[14]				
108	**VD0_OUT_15**	vd0_out[15]				
109	**VD0_CLK**	vd0_clk				
110	**VD0_VSYNC**	vd0_vsync				
111	**VD0_HSYNC**	vd0_hsync				
112	**VD0_HVLD**	vd0_hvld				

GPIO	Pin Name	Multiplexed Function				
		First	Second	Third	Fourth	Fifth
113	**VD_PWM**	pwm_0				

Table 3-15. General Purpose Input Output (GPIO) Multifunction-Capable Pins.

3.2.13 Pins: Analog to Digital Conversion (ADC)

Name	Location	Dir	Type	Description
ADC_CH_[0:3]	B4, C4, B3, C3	I	Analog	ADC analog input (4 channels)
ADC_CH_4				Reserved (Tie to analog ground)
ADC_VDDA18	E5	S	Analog Supply	ADC analog power supply
ADC_VDDA33	F3	S	Analog Supply	ADC analog power supply
ADC_VSSA	D3	G	Analog Ground	ADC analog ground

Table 3-16. ADC Interface Pins.

3.2.14 Pins: Power Controller (PWC) and Real Time Clock (RTC)

Name	Location	Dir	Type	Description
PWC_PC_REF	A1	I/O	Analog	Used to detect whether battery level is too low. Connect to voltage-divided version of **PWC_PC_VDD.**
PWC_PSEQ[1:3]	D5, C5, D4	O	CMOS	Power Up/Down control signals.
PWC_RSTINB	B5	I	CMOS	PWC reset input. Usually pulled up to **PWC_PC_VDD** through an RC circuit.
PWC_RSTOB	A5	O	CMOS	Reset signal out (also used as Power Up/Down signal)
PWC_RTC_CP	A3	S	Analog Supply	Power for RTC module and on-chip RTC oscillator. When **PWC_RTC_CP** is less than a specified voltage, the power controller will shut down and all registers will reset.
PWC_WKUP	F5	I	CMOS	In the power-off state, a positive pulse can only trigger a power on sequence.
PWC_WKUP1	F4			
XI_RTC	B2	I	XOSC	Connect to RTC crystal
XO_RTC	A2	O	XOSC	Connect to RTC crystal
PWC_PC_VDD	A4	S	Digital Supply	Power for power-management module Connected to external battery/adaptor clamping circuit. The **PWC_PC_VDD** voltage must be a specified minimum to block a **WKUP[N]**.

Table 3-17. PWC and RTC Interface Pins.

3.2.15 Pins: Timer

Name	Location	Dir	Type	Description
TIMER0	U2	I/O	CMOS	Interval Timer 0 external clock source
TIMER1	V3	I/O	CMOS	Interval Timer 1 external clock source
TIMER2	U3	I/O	CMOS	Interval Timer 2 external clock source

Table 3-18. Timer Pins.

3.2.16 Pins: Stepper Controller

Name	Location	Dir	Type	Description
SC_A0	N3	I/O	CMOS	Stepper Controller A
SC_A1	N4	I/O	CMOS	Stepper Controller A / Micro Stepper A
SC_A2	P3	I/O	CMOS	Stepper Controller A / Micro Stepper A
SC_A3	P4	I/O	CMOS	Stepper Controller A / Micro Stepper A
SC_B0	P5	I/O	CMOS	Stepper Controller B
SC_B1	R5	I/O	CMOS	Stepper Controller B / Micro Stepper B
SC_B2	R4	I/O	CMOS	Stepper Controller B / Micro Stepper B
SC_B3	T5	I/O	CMOS	Stepper Controller B / Micro Stepper B
SC_C0	R2	I/O	CMOS	Stepper Controller C
SC_C1	R1	I/O	CMOS	Stepper Controller C / Micro Stepper C
SC_C2	T1	I/O	CMOS	Stepper Controller C / Micro Stepper C
SC_C3	T2	I/O	CMOS	Stepper Controller C / Micro Stepper C
SC_D0	T3	I/O	CMOS	Stepper Controller D
SC_D1	T4	I/O	CMOS	Stepper Controller D / Micro Stepper D
SC_D2	U5	I/O	CMOS	Stepper Controller D / Micro Stepper D
SC_D3	U4	I/O	CMOS	Stepper Controller D / Micro Stepper D
SC_E0	R3	I/O	CMOS	Stepper Controller E

Table 3-19. Stepper / Microstepper Pins.

3.2.17 Pins: Pulse Width Modulator (PWM)

Name	Location	Dir	Type	Description
VD_PWM	W22	I/O	CMOS	Pulse Width Modulator Output
PWM_1	G4	I/O	CMOS	Pulse Width Modulator Output Typically used for motor control
PWM_2	H4	I/O	CMOS	Pulse Width Modulator Output Typically used for motor control
PWM_3	T5	I/O	CMOS	Pulse Width Modulator Output Typically used for motor control

Table 3-20. PWM Pins.

3.2.18 Pins: JTAG Control

Name	Location	Dir	Pad Type	Description
JTAG_CLK	C1	I	CMOS	Clock
JTAG_RST_L	D2	I	CMOS	Reset
JTAG_TDI	B1	I	CMOS	Data in
JTAG_TDO	D1	O	CMOS	Data out
JTAG_TMS	C2	I	CMOS	Test mode select

Table 3-21. JTAG Pins.

3.2.19 Pins: Global and Test

Name	Location	Dir	Type	Description
FSOURCE_0	K19	S	Power / Ground	Power supply during programming. Customer ties to digital ground for operation.
POR_L	V8	I	CMOS	Power-on reset pin (active low)
TEST_MODE	W21	I	CMOS	0 - Normal mode 1 - Test mode
XIN	H1	I	XOSC	24-MHz or 48-MHz crystal or crystal oscillator input
XOUT	J1	O	XOSC	

Table 3-22. Global and Test Pins.

3.2.20 Pins: Power, Ground and PLL

Name	Location	Dir	Type	Description
ADC_VDDA18	E5	S	Analog Supply	ADC analog power supply
ADC_VDDA33	F3	S	Analog Supply	ADC analog power supply
ADC_VSSA	D3	G	Analog Ground	ADC analog ground
DDR_VDDQ_[L]	D12, E9, E10, E11, E12, E13, E14, E15, H8, H9, H10, H11, H12, H13, H14, H15	S	Digital Supply	DDR digital I/O power supply
HDMI_AVDD25	L3	S	Analog Supply	HDMI analog power
HDMI_ AVDDFLESD	L4	S	Analog Supply	HDMI analog power (Electrostatic Discharge)
HDMI_VDD10_ [L]	M3, M4	S	Digital Supply	HDMI digital power
HDMI_VDDA_[L]	K4, J4		Analog Supply	HDMI analog power
HDMI_VSSA_[L]	J3, K3	G	Analog Ground	HDMI analog ground
LVDS_VDDA11	V9	S	Analog Supply	VIN analog power (common to primary and secondary sensors)
LVDS_VDDA18_ [L]	W8, W9	S	Analog Supply	VIN analog power (common to primary and secondary sensors)
LVDS_VSSA_[L]	Y10, Y9	G	Analog Ground	VIN analog ground (common to primary and secondary sensors)
PWC_PC_VDD	A4	S	Digital Supply	Power for power management module Connected to external battery/adaptor clamping circuit. The **PWC_PC_VDD** voltage must be a specified minimum to block a **WKUP[N]**.
USB_DVDD	AB4	S	Analog Supply	USB analog power supply
USB_VDDA18_[L]	AA3, AB3	S	Analog Supply	USB analog power supply
USB_VDDA33_[L]	Y4, Y5	S	Analog Supply	USB analog power supply
USB_VSSA_[L]	Y7, Y8	G	Analog Ground	USB analog ground
VDAC_VDDA18	E4	S	Analog Supply	Video DAC analog power supply
VDAC_VDDA33	F2	S	Analog Supply	Video DAC analog power supply
VDAC_VSSA	E3	G	Analog Ground	Video DAC analog ground

Name	Location	Dir	Type	Description
VDD_[L]	M10, M11, M12, M13, M14, M9, N10, N11, N12, N13, N14, N9, P10, P11, P12, P13, P14, P9, R10, R11, R12, R13, R14, R9	S	Digital Supply	Digital power supply
VDD33_[L]	K18, L18, V12, V13, V14, V15, W12, W13, W14, W15	S	Digital Supply	Digital power supply
NAND_VDDO_[L]	H18, H19	S	Digital Supply	NAND Flash digital power
SD_VDDO_[L]	M18, N18	S	Digital Supply	SD controller digital power
SDIO_VDDO_[L]	J18, J19	S	Digital Supply	SDIO controller digital power
VDDA10_PLL_[L]	K5, L5	S	Analog Supply	PLL analog power
VDDA18_PLL	G5	S	Analog Supply	PLL analog power
VDDP18_[L]	P18, R18, T18, V10, V11, W10, W11	S	Digital Supply	I/O pre-driver power
VSS_[L]	E16, E17, E18, E6, E7, E8, F18, G18, J10, J11, J12, J13, J14, J15, J8, J9, K10, K11, K12, K13, K14, K15, K8, K9, L10, L11, L12, L13, L14, L15, L8, L9, M15, M8, N15, N8, P15, P8, R15, R8, Y11, Y12, Y13, Y14	G	Digital Ground	Digital ground

Table 3-23. Power, Ground and PLL Pins.

4. ELECTRICAL CHARACTERISTICS

4.1 Electrical: Overview

This section provides details on the electrical characteristics of the A12A55 chip as follows:

- (Section 4.1) Electrical: Overview
- (Section 4.2) Electrical: Absolute Ratings
- (Section 4.3) Electrical: Recommended Operating Conditions
- (Section 4.4) Electrical: Fail-Safe Pins
- (Section 4.5) Electrical: Video Signal Wave Forms and Timing
- (Section 4.6) Electrical: SD Controller Timing
- (Section 4.7) Electrical: eMMC Boot Timing

Note that the electrical details provided in this section are preliminary estimates.

4.2 Electrical: Absolute Ratings

The following table provides absolute ratings for the analog/digital voltages of the A12A55 power rails.

Parameter	Minimum	Maximum
Analog supply voltage (3.0 V)	-0.3 V	3.6 V
Digital supply voltage (3.0 V)	-0.3 V	3.6 V
Analog supply voltage (1.8 V)	-0.3 V	1.98 V
Digital supply voltage (1.8 V)	-0.3 V	1.98 V
Analog supply voltage (1.0 V)	-0.3 V	1.15 V
Digital supply voltage (1.0 V)	-0.3 V	1.15 V
Digital I/O range (V)	-0.3 V	3.6 V
	-0.3 V	1.98 V
Analog I/O range (V)	-0.3 V	3.6 V
	-0.3 V	1.98 V
Operating temperature (case) (°C)	-20 C to +85 C	
Storage temperature (°C)	-40 C to +150 C	
Thermal resistance (Θ_{jc}) (°C/W)	11.22 C/W	

Table 4-1. Absolute Ratings.

This Ambarella part will support a full range of operation at the case temperature specified above, provided that the customer's PCB design, manufacturing processes, and power supply design are equal to those of the Ambarella reference hardware platform in terms of quality. All other components used during system design are also required to operate successfully at the case temperature range specified above to guarantee proper overall system operation.

4.3 Electrical: Recommended Operating Conditions

This section continues with recommended operating conditions for:

- (Section 4.3.1) Operating Conditions: Power Rails - DC Characteristics
- (Section 4.3.2) Operating Conditions: Digital I/O
- (Section 4.3.3) Operating Conditions: DRAM I/O
- (Section 4.3.4) Operating Conditions: PWC and RTC Power Supply
- (Section 4.3.5) Operating Conditions: Video Sensor Input
- (Section 4.3.6) Operating Conditions: Video DAC
- (Section 4.3.7) Operating Conditions: ADC Electrical Specifications
- (Section 4.3.8) Operating Conditions: Crystal and Reference Clock Requirements

4.3.1 Operating Conditions: Power Rails - DC Characteristics

Parameter [1]	Comments	Minimum	Typical	Maximum	Ripple
ADC_VDDA18	Channel 0	1.7 V	1.8 V	1.9 V	2%
ADC_VDDA33	All other channels	2.85 V	3.0 V	3.6 V	2%
DDR_VDDQ_CKE / DDR_VDDQ	DDR3 Mode	1.4 V	1.5 V	1.6 V	2%
	DDR3L Mode	1.28 V	1.35 V	1.45 V	2%
	LPDDR2/3 Mode	1.14 V	1.2 V	1.3 V	2%
HDMI_PLL_VDD		0.97 V	1.0 V	1.03 V	2%
HDMI_VDDA_0		1.7 V	1.8 V	1.9 V	2%
HDMI_VDDA_ESD		2.85 V	3.0 V	3.6 V	2%
HDMI_VDDA_ESD_1P8V		1.7 V	1.8 V	1.9 V	2%
LVDS_VDDA11 (Refer to Section 3.2.2.1)	Primary and Secondary Sensor SLVS Mode	0.97 V	1.0 V	1.03 V	2%
	Primary or Secondary Sensor MIPI Mode	1.08 V	1.1 V	1.13 V	2%
	Primary Sensor 1.8-V LVCMOS	1.7 V	1.8 V	1.9 V	2%
LVDS_VDDA18	Common	1.7 V	1.8 V	1.9 V	2%
PWC_PC_VDD		2.9 V	3.1 V	3.15 V	2%
USB_DVDD		0.97 V	1.0 V	1.03 V	2%
USB_VDD18_0		1.7 V	1.8 V	1.9 V	2%
USB_VDD33_0		2.85 V	3.0 V	3.6 V	2%
VDAC_AVDD18		1.7 V	1.8 V	1.9 V	2%
VDAC_AVDD33		2.85 V	3.0 V	3.6 V	2%
VDD		0.97 V	1.0 V	1.03 V	2%
VDD33		2.85 V	3.0 V	3.6 V	2%
VDD33_NAND	3.0-V mode	2.85 V	3.0 V	3.6 V	2%
	1.8-V mode	1.7 V	1.8 V	1.9 V	2%

Parameter [1]	Comments	Minimum	Typical	Maximum	Ripple
VDD33_SD / VDD33_SDIO	SD mode	2.85 V	3.0 V	3.6 V	2%
	SDXC mode	1.7 V	1.8 V	1.9 V	2%
VDDA10_PLL		0.97 V	1.0 V	1.03 V	2%
VDDA18_PLL		1.7 V	1.8 V	1.9 V	2%
VDDP18		1.7 V	1.8 V	1.9 V	2%

Table 4-2. Power Rails: DC Characteristics (Preliminary and Subject to Change).

Note:

1. The electrical details provided in this section are preliminary estimates and are subject to change. Please contact an Ambarella representative for current electrical specifications.

4.3.2 Operating Conditions: Digital I/O

Parameter	Comments	Minimum	Typical	Maximum
VIL	Input Low Voltage	-0.3 V		0.7 V
VIH	Input High Voltage	2.0 V		3.6 V (for 3.3V-tolerant pins)
VOL	Output Low Voltage			0.4 V
VOH	Output High Voltage	2.4 V		

Table 4-3. Digital I/O Characteristics (Preliminary).

4.3.3 Operating Conditions: DRAM I/O

4.3.3.1 DRAM: DC Supply Voltage Levels

Parameter	Comments	Minimum	Typical	Maximum
DDR_VDDQ		See Section 4.3.1		
DDR_VDDQ_CKE		See Section 4.3.1		
VTT	Termination voltage	DDR_VREF - 0.04 V	DDR_VREF	DDR_VREF + 0.04 V
DDR_VREF	Input reference level	0.49 * DDR_VDDQ	0.5 * VDDQ	0.51 * DDR_VDDQ

Table 4-4. DRAM I/O Characteristics - DC Supply Voltage Levels (Preliminary).

4.3.3.2 DRAM: SSTL I/O DC Specifications

Parameter	Comments	Minimum	Typical	Maximum
VIHT	DC input logic threshold high			DDR_VREF + 0.05 V
VILT	DC input logic threshold low	DDR_VREF - 0.05 V		
VIH	DC input voltage high	DDR_ VREF+100 mV		VDDQ + 0.3 V
VIL	DC input voltage low	-0.3 V		DDR_VREF- 100 mV
VOH	DC output logic high	DDR_VDDQ		
VOL	DC output logic low			0 V
RTT1	RTT effective impedance	60 Ohms	75 Ohms	90 Ohms
RTT2	RTT effective impedance	120 Ohms	150 Ohms	180 Ohms

Table 4-5. DRAM I/O Characteristics - SSTL I/O DC Specifications (Preliminary).

4.3.4 Operating Conditions: PWC and RTC Power Supply

Parameter	Comments	Minimum	Typical	Maximum
PWC_RTC_CP	RTC module supply	1.2 V	2.4 V	2.6 V
PWC_PC_VDD	Power management supply	2.9 V	3.1 V	3.15 V
PWC_PC_REF	Reference voltage	1.3 V		1.8 V
VIH	For PWC_WKUP	0.7 * PWC_ RTC_CP		
VIL	For PWC_WKUP			0.3 * PWC_ RTC_CP
VOH	PWC_PSEQ[1:3]	0.9 * PWC_ PC_VDD		
	PWC_RSTOB	0.9 * PWC_ PC_VDD		

Table 4-6. PWC and RTC Supply.

4.3.5 Operating Conditions: Video Sensor Input

Parameter		Symbol	Comment	Min	Typ.	Max.
Supply Voltage	Analog	MIPI_VDDA18		1.7 V	1.8 V	2.0 V
	Interface	MIPI_VDDA11		1.04 V	1.1 V	1.15 V
	Digital	VDD		0.97 V	1.0 V	1.03 V
Digital Input Voltage		VIL	LVCMOS 1.1 V			0.45 V
			LVCMOS 1.8 V			0.6 V
		VIH	LVCMOS 1.1 V	0.7 V		
			LVCMOS 1.8 V	1.2 V		

Parameter	Symbol	Comment	Min	Typ.	Max.
Differential Input for SLVS	V_{CM}		0.2 V		1.0 V
	V_{DIFF}		70 mV		400 mV

Table 4-7. DC Characteristics: SLVS Interface.

4.3.5.1 VIN: MIPI Receiver DC Specification

Parameter	Comments	Minimum	Typical	Maximum
VIH	Logic 1 input voltage	880 mV		
VIL	Logic 0 input voltage, not in ULP state			550 mV
VIL-ULP	Logic 0 input voltage, ULP state			300 mV
VHYST	Input hysteresis	25 mV		

Table 4-8. MIPI Receiver DC Specification.

4.3.5.2 VIN: MIPI Receiver AC Specification

Description	Minimum	Typical	Maximum
Input pulse rejection			300 V-ps
Minimum pulse width response	20 ns		
Peak interference amplitude			200 mV
Interference frequency	450 MHz		

Table 4-9. MIPI Receiver AC Specification.

4.3.6 Operating Conditions: Video DAC

Parameter	Comments	Minimum	Typical	Maximum
VDD	Operating digital supply voltage	0.97 V	1.0 V	1.03 V
VDAC_AVDD18	Operating analog supply voltage	1.7 V	1.8 V	1.9 V
VDAC_AVDD33		2.85 V	3.0 V	3.6 V
IO_{FS}	IO out current		34.6 mA	
I_{OP}	Operating Current		36 mA	
V(IO)	Out voltage full scale	1.17 V	1.28 V	1.43 V
Resolution	DAC resolution			10 bits
DNL	Differential non-linearity error			±1 LSB

Parameter	Comments	Minimum	Typical	Maximum
INL	Integral non-linearity error			±2 LSB
VREF	Reference Voltage			1.22 V

Table 4-10. Video DAC Electrical Specifications.

4.3.7 Operating Conditions: ADC Electrical Specifications

4.3.7.1 ADC Electrical: DC Specification

Parameter	Comments	Minimum	Typical	Maximum
VDD	Digital supply voltage	0.97 V	1.0 V	1.03 V
ADC_AVDD18	Analog supply (channel 0)	1.7 V	1.8 V	1.9 V
ADC_AVDD33	Analog supply (other channels)	2.85 V	3.0 V	3.6 V
IVDDA	Operating current (Fclk = 5 MHz and Fs = 1 MS/s)		4 mA	
VREF	Reference Voltage (Top) (Low reference is ADC_AVSS)	ADC_AVDD	ADC_AVDD	ADC_AVDD
VIN	Analog input voltage	ADC_AVSS		VREF
N	Resolution		12 bits	
INL	INL		±1 LSB	±4 LSB
DNL	DNL		±0.5 LSB	±1 LSB

Table 4-11. ADC DC Specification.

4.3.7.2 ADC Electrical: AC Specification

Parameter	Comments	Minimum	Typical	Maximum
Fs	Sampling rate	50 K		1 MS/s
FCLK	Sampling clock	300 K		6 MHz
SNDR	Signal-to-noise and distortion ratio (Fclk = 5 MHz and AIN = 50 KHz*)	54 dB	60 dB	

Table 4-12. ADC AC Specification.

4.3.8 Operating Conditions: Crystal and Reference Clock Requirements

4.3.8.1 Crystal and Reference Clock Requirements: 24 or 48 MHz

Description	Minimum	Typical	Maximum
Crystal frequency	N/A	24 or 48 MHz only	N/A
Crystal accuracy			± 30 PPM
Cycle-to-cycle jitter			± 200 ps
Long-term jitter			± 500 ps

Table 4-13. Jitter Specifications (24 or 48 MHz).

4.3.8.2 Crystal and Reference Clock Requirements: 32.768 KHz

Description	Minimum	Typical	Maximum
Crystal accuracy			± 30 PPM

Table 4-14. Jitter Specifications (32.768 KHz).

4.4 Electrical: Fail-Safe Pins

The A12A55 chip provides a number of fail-safe CMOS pins that can have active signals at or below 3.6 V when the A12A55 is powered down. For fail-safe pin locations, please refer to Chapter 7.

Pin Name	Multiplexed Function					
	First	Second	Third	Fourth	Fifth	GPIO
GPIO_0	sd_hs_sel					0
GPIO_1	ehci_app_prt_ovcurr0	uart_ahb_rx	ssis_sclk	sc_c0		1
GPIO_2	ehci_app_prt_ovcurr1	uart_ahb_tx	ssis_rxd	sc_c1		2
GPIO_3	ehci_prt_pwr_0	uart_ahb_cts_n	ssis_txd	sc_c2		3
GPIO_4	ehci_prt_pwr_1	uart_ahb_rts_n	ssis_en	sc_c3		4
GPIO_5	pwm_1	idsp_pip_iopad_master_hsync	vin_strig0	sc_d0	uart_ahb_cts_n	5
GPIO_6	pwm_2	idsp_pip_iopad_master_vsync	vin_strig1	sc_d1	uart_ahb_rts_n	6
SC_A0	sc_a0	ssi1_sclk	norspi_clk	pwm_0	sdxc_cmd	7
SC_A1	sc_a1	ssi1_txd	norspi_dq[0]	pwm_1	sdxc_cd	8
SC_A2	sc_a2	ssi1_rxd	norspi_dq[1]	pwm_2	sdxc_wp	9
SC_A3	sc_a3	ssi1_en0	norspi_dq[2]	pwm_3	sdxc_d[0]	10
SC_B0	sc_b0	ssi1_en1	norspi_dq[3]		sdxc_d[1]	11
SC_B1	sc_b1	ssi1_en2	norspi_en[0]	norspi_dq[2]	sdxc_d[2]	12
SC_B2	sc_b2	ssi1_en3	norspi_en[1]	norspi_dq[3]	sdxc_d[3]	13
SC_B3	sc_b3	pwm_3	norspi_en[2]		sdxc_d[4]	14
SC_C0	sc_c0	uart_ahb_rx	ssis_sclk		sdxc_d[5]	15
SC_C1	sc_c1	uart_ahb_tx	ssis_rxd	enet_crs	sdxc_d[6]	16
SC_C2	sc_c2	uart_ahb_cts_n	ssis_txd	enet_rxd_2	sdxc_d[7]	17
SC_C3	sc_c3	uart_ahb_rts_n	ssis_en	enet_rxd_3	sdxc_clk	18
SC_D0	sc_d0	uart_ahb_rx	ssis_sclk	enet_col	pwm_0	19

Pin Name	Multiplexed Function					
	First	Second	Third	Fourth	Fifth	GPIO
SC_D1	sc_d1	uart_ahb_tx	ssis_rxd	enet_tx_clk	pwm_1	20
SC_D2	sc_d2	uart_ahb_cts_n	ssis_txd	enet_tx_er	pwm_2	21
SC_D3	sc_d3	uart_ahb_rts_n	ssis_en	enet_txd_2	pwm_3	22
SC_E0	sc_e0	ssi0_en2	norspi_en[3]	enet_txd_3	pwm_1	23
TIMER0	tm11_clk			enet_2nd_ref_clk		24
TIMER1	tm12_clk		idsp_pip_iopad_master_hsync	enet_mdc		25
TIMER2	tm13_clk	ssi0_en3	idsp_pip_iopad_master_vsync	enet_mdio		26
IDCCLK	idc0clk					27
IDCDATA	idc0data					28
IDC2CLK	idc1clk		norspi_dq[2]	norspi_en[2]		29
IDC2DATA	idc1data		norspi_dq[3]	norspi_en[3]		30
IDC3CLK	idc2clk	vin_strig0				31
IDC3DATA	idc2data	vin_strig1				32
IR_IN	ir_in					33
SSI0CLK	ssi0_sclk	norspi_clk	uart_ahb_rx	ssis_sclk		34
SSI0MOSI	ssi0_txd	norspi_dq[0]	uart_ahb_tx	ssis_rxd		35
SSI0MISO	ssi0_rxd	norspi_dq[1]	uart_ahb_cts_n	ssis_txd		36
SSI0EN0	ssi0_en0	norspi_en[0]	uart_ahb_rts_n	ssis_en		37
SSI0EN1	ssi0_en1	norspi_en[1]				38
UART0RX	uart0rx	uart_ahb_rx				39
UART0TX	uart0tx	uart_ahb_tx				40
I2S_CLK	i2s_clk					41
I2S_SI	i2s_si					42
I2S_SO	i2s_so					43
I2S_WS	i2s_ws					44
CLK_AU						45
WP		nand_wp				54
SMIO_0		nand_ce	norspi_clk			55
SMIO_2		sd_clk				57
SMIO_3		sd_cmd				58
SMIO_4		sd_cd				59
SMIO_5		sd_wp				60
SMIO_18		sd_d[0]				73
SMIO_19		sd_d[1]				74
SMIO_20		sd_d[2]				75
SMIO_21		sd_d[3]				76
SMIO_22		sd_d[4]		sc_c0	ssis_sclk	77
SMIO_23		sd_d[5]		sc_c1	ssis_rxd	78
SMIO_24		sd_d[6]		sc_c2	ssis_txd	79
SMIO_25		sd_d[7]		sc_c3	ssis_en	80
SMIO_26		sdio_clk				81
SMIO_27		sdio_cmd				82
SMIO_28		sdio_d[0]		sc_d0	ssis_sclk	83
SMIO_29		sdio_d[1]		sc_d1	ssis_rxd	84

Pin Name	Multiplexed Function					
	First	Second	Third	Fourth	Fifth	GPIO
SMIO_30		sdio_d[2]		sc_d2	ssis_txd	85
SMIO_31		sdio_d[3]		sc_d3	ssis_en	86
SMIO_32		sdio_cd				87
SMIO_33		sdio_wp				88
HPD	hdmitx_hpd					89
CEC	hdmitx_cec	enet_2nd_ref_clk				90
SVSYNC	vin_svsync	idsp_pip_iopad_master_hsync				91
SHSYNC	vin_shsync	idsp_pip_iopad_master_vsync				92
VD0_CLK	vd0_clk					109
VD_PWM	pwm_0					113
DETECT_VBUS						
JTAG_TDO						

Table 4-15. Fail-Safe Pins Which Can Have Active Signals At or Below 3.6 V When the A12A55 is Powered Down.

4.5 Electrical: Video Signal Wave Forms and Timing

4.5.1 Video Waveform: Video Input (VIN) LVCMOS Timing

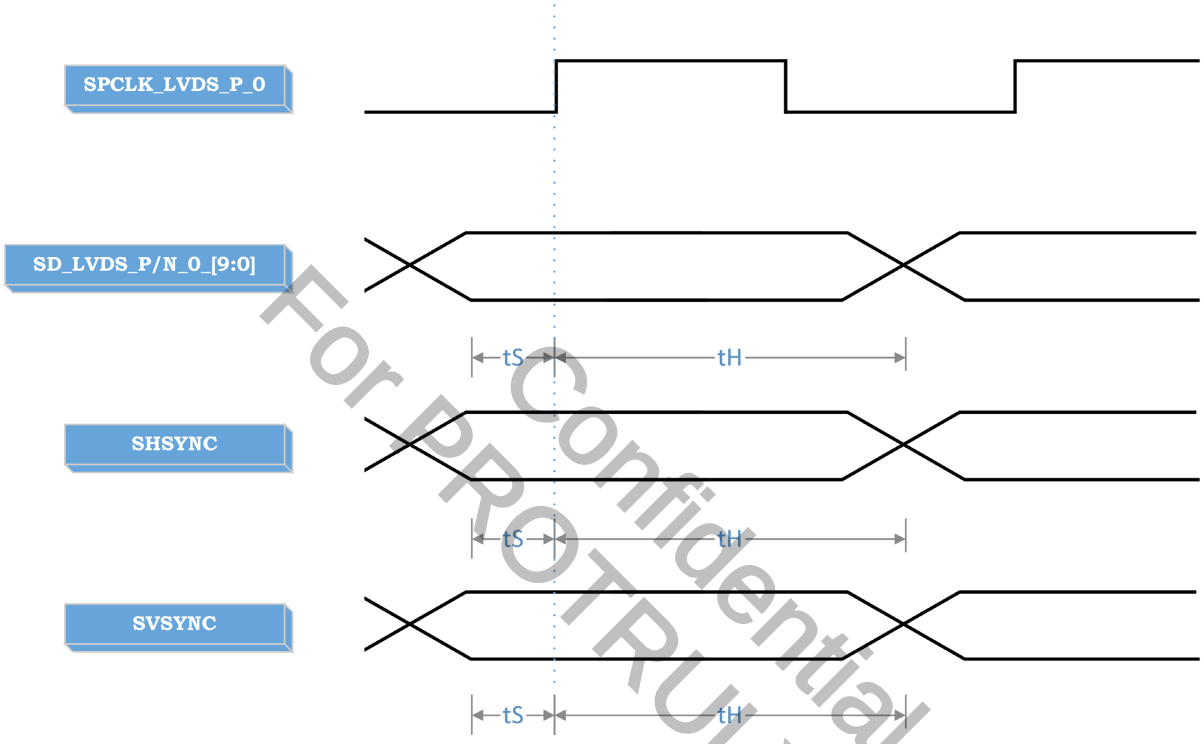


Figure 4-1. Video Input (VIN) LVCMOS Timing.

Parameter	Setup (tS)	Hold (tH)	Comment
Data: **SD_LVDS_P/N_0_[9:0]**	2 ns	2 ns	Assume the rising edge of the pixel clock **SPCLK_LVDS_P_0** is used to latch the data.
HSync: **SHSYNC**	2 ns	2 ns	
VSync: **SVSYNC**	2 ns	2 ns	
SField: (See Section 2.3)	2 ns	2 ns	

*Table 4-16. LVCMOS Video Input Timing Setup/Hold With Respect to **SPCLK_LVDS_P/N_[N]**.*

4.5.2 Video Waveform: Video Input (VIN) SLVS/MIPI Timing

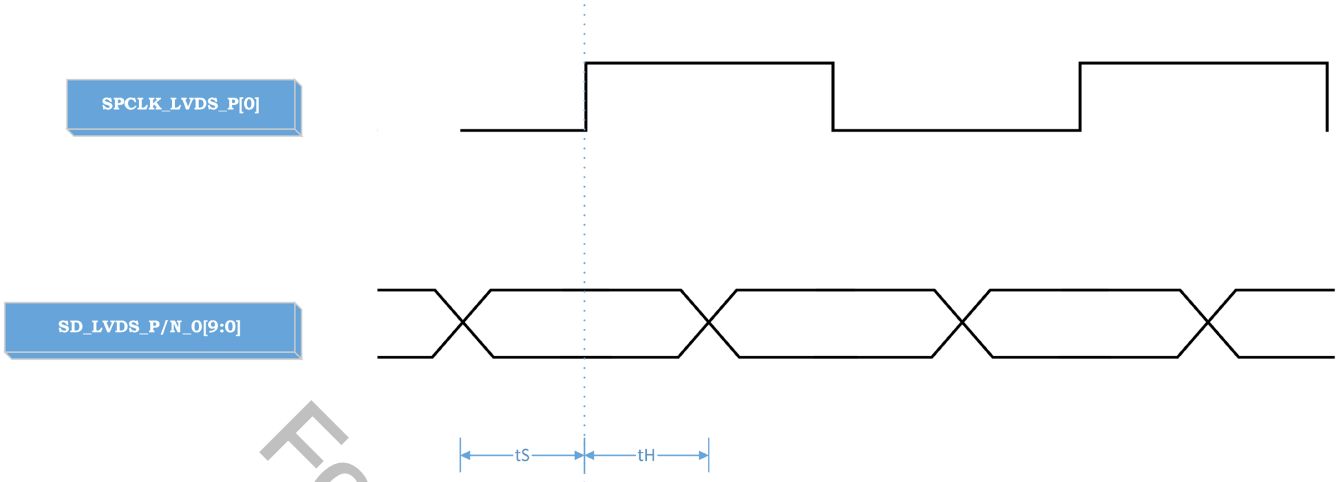


Figure 4-2. Video Input (VIN) SLVS/MIPI Timing.

Parameter	Setup (tS)	Hold (tH)	Comment
Data: **SD_LVDS_P/N_0_[9:0]**	150 ps	150 ps	Assume the rising edge of the pixel clock **SPCLK_LVDS_P[0]** is used to latch the data.

*Table 4-17. SLVS/MIPI Video Input Timing Setup/Hold With Respect to **SPCLK_LVDS_P/N_[N]**.*

4.5.3 Video Waveform: Video Output (VOUT) Timing

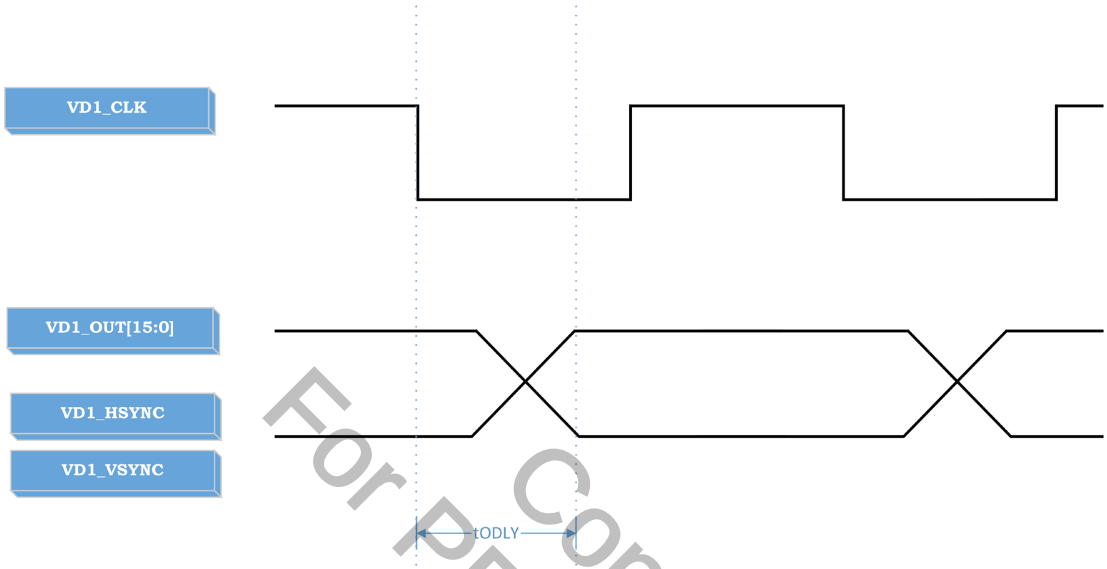


Figure 4-3. Video Output Timing.

Parameter	Minimum	Typical	Maximum	Comment
VD1_CLK Frequency		Resolution Dependent		Assume the data is latched out at the falling edge of **VD1_CLK**.
VD1_CLK Duty	40%	50%	60%	
tODLY Output Delay	-2 ns		2 ns	

*Table 4-18. Video Output Timing Setup/Hold With Respect to **VD1_CLK**.*

4.6 Electrical: SD Controller Timing

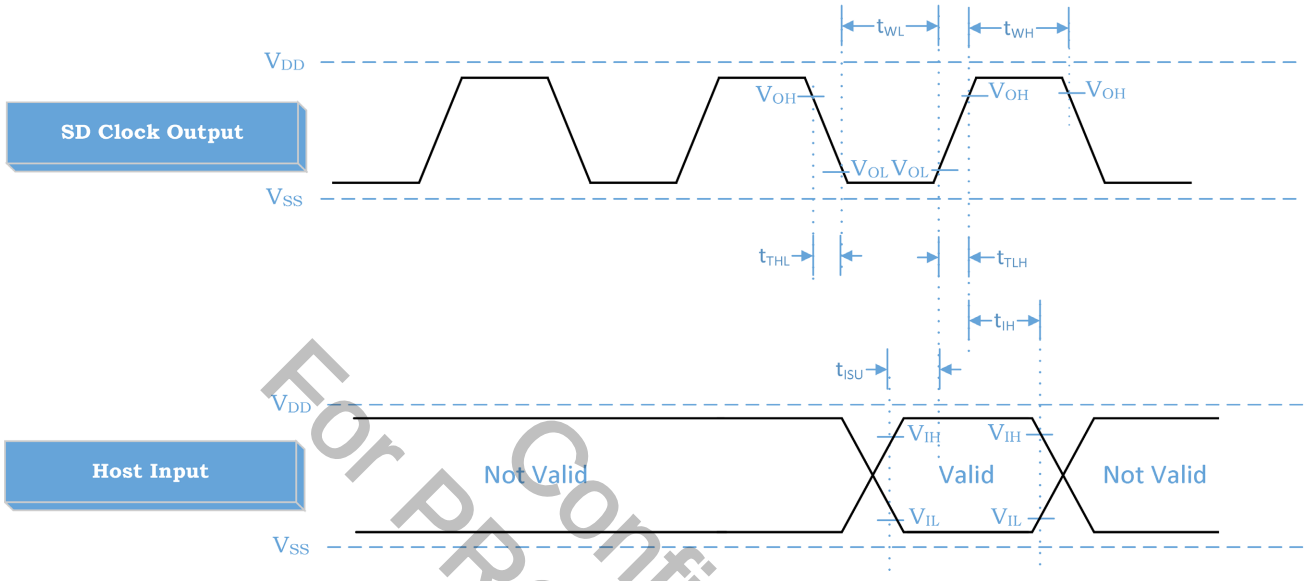


Figure 4-4. SD Host Input Timing.

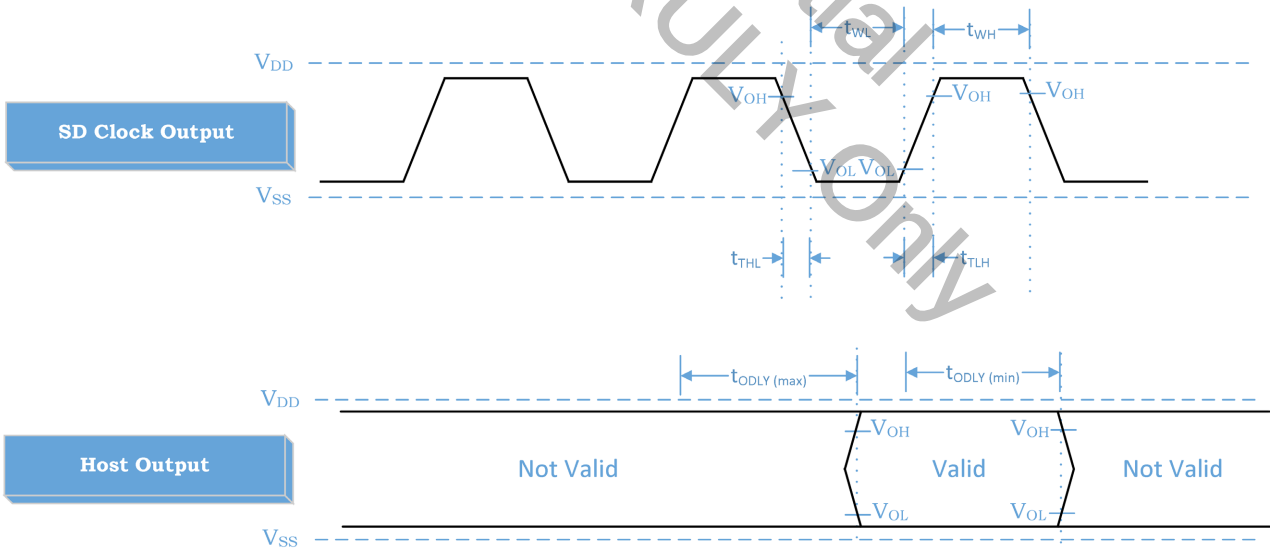


Figure 4-5. SD Host Output Timing.

Parameter	Symbol	Min	Max	Unit	Comment
Clock CLK: All values are referred to as min (VIH) and max (VIL)					
Clock Frequency: Data Transfer Mode	f_{PP}	0	48	MHz	C_{CARD} ≤ 10 pF (1 Card)
Clock Frequency: Identification Mode	f_{OD}	0/100	400	kHz	C_{CARD} ≤ 10 pF (1 Card)
Clock Low Time	t_{WL}	7		ns	C_{CARD} ≤ 10 pF (1 Card)
Clock High Time	t_{WH}	7		ns	C_{CARD} ≤ 10 pF (1 Card)
Clock Rise Time	t_{TLH}		3	ns	C_{CARD} ≤ 10 pF (1 Card)
Clock Fall Time	t_{THL}		3	ns	C_{CARD} ≤ 10 pF (1 Card)
Inputs CMD, DAT: Referenced to CLK					
Input Set-Up Time	t_{ISU}	5.83		ns	C_{CARD} ≤ 10 pF (1 Card)
Input Hold Time	t_{IH}	1.5		ns	C_{CARD} ≤ 10 pF (1 Card)
Outputs CMD, DAT: Referenced to CLK at 48 MHz					
Output Delay Time	t_{ODLY}	8.85	12.16	ns	C_L ≤ 40 pF (1 Card)

Table 4-19. SD Controller Timing Parameters.

4.7 Electrical: eMMC Boot Timing

To successfully boot from eMMC, the eMMC device should return boot data with the following timing constraints.

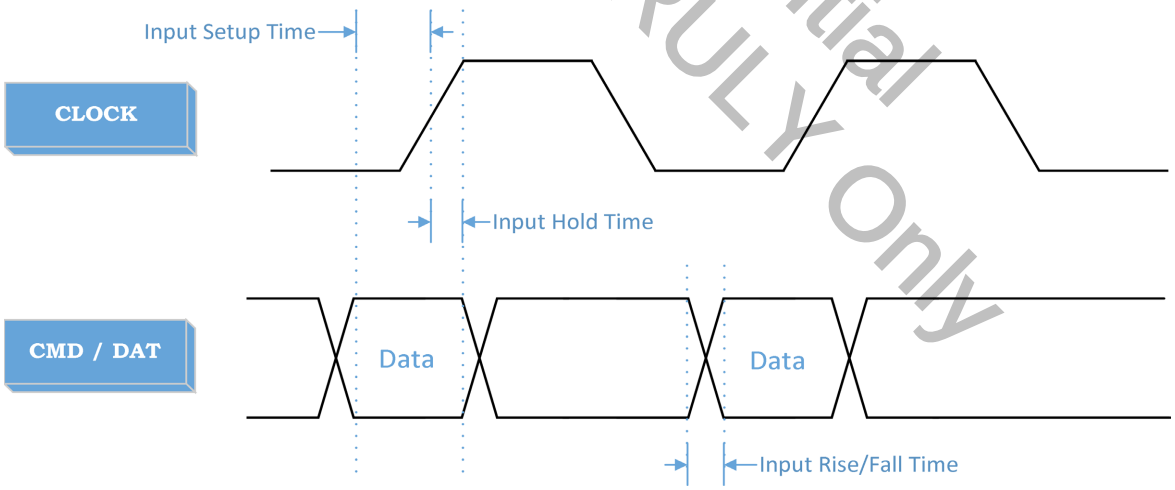


Figure 4-6. eMMC Boot Timing Diagram.

Parameter	Minimum	Maximum
Host CMD / DAT Input Timing		
Input Setup Time	5.83 ns	
Input Hold Time	1.5 ns	
Signal Rise Time		3 ns
Signal Fall Time		3 ns

Table 4-20. eMMC Boot Timing.

Note:

1. CMD / DAT input rise and fall time are measured by VIL and VIH.

5. PACKAGE

The A12A55 chip has a 404-pin LFBGA package (15 mm x 15 mm).

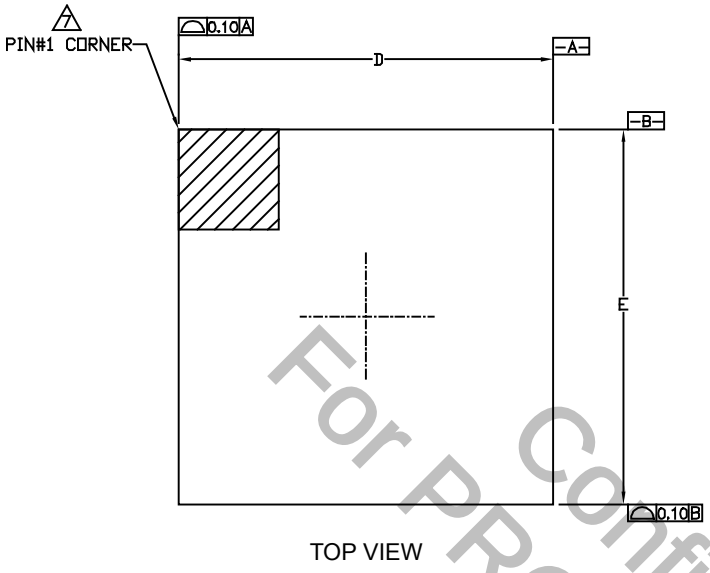


Figure 5-1. Top View of the A12A55 Package.

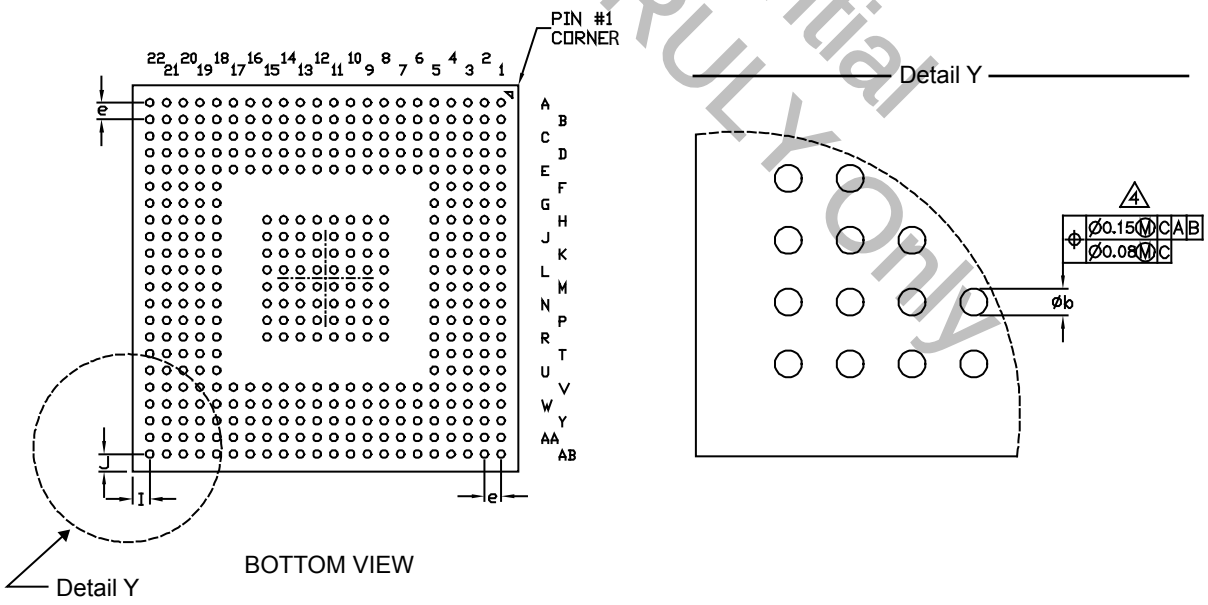


Figure 5-2. Bottom View of the A12A55 Package (left) with Detail Y (right).

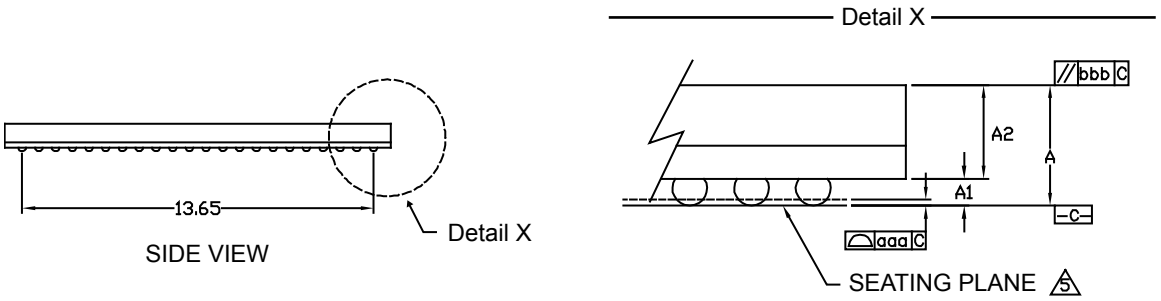


Figure 5-3. Side View of the A12A55 Package (left) with Detail X (right).

Dimension	Minimum	Nominal	Maximum
A			1.30
A1	0.18	0.23	0.28
A2	0.86	0.91	0.94
D	14.90	15.00	15.10
E	14.90	15.00	15.10
I		0.675 rEF.	
J		0.675 rEF.	
M		22 x 22 <Depopulated>	
aaa			0.10
bbb			0.10
b	0.25	0.30	0.35
e		0.65 TYP.	
Number of Balls: 404			

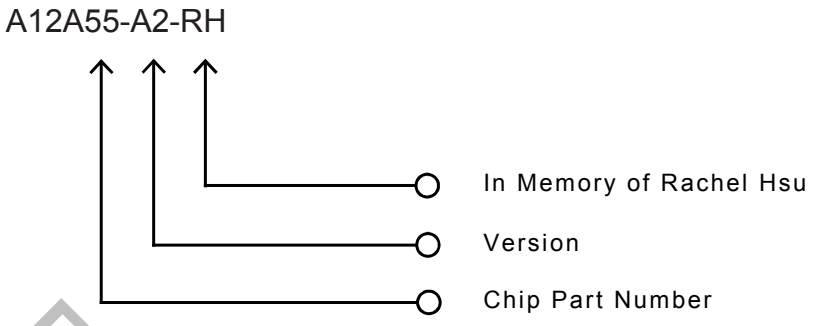
Table 5-1. Dimensions of the A12A55 Package (millimeters).

Notes for table and figures:

1. All dimensions are in millimeters.
2. Basic solder ball grid pitch (e).
3. Maximum solder ball grid size (M).
4. A1 corner must be delineated by ink or laser mark.
5. Package total height (A) tolerance must be in 1.14/+0.06 - 0.1 mm.

6. CONTACT AND ORDER INFORMATION

All chips in the A12 series are Lead-Free, Halogen-Free and RoHS compliant.



For complete Ambarella contact information, please visit www.ambarella.com.

7. PIN LIST AND MAPPING TABLE

This section provides a list of the 404 external pins according to their location on the A12A55 chip. Figure 7-1 below indicates the orientation of the pins by column (numbers) and row (letters).

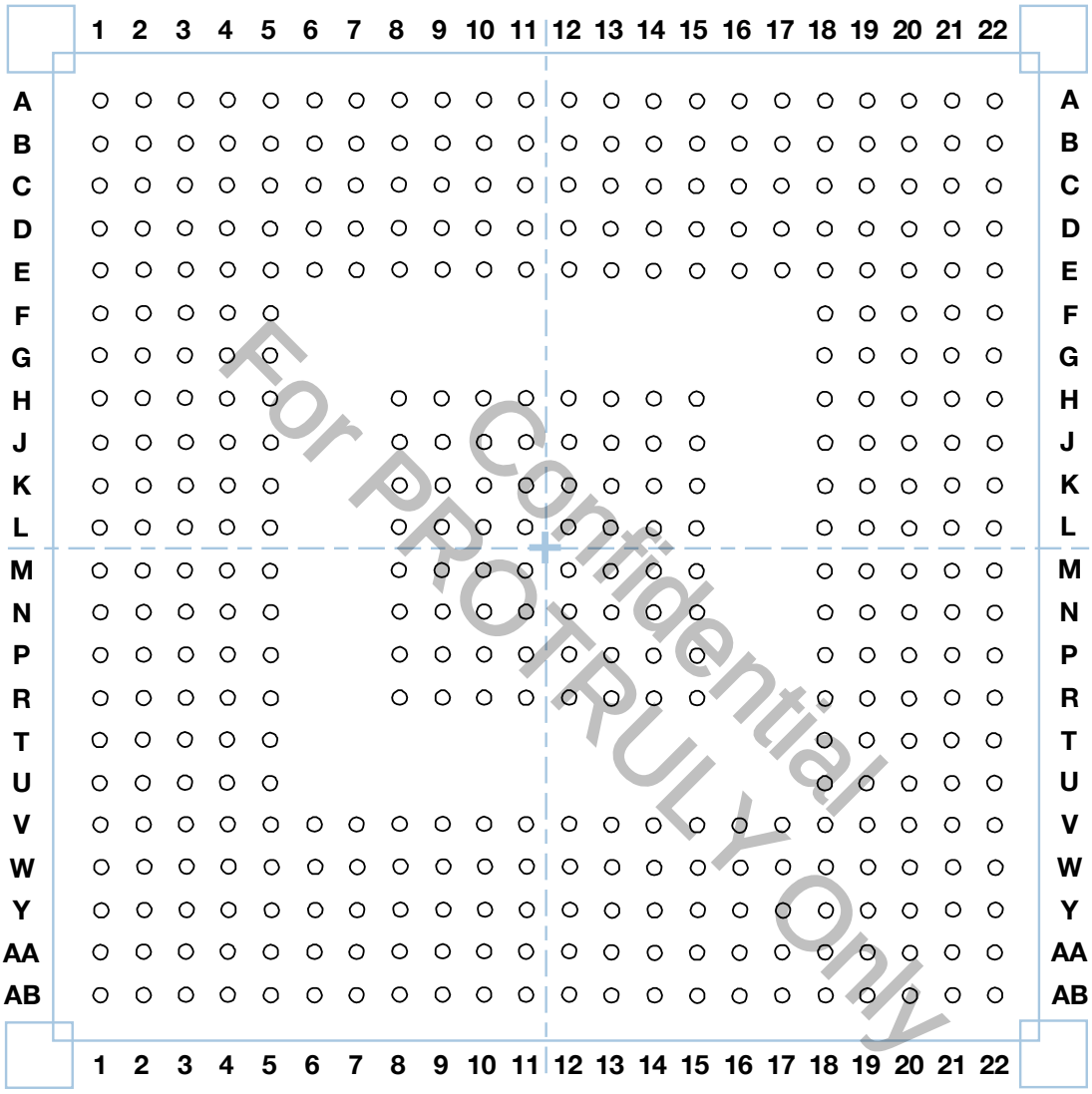


Figure 7-1. Pin Map for the A12A55 Chip.

The table below lists all of the external pins on the A12A55 chip in alphabetic order by map location. Each entry provides the pin name as it appears on the ball map, the location of the pin on the map and on schematics, the functional group, and multiplexed functionality detail if applicable.

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
A1	**PWC_PC_REF**	PWC	Analog						
A2	**XO_RTC**	Global	Analog						
A3	**PWC_RTC_CP**	PWC	CMOS						

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
A4	**PWC_PC_VDD**	Power	Supply						
A5	**PWC_RSTOB**	PWC	Analog						
A6	**DDR_CALIBR**	DDR2/3	Analog						
A7	**DDR_DQ_25**	DDR2/3	SSTL18						
A8	**DDR_DQS_BAR_3**	DDR2/3	SSTL18						
A9	**DDR_VREF_3**	Power	DDR HOST Supply						
A10	**DDR_DQ_19**	DDR2/3	SSTL18						
A11	**DDR_DQS_BAR_2**	DDR2/3	SSTL18						
A12	**DDR_DM_1**	DDR2/3	SSTL18						
A13	**DDR_DQS_BAR_1**	DDR2/3	SSTL18						
A14	**DDR_DQ_11**	DDR2/3	SSTL18						
A15	**DDR_VREF_2**	Power	DDR HOST Supply						
A16	**DDR_DQS_BAR_0**	DDR2/3	SSTL18						
A17	**DDR_DQ_3**	DDR2/3	SSTL18						
A18	**DDR_CK_BAR**	DDR2/3	SSTL18						
A19	**DDR_CKE**	DDR2/3	SSTL18						
A20	**DDR_CK_2_BAR**	DDR2/3	SSTL18						
A21	**DDR_ADDR_6**	DDR2/3	SSTL18						
A22	**DDR_ADDR_8**	DDR2/3	SSTL18						
B1	**JTAG_TDI**	JTAG	CMOS						
B2	**XI_RTC**	Global	Analog						
B3	**ADC_CH_2**	ADC	Analog						
B4	**ADC_CH_0**	ADC	Analog						
B5	**PWC_RSTINB**	PWC	Analog						
B6	**DDR_DQ_29**	DDR2/3	SSTL18						
B7	**DDR_DQ_26**	DDR2/3	SSTL18						
B8	**DDR_DQS_3**	DDR2/3	SSTL18						
B9	**DDR_DM_3**	DDR2/3	SSTL18						
B10	**DDR_DQ_18**	DDR2/3	SSTL18						
B11	**DDR_DQS_2**	DDR2/3	SSTL18						
B12	**DDR_DQ_15**	DDR2/3	SSTL18						
B13	**DDR_DQS_1**	DDR2/3	SSTL18						
B14	**DDR_DQ_10**	DDR2/3	SSTL18						
B15	**DDR_DM_0**	DDR2/3	SSTL18						
B16	**DDR_DQS_0**	DDR2/3	SSTL18						
B17	**DDR_DQ_2**	DDR2/3	SSTL18						
B18	**DDR_CK**	DDR2/3	SSTL18						
B19	**DDR_ADDR_10**	DDR2/3	SSTL18						
B20	**DDR_CK_2**	DDR2/3	SSTL18						
B21	**DDR_ADDR_4**	DDR2/3	SSTL18						

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
B22	**DDR_ADDR_11**	DDR2/3	SSTL18						
C1	**JTAG_CLK**	JTAG	CMOS						
C2	**JTAG_TMS**	JTAG	CMOS						
C3	**ADC_CH_3**	ADC	Analog						
C4	**ADC_CH_1**	ADC	Analog						
C5	**PWC_PSEQ2**	PWC	Analog						
C6	**DDR_DQ_30**	DDR2/3	SSTL18						
C7	**DDR_DQ_27**	DDR2/3	SSTL18						
C8	**DDR_DQ_22**	DDR2/3	SSTL18						
C9	**DDR_DQ_17**	DDR2/3	SSTL18						
C10	**DDR_DM_2**	DDR2/3	SSTL18						
C11	**DDR_DQ_20**	DDR2/3	SSTL18						
C12	**DDR_DQ_14**	DDR2/3	SSTL18						
C13	**DDR_DQ_13**	DDR2/3	SSTL18						
C14	**DDR_DQ_9**	DDR2/3	SSTL18						
C15	**DDR_DQ_7**	DDR2/3	SSTL18						
C16	**DDR_DQ_5**	DDR2/3	SSTL18						
C17	**DDR_DQ_1**	DDR2/3	SSTL18						
C18	**DDR_CAS**	DDR2/3	SSTL18						
C19	**DDR_WE**	DDR2/3	SSTL18						
C20	**DDR_BA_1**	DDR2/3	SSTL18						
C21	**DDR_ADDR_1**	DDR2/3	SSTL18						
C22	**DDR_ADDR_14**	DDR2/3	SSTL18						
D1	**JTAG_TDO**	JTAG	CMOS						
D2	**JTAG_RST_L**	JTAG	CMOS						
D3	**ADC_VSSA**	Power	Analog Ground						
D4	**PWC_PSEQ3**	PWC	Analog						
D5	**PWC_PSEQ1**	PWC	Analog						
D6	**DDR_DQ_31**	DDR2/3	SSTL18						
D7	**DDR_DQ_28**	DDR2/3	SSTL18						
D8	**DDR_DQ_24**	DDR2/3	SSTL18						
D9	**DDR_DQ_21**	DDR2/3	SSTL18						
D10	**DDR_DQ_23**	DDR2/3	SSTL18						
D11	**DDR_DQ_16**	DDR2/3	SSTL18						
D12	**DDR_VDDQ_D12**	Power	DDR HOST Supply						
D13	**DDR_DQ_12**	DDR2/3	SSTL18						
D14	**DDR_DQ_8**	DDR2/3	SSTL18						
D15	**DDR_DQ_6**	DDR2/3	SSTL18						
D16	**DDR_DQ_4**	DDR2/3	SSTL18						
D17	**DDR_DQ_0**	DDR2/3	SSTL18						
D18	**DDR_RAS**	DDR2/3	SSTL18						
D19	**DDR_BA_0**	DDR2/3	SSTL18						
D20	**DDR_CS_2**	DDR2/3	SSTL18						
D21	**DDR_ADDR_2**	DDR2/3	SSTL18						

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
D22	**DDR_ADDR_9**	DDR2/3	SSTL18						
E1	**DAC_COMP**	DAC	Analog						
E2	**DAC_VREFIN**	DAC	Analog						
E3	**VDAC_VSSA**	Power	Analog Ground						
E4	**VDAC_VDDA18**	Power	Analog Supply						
E5	**ADC_VDDA18**	Power	Analog Supply						
E6	**VSS_E6**	Power	Ground						
E7	**VSS_E7**	Power	Ground						
E8	**VSS_E8**	Power	Ground						
E9	**DDR_VDDQ_E9**	Power	DDR HOST Supply						
E10	**DDR_VDDQ_E10**	Power	DDR HOST Supply						
E11	**DDR_VDDQ_E11**	Power	DDR HOST Supply						
E12	**DDR_VDDQ_E12**	Power	DDR HOST Supply						
E13	**DDR_VDDQ_E13**	Power	DDR HOST Supply						
E14	**DDR_VDDQ_E14**	Power	DDR HOST Supply						
E15	**DDR_VDDQ_E15**	Power	DDR HOST Supply						
E16	**VSS_E16**	Power	Ground						
E17	**VSS_E17**	Power	Ground						
E18	**VSS_E18**	Power	Ground						
E19	**DDR_ADDR_15**	DDR2/3	SSTL18						
E20	**DDR_ADDR_12**	DDR2/3	SSTL18						
E21	**DDR_ADDR_0**	DDR2/3	SSTL18						
E22	**DDR_ADDR_13**	DDR2/3	SSTL18						
F1	**DAC_IO**	DAC	Analog						
F2	**VDAC_VDDA33**	Power	Analog Supply						
F3	**ADC_VDDA33**	Power	Analog Supply						
F4	**PWC_WKUP1**	PWC	Analog						
F5	**PWC_WKUP**	PWC	Analog						
F18	**VSS_F18**	Power	Ground						

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
F19	**DDR_CS**	DDR2/3	SSTL18						
F20	**DDR_BA_2**	DDR2/3	SSTL18						
F21	**DDR_ADDR_5**	DDR2/3	SSTL18						
F22	**DDR_ADDR_7**	DDR2/3	SSTL18						
G1	**DAC_RSET**	DAC	Analog						
G2	**GPIO_2**	GPIO	CMOS	ehci_ app_prt_ ovcurr1	uart_ahb_tx	ssis_rxd	sc_c1		2
G3	**GPIO_4**	GPIO	CMOS	ehci_prt_ pwr_1	uart_ahb_ rts_n	ssis_en	sc_c3		4
G4	**GPIO_5**	GPIO	CMOS	pwm_1	idsp_pip_io-pad_mas-ter_hsync	vin_strig0	sc_d0	uart_ahb_ cts_n	5
G5	**VDDA18_PLL**	Power	Analog Supply						
G18	**VSS_G18**	Power	Ground						
G19	**DDR_ODT**	DDR2/3	SSTL18						
G20	**DDR_VDDQ_CKE**	DDR2/3	SSTL18	Tied to Internal DDR_CK-EIN					
G21	**DDR_ADDR_3**	DDR2/3	SSTL18						
G22	**DDR_RESET**	DDR2/3	SSTL18						
H1	**XIN**	Global	XOSC						
H2	**GPIO_1**	GPIO	CMOS	ehci_ app_prt_ ovcurr0	uart_ahb_rx	ssis_sclk	sc_c0		1
H3	**GPIO_3**	GPIO	CMOS	ehci_prt_ pwr_0	uart_ahb_ cts_n	ssis_txd	sc_c2		3
H4	**GPIO_6**	GPIO	CMOS	pwm_2	idsp_pip_io-pad_mas-ter_vsync	vin_strig1	sc_d1	uart_ahb_ rts_n	6
H5	**PLL_VSSA_H5**	Power	Analog Ground						
H8	**DDR_VDDQ_H8**	Power	DDR HOST Supply						
H9	**DDR_VDDQ_H9**	Power	DDR HOST Supply						
H10	**DDR_VDDQ_H10**	Power	DDR HOST Supply						
H11	**DDR_VDDQ_H11**	Power	DDR HOST Supply						
H12	**DDR_VDDQ_H12**	Power	DDR HOST Supply						

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
H13	**DDR_VDDQ_H13**	Power	DDR HOST Supply						
H14	**DDR_VDDQ_H14**	Power	DDR HOST Supply						
H15	**DDR_VDDQ_H15**	Power	DDR HOST Supply						
H18	**NAND_VDDO_H18**	Power	Digital Supply						
H19	**NAND_VDDO_H19**	Power	Digital Supply						
H20	**SMIO_25**	SMIO	CMOS		sd_d[7]		sc_c3	ssis_en	80
H21	**SMIO_21**	SMIO	CMOS		sd_d[3]				76
H22	**SMIO_2**	SMIO	CMOS		sd_clk				57
J1	**XOUT**	Global	XOSC						
J2	**GPIO_0**	GPIO	CMOS	sd_hs_sel					0
J3	**HDMI_VSSA_J3**	Power	Analog Ground						
J4	**HDMI_VDDA_J4**	Power	Analog Supply						
J5	**PLL_VSSA_J5**	Power	Analog Ground						
J8	**VSS_J8**	Power	Ground						
J9	**VSS_J9**	Power	Ground						
J10	**VSS_J10**	Power	Ground						
J11	**VSS_J11**	Power	Ground						
J12	**VSS_J12**	Power	Ground						
J13	**VSS_J13**	Power	Ground						
J14	**VSS_J14**	Power	Ground						
J15	**VSS_J15**	Power	Ground						
J18	**SDIO_VDDO_J18**	Power	Digital Supply						
J19	**SDIO_VDDO_J19**	Power	Digital Supply						
J20	**SMIO_22**	SMIO	CMOS		sd_d[4]		sc_c0	ssis_sclk	77
J21	**SMIO_20**	SMIO	CMOS		sd_d[2]				75
J22	**SMIO_3**	SMIO	CMOS		sd_cmd				58
K1	**HDMI_REXT**	HDMI	Analog						
K2	**HPD**	HDMI	CMOS	hdmitx_hpd					89
K3	**HDMI_VSSA_K3**	Power	Analog Ground						
K4	**HDMI_VDDA**	Power	Analog Supply						
K5	**VDDA10_PLL_K5**	Power	Analog Supply						

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
K8	**VSS_K8**	Power	Ground						
K9	**VSS_K9**	Power	Ground						
K10	**VSS_K10**	Power	Ground						
K11	**VSS_K11**	Power	Ground						
K12	**VSS_K12**	Power	Ground						
K13	**VSS_K13**	Power	Ground						
K14	**VSS_K14**	Power	Ground						
K15	**VSS_K15**	Power	Ground						
K18	**VDD33_K18**	Power	Digital Supply						
K19	**FSOURCE_0**	Global	Supply/ Ground						
K20	**SMIO_23**	SMIO	CMOS		sd_d[5]		sc_c1	ssis_rxd	78
K21	**SMIO_19**	SMIO	CMOS		sd_d[1]				74
K22	**SMIO_5**	SMIO	CMOS		sd_wp				60
L1	**HDMI_CLK_P**	HDMI	Analog						
L2	**HDMI_CLK_M**	HDMI	Analog						
L3	**HDMI_AVDD25**	Power	Analog Supply						
L4	**HDMI_ AVDDFLESD**	Power	Analog Supply						
L5	**VDDA10_PLL_L5**	Power	Analog Supply						
L8	**VSS_L8**	Power	Ground						
L9	**VSS_L9**	Power	Ground						
L10	**VSS_L10**	Power	Ground						
L11	**VSS_L11**	Power	Ground						
L12	**VSS_L12**	Power	Ground						
L13	**VSS_L13**	Power	Ground						
L14	**VSS_L14**	Power	Ground						
L15	**VSS_L15**	Power	Ground						
L18	**VDD33_L18**	Power	Digital Supply						
L19	**SMIO_24**	SMIO	CMOS		sd_d[6]		sc_c2	ssis_txd	79
L20	**SMIO_13**	SMIO	CMOS		nand_d[4]	norspi_dq[0]			68
L21	**SMIO_14**	SMIO	CMOS		nand_d[5]	norspi_dq[1]			69
L22	**SMIO_15**	SMIO	CMOS		nand_d[6]	norspi_dq[2]			70
M1	**HDMI_CH0_P**	HDMI	Analog						
M2	**HDMI_CH0_M**	HDMI	Analog						
M3	**HDMI_VDD10_ M3**	Power	Digital Supply						
M4	**HDMI_VDD10_ M4**	Power	Digital Supply						
M5	**CLK_AU**	GPIO	CMOS						45
M8	**VSS_M8**	Power	Ground						
M9	**VDD_M9**	Power	Digital Supply						

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
M10	**VDD_M10**	Power	Digital Supply						
M11	**VDD_M11**	Power	Digital Supply						
M12	**VDD_M12**	Power	Digital Supply						
M13	**VDD_M13**	Power	Digital Supply						
M14	**VDD_M14**	Power	Digital Supply						
M15	**VSS_M15**	Power	Ground						
M18	**SD_VDDO_M18**	Power	Digital Supply						
M19	**SMIO_26**	SMIO	CMOS		sdio_clk				81
M20	**SMIO_12**	SMIO	CMOS		nand_d[3]	norspi_en[3]			67
M21	**SMIO_10**	SMIO	CMOS		nand_d[1]	norspi_en[1]			65
M22	**SMIO_4**	SMIO	CMOS		sd_cd				59
N1	**HDMI_CH1_P**	HDMI	Analog						
N2	**HDMI_CH1_M**	HDMI	Analog						
N3	**SC_A0**	GPIO	CMOS	sc_a0	ssi1_sclk	norspi_clk	pwm_0	sdxc_cmd	7
N4	**SC_A1**	GPIO	CMOS	sc_a1	ssi1_txd	norspi_dq[0]	pwm_1	sdxc_cd	8
N5	**CLK_SI**	Sensor	CMOS						
N8	**VSS_N8**	Power	Ground						
N9	**VDD_N9**	Power	Digital Supply						
N10	**VDD_N10**	Power	Digital Supply						
N11	**VDD_N11**	Power	Digital Supply						
N12	**VDD_N12**	Power	Digital Supply						
N13	**VDD_N13**	Power	Digital Supply						
N14	**VDD_N14**	Power	Digital Supply						
N15	**VSS_N15**	Power	Ground						
N18	**SD_VDDO_N18**	Power	Digital Supply						
N19	**SMIO_27**	SMIO	CMOS		sdio_cmd				82
N20	**SMIO_11**	SMIO	CMOS		nand_d[2]	norspi_en[2]			66
N21	**SMIO_9**	SMIO	CMOS		nand_d[0]	norspi_en[0]			64
N22	**SMIO_1**	SMIO	CMOS		nand_rb	norspi_dq[4]			56
P1	**HDMI_CH2_P**	HDMI	Analog						
P2	**HDMI_CH2_M**	HDMI	Analog						
P3	**SC_A2**	GPIO	CMOS	sc_a2	ssi1_rxd	norspi_dq[1]	pwm_2	sdxc_wp	9
P4	**SC_A3**	GPIO	CMOS	sc_a3	ssi1_en0	norspi_dq[2]	pwm_3	sdxc_d[0]	10
P5	**SC_B0**	GPIO	CMOS	sc_b0	ssi1_en1	norspi_dq[3]		sdxc_d[1]	11
P8	**VSS_P8**	Power	Ground						

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
P9	**VDD_P9**	Power	Digital Supply						
P10	**VDD_P10**	Power	Digital Supply						
P11	**VDD_P11**	Power	Digital Supply						
P12	**VDD_P12**	Power	Digital Supply						
P13	**VDD_P13**	Power	Digital Supply						
P14	**VDD_P14**	Power	Digital Supply						
P15	**VSS_P15**	Power	Ground						
P18	**VDDP18_P18**	Power	Digital Supply						
P19	**SMIO_28**	SMIO	CMOS		sdio_d[0]		sc_d0	ssis_sclk	83
P20	**SMIO_16**	SMIO	CMOS		nand_d[7]	norspi_dq[3]			71
P21	**SMIO_18**	SMIO	CMOS		sd_d[0]				73
P22	**SMIO_0**	SMIO	CMOS		nand_ce	norspi_clk			55
R1	**SC_C1**	GPIO	CMOS	sc_c1	uart_ahb_tx	ssis_rxd	enet_crs	sdxc_d[6]	16
R2	**SC_C0**	GPIO	CMOS	sc_c0	uart_ahb_rx	ssis_sclk		sdxc_d[5]	15
R3	**SC_E0**	GPIO	CMOS	sc_e0	ssi0_en2	norspi_en[3]	enet_txd_3	pwm_1	23
R4	**SC_B2**	GPIO	CMOS	sc_b2	ssi1_en3	norspi_en[1]	norspi_dq[3]	sdxc_d[3]	13
R5	**SC_B1**	GPIO	CMOS	sc_b1	ssi1_en2	norspi_en[0]	norspi_dq[2]	sdxc_d[2]	12
R8	**VSS_R8**	Power	Ground						
R9	**VDD_R9**	Power	Digital Supply						
R10	**VDD_R10**	Power	Digital Supply						
R11	**VDD_R11**	Power	Digital Supply						
R12	**VDD_R12**	Power	Digital Supply						
R13	**VDD_R13**	Power	Digital Supply						
R14	**VDD_R14**	Power	Digital Supply						
R15	**VSS_R15**	Power	Ground						
R18	**VDDP18_R18**	Power	Digital Supply						
R19	**SMIO_29**	SMIO	CMOS		sdio_d[1]		sc_d1	ssis_rxd	84
R20	**SMIO_17**	SMIO	CMOS		nand_cle				72
R21	**SMIO_7**	SMIO	CMOS		nand_we	norspi_dq[6]			62
R22	**SMIO_6**	SMIO	CMOS		nand_re	norspi_dq[5]			61
T1	**SC_C2**	GPIO	CMOS	sc_c2	uart_ahb_cts_n	ssis_txd	enet_rxd_2	sdxc_d[7]	17

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
T2	**SC_C3**	GPIO	CMOS	sc_c3	uart_ahb_ rts_n	ssis_en	enet_rxd_3	sdxc_clk	18
T3	**SC_D0**	GPIO	CMOS	sc_d0	uart_ahb_rx	ssis_sclk	enet_col	pwm_0	19
T4	**SC_D1**	GPIO	CMOS	sc_d1	uart_ahb_tx	ssis_rxd	enet_tx_clk	pwm_1	20
T5	**SC_B3**	GPIO	CMOS	sc_b3	pwm_3	norspi_en[2]		sdxc_d[4]	14
T18	**VDDP18_T18**	Power	Digital Supply						
T19	**SMIO_33**	SMIO	CMOS		sdio_wp				88
T20	**SMIO_8**	SMIO	CMOS		nand_ale	norspi_dq[7]			63
T21	**SMIO_31**	SMIO	CMOS		sdio_d[3]		sc_d3	ssis_en	86
T22	**SMIO_30**	SMIO	CMOS		sdio_d[2]		sc_d2	ssis_txd	85
U1	**I2S_CLK**	I2S	CMOS	i2s_clk					41
U2	**TIMER0**	GPIO	CMOS	tm11_clk			enet_2nd_ ref_clk		24
U3	**TIMER2**	GPIO	CMOS	tm13_clk	ssi0_en3	idsp_pip_io- pad_mas- ter_vsync	enet_mdio		26
U4	**SC_D3**	GPIO	CMOS	sc_d3	uart_ahb_ rts_n	ssis_en	enet_txd_2	pwm_3	22
U5	**SC_D2**	GPIO	CMOS	sc_d2	uart_ahb_ cts_n	ssis_txd	enet_tx_er	pwm_2	21
U18	**VD0_OUT_8**	VOUT	CMOS	vd0_ out[8]					101
U19	**VD0_OUT_0**	VOUT	CMOS	vd0_ out[0]					93
U20	**SMIO_32**	SMIO	CMOS		sdio_cd				87
U21	**VD0_OUT_11**	VOUT	CMOS	vd0_ out[11]					104
U22	**VD0_OUT_15**	VOUT	CMOS	vd0_ out[15]					108
V1	**I2S_WS**	I2S	CMOS	i2s_ws					44
V2	**I2S_SO**	I2S	CMOS	i2s_so					43
V3	**TIMER1**	GPIO	CMOS	tm12_clk		idsp_pip_io- pad_mas- ter_hsync	enet_mdc		25
V4	**IDC3CLK**	I2C/IDC	CMOS	idc2clk		vin_strig0			31
V5	**WP**	GPIO	CMOS		nand_wp				54
V6	**IR_IN**	IR	CMOS	ir_in					33
V7	**UART0RX**	GPIO	CMOS	uart0rx	uart_ahb_rx				39
V8	**POR_L**	Global	CMOS						
V9	**LVDS_VDDA11**	Power	Analog Supply						
V10	**VDDP18_V10**	Power	Digital Supply						
V11	**VDDP18_V11**	Power	Digital Supply						
V12	**VDD33_V12**	Power	Digital Supply						
V13	**VDD33_V13**	Power	Digital Supply						

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
V14	**VDD33_V14**	Power	Digital Supply						
V15	**VDD33_V15**	Power	Digital Supply						
V16	**VD0_OUT_4**	VOUT	CMOS	vd0_ out[4]					97
V17	**VD0_OUT_13**	VOUT	CMOS	vd0_ out[13]					106
V18	**VD0_CLK**	VOUT	CMOS	vd0_clk					109
V19	**VD0_OUT_12**	VOUT	CMOS	vd0_ out[12]					105
V20	**VD0_OUT_7**	VOUT	CMOS	vd0_ out[7]					100
V21	**VD0_OUT_9**	VOUT	CMOS	vd0_ out[9]					102
V22	**VD0_HVLD**	VOUT	CMOS	vd0_hvld					112
W1	**I2S_SI**	I2S	CMOS	i2s_si					42
W2	**SSI0MISO**	GPIO	CMOS	ssi0_rxd	norspi_dq[1]	uart_ahb_ cts_n	ssis_txd		36
W3	**IDCDATA**	I2C/IDC	CMOS	idc0data					28
W4	**IDC3DATA**	I2C/IDC	CMOS	idc2data	vin_strig1				32
W5	**CEC**	HDMI	CMOS	hdmitx_ cec	enet_2nd_ ref_clk				90
W6	**DETECT_VBUS**	USB	CMOS						
W7	**UART0TX**	GPIO	CMOS	uart0tx	uart_ahb_tx				40
W8	**LVDS_VDDA18_ W8**	Power	Analog Supply						
W9	**LVDS_VDDA18_ W9**	Power	Analog Supply						
W10	**VDDP18_W10**	Power	Digital Supply						
W11	**VDDP18_W11**	Power	Digital Supply						
W12	**VDD33_W12**	Power	Digital Supply						
W13	**VDD33_W13**	Power	Digital Supply						
W14	**VDD33_W14**	Power	Digital Supply						
W15	**VDD33_W15**	Power	Digital Supply						
W16	**VD0_OUT_2**	VOUT	CMOS	vd0_ out[2]					95
W17	**VD0_HSYNC**	VOUT	CMOS	vd0_ hsync					111
W18	**VD0_OUT_1**	VOUT	CMOS	vd0_ out[1]					94
W19	**VD0_VSYNC**	VOUT	CMOS	vd0_ vsync					110
W20	**VD0_OUT_10**	VOUT	CMOS	vd0_ out[10]					103

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
W21	**TEST_MODE**	Global	CMOS						
W22	**VD_PWM**	GPIO	CMOS	pwm_0					113
Y1			Reserved						
Y1	**SSI0CLK**	GPIO	CMOS	ssi0_sclk	norspi_clk	uart_ahb_rx	ssis_sclk		34
Y2	**SSI0MOSI**	GPIO	CMOS	ssi0_txd	norspi_dq[0]	uart_ahb_tx	ssis_rxd		35
Y3	**IDCCLK**	I2C/IDC	CMOS	idc0_clk					27
Y4	**USB_VDDA33_Y4**	Power	Analog Supply						
Y5	**USB_VDDA33_Y5**	Power	Analog Supply						
Y6	**USB1_REXT**	USB	Analog						
Y7	**USB_VSSA_Y7**	Power	Analog Ground						
Y8	**USB_VSSA_Y8**	Power	Analog Ground						
Y9	**LVDS_VSSA_Y9**	Power	Analog Ground						
Y10	**LVDS_VSSA_Y10**	Power	Analog Ground						
Y11	**VSS_Y11**	Power	Ground						
Y12	**VSS_Y12**	Power	Ground						
Y13	**VSS_Y13**	Power	Ground						
Y14	**VSS_Y14**	Power	Ground						
Y15	**SHSYNC**	Sensor	CMOS	vin_shsync	idsp_pip_io-pad_mas-ter_vsync				92
Y16	**SVSYNC**	Sensor	CMOS	vin_svsync	idsp_pip_io-pad_mas-ter_hsync				91
Y17	**VD0_OUT_3**	VOUT	CMOS	vd0_out[3]					96
Y18	**VD0_OUT_5**	VOUT	CMOS	vd0_out[5]					98
Y19	**VD0_OUT_14**	VOUT	CMOS	vd0_out[14]					107
Y20	**VD0_OUT_6**	VOUT	CMOS	vd0_out[6]					99
Y21	**ENET_TXEN**	ENET	CMOS	enet_txen	sc_a0	enet_txen	ssi1_sclk	norspi_clk	46
Y22	**ENET_REF_CLK**	ENET	CMOS	enet_ref_clk	sc_b3	enet_rx_clk		norspi_dq[3]	53
AA1	**SSI0EN1**	GPIO	CMOS	ssio_en1	norspi_en[1]				38
AA2	**IDC2CLK**	I2C/IDC	CMOS	idc1_clk		norspi_dq[2]	norspi_en[2]		29
AA3	**USB_VDDA18_AA3**	Power	Analog Supply						
AA4	**USB0_REXT**	USB	Analog						
AA5	**USB0_DM**	USB	Analog						
AA6	**USB1_DM**	USB	Analog						

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
AA7	**SPCLK_ LVDS_N_2**	Sensor	Sub-LVDS/ SLVS/ LVCMOS/ MIPI						
AA8	**SD_LVDS_N_8**	Sensor	Sub-LVDS/ SLVS/ LVCMOS/ MIPI						
AA9	**SD_LVDS_N_9**	Sensor	Sub-LVDS/ SLVS/ LVCMOS/ MIPI						
AA10	**SD_LVDS_N_3**	Sensor	Sub-LVDS/ SLVS/ LVCMOS/ MIPI						
AA11	**SD_LVDS_N_2**	Sensor	Sub-LVDS/ SLVS/ LVCMOS/ MIPI						
AA12	**SD_LVDS_N_1**	Sensor	Sub-LVDS/ SLVS/ LVCMOS/ MIPI						
AA13	**SD_LVDS_N_0**	Sensor	Sub-LVDS/ SLVS/ LVCMOS/ MIPI						
AA14	**SPCLK_ LVDS_N_0**	Sensor	Sub-LVDS/ SLVS/ LVCMOS/ MIPI						
AA15	**SD_LVDS_N_7**	Sensor	Sub-LVDS/ SLVS/ LVCMOS/ MIPI						
AA16	**SD_LVDS_N_6**	Sensor	Sub-LVDS/ SLVS/ LVCMOS/ MIPI						
AA17	**SD_LVDS_N_5**	Sensor	Sub-LVDS/ SLVS/ LVCMOS/ MIPI						

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
AA18	**SD_LVDS_N_4**	Sensor	Sub-LVDS/ SLVS/ LVCMOS/ MIPI						
AA19	**SPCLK_ LVDS_N_1**	Sensor	Sub-LVDS/ SLVS/ LVCMOS/ MIPI						
AA20	**ENET_CRS_DV**	ENET	CMOS	enet_crs_ dv	sc_b2	enet_crs_dv	ssi1_en3	norspi_dq[2]	52
AA21	**ENET_TXD_1**	ENET	CMOS	enet_ txd_1	sc_a2	enet_txd_1	ssi1_rxd	norspi_dq[1]	48
AA22	**ENET_RXD_1**	ENET	CMOS	enet_ rxd_1	sc_b0	enet_rxd_1	ssi1_en1	norspi_en[1]	50
AB1	**SSI0EN0**	GPIO	CMOS	ssi0_en0	norspi_en[0]	uart_ahb_ rts_n	ssis_en		37
AB2	**IDC2DATA**	I2C/IDC	CMOS	idc1data		norspi_dq[3]	norspi_ en[3]		30
AB3	**USB_VDDA18_ AB3**	Power	Analog Supply						
AB4	**USB_DVDD**	Power	Digital Supply						
AB5	**USB0_DP**	USB	Analog						
AB6	**USB1_DP**	USB	Analog						
AB7	**SPCLK_ LVDS_P_2**	Sensor	Sub-LVDS/ SLVS/ LVCMOS/ MIPI						
AB8	**SD_LVDS_P_8**	Sensor	Sub-LVDS/ SLVS/ LVCMOS/ MIPI						
AB9	**SD_LVDS_P_9**	Sensor	Sub-LVDS/ SLVS/ LVCMOS/ MIPI						
AB10	**SD_LVDS_P_3**	Sensor	Sub-LVDS/ SLVS/ LVCMOS/ MIPI						
AB11	**SD_LVDS_P_2**	Sensor	Sub-LVDS/ SLVS/ LVCMOS/ MIPI						
AB12	**SD_LVDS_P_1**	Sensor	Sub-LVDS/ SLVS/ LVCMOS/ MIPI						

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
AB13	**SD_LVDS_P_0**	Sensor	Sub-LVDS/ SLVS/ LVCMOS/ MIPI						
AB14	**SPCLK_ LVDS_P_0**	Sensor	Sub-LVDS/ SLVS/ LVCMOS/ MIPI						
AB15	**SD_LVDS_P_7**	Sensor	Sub-LVDS/ SLVS/ LVCMOS/ MIPI						
AB16	**SD_LVDS_P_6**	Sensor	Sub-LVDS/ SLVS/ LVCMOS/ MIPI						
AB17	**SD_LVDS_P_5**	Sensor	Sub-LVDS/ SLVS/ LVCMOS/ MIPI						
AB18	**SD_LVDS_P_4**	Sensor	Sub-LVDS/ SLVS/ LVCMOS/ MIPI						
AB19	**SPCLK_ LVDS_P_1**	Sensor	Sub-LVDS/ SLVS/ LVCMOS/ MIPI						
AB20	**ENET_RX_ER**	ENET	CMOS	enet_rxer	sc_b1	enet_rxer	ssi1_en2	norspi_en[2]	51
AB21	**ENET_TXD_0**	ENET	CMOS	enet_ txd_0	sc_a1	enet_txd_0	ssi1_txd	norspi_dq[0]	47
AB22	**ENET_RXD_0**	ENET	CMOS	enet_ rxd_0	sc_a3	enet_rxd_0	ssi1_en0	norspi_en[0]	49

Table 7-1. Pin List and Mapping Table for the A12A55 Chip.

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9. TYPOGRAPHICAL CONVENTIONS

This document provides technical detail using a set of consistent typographical conventions to help the user differentiate key concepts at a glance. Conventions include:

Example	Description
AmbaGuiGen, **DirectUSB** **Save, File > Save** **Power, Reset**, **Home**	Software names GUI commands and command sequences Computer / Hardware buttons
Flash_IO_control **da**, **status**, **enable**	Register names and register fields. For example, **Flash_IO_control** is the register for global control of Flash I/O, and bit 17 (**da)** is used for DMA acknowledgement.
GPIO81, **CLK_AU**	Hardware external pins
VIL, VIH, VOL, VOH	Hardware pin parameters
INT_O, RXDATA_I	Hardware pin signals
amb_performance_t **amb_operating_mode_t** **amb_set_operating_mode()**	API details (e.g., functions, structures, and type definitions)
`/usr/local/bin` `success = amb_set_operating_mode (amb_hal_base_address, & operating_mode)`	User entries into software dialogues and GUI windows File names and paths Command line scripting and Code

Table 9-1. Typographical Conventions for Technical Documents.

Additional Ambarella typographical conventions include:

- Acronyms are given in UPPER CASE using the default font (e.g., AHB, ARM11 and DDRIO).
- Names of Ambarella documents and publicly available standards, specifications, and databooks appear in *italic* type.

10. REVISION HISTORY

NOTE: Page/chapter numbers for previous drafts may differ from those in the current version.

Version	Date	Comments
0.1	26 November 2014	New A12A Part
0.2	17 December 2014	Update to version A1
0.3	24 February 2015	Update operating temperature range
0.4	19 March 2015	Update SD-related timing diagrams and specs; Change package dimensions
0.5	28 July 2015	Update to version A2
0.6	5 October 2015	Changed the maximum value for 3.3-V supply from 3.15-V to 3.6-V for the following rails: ADC_VDDA33, HDMI_VDDA_ESD, USB_VDD33_0, VDAC_AVDD33, VDD33, VDD33_NAND, VDD33_SD
0.7	23 November 2015	Updated secondary VIN description in Section 3.2.2.1

Table 10-1. Revision History.