# HONGCE ZHANG

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## EDUCATION

**Princeton University** Sep 2015 – June 2021
Electrical and Computer Engineering
Ph.D. (advisor: Sharad Malik)

**Shanghai Jiao Tong University** Sep 2011 – July 2015
School of Electronic Information and Electrical Engineering
Bachelor

## WORK EXPERIENCE

•Assistant Professor at *Hong Kong University of Science and Technology (Guangzhou)* Sep 2021 – Present
Microelectronics Thrust, Function Hub

•Intern at *Intel Strategic CAD Labs* May 2020 – Aug 2020
Synthesizing hardware abstraction from simulation traces for verification purposes

•Intern at *VMware Research* Jun 2019 – Aug 2019
Formal property verification of neural networks

•Intern at *Nokia Bell Labs* Jun 2017 – Aug 2017
Constraint-solving for systems-on-chip floor-planning

## RESEARCH FIELDS

•Model checking and invariant synthesis
•Hardware verification using formal instruction set architecture specification

## TEACHING

**MICS 6000A: Automated Reasoning in Electronic System Verification** Spring Term

- SAT, SMT, model checking, abstraction (predicate abstraction, abstract interpretation, CEGAR, etc.), SyGuS
- Theory - algorithms - tools - applications

**MICS 6000H: Logic Design Automation for Digital Systems** Fall Term

- Compiler frontend: automata theory, lexing, parsing, AST
- Digital frontend: logic synthesis and minimization, technology mapping, timing analysis, ATPG

## TOOL DEVELOPMENT

**ILAng** main developer https://github.com/PrincetonUniversity/ILAng

- A platform for Systems-on-Chip specification and verification.
- High-standard software engineering practice with CI/CD, code quality and test coverage control.
- Functionality: behavioral equivalence checking between instruction-level abstraction and hardware description languages, software-hardware co-simulation and co-verification.

**Pono** co-developer https://github.com/upscale-project/pono

- Pono is previously named CoSA2, which won the first place in Hardware Model Checking Competition 2019, and has been integrated in the commercial tool: SymbioticEDA.
- My contributions: array property interface, trace visualization, model checking algorithm SyGuS-APDR
- Functionality: automated formal property verification on Verilog.

## PROFESSIONAL SERVICES

- 59th Design Automation Conference - Research Technical Program Committee (reviewer) 2022
- IEEE Journal on Emerging and Selected Topics in Circuits and Systems (reviewer) 2021

## BOOK CHAPTER

- *EDA Whitebook* from EDA Ecosystem Development Accelerator (EDA2) 2021-2022
  Chapter D5-Whitebook on Formal Verification Tools (co-author)

## PUBLICATIONS

Conferences:

- Yu Zeng, Bo-Yuan Huang, **Hongce Zhang**, Aarti Gupta, Sharad Malik, Generating Architecture-Level Abstractions from RTL Designs for Processors and Accelerators Part I: Determining Architectural State Variables, in *International Conference On Computer Aided Design (ICCAD)*, 2021
- Makai Mann, Ahmed Irfan, Florian Lonsing, Yahan Yang, **Hongce Zhang**, Kristopher Brown, Aarti Gupta and Clark Barrett, Pono: A Flexible and Extensible SMT-based Model Checker, in *Computer-aided Verification (CAV)*, 2021
- **Hongce Zhang**, Aarti Gupta and Sharad Malik, Syntax-Guided Synthesis for Lemma Generation in Hardware Model Checking, in *Verification Model Checking and Abstract Interpretation (VMCAI)*, 2021.
- **Hongce Zhang**, Maxwell Shinn, Aarti Gupta, Arie Gurfinkel, Nham Le and Nina Narodytska, Verification of Recurrent Neural Networks for Cognitive Tasks via Reachability Analysis, in *European Conference on Artificial Intelligence (ECAI)*, 2020.
- Nina Narodytska, **Hongce Zhang**, Aarti Gupta, and Toby Walsh, In Search for a SAT-friendly Binarized Neural Network Architecture, in *International Conference on Learning Representations (ICLR)*, 2020.
- **Hongce Zhang**, Weikun Yang, Grigory Fedyukovich, Aarti Gupta and Sharad Malik, Synthesizing Environment Invariants for Modular Hardware Verification, in *Verification Model Checking and Abstract Interpretation (VMCAI)*, 2020.

Bo-Yuan Huang, **Hongce Zhang**, Aarti Gupta and Sharad Malik, ILAng: A Modeling and Verification Platform for SoCs Using Instruction-Level Abstractions, in *Tools and Algorithms for the Construction and Analysis of Systems (TACAS)*, 2019.

- **Hongce Zhang**, Caroline Trippel, Yatin A. Manerkar, Aarti Gupta, Margaret Martonosi and Sharad Malik, ILA-MCM: Integrating Memory Consistency Models with Instruction-Level Abstraction for Heterogeneous System-on-Chip Verification, in *Formal Methods in Computer-Aided Design (FMCAD)*, 2018.
- Jangseop Shin, **Hongce Zhang**, Jinyong Lee, Ingoo Heo, Yu-Yuan Chen, Ruby B. Lee, and Yunheung Paek, A Hardware-based Technique for Efficient Implicit Information Flow Tracking, in *International Conference on Computer-Aided Design (ICCAD)*, 2016

Journal

- Bo-Yuan Huang, **Hongce Zhang**, Pramod Subramanyan, Yakir Vizel, Aarti Gupta and Sharad Malik, Instruction-Level Abstraction (ILA): A Uniform Specification for System-on-Chip (SoC) Verification, in *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, 2019.

## AWARD

- ACM TODAES Best Paper Award @ DAC'20 July 2020