1. Description

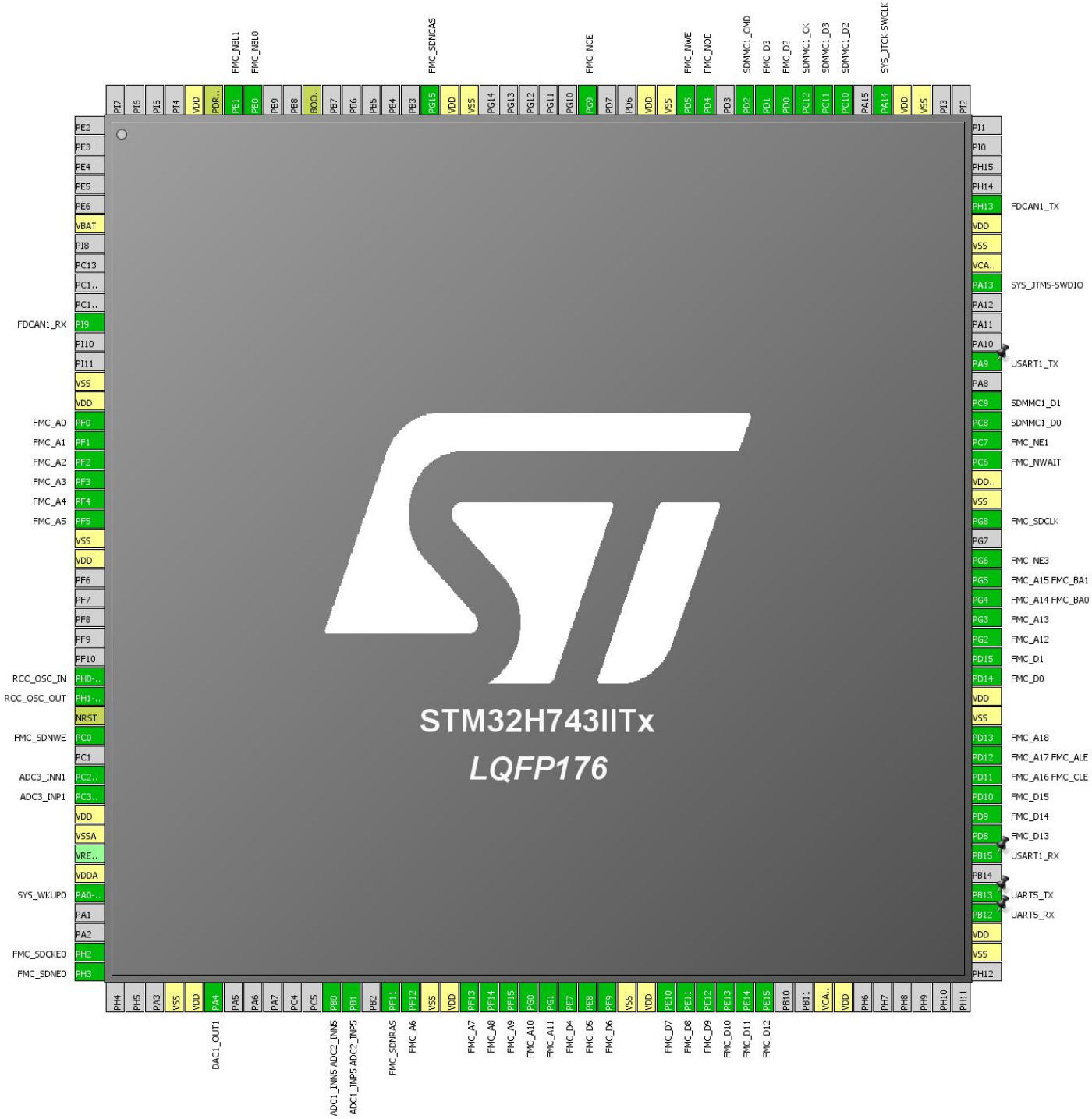
1.1. Project

Project Name	stm32H743_temp
Board Name	custom
Generated with:	STM32CubeMX 4.27.0
Date	11/25/2018

1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H743/753
MCU name	STM32H743IITx
MCU Package	LQFP176
MCU Pin number	176

2. Pinout Configuration



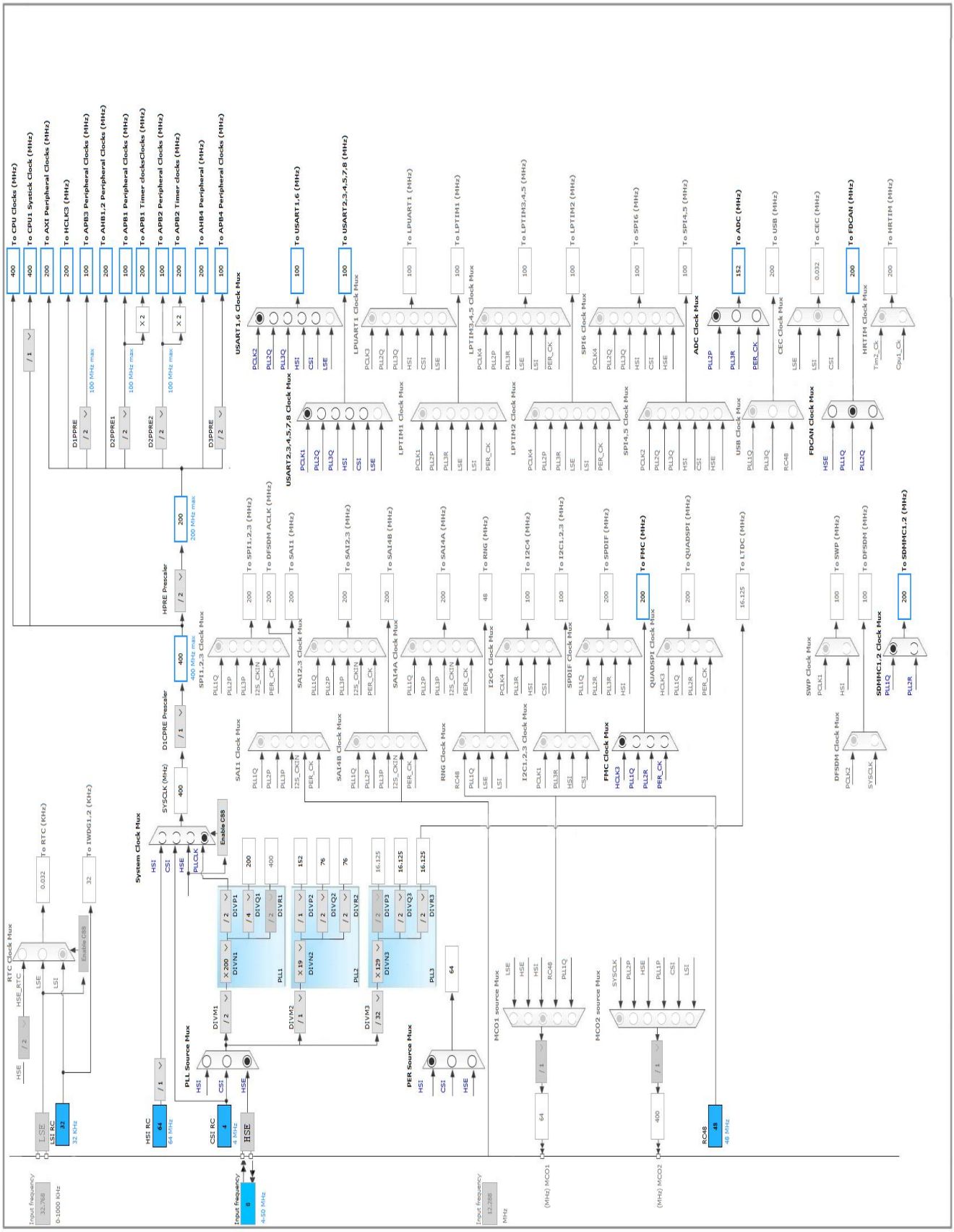
3. Pins Configuration

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
11	PI9	I/O	FDCAN1_RX	
14	VSS	Power		
15	VDD	Power		
16	PF0	I/O	FMC_A0	
17	PF1	I/O	FMC_A1	
18	PF2	I/O	FMC_A2	
19	PF3	I/O	FMC_A3	
20	PF4	I/O	FMC_A4	
21	PF5	I/O	FMC_A5	
22	VSS	Power		
23	VDD	Power		
29	PH0-OSC_IN	I/O	RCC_OSC_IN	
30	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
31	NRST	Reset		
32	PC0	I/O	FMC_SDNWE	
34	PC2_C	I/O	ADC3_INN1	
35	PC3_C	I/O	ADC3_INP1	
36	VDD	Power		
37	VSSA	Power		
39	VDDA	Power		
40	PA0-WKUP	I/O	SYS_WKUP0	
43	PH2	I/O	FMC_SDCKE0	
44	PH3	I/O	FMC_SDNE0	
48	VSS	Power		
49	VDD	Power		
50	PA4	I/O	DAC1_OUT1	
56	PB0	I/O	ADC1_INN5, ADC2_INN5	
57	PB1	I/O	ADC1_INP5, ADC2_INP5	
59	PF11	I/O	FMC_SDNRAS	
60	PF12	I/O	FMC_A6	
61	VSS	Power		
62	VDD	Power		
63	PF13	I/O	FMC_A7	
64	PF14	I/O	FMC_A8	
65	PF15	I/O	FMC_A9	

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
66	PG0	I/O	FMC_A10	
67	PG1	I/O	FMC_A11	
68	PE7	I/O	FMC_D4	
69	PE8	I/O	FMC_D5	
70	PE9	I/O	FMC_D6	
71	VSS	Power		
72	VDD	Power		
73	PE10	I/O	FMC_D7	
74	PE11	I/O	FMC_D8	
75	PE12	I/O	FMC_D9	
76	PE13	I/O	FMC_D10	
77	PE14	I/O	FMC_D11	
78	PE15	I/O	FMC_D12	
81	VCAP1	Power		
82	VDD	Power		
90	VSS	Power		
91	VDD	Power		
92	PB12	I/O	UART5_RX	
93	PB13	I/O	UART5_TX	
95	PB15	I/O	USART1_RX	
96	PD8	I/O	FMC_D13	
97	PD9	I/O	FMC_D14	
98	PD10	I/O	FMC_D15	
99	PD11	I/O	FMC_A16, FMC_CLE	
100	PD12	I/O	FMC_A17, FMC_ALE	
101	PD13	I/O	FMC_A18	
102	VSS	Power		
103	VDD	Power		
104	PD14	I/O	FMC_D0	
105	PD15	I/O	FMC_D1	
106	PG2	I/O	FMC_A12	
107	PG3	I/O	FMC_A13	
108	PG4	I/O	FMC_A14, FMC_BA0	
109	PG5	I/O	FMC_A15, FMC_BA1	
110	PG6	I/O	FMC_NE3	
112	PG8	I/O	FMC_SDCLK	
113	VSS	Power		
114	VDD33_USB	Power		
115	PC6	I/O	FMC_NWAIT	

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
116	PC7	I/O	FMC_NE1	
117	PC8	I/O	SDMMC1_D0	
118	PC9	I/O	SDMMC1_D1	
120	PA9	I/O	USART1_TX	
124	PA13	I/O	SYS_JTMS-SWDIO	
125	VCAP2	Power		
126	VSS	Power		
127	VDD	Power		
128	PH13	I/O	FDCAN1_TX	
135	VSS	Power		
136	VDD	Power		
137	PA14	I/O	SYS_JTCK-SWCLK	
139	PC10	I/O	SDMMC1_D2	
140	PC11	I/O	SDMMC1_D3	
141	PC12	I/O	SDMMC1_CK	
142	PD0	I/O	FMC_D2	
143	PD1	I/O	FMC_D3	
144	PD2	I/O	SDMMC1_CMD	
146	PD4	I/O	FMC_NOE	
147	PD5	I/O	FMC_NWE	
148	VSS	Power		
149	VDD	Power		
152	PG9	I/O	FMC_NCE	
158	VSS	Power		
159	VDD	Power		
160	PG15	I/O	FMC_SDNCAS	
166	BOOT0	Boot		
169	PE0	I/O	FMC_NBL0	
170	PE1	I/O	FMC_NBL1	
171	PDR_ON	Reset		
172	VDD	Power		

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

IN5: IN5 Differential

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 6
Resolution	ADC 16-bit resolution
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Boost Mode	Enabled
Conversion Data Management Mode	Regular Conversion data stored in DR register only
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Left Bit Shift	No bit shift
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 5
Sampling Time	1.5 Cycles
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

5.2. ADC2

IN5: IN5 Differential

5.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 6
Resolution	ADC 16-bit resolution
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Boost Mode	Enabled
Conversion Data Management Mode	Regular Conversion data stored in DR register only
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Left Bit Shift	No bit shift
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 5
Sampling Time	1.5 Cycles
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

5.3. ADC3

IN1: IN1 Differential

5.3.1. Parameter Settings:

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 6
Resolution	ADC 16-bit resolution
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Boost Mode	Enabled
Conversion Data Management Mode	Regular Conversion data stored in DR register only
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Left Bit Shift	No bit shift
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 1
Sampling Time	1.5 Cycles
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

5.4. CRC

mode: Activated

5.4.1. Parameter Settings:

Basic Parameters:

Default Polynomial State	Enable
Default Init Value State	Enable

Advanced Parameters:

Input Data Inversion Mode	None
Output Data Inversion Mode	Disable
Input Data Format	Bytes

5.5. DAC1

OUT1 mode: Connected to external pin and to on chip-peripherals

5.5.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Enable
Trigger	None
User Trimming	Factory trimming
Sample And Hold	Sampleandhold Disable

5.6. FDCAN1

Mode: FD

5.6.1. Parameter Settings:

Basic Parameters:

Frame Format	FD mode without BitRate Switshing
Mode	Normal mode
Auto Retransmission	Disable
Tx Delay Compensation	Disable
Transmit Pause	Disable
Protocol Exception	Disable
Nominal Prescaler	1
Nominal Sync Jump Width	1
Nominal Time Seg1	2

Nominal Time Seg2	2
Data Prescaler	1
Data Sync Jump Width	1
Data Time Seg1	1
Data Time Seg2	1
Message Ram Offset	0
Std Filters Nbr	0
Ext Filters Nbr	0
Rx Fifo0 Elmts Nbr	0
Rx Fifo0 Elmt Size	8 bytes data field
Rx Fifo1 Elmts Nbr	0
Rx Fifo1 Elmt Size	8 bytes data field
Rx Buffers Nbr	0
Rx Buffer Size	8 bytes data field
Tx Events Nbr	0
Tx Buffers Nbr	0
Tx Fifo Queue Elmts Nbr	0
Tx Fifo Queue Mode	FIFO mode
Tx Elmt Size	8 bytes data field

msgRam:

Standard Filter Sa	0
Extended Filter Sa	0
Rx Fifo0 Sa	0
Rx Fifo1 Sa	0
Rx Buffer Sa	0
Tx Event Fifosa	0
Tx Buffer Sa	0
Tx Fifoqsa	0
Tt Memory Sa	0
End Address	0

Error_Code:

Error Code	0

5.7. FMC

NOR Flash/PSRAM/SRAM/ROM/LCD 1

Chip Select: NE1

Memory type: SRAM

Address: 19 bits

Data: 16 bits

Wait: Asynchronous

Byte enable: 16-bit byte enable

NOR Flash/PSRAM/SRAM/ROM/LCD 3

Chip Select: NE3

Memory type: LCD Interface

LCD Register Select: A0

Data: 16 bits

NAND Flash 1

Chip Select: set

Data/Address: 8 bits

Ready or busy: NWAIT

SDRAM 1

Clock and chip enable: SDCKE0+SDNE0

Internal bank number: 4 banks

Address: 13 bits

Data: 16 bits

Byte enable: 16-bit byte enable

5.7.1. NOR/PSRAM 1:

NOR/PSRAM control:

Memory type	SRAM
Bank	Bank 1 NOR/PSRAM 1
Write operation	Disabled
Write FIFO	Enabled
Extended mode	Disabled
Wait signal polarity	Low polarity

NOR/PSRAM timing:

Address setup time in HCLK clock cycles	15
Data setup time in HCLK clock cycles	255
Bus turn around time in HCLK clock cycles	15

5.7.2. Bank Mapping:

Mapping parameters:

FMC bank mapping	Default mapping

5.7.3. NOR/PSRAM 3:

NOR/PSRAM control:

Memory type	LCD Interface
Bank	Bank 1 NOR/PSRAM 3
Write operation	Enabled
Write FIFO	Enabled
Extended mode	Disabled

NOR/PSRAM timing:

Address setup time in HCLK clock cycles	15
Data setup time in HCLK clock cycles	255
Bus turn around time in HCLK clock cycles	15

5.7.4. NAND 1:

NAND control:

Bank	NAND bank 3
ECC computation	Disabled
ECC page size	256 bytes
CLE low to RE low delay in HCLK cycles	**1 ***
ALE low to RE low delay in HCLK cycles	**1 ***

NAND common space timing in HCLK cycles:

Common space setup time	**253 ***
Common space wait time	**253 ***
Common space hold time	252
Common space Hi-Z time	**253 ***

NAND attribute space timing in HCLK cycles:

Attribute space setup time	**253 ***
Attribute space wait time	**253 ***
Attribute space hold time	252
Attribute space Hi-Z time	**253 ***

NAND characteristic information:

Page size	0
Spare area size	0
Block size	0
Block number	0
Plane number	0
Plane size	0
Extra command enable	Disabled

5.7.5. SDRAM 1:

SDRAM control:

Bank	SDRAM bank 1
Number of column address bits	8 bits
Number of row address bits	13 bits
CAS latency	1 memory clock cycle
Write protection	Disabled
SDRAM common clock	Disabled
SDRAM common burst read	Disabled
SDRAM common read pipe delay	0 HCLK clock cycle

SDRAM timing in memory clock cycles:

Load mode register to active delay	16
Exit self-refresh delay	16
Self-refresh time	16
SDRAM common row cycle delay	16
Write recovery time	16
SDRAM common row precharge delay	16
Row to column delay	16

5.8. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.8.1. Parameter Settings:

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
CSI Calibration Value	16
HSI Calibration Value	16

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	2 WS (3 CPU cycle)

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1

PLL range Parameters:

PLL1 clock Input range	Between 4 and 8 MHz
PLL2 input frequency range	Between 8 and 16 MHz

PLL1 clock Output range	Wide VCO range
PLL2 clock Output range	MEDIUM VCO range
PLL Fractional Part	0
PLL2 Fractional Part	0

5.9. SDMMC1

Mode: SD 4 bits Wide bus

5.9.1. Parameter Settings:

SDMMC parameters:

Clock transition on which the bit capture is made	Rising transition
SDMMC Clock output enable when the bus is idle	Disable the power save for the clock
SDMMC hardware flow control	The hardware control flow is disabled
SDMMC clock divide factor	**4 ***

5.10. SYS

Debug: Serial Wire

mode: System Wake-Up 0

Timebase Source: TIM6

5.11. TIM1

Clock Source : Internal Clock

5.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

5.12. TIM2

Clock Source : Internal Clock

5.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	0
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

5.13. TIM3

Clock Source : Internal Clock

5.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**19999 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**4999 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

5.14. TIM4

Clock Source : Internal Clock

5.14.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

5.15. TIM5

Clock Source : Internal Clock

5.15.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	0
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

5.16. TIM7

mode: Activated

5.16.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.17. TIM8

Clock Source : Internal Clock

5.17.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

5.18. TIM12

mode: Clock Source

5.18.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

5.19. TIM13

mode: Activated

5.19.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division

auto-reload preload	Disable

5.20. TIM14

mode: Activated

5.20.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

5.21. TIM15

mode: Clock Source

5.21.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.22. TIM16

mode: Activated

5.22.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up

Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

5.23. TIM17

mode: Activated

5.23.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

5.24. UART5

Mode: Asynchronous

5.24.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
Prescaler	clock /1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable

RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

5.25. USART1

Mode: Asynchronous

5.25.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
Prescaler	clock /1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

5.26. FATFS

mode: SD Card

5.26.1. Set Defines:

Version:

FATFS version	R0.12c

Function Parameters:

FS_READONLY (Read-only mode)	Disabled
FS_MINIMIZE (Minimization level)	Disabled
USE_STRFUNC (String functions)	Enabled with LF -> CRLF conversion
USE_FIND (Find functions)	Disabled
USE_MKFS (Make filesystem function)	Enabled
USE_FASTSEEK (Fast seek function)	Enabled
USE_EXPAND (Use f_expand function)	Disabled
USE_CHMOD (Change attributes function)	Disabled
USE_LABEL (Volume label functions)	Disabled
USE_FORWARD (Forward function)	Disabled

Locale and Namespace Parameters:

CODE_PAGE (Code page on target)	Latin 1
USE_LFN (Use Long Filename)	Disabled
MAX_LFN (Max Long Filename)	255
LFN_UNICODE (Enable Unicode)	ANSI/OEM
STRF_ENCODE (Character encoding)	UTF-8
FS_RPATH (Relative Path)	Disabled

Physical Drive Parameters:

VOLUMES (Logical drives)	1
MAX_SS (Maximum Sector Size)	512
MIN_SS (Minimum Sector Size)	512
MULTI_PARTITION (Volume partitions feature)	Disabled
USE_TRIM (Erase feature)	Disabled
FS_NOFSINFO (Force full FAT scan)	0

System Parameters:

FS_TINY (Tiny mode)	Disabled
FS_EXFAT (Support of exFAT file system)	Disabled
FS_NORTC (Timestamp feature)	Dynamic timestamp
NORTC_YEAR (Year for timestamp)	2015
NORTC_MON (Month for timestamp)	6
NORTC_MDAY (Day for timestamp)	4
FS_REENTRANT (Re-Entrancy)	Enabled
FS_TIMEOUT (Timeout ticks)	1000
SYNC_t (O/S sync object)	osSemaphoreId
FS_LOCK (Number of files opened simultaneously)	2

5.26.2. IPs instances:

SDIO/SDMMC:

SDMMC instance	SDMMC1
Use dma template	Enabled

5.27. FREERTOS

mode: Enabled

5.27.1. Config parameters:

Versions:

FreeRTOS version	9.0.0
CMSIS-RTOS version	1.02

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled

Memory management settings:

Memory Allocation	Dynamic
TOTAL_HEAP_SIZE	15360
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled

USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Disabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Disabled

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

5.27.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Disabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PB0	ADC1_INN5	Analog mode	No pull-up and no pull-down	n/a	
	PB1	ADC1_INP5	Analog mode	No pull-up and no pull-down	n/a	
ADC2	PB0	ADC2_INN5	Analog mode	No pull-up and no pull-down	n/a	
	PB1	ADC2_INP5	Analog mode	No pull-up and no pull-down	n/a	
ADC3	PC2_C	ADC3_INN1	Analog mode	No pull-up and no pull-down	n/a	
	PC3_C	ADC3_INP1	Analog mode	No pull-up and no pull-down	n/a	
DAC1	PA4	DAC1_OUT1	Analog mode	No pull-up and no pull-down	n/a	
FDCAN1	PI9	FDCAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH13	FDCAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
FMC	PF0	FMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF1	FMC_A1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF2	FMC_A2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF3	FMC_A3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF4	FMC_A4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF5	FMC_A5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC0	FMC_SDNWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH2	FMC_SDCKE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH3	FMC_SDNE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF11	FMC_SDNRAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF12	FMC_A6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF13	FMC_A7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF14	FMC_A8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF15	FMC_A9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG0	FMC_A10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG1	FMC_A11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD9	FMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD11	FMC_A16	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD12	FMC_A17	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD13	FMC_A18	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG2	FMC_A12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG3	FMC_A13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG4	FMC_A14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG5	FMC_A15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG6	FMC_NE3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG8	FMC_SDCLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC6	FMC_NWAIT	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC7	FMC_NE1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD4	FMC_NOE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD5	FMC_NWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG9	FMC_NCE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG15	FMC_SDNCAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE0	FMC_NBL0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE1	FMC_NBL1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SDMMC1	PC8	SDMMC1_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC9	SDMMC1_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC10	SDMMC1_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC11	SDMMC1_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC12	SDMMC1_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD2	SDMMC1_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SYS	PA0-WKUP	SYS_WKUP0	n/a	n/a	n/a	
	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
UART5	PB12	UART5_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB13	UART5_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PB15	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	

6.2. DMA configuration

nothing configured in DMA service

6.3. BDMA configuration

nothing configured in DMA service

6.4. MDMA configuration

nothing configured in DMA service

6.5. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
TIM3 global interrupt	true	5	0
USART1 global interrupt	true	5	0
SDMMC1 global interrupt	true	5	0
UART5 global interrupt	true	5	0
TIM6 global interrupt, DAC1_CH1 and DAC1_CH2 underrun error interrupts	true	0	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupts	unused		
FDCAN1 interrupt 0	unused		
FDCAN1 interrupt 1	unused		
TIM1 break interrupt	unused		
TIM1 update interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM4 global interrupt	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM8 update interrupt and TIM13 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
TIM8 capture compare interrupt	unused		
FMC global interrupt	unused		
TIM5 global interrupt	unused		
TIM7 global interrupt	unused		
FDCAN calibration unit interrupt	unused		
FPU global interrupt	unused		
TIM15 global interrupt	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
TIM16 global interrupt	unused		
TIM17 global interrupt	unused		
HSEM1 global interrupt	unused		
ADC3 global interrupt	unused		
Interrupt for all 6 wake-up pins	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32H7
Line	STM32H743/753
MCU	STM32H743IITx
Datasheet	030538_Rev1

7.2. Parameter Selection

Temperature	25
Vdd	3.0

8. Software Project

8.1. Project Settings

Name	Value
Project Name	stm32H743_temp
Project Folder	F:\other\bld\STM32H7\project\stm32h743ii\stm32H743_temp
Toolchain / IDE	EWARM V8
Firmware Package Name and Version	STM32Cube FW_H7 V1.3.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

9. Software Pack Report