# iMX6QD HDMI TX

## Overview

HDMI (High-Definition Multimedia Interface) is an audio/video interface for transmitting uncompressed digital video data and uncompressed/compressed digital audio data. HDMI supports (on a single cable) any TV or PC video format (standard, enhanced and high-definition) in addition of up to eight channels of digital audio and a Consumer Electronics Control (CEC) connection. The CEC allows HDMI devices to control each other when necessary and allows the user to operate multiple devices with one remote control handset.

HDMI is electrically compatible with the signals used by the Digital Visual Interface (DVI) and therefore no signal conversion is required. Since the interface is fully compatible, there is no loss of video quality when an HDMI-to-DVI adapter is used.

On i.MX6Quad/Dual, the HDMI Transmitter module (HDMI TX) consists of two parts:

* HDMI TX Controller
* HDMI TX PHY

The figure ***(8-10 from RM)*** below shows the HDMI TX integration in the iMX6Quad/Dual



## Features

These are some of the key features to the HDMI TX module on iMX6Quad/Dual:

* Compliant with HDMI v1.4a (DVI 1.0), HDMI CTS v1.4a, HDMI HDCP 1.4
* Consumer Electronic Control (CEC)
* Video Resolutions up to 1080p@120Hz HDTV display
* Up to QXGA graphics display
* HDMI 1.4a 4K x 2K video formats
* HDMI 1.4a 3D video modes with up to 340MHz HDMI\_CLKM/P clock
* Audio Sampling rate of up to 192kHz

## Hardware Interface

### External Signals and Power

This section provides an overview and description of the available HDMI external signals on iMX6Quad/Dual. The table below lists all the signals.

|  | Table 1. HDMI External Signals | |
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| Signal Name | I/O | Description |
| HDMI\_VP | Power | 1.1V analog power supply |
| HDMI\_VPH | Power | 2.5V analog power supply |
| HDMI\_REF | I/O | Reference Resistor Connection |
| HDMI\_HPD | I | Hot Plug Detect |
| HDMI\_DDCCEC | O | Ground Reference for HDMI\_HPD signal |
| HDMI\_CLKM/P | O | Minus/Plus differential line clock output |
| HDMI\_D[2:0]M/P | O | Minus/Plus differential lines for data channel 0,1 and 2 outputs |
| HDMI\_CEC\_LINE | I/O | CEC data bus (MUXed on imx6) |
| HDMI\_DDC\_SDA | I/O | HDMI I2C data bus (MUXed on imx6) |
| HDMI\_DDC\_SCL | O | HDMI I2C clock (MUXed on imx6) |

## Clocks

The main clock source for the HDMI block is the pixel clock output from the Image Processing Unit (IPU). Using the pixel clock, the HDMI PHY provides PLL/MPLL that synthesizes the high-speed HDMI serial bit clock. The serial bit clock can be configured in the PLL/MPLL registers in the HDMI PHY.

In addition, there is the HDMI internal register configuration clock (referred to as isfrclk) which can be gated from the Clock Control Module (CCM). This clock is referred to as the *video\_27M\_clk\_root* in the CCM. This clock is also used in HDCP and should be configured to 27MHz. The figure below shows the clock tree portion from the CCM of the *video\_27M\_clk\_root* clock.

\*\*\*\*\* fix this image of video\_27M\_clk\_root \*\*\*\*\*





Also, in the same CCM clock gate register (CCM\_CCGR2) for the video\_27M\_CLK\_ROOT (hdmi\_tx\_isfrclk) there is also a clock gate available for the clock signal hdmi\_tx\_iahbclk. This clock comes from the ahb\_clk\_root in the CCM and is used with the amba ahb bus interface of the HDMI TX block. Both clocks should be gated ON (enabled) for the HDMI TX block to operate correctly.

## HDMI Video Input Set-Up

On iMX6Quad/Dual the video input source to the HDMI TX block can be any output stream from the IPU block. Therefore there are four possible inputs to the HDMI TX block, IPU1-Display Interface 0 or 1 and IPU2 – Display Interface 0 or 1. There is a MUX which selects the input to the HDMI TX block, this is configured in the IOMUXC\_GPR3 register with bits 3:0 of that register. The possible settings are as follows (for HDMI\_MUX\_CTL bit field, bits 3:2):

0b00 – IPU1-DI0

0b01 – IPU1-DI1

0b10 – IPU2-DI0

0b11 – IPU2-DI1

The image below **(figure 20-1 from RM)** shows the available MUX configurations.



In order to be able to get a video out of the HDMI block, the IPU input to the HDMI block must be properly configured first. In addition to properly selecting the video input MUX configuration for the HDMI block, the video input source must be set up for RGB4:4:4, YCbCr4:2:2, or YCbCr4:4:4 (the IPU output must be set up accordingly).

## HDMI Video Output Set-Up

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## HDMI Audio Set-Up

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## HDCP Encryption Engine

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## Appendices

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