i.MX61 LDB Application Notes

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# System Overview

LVDS or Low-Voltage Differential Signaling is known as an electrical digital signaling system, which can run at very high speeds over inexpensive twisted-pair copper cables. It transmits information as the difference between the voltage on a pair of wires, and the two-wire voltages are compared at the receiver end. The low common voltage (the average of the voltages on the paired wires, ~1.2V) and the low differential voltage (~350mV) cause LVDS to consume low power compared to other systems; therefore it is widely used in consumer electronic fields.

LVDS Display Bridge (LDB) is an integrated IP inside mx53/mx6x and the future SoC, which is used to connect the internal IPU (Image Processing Unit) to the external LVDS display interface.

LDB support covers all aspects of these activities:

• Connectivity to relevant devices – displays with LVDS receivers

• arranging the data as required by the external display receiver and by LVDS display standards

• Synchronization and control capabilities (to avoid tearing artifacts).

# Hardware interfaces

the detailed LDB diagram is shown as figure 2-1.

**Lvds\_clk**

**Lvds\_tx3**

**Lvds\_tx2**

**Lvds\_tx1**

**Obe\_lvds**

**Lvds\_tx0**

**AHB**

**LDB Mux**

**&Control**

**Ipu\_di\_data**

**Ipu\_di\_hsync**

**Ipu\_di\_vsync**

**Ipu\_di\_de**

**Ipu\_di\_ctrl**

**Ipu\_di\_clk**

**Ch\_data\_width**

**Ch\_bit\_mapping**

**Ldb\_chan\_mode**

**BANDGAP**

**NGND\_LVDS\_BG**

**LVDS\_BG\_RES**

**NVCC\_LVDS\_BG**

**Ldb\_ser\_clk**

**LVDS\_BIAS**

**LDB**

**Channel**

**Serializer**

**Ch\_data0**

**Ch\_data1**

**Ch\_data2**

**Ch\_data3**

**Ch\_en**

**Ch\_data\_en**

**Ch\_ser\_clk**

Figure 2‑1 detailed LDB block diagram

1. LDB mux & control: interface to the IPU and system CCM module, LDB configuration registers
2. Channel serializers: convert the parallel data into serial format
3. BANDGAP: provide reference current to the LVDS I/O pad

## Input ports

LDB module can get its input from IPU display interfaces. There are two IPU modules with two display port per IPU, that means the LVDS channel has four choices to route its data path. However, there is no point to connect LVDS channel 0 to ipu di1 in a single display mode, this is only supported in dual display operation.

### Single display mode

In single display mode, only LVDS channel 0 or channel 1 is enabled.

To set the LVDS channel 0 connected to DI0, we can have below settings:

* Configure LVDS0\_MUX\_CTL in IOMUXC\_GPR3 to be 0x0 or 0x2
* Enable channel 0 by setting CH0\_MODE to be 0x1 in IOMUXC\_GPR2

To set the LVDS channel 1 connected to DI1, we can have below settings:

* Configure LVDS0\_MUX\_CTL in IOMUXC\_GPR3 to be 0x1 or 0x3
* Enable channel 0 by setting CH0\_MODE to be 0x3 in IOMUXC\_GPR2

### Dual display mode

In this mode, LVDS channel 0 and 1 are together enabled. LVDS channels must be connected to the same IPU DI.

### Separate display mode

Channel 0 and channel 1 are both enabled, and they are connected to different DIs separately. That means the display contents could be different on the two displays.

### Split mode

In this mode, the LDB has one input and two outputs. The parallel data will be serialized and then output in horizontal interlaced mode. Odd columns are outputted from LVDS channel0, and even columns are outputted from LVDS channel1.

The channel mapping mode can be summarized in table 2.1

|  |  |  |
| --- | --- | --- |
| Use Case | LVDS channel 0 | LVDS channel 1 |
| Single channel di0 on channel 0 | Di0 | disabled |
| Single channel di1 on channel 1 | Disabled | Di1 |
| Separate channels | Di0 | Di1 |
| Dual channels to di0 | Di0 | Di0 |
| Dual channel to di1 | Di1 | Di1 |
| Split mode to di0 | Di0(odd pixels in line) | Di0(even pixels in line) |
| Split mode to di1 | Di1(odd pixels in line) | Di1(even pixels in line) |

## Output ports

table 2‑1 LVDS channel mapping

There are four pairs of wires for the LVDS output, which are TX0\_P/N, TX1\_P/N, TX2\_P/N, TX3\_P/N, TXC\_P/N.

LVDS uses a current-mode driver output from a 3.5mA current source. This drives a differential line that is terminated by a 100 ohm resistor, generating about 350 mV across the receiver. The +350mV voltage swing is centered on a 1.2V offset voltage.

# LDB Processing

The main job of LDB is to convert the parallel data lines into differential serial data lines.

The LDB can support SPWG and JEIDA mapping mode.

## Data map

### SPWG mapping

SPWG (Standard Panel Working Group) was formed to establish a set of standard LCD panels with dimensions and interface characteristics that allow both notebook and LCD supplier industries to manage the volatile LCD supply and demand in an easier fashion. 

### JEIDA mapping

The Japan Electronic Industry Development Association (JEIDA) was an industry research, development, and standards body for electronics in Japan. The JEIDA mapping mode is also popular in LVDS panels.

The data mapping mode and data width can be configured in the LDB\_CTRL register.

## Data Serialization

The parallel 18/24 bit data output from IPU will be serialized in the LDB module. In both SPWG and JEIDA mode, one pixel is reordered into 3 or 4 lines, with 7 bit per line. That means in non-split mode, in the IPU side, one pixel is driven to LDB during a pixel clock period, and in the LDB side, one pixel is driven to the display in 7 serialization clock period. In split mode, one frame is split into two horizontal field, the serialization clock is x3.5 of the pixel clock.

The IPU pixel clock and the serialization clock of LDB must be synchronous, that could be done by selecting the IPU DI clock to be external in IPU configuration registers, and then choose the clock branch in CCM to root the IPU DI clock from LDB DI clock.

In mx6qd, the LDB serialization clock is generated as below:



According to the LDB serialization clock, pixel clock is generated by dividing 3.5 or 7.

IPU\_DI\_CLK\_ROOT should be routed to ipp\_di\_clk.

## Register configuration

The following parameters could be configured in the LDB CONTROL REGISTER.

* vs\_polarity: the polarity of VSYNC signal, it should match with the IPU output.
* Bit\_mapping: using SPWG or JEIDA standard
* Data\_width: 18bit or 24bit selection
* Split\_mode: enable or disable split mode
* Channel\_mode: channel route to IPU di.

# Use Cases

## Image Display on Hannstar HSD100PXN1 XGA panel

### Power Supply

The Hannstar LVDS panel needs 3.3V for core&IO, and 5V for backlight LED driven.

### Clock Settings

The typical pixel clock for XGA resolution is 65MHz, so the ldb\_di\_clk should be 65MHz, and the LDB\_DI\_SERIAL\_CLK\_ROOT should be 65\*7=455MHz in the non-split display mode. Ldb\_di\_ipu\_div is set to 7 accordingly.

### LDB configuration

ldb\_config(IPU1\_DI0, LVDS \_PORT0, SPWG, LVDS\_PANEL\_18BITS\_MODE);

The LDB is connected to IPU1 DI0 output, and LVDS port0 is enabled. LVDS output is in SPWG standard with 18bit width, so the TX3 lane is ignored.

ldb\_config(IPU1\_DI0, LVDS \_DUAL\_PORT, SPWG, LVDS\_PANEL\_18BITS\_MODE);

In this mode, IPU output is sent to the both LVDS channels, the content is totally identical.

## Image Display on CHIMEI M216H1 1080HD panel

### Power Supply

The Hannstar LVDS panel needs 5V for backlight LED driven and core/IO.

### Clock Settings

The typical pixel clock for HD1080 resolution with refresh rate at 30Hz is 74.25MHz, so the ldb\_di\_clk should be 74.25MHz, and the LDB\_DI\_SERIAL\_CLK\_ROOT should be 74.25\*3.5=260MHz in the split display mode. Ldb\_di\_ipu\_div is set to 3.5 accordingly.

### LDB configuration

ldb\_config(IPU1\_DI0, LVDS \_SPLIT\_PORT, SPWG, LVDS\_PANEL\_18BITS\_MODE);

The LDB is connected to IPU1 DI0 output, and LVDS port0 is enabled. LVDS output is in SPWG standard with 18bit width, and data are processed in split mode.

1. References
2. i.Mx61 User Guide
3. LVDS Owner’s Manual
4. SPWG Notebook Panel Specification
5. Platlib SDK code

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