

A

A

B

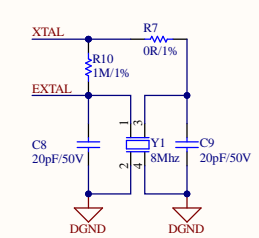
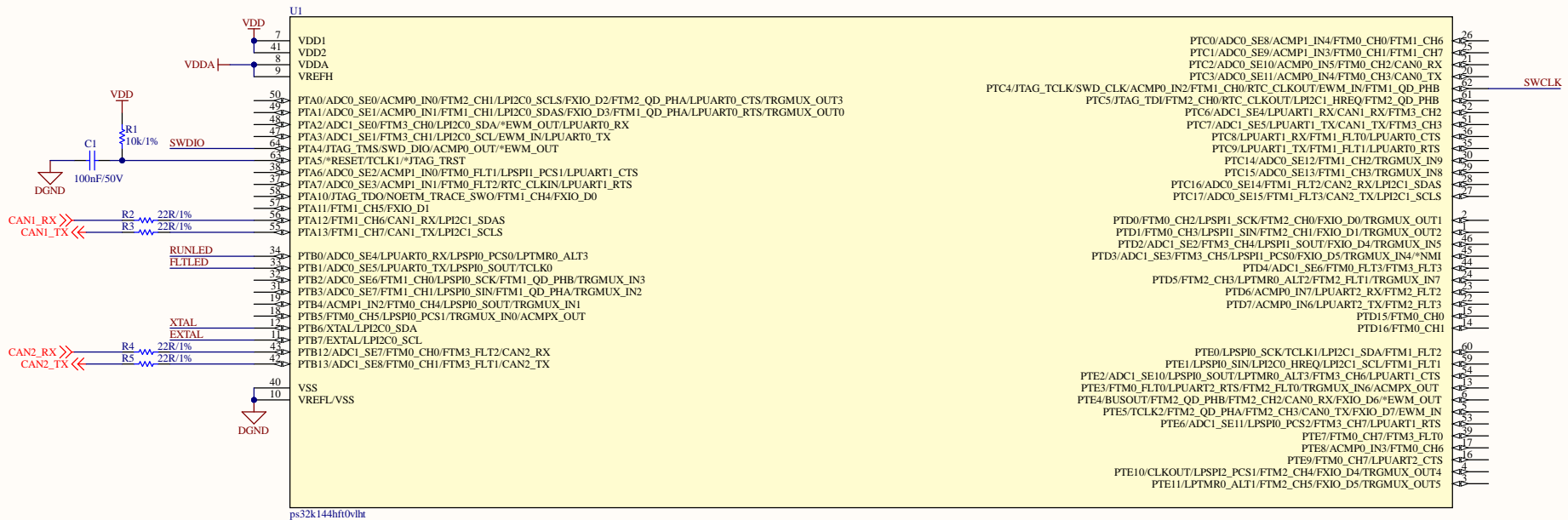
B

C

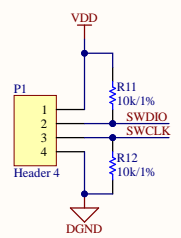
C

D

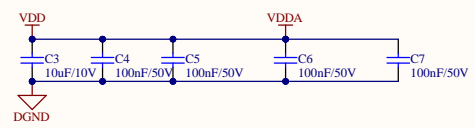
D



Clock



SWD Debug Port



Decoupling Cap

