Current Surging in Parallel Connectivity Enabled Multilevel Converters

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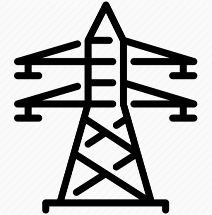
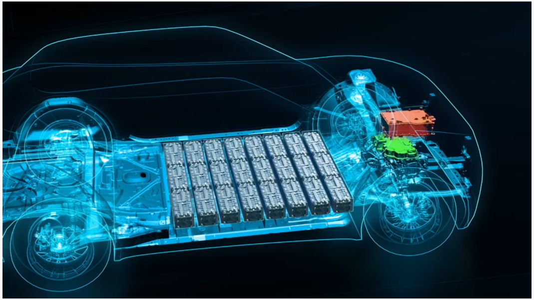
Background

Popular MMC

Modular multilevel converter (MMC) is everywhere ...





Credit to Stellantis

Parallel Connectivity Unlocking Great Flexibility

Benefits of parallel connectivity

- Ideal voltage balancing
- Lower output impedance [a]
- Better use of capacitors

Example used in this research:
Cascaded double-H bridge(CH2B) circuit

[a] D05.06: Frequency-Dependent Impedance Variation in Multilevel Converters with Parallel Connectivity

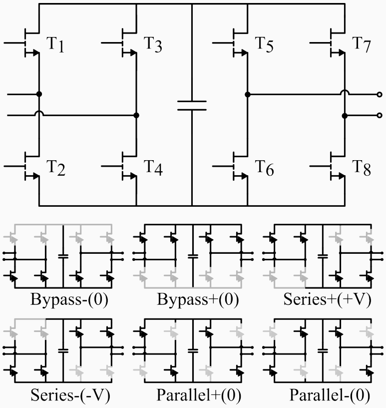
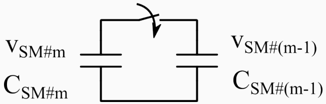


Figure 1: Topology and working principle of CH2B circuits.

The Elephant in The Room

The Elephant in The Room: Current Surge

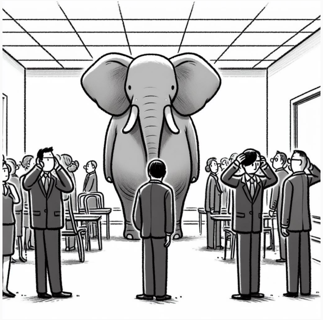


When paralleling two capacitors together, the current follows

$$I \propto \frac{\Delta V}{Z} \tag{1}$$

The current will be overwhelming when

- Voltage difference is big
- Impedance is small

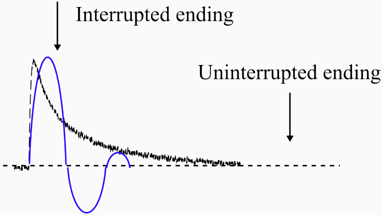


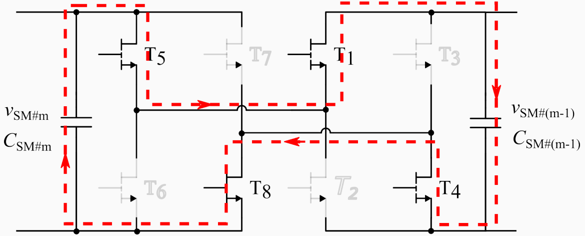
Formalizing the problem

1. Characterizing issue with temporal description
2. Identifying where / when the issue is more likely to occur
3. Solutions to mitigate the issue

Characterization: Parallelization Interval

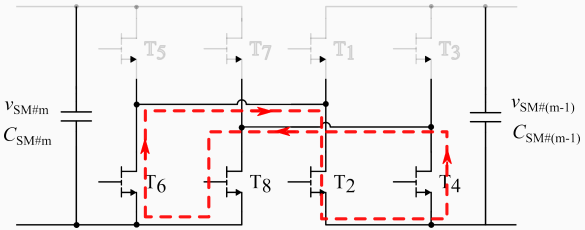
$$C\frac{\mathrm{d}v}{\mathrm{d}t} = -i$$
$$v = L\frac{\mathrm{d}i}{\mathrm{d}t} + iR \qquad (2)$$
$$V_0 = \Delta v_{\mathrm{sm}}(0)$$
$$I_0 = 0$$





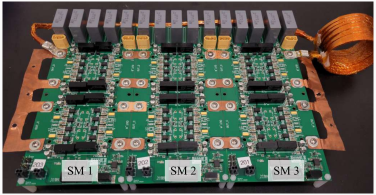
Characterization: Post-Parallelization Interval

$$L\frac{\mathrm{d}i}{\mathrm{d}t} = -iR \qquad (3)$$
$$I_0 = I_{0,\mathrm{post}}$$



Characterization: Verifying Parallelization Current

Experimental configurations	
Prototype	GaN based CH2B circuit
Switching rate	up to 5 MHz
Modulation	Nearest level modulation



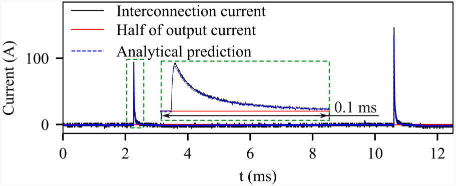


Figure 2: Uninterrupted paralleling current

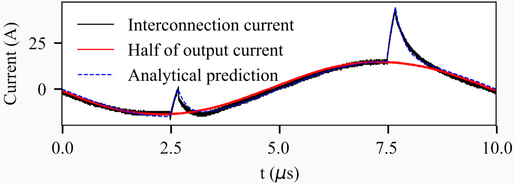


Figure 3: Interrupted paralleling current

Characterization: Different Parallelization Behaviors

Equilibration type	**Uninterrupted**	**Interrupted**
Quantitative feature	$I_{0,\mathrm{post}} = 0$	$I_{0,\mathrm{post}} \neq 0$
Ending of parallelization	Passively decaying	Actively terminating
Risk	Current surge; Over-heating	Current surge; Over-heating; Voltage overshoot

Identifying Where/When This Issue Will Occur

Method 1

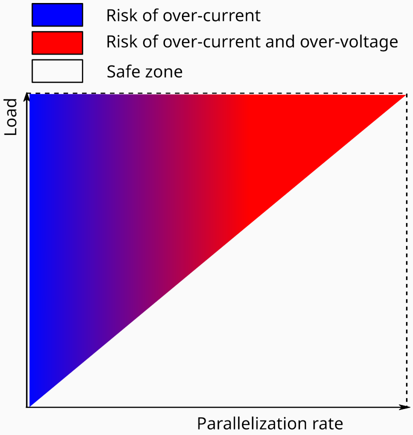


Figure 4: Pattern on circuit operation.

Method 2

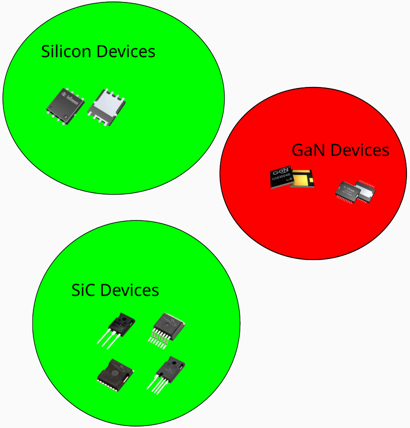
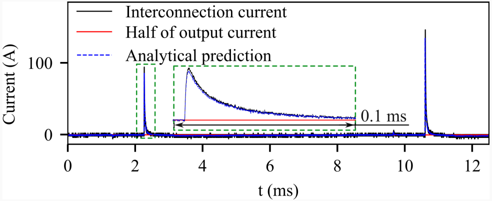


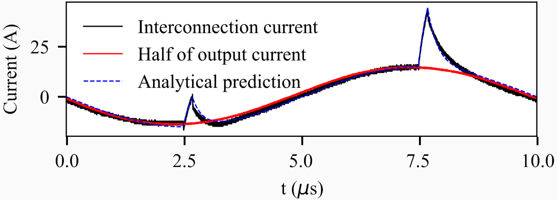
Figure 5: Pattern on device selection.

Identifying Type of Paralleling Surge

Equilibration type	Uninterrupted	Interrupted
Current behavior	Load current superimposed surges	
second-order differentiability	Yes	No



Uninterrupted paralleling current



Interrupted paralleling current

Solution: Device Selection and Design

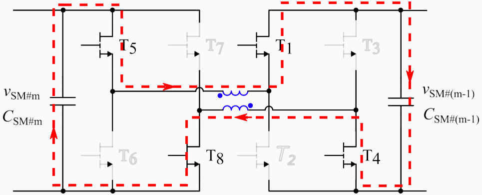
- Transient current overloading capability is unprecedentedly important
- Silicon and Silicon Carbon devices are more suitable than GaN in parallel multilevel converters
- If GaN, or other minimal-package transistors, is inevitable, add extra metal mass to provide sufficient thermal capacitance[1]

[1] J. Zhang, et al, "Gallium-Nitride (GaN) Transistor Design for Transient-Overload Power Applications," 2023 APEC, doi: 10.1109/APEC43580.2023.10131164.

Solution: Differential-Mode Magnetics

Using differential-mode inductor as inter-module connection

- contributing negligible output impedance
- mitigating the current surge



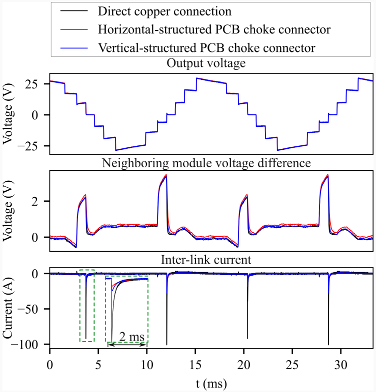


Figure 6: Output voltage, voltage difference and paralleling current with / without inter-module differential mode inductance.

Summary

Summary

- Parallel-connectivity-enabled MMC offers advantages of sensorless voltage balancing and reduced output impedance
- Challenges arise in the form of current and voltage surges during and after equilibration
- We categorize parallelization behavior as uninterrupted (mainly thermal concerns) and interrupted (also causing voltage overshoot)
- Mitigating stress involves using sturdier devices (e.g., Si or SiC with high thermal capacitance) and implementing solutions like differential mode choke for inter-module connections

Questions?