

完成SPI Verilog程序训练;

数据输入是在时钟沿的上升沿进入;

数据进来是在时钟沿的下降沿;

链接:

[https://v.youku.com/v_show/id_XMTcwNzEzNTQyMA==.html?
spm=a2h0k.11417342.soreults.dtitle](https://v.youku.com/v_show/id_XMTcwNzEzNTQyMA==.html?spm=a2h0k.11417342.soreults.dtitle)

一次发送8byte; ;

将数据和命令存储到RAM中去;

M9K代表 9K的RAM;

画出程序框图;

用Verilog描述, 将RAM用 reg代替;

使用独热码来表示系统的状态;

BUG统计:

1. 独热码的状态，要注意有多少个状态就要用多少位；
2. 独热码状态要不同

```

32     output                spi_sck;
33     output                spi_sdo
34     //input              spi_sdi
35 );
36     localparam            SCK_COUNT_Half = CLK_FRE/SPI_FRE/2;
37     localparam            IDLE   = 5'b0_0001;
38     localparam            WAIT   = 5'b0_0010;
39     localparam            READ_MEM = 5'b0_0100;
40     localparam            WRITE_REG = 5'b0_1000;
41     localparam            STOP    = 5'b1_0000;
42
43     localparam            REG0    = 8'h01;
44     localparam            REG1    = 8'h02;
45     localparam            REG2    = 8'h03;
46     localparam            REG3    = 8'h04;
47
48     reg [4:0]             state;
49
50     //FSM
51     always @(posedge clk_i) begin
52         if(!rst_n)
53             state <= IDLE;
54         else begin
55             case(state)
56                 IDLE:

```

- ### 3. SCK一直有输出

4. 状态一直在WRITE_REG

timescale 用法: https://blog.csdn.net/super_haifeng/article/details/50110371