InfiniteHBD: Building Datacenter-Scale High-Bandwidth Domain for LLM with Optical Circuit Switching Transceivers

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Abstract

Scaling Large Language Model (LLM) training relies on multi-dimensional parallelism, where High-Bandwidth Domains (HBDs) are critical for communication-intensive parallelism like Tensor Parallelism (TP) and Expert Parallelism (EP). However, existing HBD architectures face fundamental limitations in scalability, cost, and fault resiliency: switch-centric HBDs (e.g., NVL-72) incur prohibitive scaling costs, while GPU-centric HBDs (e.g., TPUv3/Dojo) suffer from severe fault propagation. Switch-GPU hybrid HBDs such as TPUv4 take a middle-ground approach, but the fault explosion radius remains large at the cube level (e.g., 64 TPUs).

We propose ***InfiniteHBD***, a novel transceiver-centric HBD architecture that *unifies connectivity and dynamic switching at the transceiver level* using Optical Circuit Switching (OCS). By embedding OCS within each transceiver, *InfiniteHBD* achieves reconfigurable point-to-multipoint connectivity, allowing the topology to adapt to variable-size rings. This design provides: i) datacenter-wide scalability without cost explosion; ii) fault resilience by isolating failures to a single node, and iii) full bandwidth utilization for fault-free GPUs. Key innovations include a Silicon Photonic (SiPh)-based low-cost OCS transceiver (***OCSTrx***), a reconfigurable k-hop ring topology co-designed with intra-/inter-node communication, and an HBD-DCN orchestration algorithm maximizing GPU utilization while minimizing cross-ToR datacenter network traffic. The evaluation demonstrates that *InfiniteHBD* achieves **31%** of the cost of NVL-72, **near-zero** GPU waste ratio (over one order of magnitude lower than NVL-72 and TPUv4), **near-zero** cross-ToR traffic when node fault ratios are under 7%, and improves Model FLOPs Utilization by **3.37x** compared to NVIDIA DGX (8 GPUs per Node).

CCS Concepts

• **Networks** → **Network architectures**; **Network components**; **Data center networks**; • **Hardware** → **Networking hardware**; • **Computing methodologies** → **Machine learning**.

Keywords

High-Bandwidth Domain, Optical Circuit Switching, Large Language Model

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1 Introduction

Large Language Models (LLMs) training relies on various parallelism strategies [67, 72], such as Tensor Parallelism (TP), Expert Parallelism (EP), Data Parallelism (DP), Pipeline Parallelism (PP), Context Parallelism (CP) and Sequence Parallelism (SP). These strategies communicate over two types of AI datacenter compute fabrics, each with distinct bandwidth requirements. First, Datacenter Networks (DCNs) provide hundreds of Gbps per GPU and primarily handle DP, PP, CP, and SP traffic, which has lower communication demands. Second, High-Bandwidth Domains (HBDs) offer Tbps-level bandwidth, which is crucial for communication-intensive TP and EP. Efficient HBD design can reduce communication overhead, thereby improving Model FLOPs Utilization (MFU) - a key performance metric for LLM training.

The community has made significant advancements in designing DCNs for LLM training [24, 52, 65, 80]. However, scaling HBD to optimize MFU in LLM training remains a challenging problem. Existing HBD architectures [33, 34, 55, 75, 77] take important steps but still suffer from fundamental limitations in scalability, cost, and fault resiliency.

- **Switch-centric HBDs**, such as NVIDIA NVL-72 [55], build multilayer non-blocking networks for HBD with switch chips. However, the switch fabric incurs superlinear cost growth as it scales, constraining the number of GPUs per HBD. This limitation prevents optimal large TP and EP and causes severe *resource fragmentation* when the size of TP/EP group increases. For instance, with 2 HBDs (32 GPUs each), 30 GPUs are wasted for TP-16 jobs if each HBD has a single GPU failure. This waste reduce to 14 GPUs if the two HBDs are combined into a 64-GPU unit.
- **GPU-centric HBDs**, such as Dojo [75], NVIDIA V100 [11], TPUv3 [34], and SiP-Ring [35], adopt low-cost GPU-to-GPU links to construct large-scale ring or mesh topologies, forwarding traffic directly through GPUs. However, these architectures suffer from a large *fault explosion radius*, where a single GPU

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failure degrades bandwidth for a group of adjacent GPUs, compromising the entire topology. For example, in SiP-Ring, one single GPU failure breaks the ring and reforms the topology into a line.

- **Switch-GPU Hybrid HBDs**, TPUv4 [33] alleviates the limitation of a large fault explosion radius via OCS-based switches[1]: each set of 64 TPUs is connected as a cube, with these cubes connected to multiple OCS-based switches to isolate faults within the cubes. However, it does not fundamentally resolve the issue, as the fault explosion radius remains large at the cube level (64 TPUs).

In this paper, we take a first-principles approach to redesigning HBD for LLM training workloads. Through a top-down analysis of parallelism strategies (§2.3) for maximizing MFU, we show that increasing TP size yields the most significant MFU gains for both dense and sparse LLM models. For large dense models [26], the optimal TP size scales from 16 to 64 as the number of GPUs increases. For sparse MoE models [12, 30, 73], enlarging TP improves MFU more effectively than EP, particularly when considering the expert imbalance problem [40].

These findings lead to two key design principles: i) HBD should be optimized exclusively for TP Ring-Allreduce communication with large message sizes, which communicates with only logical neighboring nodes, eliminating the need for EP and the associated any-to-any communication; ii) Supporting large and adaptable TP is essential, as different GPU numbers and model sizes require varying TP configurations to maximize MFU.

Based on these principles, we propose ***InfiniteHBD***, a scalable and fault-resilient HBD architecture designed for optimizing TP communication. Our key insight is *unifying connectivity and dynamic switching at the transceiver level* using OCS. By embedding OCS in each transceiver, we achieve reconfigurable point-to-multipoint connectivity. This marks a departure from traditional designs, where transceivers support only point-to-point connections and rely on high-radix switches for routing. We call this new design **transceiver-centric HBD architecture**. This transceiver-centric architecture offers two key benefits: i) It enables the flexible construction of arbitrarily large ring topologies by intra-node loopback mechanism. This can support optimal TP group sizes for different models, while effectively minimizing resource fragmentation; ii) When one node fails, its neighboring transceivers dynamically reconfigure connections to reroute traffic, significantly reducing the fault explosion radius and improving system resilience.

We realize the transceiver-centric HBD architecture in production by combining the following key ideas:

- *Silicon Photonics based OCS transceiver (OCSTrx):* To design a cost-effective low-power transceiver with OCS support, we leverage the current advances of Silicon Photonics (SiPh) technology. Compared to MEMS [78, 86] technology which has been widely used to realize OCS, SiPh offers simpler structures, lower cost and power consumption. We build OCS with Mach-Zehnder interferometer (MZI) matrix [83], taped out with 65nm CMOS processes. The chip area is smaller than 136.5mm^2 while the chip power consumption is 3.2$Watts$, which can be integrated into commercial QSFP-DD 800$Gbps$ transceiver [46] with 60-80 μs reconfiguration latency. *OCSTrx* introduces zero additional bit error rate in most cases, with an average insertion loss of 3.3dB at room temperature.
- *Reconfigurable K-Hop Ring Topology:* While OCSTrx offers reconfigurable connections at the transceiver level, constructing adaptive-size rings that maximize GPU utilization remains a challenge. For example, a naive full-mesh topology built with OCSTrx would impose strict limits on TP size, while also resulting in significant bandwidth waste and fragmentation. To address this, we propose a reconfigurable K-Hop Ring, where each node connects to all other nodes within $\leq K$ hops via *OCSTrx*. The intra-node *loopback* mechanism enables dynamic ring construction, while the inter-node *backup link* bypasses faulty nodes, ensuring high fault tolerance.
- *HBD-DCN Orchestration Algorithm:* While an optimal HBD topology is critical, end-to-end training performance also depends on efficient HBD-DCN coordination. For example, the orchestration of TP groups in HBD directly determines DP traffic distribution, which impacts congestion in DCN, ultimately governing training performance. Unfortunately, existing approaches lack mechanisms to jointly coordinate DCN and HBD to mitigate congestion and optimize communication efficiency. To address this, we propose a new orchestration algorithm that minimizes cross-ToR traffic, thereby minimizing congested traffic.

To the best of our knowledge, *InfiniteHBD* is the first HBD design capable of scaling to datacenter scale while avoiding cost explosion and increased failure-induced waste. We evaluated *InfiniteHBD* with the real 348-day fault trace from our 3K-GPU cluster[2]. When executing TP32 jobs with the trace, it demonstrates 0.53% GPU waste ratio - 20x and 14x lower than NVL-72 (10.04%) and TPUv4 (7.56%). It achieves 3.24x and 1.59x cost reductions compared to NVIDIA NVL-72 and Google TPUv4 respectively. Through the orchestration algorithm, it maintains near-zero cross-ToR traffic under 7% node failure rates. Its dynamic ring formation capability enables 3.37x higher MFU than NVIDIA DGX systems [62] (8 GPUs/node).

This work does not raise any ethical issues.

2 Background and Motivation

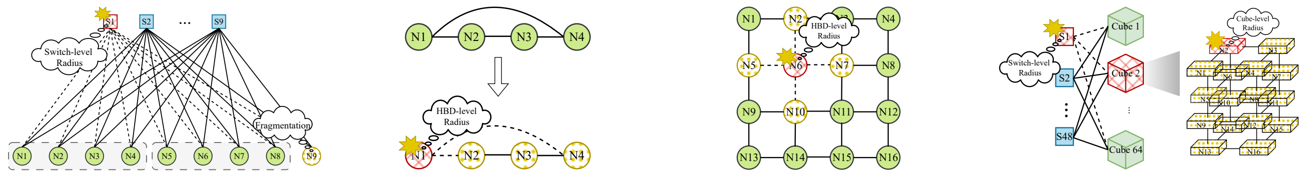
In this section, we first introduce LLM training in AI datacenters (DCs) (§2.1). Then, we examine existing High-Bandwidth Domain (HBD) architectures and discuss their limitations (§2.2). Finally, we summarize key design principles of HBD for LLM training (§2.3).

2.1 LLM Training in AI DC

LLM training parallelism and communication. LLM training jobs employ various parallelism strategies to efficiently utilize GPUs distributed across AI DCs [67, 71]. Based on communication loads, parallelism can be categorized into two types. The first type is *communication-intensive parallelism* which involves high communication load. Tensor Parallelism (TP) splits the model across multiple GPUs and synchronizes via AllReduce. The ring algorithm for AllReduce is theoretically optimal [60], making ring-based topologies

[1]In this paper, "OCS" specifically denotes *optical circuit switching capability*, while OCS-based switch denotes *optical circuit switch*.

[2]Details in Appendix §A. We have open-sourced this trace at https://github.com/stepfun-ai/InfiniteHBD-Trace.



(a) Switch-centric: NVL36 **(b) GPU-centric: SiP-Ring** **(c) GPU-centric: Dojo** **(d) Hybrid: TPUv4**

Figure 1: Illustrative examples of HBD architectures. N represents Node, and S represents Switch. Red (with cross hatch) represents fault device and yellow (with dots) represents unavailable or downgraded GPU.

Architecture	Type	Scalability	Collective Primitives	Fault Explosion Radius Node-Side	Fault Explosion Radius Switch-Side	Interconnect Cost	Fragmentation
NVL	Switch-centric	Low	Full CCL	Node-level	Switch-level	High	Many
Dojo, TPUv3, SiP-Ring	GPU-centric	High	Ring-Allreduce	HBD-level	✗	Low	Few
TPUv4, TPUv5p	Switch-GPU Hybrid	Moderate	Ring-Allreduce	Cube-level	Switch-level	Moderate	Few
InfiniteHBD	Transceiver-centric	High	Ring-Allreduce	Node-level	✗	Low	Few

Table 1: Comparative analysis of HBD architectures.

ideal for TP. Expert Parallelism (EP), designed for Mixture of Experts (MoE) models [12, 30, 73], assigns experts to different GPUs and relies on AlltoAll communication, requiring topologies with high bisection bandwidth (e.g., Full-Mesh). In contrast, parallelism strategies such as Data Parallelism (DP), Pipeline Parallelism (PP), Context Parallelism (CP), and Sequence Parallelism (SP) introduce lower communication overhead, placing less demands on network performance.

Compute fabric. Compute fabric in AI DC interconnects GPUs to efficiently transmit model gradients and parameters. It consists of two primary components: Datacenter Network (DCN) and High-Bandwidth Domain (HBD). DCN provides communication across the entire AI DC via Ethernet or Infiniband, the bandwidth is around $200 \sim 800Gbps$. Widely used DCN architectures include Fat-Tree [2] and Rail-Optimized [52]. In comparison, HBD offers Tbps-level throughput, and is more suitable for TP/EP. However, its scale is typically constrained by interconnection costs and fault tolerance considerations. For example, NVL-72 [55] only interconnects 72 GPUs per HBD.

Faults and fault explosion radius. As revealed by current advances of AI DCs [24, 65], training jobs experience a variety of faults, such as GPU faults, optical transceiver faults, switch faults, and link faults. We quantify the fault impact using the *fault explosion radius*, defined as *the number of GPUs degraded by a single fault event*. The fault explosion radius varies depending on both the system architecture and the fault component. For example, if a switch fails, the bandwidth of all devices connected to it will degrade, illustrating the switch-level fault explosion radius.

HBD fragmentation. When the number of GPUs in the HBD cannot be evenly divided by the size of the parallel group (i.e., TP size), the remaining GPUs become unusable, leading to resource waste. The GPU waste ratio for each HBD can be expressed by the formula $\{(HBD_{size} - N_{fault}) \mod TP_{size}\}/HBD_{size}$. In AI DCs with small-scale HBDs, GPU waste due to fragmentation is significant because each HBD experiences independent fragmentation. This issue worsens as the TP group size increases with model scale. For example, for NVL-36 shown in Figure 1a, running TP-16 causes $\geq$11% GPU waste ratio.

2.2 Limitations of Existing HBDs

Existing HBD architectures for LLM training can be categorized into three types, based on the key components that provide connectivity. A summary is shown in Table 1.

Switch-centric HBD. This type of architecture leverages switch chips to interconnect GPUs, as shown in Figure 1a. A prominent example is NVIDIA, which utilizes NVLink and NVLink Switch [50, 57], e.g., DGX H100 [62] with 8-GPU and GB200 NVL-36, NVL-72, and NVL-576 [55]. These architectures offer high-performance any-to-any communication. However, switch-centric HBDs have several drawbacks: i) They require a large number of switch chips due to their limited per-chip throughput; ii) They are vulnerable to a switch-level fault explosion radius—when a switch chip fails, all connected nodes experience bandwidth degradation; iii) High interconnect costs constrain the scale of HBDs, leading to significant fragmentation when serving large models.

GPU-centric HBD. GPU-centric HBD architectures construct the HBD using direct GPU-to-GPU connections, eliminating the need for switch chips. As a result, cost scales linearly with HBD size. A representative example is SiP-Ring [35], shown in Figure 1b, where GPUs are organized into fixed-size rings. However, this design imposes a strict limitation: the TP group size must remain fixed. To enable communication at dynamic scales and support a wider range of workloads, more complex topologies are adopted (e.g., Dojo [75], NVIDIA V100 [11], TPUv3 [34], and AWS Trainium [77]), which support dynamic scaling by allowing jobs to execute on topology subsets of varying sizes. As shown in Figure 1c, Dojo [75] connects GPUs via mesh-like topologies and employs GPUs to forward traffic. While GPU-centric architectures mitigate cost explosion and can support various scales, they suffer from a large fault explosion radius. A single GPU failure can disrupt the entire HBD by altering its connectivity, degrading communication performance even for healthy GPUs—such as the yellow GPUs in Figure 1c.

Switch-GPU Hybrid HBD. This architecture interconnects GPUs via a combination of direct GPU-to-GPU connections and switch links. A typical example is TPUv4 [33], which organizes TPUs into 4^3 TPU cubes and connects them via centralized OCS-based switches (Figure 1d). TPUv4 scales up to 4,096 TPUs, with its expansion primarily limited by the port count of the OCS-based switch. Furthermore, it suffers from a cube-level fault explosion radius—a failure in any single TPU affects the entire 64-TPU cube, leading to significant performance degradation. Furthermore, OCS-based switches face challenges of high costs and manufacturing complexity, which undermines the cost-effectiveness of TPUv4. TPUv5p cluster [25] is similar to TPUv4 but can scale out to 8,960 TPUs.

2.3 Key Attributes of An Ideal HBD

GPU	TP	PP	DP	MFU	MFU$_{TP-8}$	Improve
1024	16	4	16	0.5236	0.5217	1.0036
4096	16	8	32	0.4668	0.4282	1.0901
8192	32	8	32	0.4247	0.3512	1.2093
16384	32	16	32	0.3756	0.2584	1.4536
32768	32	16	64	0.3090	0.1690	1.8284
65536	64	16	64	0.2493	0.0999	2.4955
131072	64	16	128	0.1851	0.0550	3.3655

Table 2: Optimal parallelism strategy for maximum MFU of Llama 3.1-405b, compared to the baseline MFU for TP-8 (e.g., in widely-deployed NVLink architectures), when GPU number varies.

Existing HBD architectures face fundamental limitations in interconnection cost, resource utilization, and failure resiliency when scaling. To guide a better design, we analyze existing training workloads and explore two key questions without the limitations imposed by current HBD: i) What is the optimal group size that HBD should support? ii) What traffic patterns should HBD accommodate?

Large and adaptable TP size is critical for dense models. The optimal LLM training parallelism depends on model architectures and cluster configurations. For example, as illustrated by previous work [87, 88]. We evaluate the Model FLOPs Utilization (MFU) for Llama 3.1-405B [44] using our in-house LLM training simulator (§6.3) and report the results in Table 2. MFU and TP/PP/DP columns denote the optimal MFU when TP size is unconstrained and the corresponding parallelism strategies respectively. MFU_{TP-8} column denotes the optimal MFU when TP size is limited to 8. As we increase the number of GPUs, the optimal TP size grows from 16 to 64, a trend we observe across other large dense models. In this case, the HBD scale restricts the maximum size of TP, which affects training performance as a result.

Parallelism	Operation	Traffic Load
TP	AllReduce	$2bsh \cdot \frac{n-1}{n}$
EP	AllToAll	$2bsh \cdot \frac{n-1}{n} \cdot \frac{k}{n}$

Table 3: Communication load of TP and EP on a single MoE layer. *b*: batch size; *s*: sequence length; *h*: hidden dim; *k*: topK of MoE router; *n*: parallel size. Assume each expert is assigned equal number of tokens.

MoE can also be efficient with large-size TP. Beyond widely used dense models, we also examine sparse MoE models, which are trending toward larger scales (e.g., 1T parameters [15]). The distributed training for MoE can be achieved through TP or EP (or a combination of them)[3] [40], both TP and EP are communication-intensive [36], making them heavily reliant on HBD.

	TP	EP			
imbalance coef	-	0%	10%	20%	30%
MFU (%)	31.2	31.5	30.5	29.8	28.8

Table 4: Performance comparison of TP and EP when training GPT-MoE.

Our production training experience on a 1T MoE model in production brings the following insights into the pros and cons of TP and EP. On the one hand, EP is more communication-efficient than TP. Table 3 compares the communication volume of TP and EP. Clearly, EP is better if $k < n$, which is common [12] because existing models often choose small k for higher computation sparsity. On the other hand, EP suffers from the well-known expert imbalance problem [40], especially when the MoE routers use the no-token-left-behind algorithm [12, 13, 23]. This will result in a non-equivalent number of tokens that each expert will receive, which hence causes straggler nodes that waste GPU cycles of other nodes. Table 4 shows the simulated result of training GPT-MoE with 1.1T parameters (details in Appendix §B) under different expert imbalance coefficients[4]. When $coef = 0$, EP is better than TP due to smaller communication overhead. As $coef$ increases, the MFU drops because of the straggler issue.

Key findings. These experiments provide us with two key findings for HBD design. First, larger HBD size is increasingly needed for rapidly scaling LLMs (i.e., more than 1T parameters). Second, with larger HBD enabled, using TP is more favorable than EP to train an MoE model, because TP shards the computation equally across GPUs and hence bypasses the expert imbalance problem.

These findings reveal two key design principles for HBD: i) HBD must inherently support large and adaptable TP sizes, which fundamentally requires the scalability of HBD architecture; ii) the HBD designs need to ensure the effective support for the Ring-AllReduce communication. Given the demonstrated efficiency of TP in MoE training, ensuring support for Ring-AllReduce is sufficient for mainstream LLM training scenarios; iii) small fault explosion radius. Thus, ***we propose designing a large and adaptable HBD architecture tailored for ring-based TP communication to optimize LLM parallelism strategies.***

3 Design Overview

In this section, we first present our new HBD architecture *Infinite-HBD* guided by the design principles outlined above. We then provide an overview of its key components.

Transceiver-centric HBD architecture. As discussed in §2.2 and summarized in Table 1, existing architectures face a fundamental tradeoff among scalability, cost, and fault isolation. The GPU-centric architecture offers high scalability and low cost connectivity but suffers from a large fault explosion radius. In contrast, the switch-centric architecture improves fault isolation by leveraging centralized switches to confine failures to the node level. However, this

[3]For TP, each expert is equally sharded to GPUs. For EP, each expert is indivisible and allocated to one GPU in the EP group.

[4]Calculated as $\frac{max-min}{max}$, where max and min represent the maximum and minimum tokens allocated to each expert respectively.

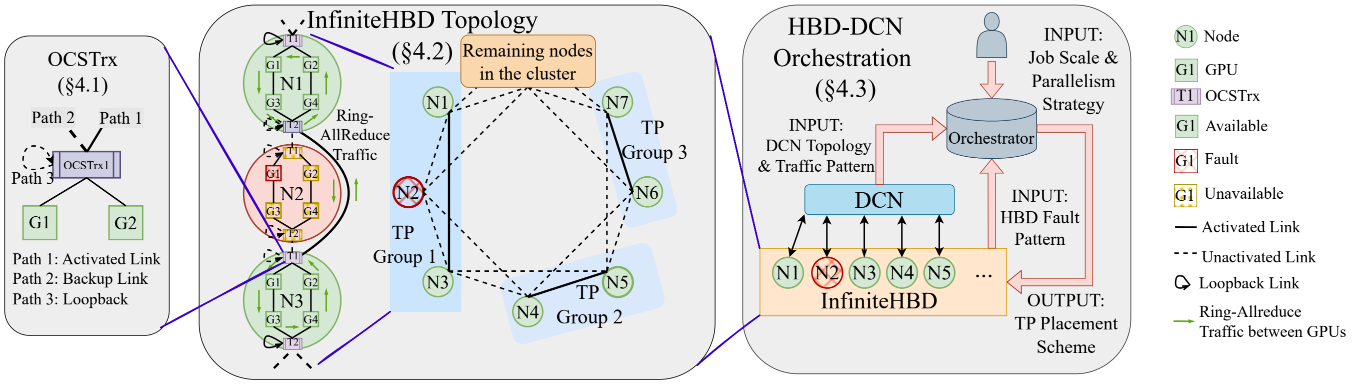
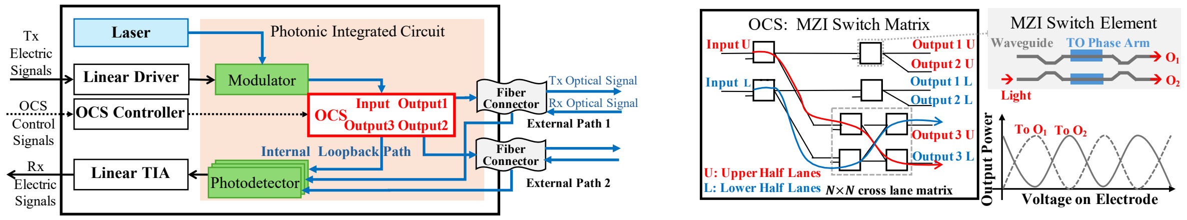


Figure 2: *InfiniteHBD* overview.



(a) Components of OCS transceivers. **(b) Zoom into OCS MZI switch matrix.**

Figure 3: Design of OCS Transceivers. The core component is OCS integrated in transceivers.

comes at the cost of reduced scalability and higher connection overhead. The GPU-switch hybrid architecture takes a middle-ground approach but still suffers from significant fault propagation. As a result, no existing architecture fully meets all requirements.

Our key insight is that *connectivity and dynamic switching can be unified at the transceiver level* using Optical Circuit Switching (OCS). By embedding OCS within each transceiver, we can enable reconfigurable point-to-multipoint connectivity, effectively combining both connectivity and switching at the optical layer. This represents a fundamental departure from conventional designs, where transceivers are limited to static point-to-point links and rely on high-radix switches for dynamic switching. We refer to this novel design as the *transceiver-centric HBD architecture*.

We realize this design with *InfiniteHBD*, which has three key components as shown in Figure 2.

Design 1: Silicon Photonics based OCS transceiver (OCSTrx) (§4.1). To enable large-scale deployment, we require a low-cost, low-power transceiver with Optical Circuit Switching (OCS) support. Unlike prior high-radix switches solutions that rely on MEMS-based switching [78, 86], we leverage advances in Silicon Photonics (SiPh), which offer a simpler structure, lower cost, and reduced power consumption—making them well-suited for commercial transceivers.

Our SiPh-based OCS transceiver (OCSTrx), shown on the left side of Figure 2, provides two types of communication paths: i) *Cross-lane loopback path (path 3)*, enabling direct GPU-to-GPU communication within the node, which can be used to construct dynamic size topologies; ii) *Dual external paths (path 1&2)*, connecting to external nodes. All these paths utilize time-division bandwidth allocation, featuring 60-80 μs reconfiguration latency. With this capability, our *OCSTrx* allows the dynamic reallocation of full GPU bandwidth to a single active external path, rather than splitting it across multiple paths. This eliminates redundant link waste—for instance, activating one external path completely disables the other, ensuring efficient bandwidth utilization.

Design 2: Reconfigurable K-Hop Ring topology (§4.2). With *OCSTrx* that provides reconfigurable connections at the transceiver, the next challenge is designing the topology. A naive starting point is the full-mesh topology [59] which can provide full connectivity among all nodes using *OCSTrx* . However, full-mesh design requires $O(N^2)$ links, inducing prohibitive complexity and cost. To reduce costs while maintaining near-ideal fault tolerance and performance, we prune the full-mesh topology into a K-Hop Ring topology based on traffic locality and fault non-locality (Details in §4.2). The topology's cost and wiring complexity grow linearly with node count, enabling high scalability. Combining the reconfigurability of *OCSTrx*, we propose a *reconfigurable K-Hop Ring topology*, shown in the middle of Figure 2, which consists of two key parts:

i) *Intra-node topology:* dynamic GPU-granular ring construction is enabled by activating loopback paths. For example, while N_1-N_3 physically form a line topology, activating loopback paths creates a ring between N_1's GPUs (1–4) and N_3's GPUs (1–4). This mechanism allows for the construction of arbitrary-sized rings at any location, supporting optimal TP group sizes for different models while effectively minimizing resource fragmentation.

ii) *Inter-node fault isolation:* dual external paths connect to primary and secondary neighbors (e.g., 2-Hop Ring). When a node fails (e.g., N_2), its neighbor (N_1) activates the backup path (N_1-N_3) to bypass the fault while maintaining full bandwidth, thus reducing the fault explosion radius to the node-level. §4.2 generalizes this design to $K > 2$.

Design 3: HBD-DCN Orchestration Algorithm (§4.3). Designing an optimal HBD topology is crucial, but end-to-end training performance also depends on the efficient coordination between HBD and DCN. For instance, improper orchestration of TP groups can cause DP traffic to span across ToRs, resulting in DCN congestion. However, existing methods lack the ability to jointly optimize HBD and DCN coordination to alleviate congestion and enhance communication efficiency. To address this, we propose the HBD-DCN Orchestration Algorithm, as shown on the right side of Figure 2. The orchestrator takes three inputs: the user-defined job scale and parallelism strategy, the DCN topology and traffic pattern, and the real-time HBD fault pattern. It then generates the TP placement scheme, which maximizes GPU utilization and minimizes cross-ToR communication within the DCN.

4 *InfiniteHBD* Design

This section first introduces the innovative design of OCS transceivers (OCSTrx) based on Silicon Photonics (SiPh) chips (§4.1), a key enabler for *InfiniteHBD*, providing both cost efficiency and reconfigurability. Next, we present the DC-scale *InfiniteHBD* topology design (§4.2) based on OCSTrx. Finally, we outline the HBD-DCN orchestration algorithm (§4.3), designed to optimize communication efficiency for training jobs.

4.1 SiPh-based OCS transceiver (OCSTrx)

The *OCSTrx* is designed for reconfigurable point-to-multipoint connectivity. It incorporates a compact OCS-based switch with three Rx/Tx paths, utilizing the MZI switch [83] micro-structure with thermo-optic (TO) effect [29] phase arms. This OCS-based switch is seamlessly integrated into the Photonic Integrated Chip (PIC) of the transceiver, serving as the MZI switch matrix within the Tx light path, and providing photodetector (PD) modules for each Rx path.

SiPh-Based OCS. Currently, there are two predominant technological approaches for OCS. Micro Electromechanical systems (MEMS) [78, 86] are attractive for commercial adoption because they support large port radix, up to a 320×320 matrix [7]. Another option is SiPh-based OCS. Its structure is simpler and cheaper to manufacture, the limitation is its radix due to optical losses in the multistage light path selector. Given that the locality of traffic and external paths count of *OCSTrx* is only two, SiPh-based OCS offers greater advantages.

So we choose the design of an SiPh-based OCS using the MZI micro-structure [83]. The basic mechanism of MZI switch elements is controlling the phase difference between light paths in two phase arms, and then directs the output light to specific ports through interference at the output combiner. TO effect is utilized for phase arm control, for lower reconfiguration latency compared to MEMS.

OCS Micro-Structure Design. As shown in Figure 3a, the initial routing decision is made by two MZI switch elements, determining whether to direct the signal through external output 1&2, or the internal loopback path. Subsequently, an internal $N \times N$ MZI switch matrix is incorporated to facilitate the cross-lane loopback mechanism, exemplified by the blue and red paths. Notably, this design can reduce stages count and light attenuation of output 1&2, while ensuring consistent light attenuation for them. The design is implemented on the Photonic Integrated Circuit (PIC) chip.

Transceiver Design. In *OCSTrx*, the Tx electrical signal is amplified by linear driver and converted to optical signal by modulators as in Figure 3. One laser is coupled into the PIC as the optical source. On the receiving end, multiple photodetectors capture the Rx optical signal from all available paths separately. The output from the activated photodetector is then amplified by a linear transimpedance amplifier (TIA). *OCSTrx* offers significant benefits, including high compactness, low power consumption, and cost-effective mass production. Moreover, *OCSTrx* is integrated into commercial transceivers, and its failures manifest as regular transceiver failures without introducing new failure patterns.

4.2 *InfiniteHBD* Topology

In this section, we present the *InfiniteHBD* topology design (Figure 2) integrating *OCSTrx* that allows all GPUs within the datacenter to be connected in a *reconfigurable K-Hop Ring topology*, while supporting dynamic ring construction and high fault tolerance.

Intra-node Topology. The intra-node topology is designed for *dynamic ring construction* and complies with the OCP UBB 2.0 standard [58]. As shown in Figure 4, one node equipped with R GPUs can support R bundles of *OCSTrx*. Each *OCSTrx* bundle is connected to a pair of GPUs, with one GPU linking to the upper-half SerDes and the other to the lower-half. For one group of nodes connected as one line, the two GPU pairs at each end can interconnect with the *OCSTrx* internal loopback path, forming a GPU-level ring. As shown in Figure 2, nodes N_1 and N_3 are connected in a line, where $OCSTrx_1(N_1)$ and $OCSTrx_2(N_3)$ activate the cross-lane loopback path, creating a ring between the 8 GPUs of N_1 and N_3. During ring construction, only two *OCSTrx* bundles per node are utilized, while the remaining *OCSTrx* operate in loopback mode. These idle *OCSTrx* can be replaced with direct connections, such as DAC links, offering a trade-off between cost and reliability. Figure 5(a,b) shows a 4-GPU node with varying numbers of *OCSTrx* bundles. Note that the topology design in this section utilizes a 4-GPU node as an example; it can be easily scaled for 8-GPU nodes.

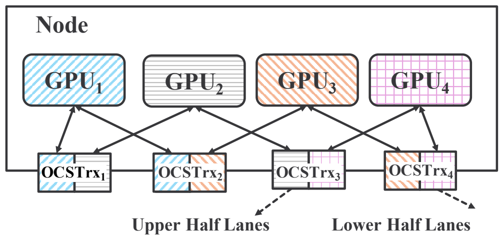
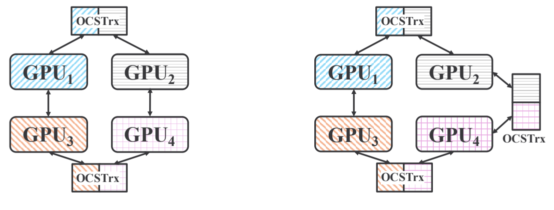


Figure 4: *OCSTrx* connection within nodes. Each block contains multiple *OCSTrx* as one bundle, e.g., $8 \times 800Gbps$ ***OCSTrx* for a 6.4Tbps GPU.**

Inter-node Topology. We construct the inter-node topology by pruning the full-mesh design, based on two key observations: i) *Traffic locality*: TP Ring-AllReduce in HBD exhibits neighbor communication patterns, eliminating the need for distant connections; ii) *Fault non-locality*: node-side failures typically occur independently at the node level, meaning consecutive multi-node failures follow an exponentially decaying probability. Each node provides up to $2R$ external paths, allowing us to construct a DC-scale reconfigurable K-Hop Ring topology ($K \leq R$) by connecting them to nodes at $\pm1, ..., \pm K$ ($K \leq R$). Under this design, each node has a degree of $2K$, which is sufficient for traffic locality and tunable via

OCSTrx count and intra-node design. For AllReduce communication, only two out of the $2K$ links are simultaneously activated, with the others serving as backup links for fault isolation. For example (Figure 2), if N_2 fails, $OCSTrx_2(N_1)$ and $OCSTrx_1(N_3)$ can switch to backup links, maintaining connectivity between N_1 and N_3 while isolating N_2's fault. As K increases, the probability of encountering an unbypassed failure rapidly decreases, which is nearly negligible for $K = 3$ (detailed analysis in Appendix §C). Thus, this architecture typically achieves a node-level explosion radius. Moreover, the K-Hop Ring can be broken into the K-Hop line topology, with the trade-off of reduced fault tolerance, affecting the $2K$ nodes at both ends.



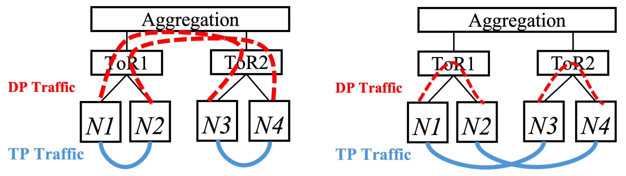
(a) 2 bundles of *OCSTrx* **(b) 3 bundles of *OCSTrx***

Figure 5: 4-GPU node with *OCSTrx*.

4.3 HBD-DCN Orchestration Algorithm

InfiniteHBD is designed to work with arbitrary DCNs, including Rail-Optimized [52, 65] and Fat-Tree [2]. This section co-optimizes communication performance for both HBD and DCN in *InfiniteHBD*.

Problem Statement. In *InfiniteHBD*, GPUs communicate without routing traffic, preventing congestion at any scale. In contrast, DCNs experience inevitable congestion, leading to performance degradation. To mitigate this, we leverage traffic locality to orchestrate nodes, minimizing cross-ToR traffic. Given a job J requiring N nodes from an available pool of M ($M \geq N$), we must select and order N nodes to satisfy two requirements: (1) nodes in the same TP group should communicate via *InfiniteHBD*, and (2) other parallel traffic should be arranged to minimize congestion. Ideally, communication remains within the same ToR, confining congestion to switch-to-node links.



(a) Orchestration scheme 1. **(b) Orchestration scheme 2.**

Figure 6: Illustration of the node orchestration problem statement.

A naive approach is sorting nodes based on deployment order in *InfiniteHBD*, fulfilling the first requirement but not the second. As shown in Figure 6a, this method places (N_1, N_2) in the same TP group and (N_1, N_3) in the same DP group, forcing DP traffic across ToRs. A better scheme (Figure 6b) eliminates cross-ToR traffic and congestion. However, considering failures and multiple parallel dimensions complicates orchestration, necessitating an efficient method.

Our key insight is to arrange nodes in *InfiniteHBD* based on DCN traffic locality, prioritizing appropriate network distances over minimal ones. For example, in Figure 6b, N_1's *InfiniteHBD* neighbor is N_3, despite a 3-hop network distance in DCN. We propose a two-phase solution: (1) a deployment phase defining physical connections in DCN and *InfiniteHBD*, and (2) a runtime phase using an algorithm to orchestrate nodes for arbitrary-scale jobs.

Algorithm 1: Orchestration For Fat-Tree

```
Input: Topology of DCN and HBD $G$, Faulty Node Set $F$, Job
       Information $J$.
Output: Placement scheme that satisfies job scale and minimizes
        cross-ToR traffic.
Create graph
  $G_{deploy} =< S_{deploy}, E_{deploy} >=$ Deployment-Strategy($G$);
Initialize $high = n_{allconstraints}$, $low = 0$, $placement = \{\}$;
while $low \leq high$ do
    $mid = \lfloor \frac{low+high}{2} \rfloor$;
    $placement$ = Placement-Fat-Tree($G_{deploy}, mid, F, J$);
    if $placement$ satisfies job $J$ then
        $low = mid + 1$;
    else
        $high = mid - 1$;
return $placement$
```

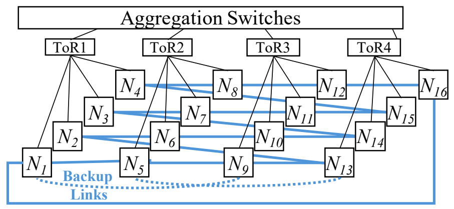


Figure 7: Illustration of the deployment phase, showing only two backup links for simplicity.

Deployment Phase. Figure 7 shows node deployment in HBD and DCN. *InfiniteHBD* connects nodes at a network distance of 3 (i.e., cross-ToR). In a DCN with r nodes per ToR, node N_n connects to $N_{n\pm r}$ as main links, while backup links connect to $N_{n\pm 2r}$. For $1 < n \leq r$, N_n connects to $N_{D+n-r-1}$, where D is the total node count (e.g., N_3 connects to N_{14}). Additionally, N_1 may link to the last node, forming a ring.

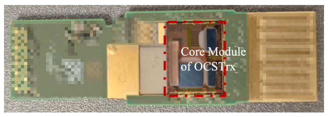
Runtime Phase. Without considering DCN topology, *InfiniteHBD* orchestrates nodes in three steps: (1) identifying cluster faults and modeling healthy nodes as a graph, (2) using Depth-First Search to find connected components, and (3) sequentially placing TP groups within these components. Due to *InfiniteHBD*'s topology, each TP group forms a ring.

For real-world DCNs, topology constraints refine step (2) and (3). In Fat-Tree networks, congestion arises when (1) a TP group spans multiple Aggregation-Switch domains, or (2) GPUs within a ToR have mismatched TP group ranks, forcing DP, CP, PP, SP traffic across ToRs. Thus, we aim to localize TP groups within the same Aggregation-Switch domain and align ranks within each ToR. Our scheduling algorithm minimizes cross-ToR traffic while meeting job scale requirements via a binary search over constraint variables. Algorithm 1 outlines the approach, with full details in Appendix §D.

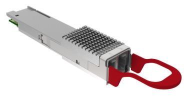
5 Hardware and Small-Scale Cluster Evaluation

5.1 *OCSTrx* Hardware Evaluation

Following the design principles outlined in §4.1, we have successfully implemented *OCSTrx*, a fully integrated module within a QSFP-DD 800Gbps transceiver, as illustrated in Figure 8. As depicted in Figure 9, *OCSTrx* integrates an OCS Controller Chip and a Photonic Integrated Circuit (PIC) that includes an MZI switch matrix. The Controller Chip, measuring $4mm \times 4mm$, is manufactured using a 28nm process, while the PIC, sized at $10.5mm \times 13mm$, uses a 65nm CMOS process. *OCSTrx* supports 8 pairs of TX/RX SerDes at each end and has been validated for compatibility with various link layer protocols, including PCIe (32Gbps, 64Gbps) and Ethernet (56Gbps, 112Gbps). *OCSTrx* has also passed temperature cycling tests, validating its reliability and availability.



(a) Main hardware components.



(b) Packaged module.

Figure 8: *OCSTrx* integrated in QSFP-DD 800Gbps transceiver.

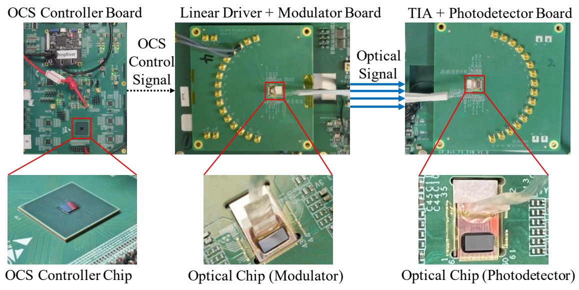


Figure 9: Evaluation board for components of *OCSTrx*.

Reconfiguration latency. Experimental results show that *OCSTrx* achieves a reconfiguration latency of 60–80 μs, which is significantly faster than traditional centralized OCS-based switches employing MEMS [78], Piezo [63], or Robotic [74] mechanisms, whose latencies typically range from milliseconds to minutes. Notably, this measurement excludes software-level delays such as reconnection at the network protocol layer.

Insertion loss. We evaluated the insertion loss of the core module within *OCSTrx*, which provides the OCS capability, under various ambient temperatures. Figure 10a summarizes the statistical results, while Figure 11 shows the distribution. The measured insertion loss ranges from 2.5 dB to 4.0 dB, with an average of 3.3 dB at room temperature (25°C).

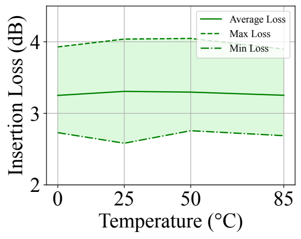
Power consumption. Under the $8 \times 112G$ configuration, the peripheral circuitry consumes 8.5 *Watts*. We further measured the power consumption of *OCSTrx*'s core module which provides the OCS capability across different temperatures when activating three paths (two external paths and one internal loopback), as illustrated in Figure 10b. Across all conditions, the core module consumed less than 3.2 *Watts*, keeping the total power below 12 *Watts*, meeting the QSFP-DD 800Gbps specification [49].

Bit error rate. With the Amplitude Control (AC) driving power set to 620 mW, we measured the bit error rate (BER) of *OCSTrx* under different optical modulation amplitudes (OMAs) and ambient temperatures, as shown in Figure 12. At -5°C and 25°C, BER was consistently 0. At 50°C and 75°C, BER remained 0 in most cases, with occasional errors only at very low OMAs. These results confirm compliance with the industrial BER threshold.

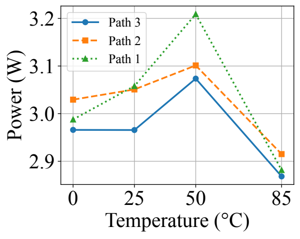
5.2 Small-Scale Cluster Evaluation

We constructed a small-scale cluster to evaluate the communication performance of the ring topology. Using 32 experimental GPUs equipped with inter-host HBD support (96 lanes on PCIe 4 protocol), we formed a physical ring utilizing fixed optical modules. This mini-cluster was manually reconfigured for both 32-GPU and 16-GPU ring topologies. The communication latency and AllReduce performance are evaluated. For small packets, direct GPU-to-GPU links reduced latency by approximately 13% compared to the NVLink switch design. For large packets, the 16-GPU AllReduce utilized 77.11% of the ring bandwidth, with the utilization rate increasing to 77.26% for the 32-GPU configuration, showing minimal degradation with scaling. In comparison, the NVIDIA H100 8-GPU machine achieves an 81.77% utilization rate without SHARP.

Additionally, a control plane is included to manage the *Infinite-HBD*. At the device level, the **node fabric manager** configures individual *OCSTrx* modules and handles topology switching. At the system level, **cluster manager** coordinates global control across the cluster. As control-plane mechanisms are not the focus of this work, we omit further details.



(a) Insertion loss.

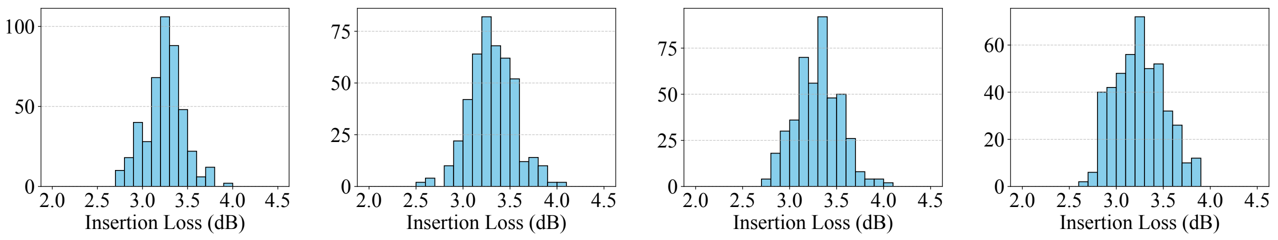


(b) Power consumption.

Figure 10: Insertion loss and power consumption of the core module in *OCSTrx*.

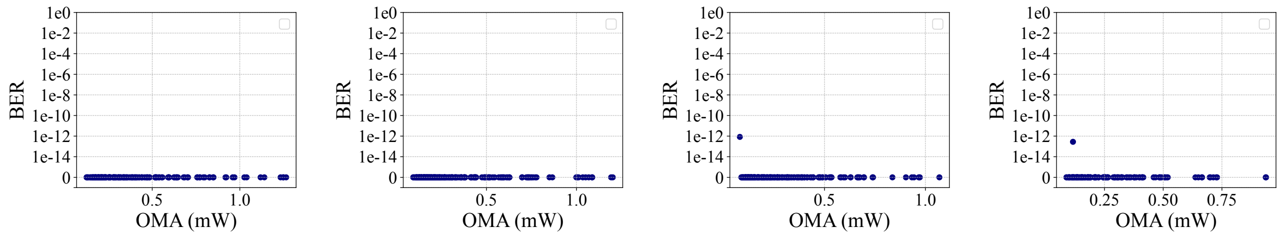
6 Large-Scale Simulation

We begin by outlining the experimental methodology and setup (§6.1). Next, we assess fault tolerance across different HBD architectures (§6.2), followed by end-to-end simulations to evaluate training performance under varying parallelism and GPU resource allocations (§6.3). We then examine the improvements in communication efficiency achieved by our orchestration algorithm (§6.4). Finally, we present a comparative cost and power analysis of different HBD



(a) 0°C. **(b) 25°C.** **(c) 50°C.** **(d) 85°C.**

Figure 11: Insertion loss distribution of the core module in *OCSTrx* under different ambient temperatures.



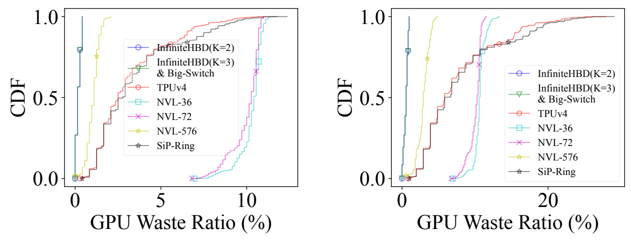
(a) -5°C. **(b) 25°C.** **(c) 50°C.** **(d) 75°C.**

Figure 12: Bit error rate of *OCSTrx* under varying OMA and ambient temperatures.

architectures (§6.5). The simulations demonstrate that *InfiniteHBD* outperforms other architectures across all metrics.

6.1 Methodology and Setup

An in-house simulator dedicated to LLM training is used to evaluate *InfiniteHBD* comprehensively. The simulator supports end-to-end simulations of both model training performance and hardware faults, with the HBD-DCN orchestration algorithm seamlessly integrated into the system.



(a) TP-16. **(b) TP-32.**

Figure 13: CDF of GPU waste ratio over 4-GPU node based on production fault trace.

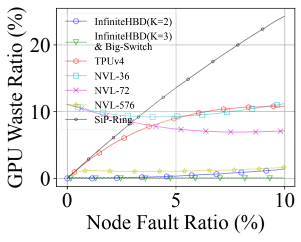
GPU and network specification. The NVIDIA H100 [56] (989 TFLOPS, 80GiB) is used as the configuration of GPU in simulation. The HBD bandwidth of GPU is set to 6.4*Tbps*, which is the sum of 8 QSFP-DD *OCSTrx*. The DCN bandwidth is configured to match the NVIDIA ConnectX-7 (400*Gbps*). Since the simulation primarily focuses on HBD, the DCN is configured as a Fat-Tree topology [2]. Several HBD architectures are then evaluated, including:

- **Big-Switch**: The ideal HBD design, featuring a large centralized switch with no forwarding latency that connects all nodes, as the theoretical upper limit of communication performance and fault resilience.
- ***InfiniteHBD***: Two configurations are evaluated: the *OCSTrx* bundle is set to either $K = 2$ or $K = 3$ (§4.2), constructing 2/3-Hop Ring respectively.
- **NVL-36, NVL-72, NVL-576** [55]: HBDs with 36, 72, or 576 GPUs, GPUs are interconnected via NVLink Switches.
- **TPUv4** [33]: Centralized OCS capable of scheduling with a 4^3 TPU cube granularity.
- **SiP-Ring** [35]: All nodes are connected in a series of static rings with fixed sizes equal to the TP sizes.

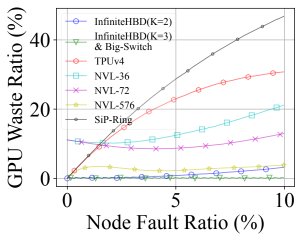
GPU count per node. The simulation aligns with both 4-GPU node (e.g., NVIDIA GB200 NVL-36/72/576 [55] and TPUv4 [33]) and 8-GPU node designs (NVIDIA H100, AMD MI300X [3], Intel Gaudi3 [10], and UBB 2.0 standard [58]).

Parallelism strategy. Since *InfiniteHBD* is primarily designed for TP, the key variable is the TP size. TP-8, TP-16, TP-32, and TP-64 are tested to evaluate the fault resilience of various HBD architectures (§6.2). Additionally, other parallelism strategies, such as PP and DP, are used to simulate cross-ToR traffic and evaluate the orchestration algorithm (§6.4).

Fault patterns. The fault trace used in the simulation was collected from an 8-GPU node cluster with approximately 3K-GPUs over 348 days. On average, the ratio of faulty 8-GPU nodes is 2.33%, with the P99 value as 7.22%, more details in Appendix §A. In some simulations, fault traces generated based on this trace statistics are also derived.



(a) TP-16.



(b) TP-32.

Figure 14: GPU wastes ratio over the 4-GPU node with different GPU fault ratio based on fault model.

6.2 HBD Fault Resilience

This section evaluates the fault resilience of various HBD architectures, focusing on GPU waste ratio, job fault-waiting time, and the maximum job scale supported by the cluster. The main text presents the key results, with more detailed results provided in Appendix §E.

GPU waste. Apart from faulty GPUs, issues such as fragmentation, topology disconnections, and bandwidth degradation can render healthy GPUs wasted. The GPU waste ratio quantifies the number of wasted GPUs under different fault scenarios. Figure 13 illustrates GPU waste ratios over production trace, while Figure 14 depicts the GPU waste ratio as node fault ratio varies.

GPU Num	TP	DP	PP	EP	MFU
1024	16	16	4	1	0.4276
2048	16	16	8	1	0.4140
4096	32	16	8	1	0.3894
8192	32	16	16	1	0.3656
16384	64	16	16	1	0.3116

Table 5: Optimal parallelism strategies for maximizing MFU of GPT-MoE under varying GPU numbers.

In these scenarios, *InfiniteHBD* ($K = 3$) achieves near-zero GPU waste ratio, and outperforms all other architectures. Especially, the waste ratio for *InfiniteHBD* ($K = 2$) remains almost identical to that of *InfiniteHBD* ($K = 3$), allowing one bundle of *OCSTrx* to be saved for clusters with low fault rates. NVL-36 and NVL-72 typically experience an 11% waste ratio for TP sizes of 16 or larger, as 1/9 of GPUs are reserved for redundant backups. NVL-576 has less fragmentation, benefiting from its larger size. TPUv4 performs well at low fault ratios and small TP sizes, but significantly degrades with larger TP sizes due to its coarse 4^3 cube-based resource management, which amplifies the fault explosion radius. To sum up, *InfiniteHBD* demonstrates the strongest fault resilience among all architectures.

Maximum job supported. In fixed-size clusters, large jobs must pause when the available GPUs drop below the required count. Faced with the same fault rate, clusters with lower GPU waste ratio can support larger job scales. Figure 15 shows the maximum job scale supported for various HBD architectures cluster with 2,880-GPU, simulated with the fault traces normalized for 4-GPU nodes. *InfiniteHBD* ($K = 2$ or $K = 3$) and NVL-576 lead in performance, and SiP-Ring exhibits declining efficiency as TP size increases.

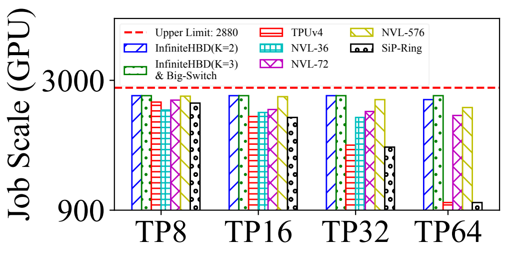
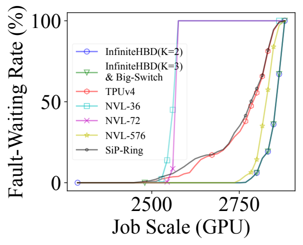


Figure 15: Maximal job scale supported by 2,880 GPUs.

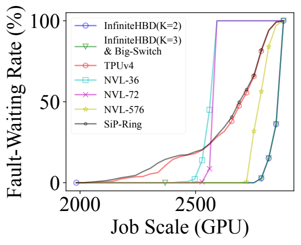
Job fault-waiting time. Large jobs must wait for repairs when GPU availability falls below the required threshold. These simulations assume the average recovery time in the fault trace as a fixed repair duration. The total wasted time during 348 days is evaluated (Figure 16). For smaller TP sizes (TP-8/TP-16), NVL-36/NVL-72 exhibit the weakest resilience due to their 11% backup overhead. For larger TP sizes (TP-32/TP-64), SiP-Ring and TPUv4 perform worst.

6.3 Training Performance

This section analyzes the training performance of two representative large models, LLama 3.1-405B [26] and GPT-MoE (configuration detailed in Appendix §B), under various GPU resource configurations and parallelism strategies. The simulation results validate the practical applicability of the *InfiniteHBD* architecture. In simulations, we model practical TP and EP behaviors: For TP, increasing parallelism splits GEMMs into smaller, less efficient tasks, reducing hardware efficiency [53]; for EP, we practically set expert imbalance coefficient at 20%.



(a) TP-16.



(b) TP-32.

Figure 16: Job fault-waiting time over the 4-GPU node with different levels of job-scale.

LLama 3.1-405B[5]**.** The model adopts a classic decoder-only Transformer architecture. The simulation employs the conventional 3D parallelism strategy[6], which combines TP, DP, and PP for performance analyses. Table 2 presents the optimal parallelism strategies and their corresponding MFU for LLama 3.1-405B under varying GPU resources. As GPU resources increase, the optimal TP size also increases. When the number of GPUs exceeds 8192, the traditional

[5]To support larger-scale TP parallelism, we simplified the GQA [1] architecture of LLama 3.1-405B to a traditional MHA architecture.

[6]$TP \in \{1, 2, 4, 8, ..., 128\}$, $DP \in \{1, 2, 4, 8, ..., 1024\}$, $PP \in \{1, 2, 4, 8, 16\}$, $bsz = 2048$

8-GPU HBD architecture within a single node begins to limit training efficiency. As the cluster size expands, larger TP sizes become increasingly optimal.

GPT-MoE. The model utilizes the Mixture-of-Experts (MoE) architecture, with $EP \in \{1, 2, 4, 8\}$ introduced in the simulation. Table 5 shows the optimal parallelism strategy and the corresponding MFU for GPT-MoE under various GPU resources. The optimal EP value is 1, suggesting that MoE can also achieve high efficiency with TP.

6.4 Communication Efficiency

This section examines the impact of orchestration algorithms on DCN communication efficiency. Experiments were performed on a Fat-Tree architecture, like the setup in [24]. As shown in Figure 17a, the algorithm is not sensitive to cluster size. Therefore, the evaluation is based on TP-32 operations on *InfiniteHBD* with 8192 GPUs.

- **Baseline:** A greedy algorithm, which randomly selects nodes from the cluster and uses the first permutation that meets the requirements.
- **Optimized:** The HBD-DCN orchestration algorithm proposed in §4.3.

Figure 17b illustrates the impact of job-scale ratios (job size/total cluster GPUs) on cross-ToR traffic, where node fault ratio is 5%. The Baseline consistently results in approximately 10% cross-ToR traffic. In contrast, the Optimized algorithm significantly outperforms the Baseline, reducing cross-ToR traffic to just 1.72% even at a 90% job-scale ratio. Figure 17c explores the sensitivity to node faults, with the job scale ratio fixed at 85%. The Baseline shows a linear increase of cross-ToR traffic, while the Optimized algorithm sustains near-zero cross-ToR traffic for fault ratios under 7%.

6.5 Cost and Power Analysis

To evaluate the interconnect costs of HBD architectures, we gather the cost and power information with the following methodologies:

- For standard components (DAC cables, optical transceivers, fibers), pricing is sourced from official retailer websites [17, 18, 48] with a 60% wholesale discount validated against internal data.
- For components with scarce public pricing information, such as Google Palomar OCS, NVIDIA NVLink Switch, 1.6 Tbps ACC cables/optical transceivers, the data is amalgamated from multiple sources [68–70] to enhance accuracy.
- Public power consumption data is available for most components, though for NVLink Switch, multiple sources are combined to estimate a reasonable value.

The breakdown analysis of each architecture is provided in the Appendix §F. Based on this, the cost and power consumption are normalized according to GPU count and per-GPU bandwidth. As depicted in Table 6, *InfiniteHBD* exhibits the lowest interconnect cost per GPU per GBps. Under the $K = 2$ configuration, its cost is only 62.84% of Google TPUv4 and 30.86% of the NVIDIA GB200 NVL-36/72, with minimal power consumption. This efficiency is primarily attributed to the avoidance of centralized switches. TPUv4 ranks second in interconnect cost and lowest in power consumption, achieved by reducing optical module use and per-port OCS costs. The NVL series has higher interconnect costs and power consumption due to its fully-connected topology and high-cost NVLink Switches. Notably, NVL-576 incurs the highest cost and power consumption due to its multilayer non-blocking topology, which increases optical module expenses and requires more NVLink Switches.

Architecture	**Per-GPU**		**Per-GPU Per-GBps**	
	Cost	Watts	Cost	Watts
TPUv4	1567.20	19.39	5.22	0.06
NVL-36	9563.20	75.95	10.63	0.08
NVL-72	9563.20	75.95	10.63	0.08
NVL-36x2	17924.00	150.33	19.92	0.17
NVL-576	30417.60	413.45	33.80	0.46
InfiniteHBD ($K = 2$)	2626.80	48.10	3.28	0.06
InfiniteHBD ($K = 3$)	3740.60	72.05	4.68	0.09

Table 6: Interconnect cost ($) and power ($Watts$).

Beyond interconnect costs, fault resilience variations also affect aggregate costs. The aggregate cost is defined as:

$$Cost_{GPU} \times (N_{Wasted-GPU} + N_{Faulty-GPU}) + Cost_{Interconnect}$$

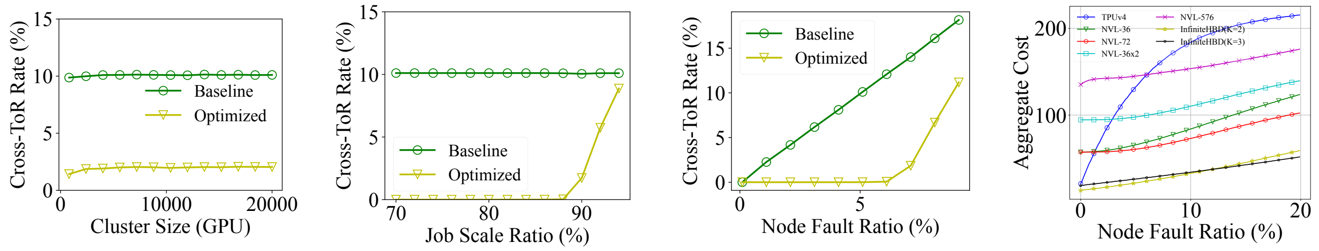
Simulations on a 3K-GPU cluster using the TP-32 configuration evaluate GPU availability under varying fault ratios across different architectures. The variation in aggregate cost for different HBD architectures under varying node fault ratios is illustrated in Figure 17d. *InfiniteHBD* consistently exhibits the lowest aggregate cost. Furthermore, when the fault ratio is below 12.1%, the aggregate cost of *InfiniteHBD* ($K = 2$) is less than that of *InfiniteHBD* ($K = 3$), suggesting that ($K = 2$) is the optimal design for most scenarios.

7 Discussion

AllToAll communication. Ring topology in *InfiniteHBD* struggles with AllToAll communication (e.g., EP), exhibiting poor performance at $O(p^2)$, where p is the group size. This can be improved by linking backup lines to nodes indexed at $n \pm 2^i$ instead of $n \pm i$ and applying the Binary Exchange algorithm, reducing time complexity to $O(p \log_2 p)$. During the algorithm, *OCSTrx* needs to connect to different GPUs with runtime switching; since *OCSTrx* switches in 60-80 μs, reconfiguration can be overlapped with computation. For $K = 2$ *InfiniteHBD* designs, performance matches the ideal Bruck algorithm [6] when $p < 8$. However, this design introduces complexities in construction, failover, and orchestration, and necessitates GPU routing capabilities. Therefore, it is not applied. We provide a detailed theoretical discussion on how *InfiniteHBD* supports AllToAll communication in Appendix §G.

Simulation Scale. Simulations using real fault traces from 3,200 GPUs, as detailed in §6.2, were conducted on a cluster comprising 2,880 GPUs. This is because the simulation's GPU count must be less than the total GPUs in the fault trace, and 2,880 is the largest number divisible by 576 and less than 3,200. This configuration allows the entire cluster to be divided into 5 NVL-576 units for the simulation.

Multi-dimension parallelism. *InfiniteHBD* is optimized for single-dimension parallelism. To support multi-dimensional communication, two approaches are viable. 1) *Independent Interconnects:* Each *OCSTrx* bundle includes multiple *OCSTrx* units (e.g., 4 or 8), then



(a) Sensitivity to cluster size. **(b) Impact of job-scale ratio.** **(c) Sensitivity to fault ratio.** **(d) Aggregate cost.**

Figure 17: DCN traffic optimization analysis and aggregate normalized cost varies across different architectures under different fault ratios.

links each of the units to a separate inter-host topology. This isolates parallel dimensions but results in fixed bandwidth per dimension, leading to inefficiencies. 2) *Time-Division multi-dimension:* Main and backup lines of *OCSTrx* can be used to form separated inter-host topologies. Rapidly switching between them can support multi-dimensional parallelism. However, this introduces complexity in managing multi-dimensional overlap and reduces the fault tolerance of *InfiniteHBD*.

Single-Job vs. Multi-Job. Existing studies explore multi-job scheduling in GPU clusters [37, 82]. Deploying certain small jobs, such as inference tasks, can mitigate GPU fragmentation. However, given the shortage of GPUs in LLM training, any idle GPU—whether repurposed for small jobs or not—is undesirable. Thus, *InfiniteHBD* prioritizes single-job execution for simplicity.

OCS vs. EPS. *OCSTrx* enables multi-path selection, a feature also achievable with Electronic Packet Switching (EPS). For example, the inter-host topology of *InfiniteHBD* can be implemented using UBB 2.0-based servers by adding external optical interfaces to switches in servers. However, this would require twice the number of optical modules and numerous high-throughput switching chips for the entire system, significantly increasing cost and power consumption compared to *OCSTrx*.

8 Related Work

HBD Architectures. HBDs are crucial for enabling communication-intensive parallelism strategies (TP/EP) for LLM training. NVIDIA DGX SuperPOD [54] and GB200 NVL series [55] use any-to-any electrical switching, delivering high performance but suffering from high costs, scalability limitations, and fragmentation. In contrast, direct interconnect HBDs like Dojo [75], TPUv3 [34], and SiP-Ring [35] improve scalability but have a large fault explosion radius. TPUv4 [33] and TPUv5p [25] attempt a middle ground but still lack full node-level fault isolation. *InfiniteHBD* introduces a novel architecture that reduces cost, improves scalability, minimizes fragmentation, enhances fault isolation, and dynamically supports TP.

AI DCN Architectures. MegaScale [32] and Meta's [24] AI DC use Clos-based topologies, while Rail-Optimized [52] and Rail-Only [80] architectures optimize for LLM traffic patterns. Alibaba HPN [65] enhances fault tolerance with a dual-plane design. *InfiniteHBD* is compatible with all of them for LLM training.

OCS Technologies. OCS enables dynamic topology reconfiguration in datacenters [33, 38, 78]. A MEMS OCS-based switch supports high port counts [7, 78], while silicon photonics (SiPh) achieves lower reconfiguration latency and cost [29]. This work proposes a SiPh-based OCS transceiver (*OCSTrx*), which constructs an interconnect fabric without centralized switches.

Reconfigurable Networks. Traditional studies [4, 5, 8, 9, 14, 28, 42, 43, 64, 79, 84] focus on generic DCN architectures without optimizing for LLM training traffic, leading to suboptimal topologies. Recent advancements like SiP-ML [35], TopoOpt [81], and mFabric [38] introduce dedicated training optimizations but still underutilize optical network reconfigurability for better fault tolerance and GPU utilization.

AI Job Schedulers. Schedulers such as [27, 31, 41, 61, 66, 85] aim to improve GPU utilization. However, they exhibit dual limitations: their designs are premised on a non-reconfigurable network, while also failing to consider job scheduling within HBD for optimizing traffic patterns in DCN. This work proposes a HBD-DCN orchestration algorithm based on reconfigurable networks to address these limitations.

9 Conclusion

In this paper, we propose *InfiniteHBD*, a novel HBD design that supports datacenter scale, dynamic TP group size and near-ideal fault explosion radius. *InfiniteHBD* is built upon a novel design of optical transceivers integrated with SiPh-based *OCSTrx*, a reconfigurable K-Hop Ring topology and a HBD-DCN orchestration algorithm to leverage the capabilities of the new hardware. Using a real fault trace of 3K-GPU cluster and the in-house simulator, we demonstrate that *InfiniteHBD* achieves GPU utilization close to the ideal model during faults, delivers superior cost and energy efficiency compared to existing designs, and provides effective control over cross-ToR DCN traffic. We believe *InfiniteHBD* provides an efficient scaling solution for HBD, which offers new insights for the next-generation infrastructure for training trillion-parameter LLMs.

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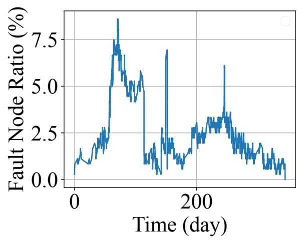
APPENDICES

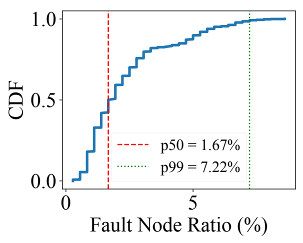
Appendices are supporting material that has not been peer-reviewed.

A Production Fault Trace

The production fault trace was collected from a 3K-GPU cluster dedicated to pretrain with 8-GPU nodes during a period of 348 days. The trace includes details such as fault start time, fault end time, and the ID of the faulty node. Figure 18a and Figure 18b provide a macro-level overview of the production fault trace. On average, the ratio of faulty 8-GPU nodes at any given time is 2.33%, with a P99 value of 7.22%.



(a) Fault Node Ratio Trace.



(b) Cumulative Distribution.

Figure 18: Fault node trace in the production AI DC.

Since most of the failure events are GPU faults, we normalized the trace of 8-GPU nodes to generate 4-GPU nodes trace. Assuming that the fault rates of GPUs are i.i.d. with a fault probability of p for each GPU, and considering that a node is deemed faulty if any GPU within it fails, the fault rate of an 8-GPU node is calculated as:

$$P_{fault}(\text{8-GPU}) = 1 - (1-p)^8 = 2.33\%.$$

From this, we derive $p = 0.29\%$. The fault rate for a 4-GPU node is then:

$$P_{fault}(\text{4-GPU}) = 1 - (1-p)^4 = 1.17\%.$$

The fault event trace for 4-GPU nodes is generated using Bayes' theorem as follows:

$$\begin{aligned} &P_{fault}(\text{4-GPU} \mid \text{8-GPU}) \\ &= \frac{P_{fault}(\text{8-GPU} \mid \text{4-GPU})P_{fault}(\text{4-GPU})}{P_{fault}(\text{8-GPU})} \\ &= \frac{1 \times 1.17\%}{2.33\%} = 50.21\% \end{aligned}$$

Thus, whenever a fault occurs in an 8-GPU node in the original trace, each of the two corresponding 4-GPU nodes at the same location has a 50.21% probability of failure. This method is used to convert the traces.

As node faults are assumed to be i.i.d., the simulator linearly maps the fault trace onto different network architectures.

B GPT-MoE Architecture

This model is a mixture-of-experts (MoE) model with the following configuration:

Model Configuration:

- **Number of Layers:** 192
- **Inner Layer Dimension:** 49152
- **Embedding Dimension:** 12288
- **Hidden Dimension:** 12288
- **Vocabulary Size:** 64000
- **Number of Attention Heads:** 128
- **Maximum Sequence Length:** 2048
- **Number of Experts:** 8
- **MoE Layer Ratio:** 0.5
- **Top-K Experts:** 2

Runtime Configuration:

- **Virtual Pipeline Parallelism:** 3
- **Micro Batch Size:** 1
- **Global Batch Size:** 1536
- **Max Sequence Length:** 2048

C Theoretical analysis of GPU waste ratio for *InfiniteHBD*

The number of backup lines, given by $2K - 2$, will significantly influence the fault tolerance of *InfiniteHBD*. We use the expectation of waste ratio caused by GPU failure and the fragmentation problem to evaluate this design, the result is shown in Table 7.

For a single working node in the middle of the line, the count of breakpoints B on its two sides has the expectation as:

$$E_B(\eta = 1, middle) = 2(P_s^K + P_s^{2K})$$

where P_s is the failure probability of GPU node, and η is the count of nodes.

Once the distance between one node and the tail of the line is $\alpha < K$, it will connect to all nodes between itself and the last one, so there will be no breakpoints on this side, and the expectation of breakpoints count is less than nodes in the middle of line. Then, for any node in the line topology:

$$E_B(\eta = 1) \leq E_B(\eta = 1, middle)$$

When the distance between two nodes is $\beta \geq K$, the breakpoints among them can be considered independent. Once the distance $\beta < K$, as all nodes in this range are connected to these two nodes, there will be no breakpoints between them. So, the expectation is less than two independent nodes. Then,

$$E_B(\eta = 2) < E_B(\eta = 2, \beta \geq K) = 2E(\eta = 1)$$
$$E_B(\eta = N_s) \leq N_s E_B(\eta = 1)$$

For a LLM job which require a ring communication size (TP .etc) as N_t, *InfiniteHBD* will cut the whole line topology into several sub-lines with the length of N_t/R. Once *InfiniteHBD* cuts a new sub-line from the remaining nodes in the line, all N_t GPUs will be wasted when one break point exists in the middle of this sub-line required, shown in Figure 19. Then the expectation for waste GPU caused by one single break point is:

$$E_W(B = 1) = N_t R \cdot (1 - (N_t/R)^{-1}) = R(N_t - R)$$

As the influence between two break points only reduce the expectation of wasted GPUs, we can have this for X break points:

$$E_W(B = X) \leq X E_W(B = 1) = XR(N_t - R)$$

So the expectation of wasted GPU for a cluster with N_s GPU nodes is:

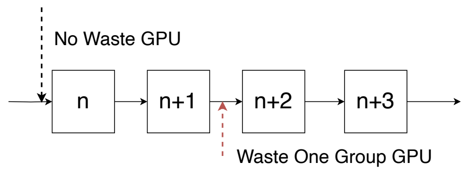


Figure 19: Break point can cause node waste compared to ideal situation.

$$
\begin{aligned}
E_W(\eta = N_s) &\le \sum P(B = X, \eta = N_s) \cdot X \cdot E_W(B = 1) \\
&= E_B(\eta = N_s) \cdot E_W(B = 1) \\
&\le \lim_{P_s \to 0} 2N_s \cdot R \cdot (N_t - R) P_s^K
\end{aligned}
$$

The final expectation of GPUs waste ratio is (1):

$$E_{WR}(\eta = N_s) = \frac{E_W(\eta = N_s)}{N_g} \le 2(N_t - R)(P_s)^K \qquad (1)$$

In our trace from a 3K-GPU cluster over 348 days, the 99th percentile (p99) failure rate for 8-GPU nodes is 7.22%. Therefore, we set the node failure rate $P_s = 7.22\%$ when $R = 8$. Based on the calculations in Appendix §A , given a GPU failure rate of 0.93%, we derive the corresponding node failure rate $P_s = 3.67\%$ for $R = 4$. If a TP32 job is running on *InfiniteHBD* (i.e., $N_t = 32$), plugging these values into Equation (1), we obtain the upper bound of the expected waste ratio for different configurations, as shown in Table 7.

	$K = 2$	$K = 3$	$K = 4$
R=4	7.54%	0.28%	1.02×10^{-4}
R=8	25.02%	1.81%	0.13%

Table 7: Upper bound for waste ratio expectation of GPU, where GPU failure rate is 0.93% and N_t is 32

For example, the 4-GPU node ($R = 4$), 3-bundle ($K = 3$) design incurs less than 0.28% additional GPU waste, while the waste ratio for the $R = 8, K = 4$ configuration remains below 0.13%. Both are sufficiently low for production cluster deployment.

D Orchestration For Fat-Tree

In this section, we introduce the orchestration algorithm under Fat-Tree DCN in detail.

Notations To ensure rigorous mathematical reasoning, we introduce the following notations:

- n: number of nodes in the data-center.
- K: *OCSTrx* bundle (see §4.2).
- S_{all}: ordered set, represents all nodes numbered from 1 according to their physical connection order in DCN fabric. $|S_{all}| = n$.
- S: ordered subset, represents nodes, $\forall u \in S, u \in S_{all}$. Adjacent elements in S are also adjacent from the perspective of the ***InfiniteHBD*** topology.
- E: The set of edges across S, should be equal to $\{(S_i, S_j) \mid 1 \le i < j \le n, j - i \le K\}$, representing the connections between nodes, including both primary and backup links, and $O(|E|) = O(K|S|)$.
- $InfHBD =< S, E >$: the topology of ***InfiniteHBD*** as an undirected graph.
- F: faulty nodes.
- $HealthyHBD =< H, HE >$: healthy node subgraph where the set of healthy nodes $H = S - F$ and the edge set $HE = \{(u, v) \mid u \in H \text{ and } v \in H \text{ and } (u, v) \in E\}$.
- t: TP size, number of GPUs in one TP Group.
- r: GPU ranks per node.
- $m = t/r$: number of nodes in a TP group.
- s: job scale, number of GPUs required for the job.
- d: Aggregation-Switches Domain size. Number of nodes under coverage of one group of Aggregation-Switches.
- $n_{constrains}$: number of applied constraints in binary-search-based orchestration algorithm.
- p: number of nodes under each ToR.
- l: shortest sub-line length under fat-tree orchestration.
- $n_{maxsubline} = \lfloor \frac{nd}{p} \rfloor$: max number of sub-lines.
- $G_{deploy} =< S_{deploy}, E_{deploy} >$: deployed topology. After applying the deployment strategy, the topology from the perspective of ***InfiniteHBD*** is described as follows: S_{deploy} is an ordered set where adjacent elements correspond to adjacent nodes in ***InfiniteHBD***, and E_{deploy} represents the connections between nodes.

The orchestration algorithm (Algorithm 2) without considering DCN has the overall time complexity $3 \cdot O(|H| + |HE|) = O(|S| + |E|) = O((K + 1)|S|) = O(|S|)$.

Algorithm 2: Orchestration-DCN-Free

```
Input: InfHBD = $\langle S, E \rangle$, $F$, $m$
Output: Placement scheme that maximizes GPU utilization
Initialize $H = S - F$;
Initialize $HE = \{(u, v) \mid u \in H \text{ and } v \in H \text{ and } (u, v) \in E\}$;
Create subgraph $HealthyHBD = \langle H, HE \rangle$;
Initialize $component\_list = []$;
Initialize $visited = \{\}$;
Initialize $placement\_scheme = \{\}$;
for each node $s$ in $H$ do
    if $s$ not in $visited$ then
        $component = Connected-Component-DFS(s, HealthyHBD, visited)$;
        Add $component.sortedInHBD()$ to $component\_list$;
for each $component$ in $component\_list$ do
    while $component.size() \ge m$ do
        Add $component.pop(m)$ to $placement\_scheme$;
return $placement\_scheme$
```

The Fat-Tree is another common topology used in data centers. A typical training strategy for this topology aims to maximize the bandwidth utilization under ToR (Top of Rack) Switches. Using Meta's two-stage clos topology[24] as a reference, it can be observed that there is an attempt to run CP under ToR Switches.

Deployment Strategy. Assuming there are p nodes under each ToR, nodes with the same index under each ToR are deployed along

Algorithm 3: Deployment-Strategy

```
Input: Node ordered set $S$, $OCSTrx$ direction $K$, parallel factor $p$
Output: Deployment topology $G_{deploy} =< S_{deploy}, E_{deploy} >$
Initialize ordered set $S_{deploy} = [\,]$;
Initialize $l = \lfloor \frac{|S|}{p} \rfloor$;
for $i$ in $0...p-1$ do
    for $j$ in $0...l-1$ do
        Add $i + j \cdot p$ to $S_{deploy}$;
Create $E_{deploy} = \{(S^i_{deploy}, S^j_{deploy}) | 1 \le i \le j \le |S_{deploy}|, j - i \le K\}$;
return $G_{deploy} =< S_{deploy}, E_{deploy} >$
```

the same parallel sub-line, and the p sub-lines are connected end-to-end, as shown in Figure 7. The training strategy involves running CP p across the sub-lines and running TP within them.

Orchestration Constraints. To maximize the utilization of ToR bandwidth and minimize cross-ToR traffic, the fat-tree topology introduces two constraints:

- **Aggregation-Switches Domain Constraint:** The coverage domain of a group of Aggregation Switches is limited, meaning that TP groups spanning across Aggregation Switches domains would result in cross-rail traffic, which should be avoided as much as possible.
- **TP Group Alignment Constraint:** A CP Group consists of TP Groups across parallel sub-lines. To keep CP traffic within the ToR switches, the TP Groups must be aligned. If a node fails under one ToR, all nodes under that ToR are considered to have failed, expanding the failure radius by a factor of p.

Binary-Search-Based Orchestration Algorithm. Based on the constraints and deployment strategy, we develop a binary search orchestration algorithm (see Algorithm 5) that adjusts the number of satisfied constraints. The binary search first relaxes the TP Group alignment constraints within the Aggregation-Switches Domain and then relaxes the TP Group crossing constraints between Aggregation-Switch domains (see Algorithm 4). This process is monotonic.

The time complexity of Algorithm 2 is $O(|S|)$, and the complexity of Algorithm 4 is:

$$\sum_{i=1}^{n_{subline}} O(|S_{subline}|) = O(\sum_{i=1}^{n_{subline}} |S_{subline}|) = O(|S_{all}|) = O(n)$$

Thus, the overall time complexity of Algorithm 5 is $O(n \log n)$.

E Additional Simulation Results for Fault Resilience

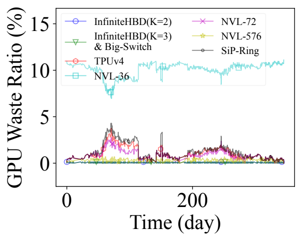
This section presents additional simulation results related to §6.2. Figure 20 shows the variation of the GPU waste ratio over time under the production fault trace. Figure 21 presents the CDF data for the GPU waste ratio. Figure 22 illustrates the GPU waste ratio for different HBD architectures under various node failure rates, including the results for TP-8 to TP-64. Figure 23 shows the proportion of job-fault waiting time relative to total time for different job scales. All the aforementioned experiments include results for TP-8, TP-16, TP-32, and TP-64 configurations.

Algorithm 4: Placement-Fat-Tree

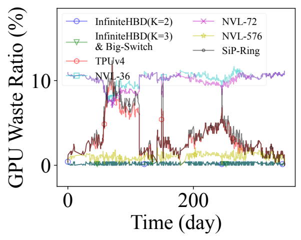
```
Input: $G_{deploy} =< S_{deploy}, E_{deploy} >, n_{constraints}, F, l, m, n_{maxsubline}, d, p$
Output: Placement scheme
Initialize $placement\_scheme = \{\}$;
Initialize $n_{align} = max(0, n_{constraints} - n_{maxsubline})$, $n_{subline} = min(n_{maxsubline}, n_{constraints})$;
for $i$ in $0..n_{align} - 1$ do
    for $j$ in $1..d$ do
        $sid = i * d + j$;
        if $sid \in F$ then
            $F \cup \{\lfloor \frac{sid-1}{p} \rfloor \cdot p + 1..(\lfloor \frac{sid-1}{p} \rfloor + 1) \cdot p\}$;
for $i$ in $1..n_{subline}$ do
    $S_{subline} = S_{deploy}.pop(l)$;
    $E_{subline} = \{(u, v) \mid u \in S_{subline}$ and $v \in S_{subline}$ and $(u, v) \in E_{subline}\}$;
    $F_{subline} = F \cap S_{subline}$;
    $placement\_scheme = placement\_scheme \cup$ Orchestration-Ideal$(< S_{subline}, E_{subline} >, F_{subline}, m)$;
$E_{res} = \{(u, v) \mid u \in S_{deploy}$ and $v \in S_{deploy}$ and $(u, v) \in E_{deploy}\}$;
$F_{res} = F \cap S_{deploy}$;
$placement\_scheme = placement\_scheme \cup$ Orchestration-Ideal$(< S_{deploy}, E_{res} >, F_{res}, m)$;
return $placement\_scheme$
```

Algorithm 5: Orchestration-Fat-Tree

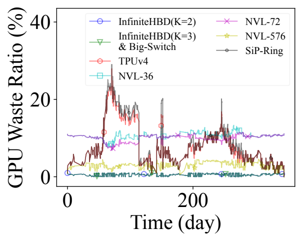
```
Input: $S, r, p, F, t, s, d, K$.
Output: Placement scheme that satisfies job scale and minimizes
        cross-rail traffic.
Initialize $m = t/r$, $n = |S|$, $l = \lfloor \frac{d}{p} \rfloor$ $n_{domain} = \lfloor \frac{n}{d} \rfloor$, $n_{maxsubline} = \lfloor \frac{nd}{p} \rfloor$;
Create graph $G_{deploy} =< S_{deploy}, E_{deploy} >=$ Deployment-Strategy$(S, K, p)$;
Initialize $high = n_{domain} + n_{maxsubline}$;
Initialize $low = 0$;
Initialize $placement\_scheme = \{\}$;
while $low \le high$ do
    $mid = \lfloor \frac{low+high}{2} \rfloor$;
    $placement\_scheme =$
      Placement-Fat-Tree$(G_{deploy}, mid, F, l, m, n_{maxsubline}, d, p)$;

    if $|placement\_scheme| \cdot m \cdot r \ge s$ then
        $low = mid + 1$;
    else
        $high = mid - 1$;
if $|placement\_scheme| \cdot m \cdot r \ge s$ then
    return $placement\_scheme$
else
    return $None$
```



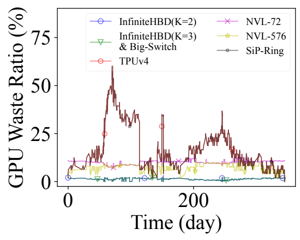
(a) TP-8.



(b) TP-16.

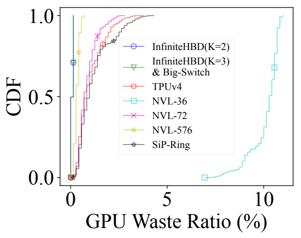


(c) TP-32.

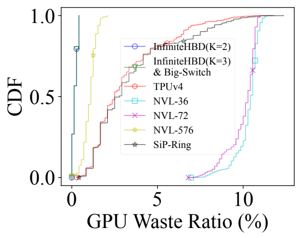


(d) TP-64.

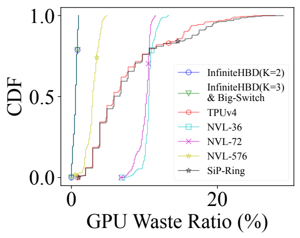
Figure 20: GPU waste ratio over production fault trace, 4-GPU node.



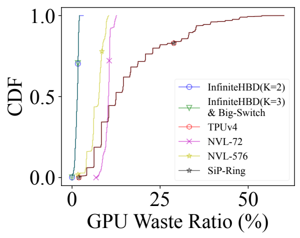
(a) TP-8.



(b) TP-16.

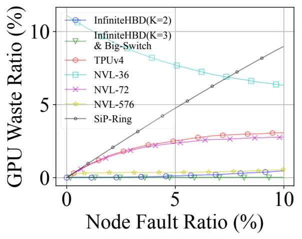


(c) TP-32.

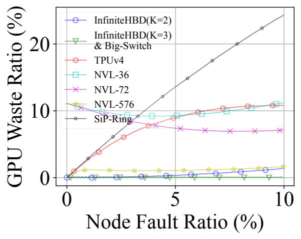


(d) TP-64.

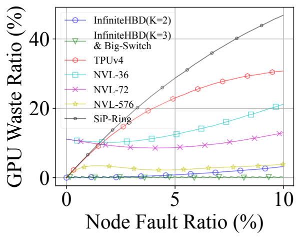
Figure 21: CDF of GPU waste ratio over production fault trace, 4-GPU node.



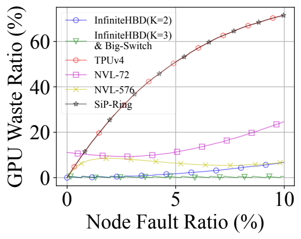
(a) TP-8.



(b) TP-16.

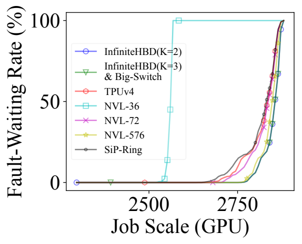


(c) TP-32.

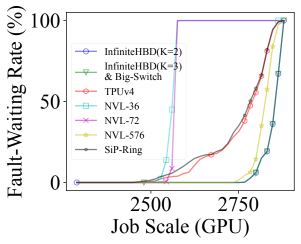


(d) TP-64.

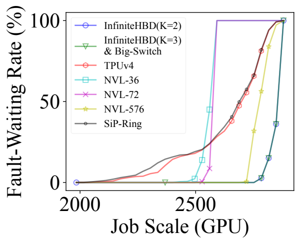
Figure 22: GPU waste ratio with different GPU fault ratio, 4-GPU node.



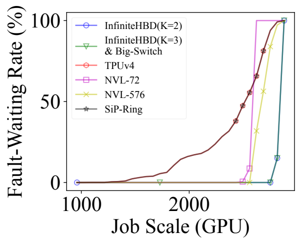
(a) TP-8.



(b) TP-16.



(c) TP-32.



(d) TP-64.

Figure 23: Job fault-waiting duration under different job scales, 4-GPU node.

F Detailed Cost and Power Consumption Analysis

In this section, Table 8 provides a detailed description of the quantity, cost, bandwidth, and power consumption of the interconnect components in various network architectures, including Google TPUv4 [33], NVIDIA GB200 NVL series [55], Alibaba HPN[65], and *InfiniteHBD*.

Component	Quantity	Unit Cost ($)	Unit Bandwidth (GBps)	Unit Power (W)
Google TPUv4[33] with 4096 GPU, bandwidth 300GBps/GPU				
OCS[39]	48	80000	6400	108
DAC Cable[19]	5120	63.60	50	0.1
Optical Module[16]	6144	360	50	12
Fiber[22]	6144	6.80	50	0
NVIDIA GB200 NVL-36[69] with 36 GPU, bandwidth 900GBps/GPU				
NVLink Switch[70]	9	28000	3600	275
DAC Cable[20]	2592	35.60	25	0.1
NVIDIA GB200 NVL-72[55][69] with 72 GPU, bandwidth 900GBps/GPU				
NVLink Switch[70]	18	28000	3600	275
DAC Cable[20]	5184	35.60	25	0.1
NVIDIA GB200 NVL-36x2[69] with 72 GPU, bandwidth 900GBps/GPU				
NVLink Switch[70]	36	28000	3600	275
DAC Cable[20]	6480	35.60	25	0.1
ACC Cable[70]	162	320	200	2.5
NVIDIA GB200 NVL-576[69] with 576 GPU, bandwidth 900GBps/GPU				
NVLink Switch[70]	432	28000	3600	275
DAC Cable[20]	41472	35.60	25	0.1
Optical Module[45]	4608	850	200	25
Fiber[22]	4608	6.80	200	0
Alibaba HPN[65] with 16320 GPU, bandwidth 50GBps/GPU				
EPS[47]	360	14960	6400	3145
DAC Cable[20]	32640	35.60	25	0.1
Optical Module[16]	28800	360	50	12
Fiber[22]	14400	6.80	50	0
***InfiniteHBD*($K = 2$) with 4 GPU, bandwidth 800GBps/GPU**				
DAC Cable[21]	4	199.60	200	0.1
OCSTrx	16	600	100	12
Fiber[22]	16	6.80	100	0
***InfiniteHBD*($K = 3$) with 4 GPU, bandwidth 800GBps/GPU**				
DAC Cable[21]	2	199.60	200	0.1
OCSTrx	24	600	100	12
Fiber[22]	24	6.80	100	0

Table 8: Interconnect cost and power consumption of components used in different network architectures.

G AllToAll Communication of *InfiniteHBD*

Nowadays, training MoE models has become one of the primary application scenarios for GPU clusters. For large MoE models such as DeepSeek-v3 [12], both training and inference heavily rely on expert parallelism (EP). As analyzed earlier (§2.3), while TP can still effectively support MoE model training, for the sake of generality, we have **theoretically** explored how *InfiniteHBD* can be utilized to support EP AllToAll communication. Based on the *OCSTrx* Fast Switch Mechanism, we propose a method to enable the Binary Exchange AllToAll algorithm, though this approach has **not yet been validated on real hardware**.

G.1 *OCSTrx* Fast Switch Mechanism

In the original assumption, *InfiniteHBD* maintains a fixed topology configuration during any collective communication operation, meaning that only pre-activated links are used for communication. These links form a ring topology, which is inefficient for supporting AllToAll communication. This limitation is particularly common in traditional optical interconnect networks, where the end-to-end reconfiguration latency of OCS—composed of both hardware switching latency and control plane latency—is typically on the order of milliseconds, and in some cases even minutes [78], making it impractical to dynamically reconfigure for each communication pair.

However, *OCSTrx* adopts a more simplified hardware architecture that significantly reduces the reconfiguration latency compared to centralized OCS-based switches. Specifically, the hardware switching latency of our *OCSTrx* module is only 60–80 µs. Moreover, the control plane latency can be optimized and minimized by preloading Top-Session configurations in its control module and triggering flow switching as needed. As a result, the total end-to-end reconfiguration latency of *OCSTrx* is reduced to approximately 60-80 μs. We refer to this combined capability as the ***OCSTrx* Fast Switch** mechanism.

The Fast Switch mechanism allows us to fully utilize all backup links instead of being restricted to pre-activated ones. This means that active links can be dynamically configured in real-time based on any communication pair's requirements, thereby improving the efficiency of AllToAll communication.

G.2 Binary Exchange AllToAll Algorithm

Fast Switch enables the system to fully utilize all available links. However, since nodes equipped with *OCSTrx* have a limited radix, the topology cannot achieve a fully connected structure at any arbitrary scale or location, but rather supports only **sparse interconnects**. Additionally, architectures like *InfiniteHBD* do not support **node-level loopback** at arbitrary scales.

Due to these limitations, AllToAll algorithms based on fully connected topologies (such as those used in NCCL [51]) are not suitable for sparse interconnect environments. Similarly, the lack of node-level loopback makes algorithms that rely on sequential communication infeasible, even if they are inherently sparse. For instance, algorithms like Bruck [6] and Pairwise Exchange [76], which depend on node-level loopback communication, cannot be directly applied to *InfiniteHBD*.

To better accommodate the interconnect characteristics of *InfiniteHBD*, we adopt the **Binary Exchange AllToAll** algorithm. In Binary Exchange, a node i only communicates with node $i \oplus 2^k$. For example, in a communication group of 8 nodes, node 0 only exchanges data with nodes 1, 2, and 4 in different rounds. This communication pattern ensures sparsity and eliminates the need for node-level loopback, making it highly compatible with the topology of *InfiniteHBD*.

The detailed procedure of Binary Exchange is shown in Algorithm 6. Suppose the AllToAll group consists of p nodes, and each node initially stores $p \cdot m$ units of data. Each node maintains the following two variables:

- *Msg*: Stores all data currently held by the node, including both its original data and any received data.
- *Commset*: Records the set of nodes that have already exchanged data (either directly or through intermediate nodes). Initially, this set contains only the node's own index.

The algorithm runs for $\log_2 p$ rounds. In the k-th step ($1 \le k \le \log_2 p$), node i exchanges data with node $r = i \oplus 2^{\log_2 p - k}$:

(1) Node i sends the following data fragment to node r:

$$Msg[Commset][r \,\&\, 2^{\log_2 p-k} : r \,\&\, 2^{\log_2 p-k} + 2^{\log_2 p-k}]$$

and receives data from node r. The transmitted data size per round is $\frac{p \cdot m}{2}$.

(2) The communication set is updated:

$$i.Commset = i.Commset \cup r.Commset$$

The total execution time of Binary Exchange is:

$$T = \sum_{i=1}^{\log_2 p} \left(t_s + t_w \frac{pm}{2}\right) = t_s \log_2 p + \frac{1}{2} t_w mp \log_2 p = O(p \log_2 p)$$

where t_s is the transmission setup time and t_w is the per-unit data transfer time.

This algorithm achieves a significantly lower communication complexity, making it well-suited for sparse interconnect architectures without node-level loopback, such as *InfiniteHBD*. Compared to the $O(p^2)$ complexity of ring-AllToAll when Fast Switch is not used, Binary Exchange reduces the complexity to $O(p \log_2 p)$, greatly improving communication efficiency.

Algorithm 6: Binary-Exchange-AllToAll

```
Input: Group size $p$, Node index $i$, Initial message $m_{init}$
Output: AllToAll personalized data
Initialize $Msg[i] = m_{init}$, $Commset = \{i\}$;
for $k$ in $1, ..., log_2 p$ do
    $r = i \oplus 2^{log_2 p - k}$;
    $m_{send} = \{Msg[m][n] | m \in Commset, n \in [r \,\&\, 2^{\log_2 p-k}, r \,\&\, 2^{\log_2 p-k} + 2^{\log_2 p-k})\}$;
    Node $i$ sends message $m_{send}$ to node $r$;
    Node $i$ receives message $m_{recv}$ from node $r$;
    Update $Msg$ with $m_{recv}$;
    $Commset = Commset \cup r.Commset$;
return $\{Msg[m][i] | m \in Commset\}$
```

G.3 *InfiniteHBD* Topology for AllToAll

To support dynamically scalable Binary Exchange AllToAll, we propose a novel topology based on *InfiniteHBD*.

The topology retains the one-dimensional arrangement of nodes in *InfiniteHBD* but modifies the wiring pattern. Since in Binary Exchange AllToAll, node i only communicates with node $i \oplus 2^k$, the distance between any two communicating nodes satisfies:

$$\Delta = i - (i \oplus 2^k) \in \{+2^k, -2^k\}$$

Based on this, instead of connecting each node to neighbors at distances $\pm 1, 2, ..., K$ as in the original K-Hop Ring topology, we rewire nodes to connect at distances $\pm 1, 2, 4, ..., 2^{K-1}$, aligning with the Binary Exchange AllToAll communication pattern.

This topology supports 2D parallelism of **hybrid TP+EP** in *InfiniteHBD*, where TP is the inner-layer parallelism and EP is the outer-layer parallelism. Figure 24 illustrates a TP4+EP4 configuration based on a 4-GPU Node setup, where TP4 is applied within each 4-GPU node, and EP4 is applied across four such nodes. The figure shows the steps of the Binary Exchange AllToAll algorithm used for EP4 communication: in Step 1, Node 0 exchanges data with Node 2, and Node 1 with Node 3; in Step 2, Node 0 exchanges data with Node 1, and Node 2 with Node 3.

However, this topology fundamentally emphasizes a trade-off between AllToAll performance and fault resilience, thereby introducing the following significant challenges:

- **Additional GPU forwarding overhead**: Since interconnects are not GPU-level, some traffic must be forwarded through intermediate GPUs, introducing extra communication overhead.

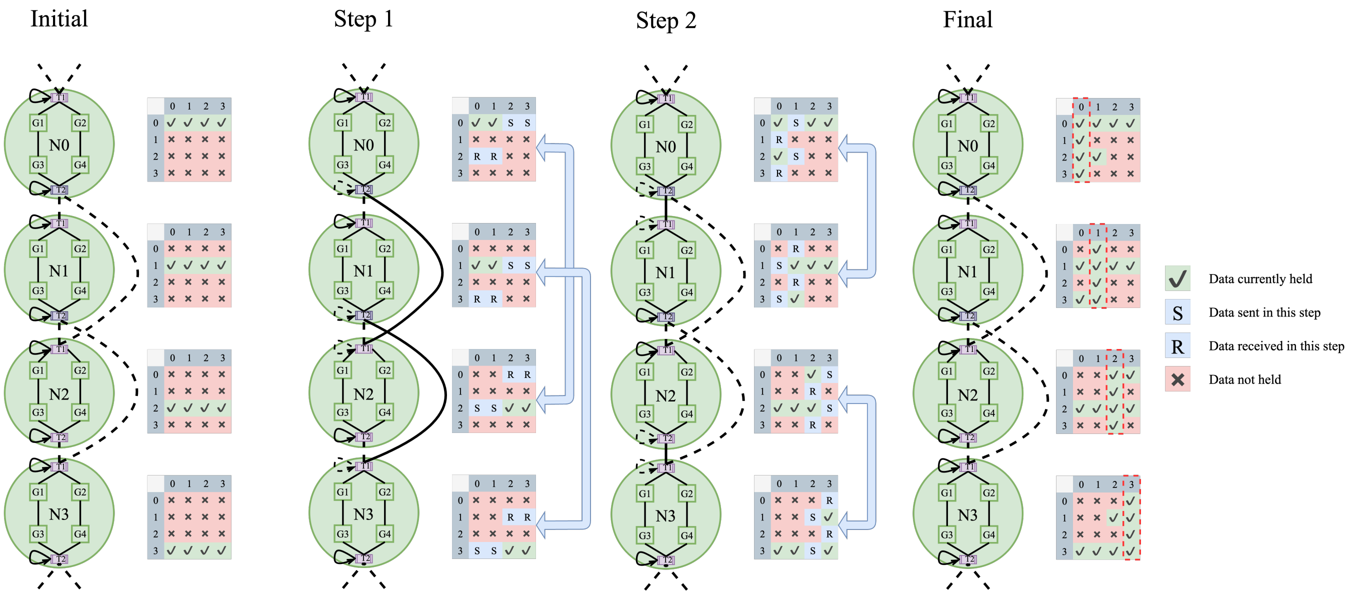


Figure 24: Illustration of Binary Exchange AllToAll algorithm under TP4+EP4 configuration and *InfiniteHBD* topology for AllToAll.

- **Coupling between TP and EP**: In 4-GPU Node, the number of OCSTrx bundles is limited, allowing each node to connect at most to ±1, 2, 4, 8 distant nodes. As a result, the TP group size affects the EP group size, constrained by: $TP_{\text{size}} \times EP_{\text{size}} \leq 64$. This limits general applicability in some scenarios. The 8-GPU Node alleviates this issue, as it supports up to 8 OCSTrx bundles, enabling connections at distances ±1, 2, 4, 8, 16, 32, 64, 128, relaxing the constraint to: $TP_{\text{size}} \times EP_{\text{size}} \leq 2048$, making it suitable for most scenarios.
- **High scheduling complexity**: Node failures affect not only their own availability but also reduce bandwidth on backup links. Scheduling algorithms must simultaneously optimize GPU utilization and inter-node bandwidth, increasing system complexity.