

多周期大作业实验报告

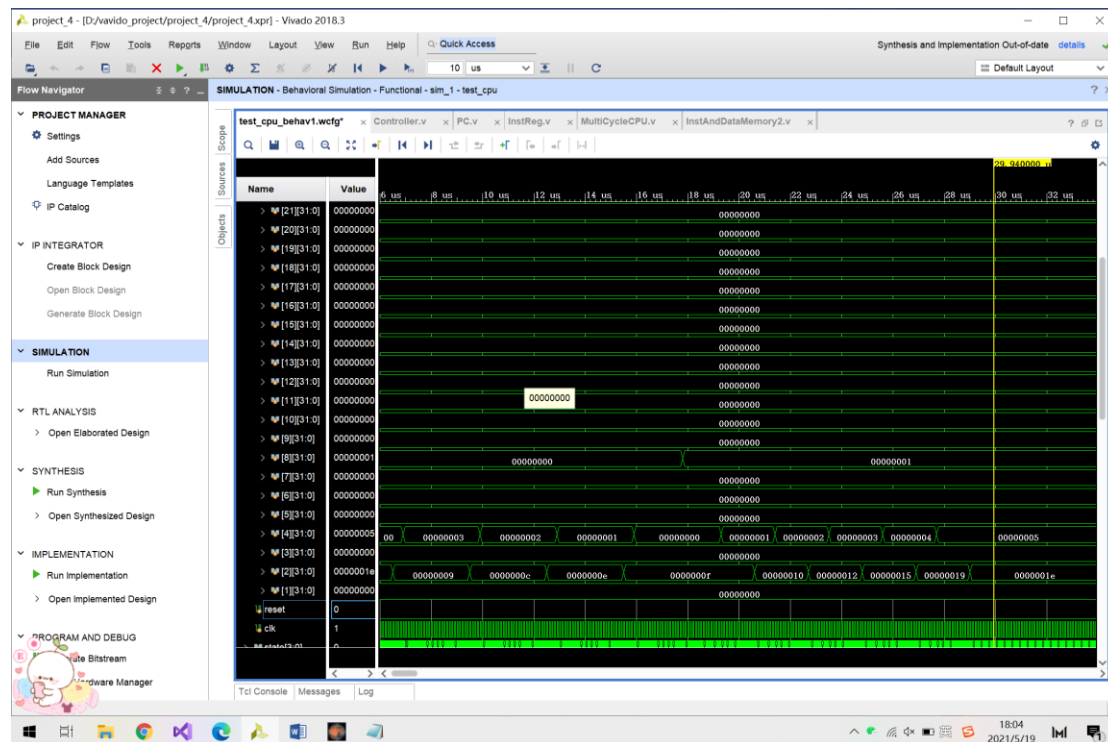
Xuan

(1)代码见 code 中的文件

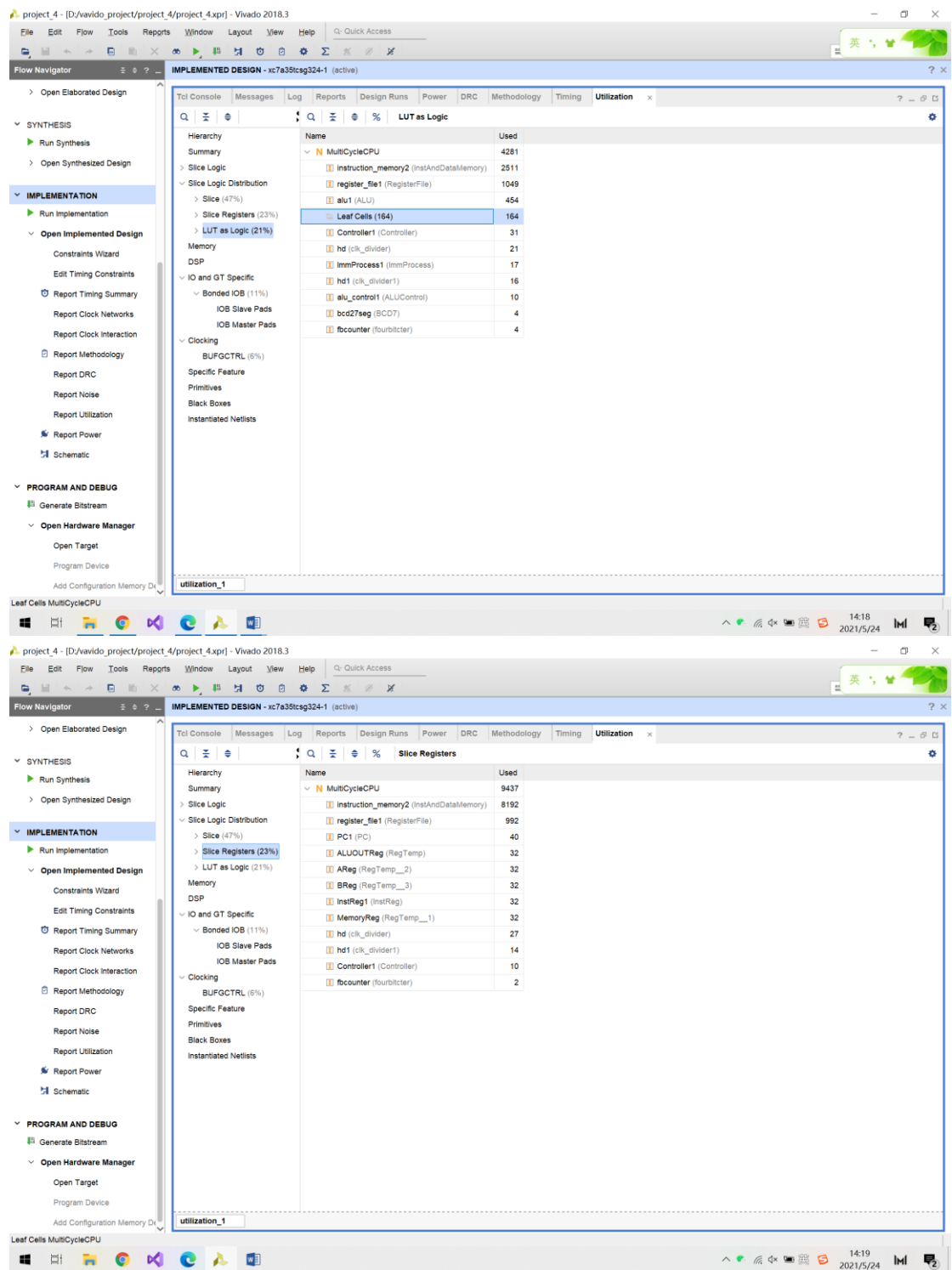
(2) 修改后的 `InstAndDataMemory.v` 为 code 中的 `InstAndDataMemory2.v`, 仿真结果为 $\$a0=5, \$v0=0x1e=30=5*(5+1)$, 与预期一致。

如图，最终结果为光标处的\$2=0x1e,\$4=5;\$t0=1

仿真波形见 test_cpu_behav2.wcfg



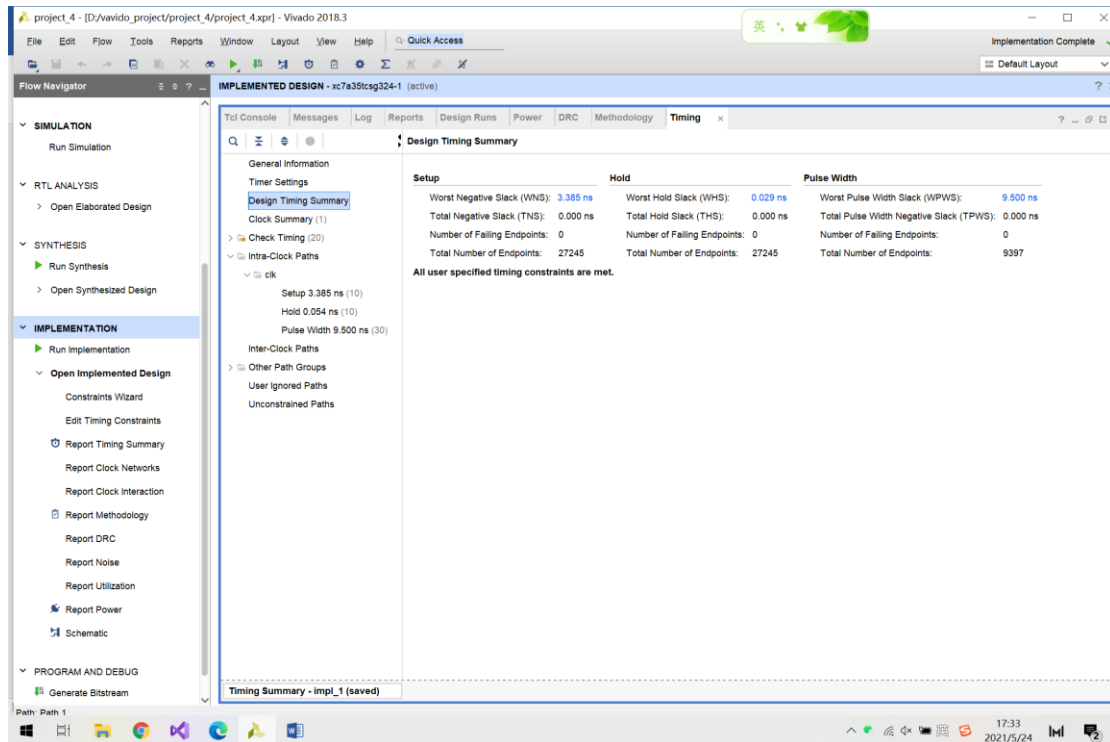
键路径是什么, 路径上有哪些单元, 哪些单元是最耗时的), FPGA 资源消耗情况 等。
FPGA 资源消耗情况



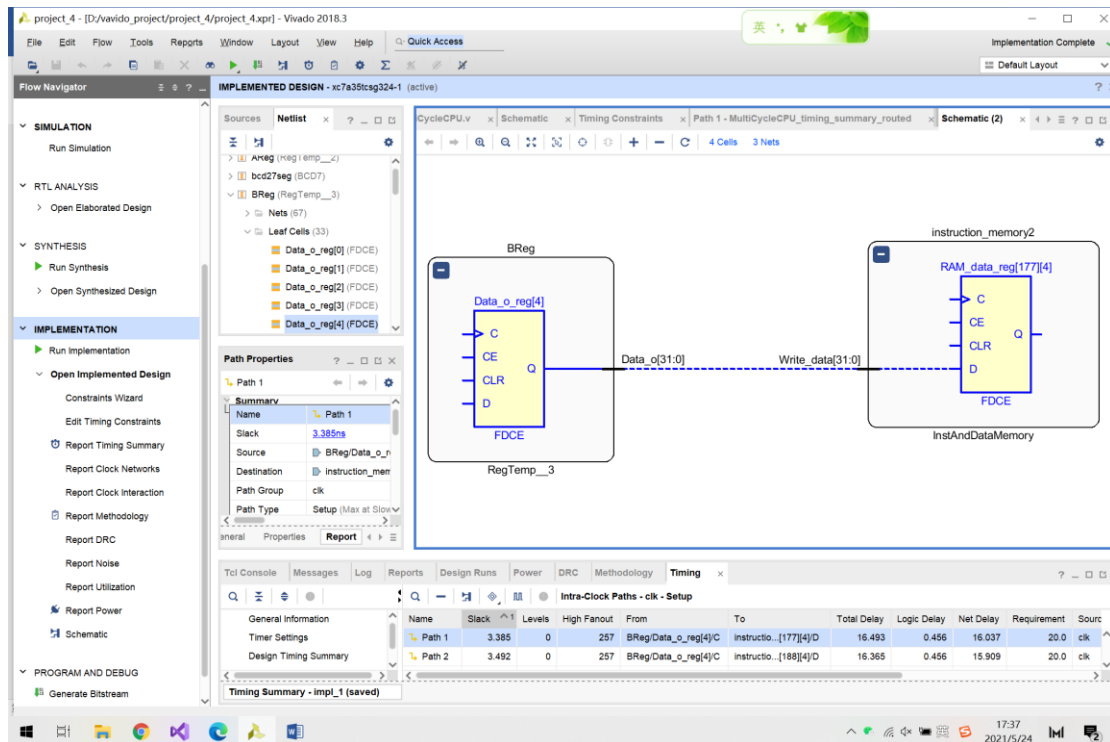
时序性能:

约束文件使用的是 50MHz 的时钟, 即单个周期 20ns,尚有 3.385ns 余裕量, 所以最高频率为

$$\frac{1}{20-3.385\text{ns}} = 60.187\text{MHz}$$



限制最高工作频率的关键路径是:从 B 寄存器到指令和数据存储器的通路, 即 MEM 阶段的内存写入操作, 符合理论



project_4 - [D:/avido_project/project_4/project_4.xpr] - Vivado 2018.3

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Implementation Complete

Flow Navigator

- SIMULATION
 - Run Simulation
- RTL ANALYSIS
 - Open Elaborated Design
- SYNTHESIS
 - Run Synthesis
 - Open Synthesized Design
- IMPLEMENTATION
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 - Report Clock Networks
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 - Report Methodology
 - Report DRC
 - Report Noise
 - Report Utilization
 - Report Power
 - Schematic
 - PROGRAM AND DEBUG
 - Generate Bitstream

IMPLEMENTED DESIGN - xc7a35tcsq324-1 (active)

Tcl Console Messages Log Reports Design Runs Power DRC Methodology Timing

Intra-Clock Paths - clk - Setup

Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source
Path 1	3.385	0	257	BReg/Data_o_reg[4]C	instructio...[177][4]D	16.493	0.456	16.037	20.0	clk
Path 2	3.492	0	257	BReg/Data_o_reg[4]C	instructio...[188][4]D	16.365	0.456	15.909	20.0	clk
Path 3	3.540	0	257	BReg/Data_o_reg[4]C	instructio...[191][4]D	16.367	0.456	15.911	20.0	clk
Path 4	3.633	0	257	BReg/Data_o_reg[4]C	instructio...[187][4]D	16.224	0.456	15.768	20.0	clk
Path 5	3.678	0	257	BReg/Data_o_reg[4]C	instructio...[145][4]D	16.212	0.456	15.756	20.0	clk
Path 6	3.812	0	257	BReg/Data_o_reg[4]C	instructio...[176][4]D	16.063	0.456	15.607	20.0	clk
Path 7	3.972	0	257	BReg/Data_o_reg[4]C	instructio...[153][4]D	15.902	0.456	15.446	20.0	clk
Path 8	4.103	0	257	BReg/Data_o_reg[4]C	instructio...[149][4]D	15.752	0.456	15.296	20.0	clk
Path 9	4.131	0	257	BReg/Data_o_reg[4]C	instructio...[159][4]D	15.749	0.456	15.293	20.0	clk
Path 10	4.189	0	257	BReg/Data_o_reg[4]C	instructio...[190][4]D	15.691	0.456	15.235	20.0	clk

Timing Summary - impl_1 (saved)

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IMPLEMENTED DESIGN - xc7a35tcsq324-1 (active)

Sources Netlist

- Arreg (reg [emp_c])
- bcd27seg (BCD7)
- BReg (RegTemp_3)
 - Nets (57)
 - Leaf Cells (33)
 - Data_o_reg[0] (FDCE)
 - Data_o_reg[1] (FDCE)
 - Data_o_reg[2] (FDCE)
 - Data_o_reg[3] (FDCE)
 - Data_o_reg[4] (FDCE)

Path Properties

Summary

Name Path 1

Slack 3.385ns

Source BReg/Data_o_reg[4]C

Destination instruction_memory2/RAM_data_reg[177][4]D

Path Group clk

Path Type Setup (Max at Slow Process Corner)

Requirement 20.000ns (clk rise@20.000ns - clk rise@0.000ns)

Data P...Delay 16.493ns (logic 0.456ns (2.765%) route 16.037ns (97.235%))

Logic Levels 0

Clock ... Skew -0.027ns

Clock U...tainty 0.035ns

Source Clock Path

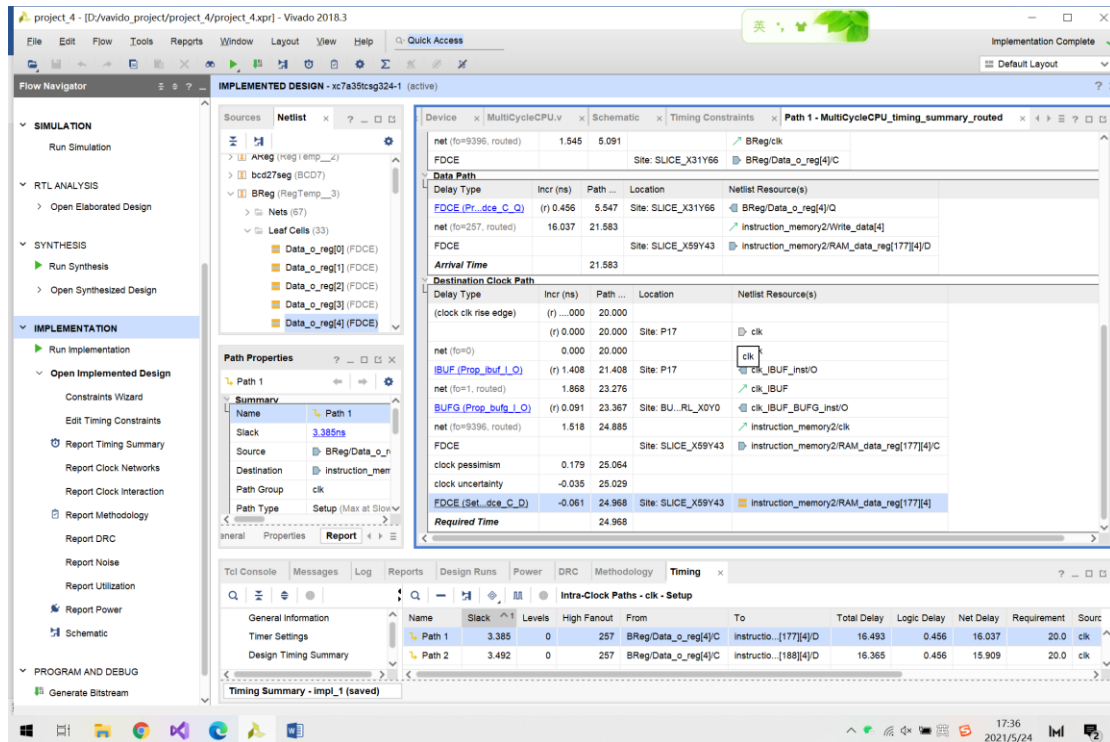
Delay Type	Incr (ns)	Path...	Location	Netlist Resource(s)
(clock clk rise edge)	(r) 0.000	0.000	Site: P17	clk
net (f0=0)	0.000	0.000	Site: P17	clk
IBUF (Prop_buf_I_O)	(r) 1.478	1.478	Site: P17	clk_IBUF_inst/O
net (f0=1, routed)	1.972	3.450		clk_IBUF
BUF (Prop_bufg_I_O)	(r) 0.096	3.546	Site: BU...Rt_X0Y0	clk_IBUF_BUFG_inst/O
net (f0=9396, routed)	1.545	5.091		BReg/clk
FDCE			Site: SLICE_X31Y66	BReg/Data_o_reg[4]C

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Timing Summary - impl_1 (saved)



路径上有哪些单元:有 B 寄存器、指令和数据存储器

哪些单元是最耗时的: 指令和数据存储器的内存读写操作最耗时