2.4.2 Processor Unit (Core)

Each processor unit (see Figure 2-14) or core is a superscalar and out-of-order processor that includes 10 execution units.

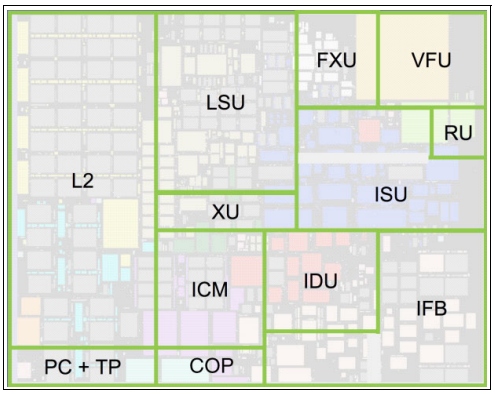

Figure 2-14 PU Core layout

Consider the following points:

- Fixed-point unit (FXU): The FXU handles fixed-point arithmetic.
- Load-store unit (LSU): The LSU contains the data cache. It is responsible for handling all types of operand accesses of all lengths, modes, and formats as defined in the z/Architecture.
- The instruction fetch and branch (IFB) (prediction) and instruction cache and merge (ICM) sub units contain the instruction cache, branch prediction logic, instruction fetching controls, and buffers. Its relative size is the result of the elaborate branch prediction.
- Instruction decode unit (IDU): The IDU is fed from the IFU buffers, and is responsible for parsing and decoding of all z/Architecture operation codes.
- Translation unit (XU): The XU has a large translation lookaside buffer (TLB) and the Dynamic Address Translation (DAT) function that handles the dynamic translation of logical to physical addresses.
- Instruction sequence unit (ISU): This unit enables the out-of-order (OoO) pipeline. It tracks register names, OoO instruction dependency, and handling of instruction resource dispatch.
- Recovery unit (RU): The RU keeps a copy of the complete state of the system that includes all registers, collects hardware fault signals, and manages the hardware recovery actions.
- Dedicated Co-Processor (COP): The dedicated coprocessor is responsible for data compression and encryption functions for each core.
- Core pervasive unit (PC) for instrumentation, error collection.
- Vector and Floating point Units (VFU).
- Binary floating-point unit (BFU): The BFU handles all binary and hexadecimal floating-point and fixed-point multiplication operations.
- Decimal floating-point unit (DFU): The DU runs floating-point, decimal fixed-point, and fixed-point division operations.
- Vector execution unit (VXU).
- Level 2 cache (L2) for instructions and data (L2I/L2D).