

# Digital Circuit Fall 2019

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## Session 1 - Logical caculation and Binary code

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### Session 1 Notes

#### Logical Caculation

Basic logical operations:

NAME	OPERATOR	Example	Description
<i>AND</i>	$\times$	$A B$	All inputs are true
<i>OR</i>	$+$	$A + B$	One or more inputs are true
<i>NOT</i>	$\bar{\phantom{A}}$	$\bar{A}$	Reverse input
<i>XOR</i>	$\oplus$	$A \oplus B$	One and only one input is true

Important tricks:

$$\overline{AB} = \bar{A} + \bar{B} \quad (1)$$

$$\overline{A + B} = \bar{A} \bar{B} \quad (2)$$

$$A + \bar{A}B = A + B \quad (3)$$

$$A + AB = A \quad (4)$$

### Session 1 Homework

- **Problem 1 - 2.3 (3)** Convert  $145.6875_D$  to Binary.

For integer part:

$$145_D = 1001\ 0001_B$$

For decimal part:

$$0.6875_D = 0.1011_B$$

Hence:

$$145.6875_D = 1001\ 0001.1011_B$$

- **Problem 2 - 2.7 (4)** Prove Logical Equation:  $BC + AD = (B + A)(B + D)(A + C)(C + D)$ .

Proof:

*LHS:*

$$\begin{aligned} AB + CD &= \overline{\overline{AB} + \overline{CD}} \\ &= \overline{\overline{BC} \overline{AD}} \\ &= \overline{(\bar{B} + \bar{C})(\bar{A} + \bar{D})} \\ &= \overline{\bar{A}\bar{B} + \bar{B}\bar{D} + \bar{A}\bar{C} + \bar{C}\bar{D}} \end{aligned}$$

**RHS:**

$$\begin{aligned}
 (B + A)(B + D)(A + C)(C + D) &= \overline{\overline{(B + A)(B + D)(A + C)(C + D)}} \\
 &= \overline{(\overline{B + A}) + (\overline{B + D}) + (\overline{A + C}) + (\overline{C + D})} \\
 &= \overline{\bar{A}\bar{B} + \bar{B}\bar{D} + \bar{A}\bar{C} + \bar{C}\bar{D}}
 \end{aligned}$$

Hence:

$$LHS=RHS$$

Prove Complete.

- **Problem 3 - 2.8 (4)** Find the Reverse Expression of Logical function  $L_4 = (A + \bar{B})(\bar{A} + \bar{B} + C)$ .

$$\begin{aligned}
 \overline{L_4} &= \overline{(A + \bar{B})(\bar{A} + \bar{B} + C)} \\
 &= \overline{(A + \bar{B})} + \overline{(\bar{A} + \bar{B} + C)} \\
 &= \bar{A}B + (\bar{A} + \bar{B})\bar{C} \\
 &= \bar{A}B + \bar{A}\bar{C} + \bar{B}\bar{C} \\
 &= \bar{A}B + \bar{B}\bar{C}
 \end{aligned}$$

- **Problem 4 - 2.11** Consider a specific Logical Circuit with three input  $A, B$  and  $C$ , its output is 1 when ture inputs are more than false inputs, vice versa. Draw value chart of this circuit and find its Logic Expression.

$A$	$B$	$C$	Output
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	1
0	1	1	1
1	1	1	1
0	0	1	0
1	0	1	1

$$L = AB + BC + AC$$

- **Problem 5 - 2.13 (7)** Simplify Logical Function:  $L = \overline{(AB + \bar{B}C)(AC + \bar{A}\bar{C})}$ .

$$\begin{aligned}
L &= \overline{(AB + \bar{B}C)(AC + \bar{A}\bar{C})} \\
&= \overline{(AB + \bar{B}C)} + \overline{(AC + \bar{A}\bar{C})} \\
&= \overline{AB} \overline{\bar{B}C} + \overline{AC} \overline{\bar{A}\bar{C}} \\
&= (\bar{A} + \bar{B})(B + \bar{C}) + (\bar{A} + \bar{C})(A + C) \\
&= \bar{A}B + \bar{A}\bar{C} + \bar{B}B + \bar{B}\bar{C} + \bar{A}A + \bar{A}C + \bar{C}A + \bar{C}C \\
&= \bar{A}(\bar{C} + C) + \bar{A}B + \bar{B}\bar{C} + \bar{C}A \\
&= \bar{A} + \bar{B}\bar{C} + \bar{C}A \\
&= \bar{A} + \bar{B}\bar{C} + \bar{C} \\
&= \bar{A} + \bar{C}
\end{aligned}$$

- **Problem 6 - 2.15 (6)** Use Carno Chart to simplify  $L = \Sigma m(2, 3, 4, 5, 9) + \Sigma d(10, 11, 12, 13)$ .

$CD \backslash AB$	00	01	11	10
00			1	1
01	1	1		
11	x	x		
10		1	x	x

$$L = \bar{A}D + A\bar{D} + BC\bar{D}$$

## Session 2 - Digital circuit architecture

### Session 2 Homework

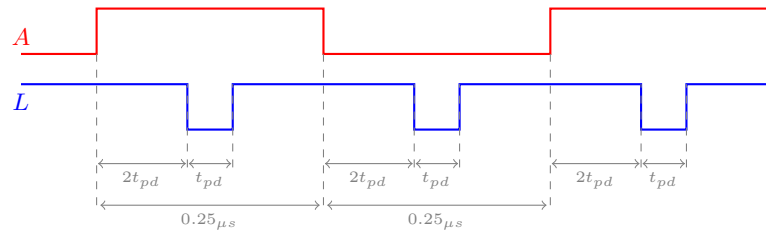
#### • Problem 1 - 3.11 Analyze logic circuit.

Truth Table:

$A$	0	1
$L$	1	1

$$L = \text{True}$$

Wave Form ( $t_{pd} = 50ns$ ):



#### • Problem 2 - 3.15 (c) Analyze logic circuit.

At the case of  $X \rightarrow \text{HIGH}$ :

$$L = Z$$

At the case of  $X \rightarrow \text{LOW}$ :

$$L = \overline{A\overline{B}}$$

#### • Problem 3 - 3.16 Pull or Push.

应该选用 (a) 方案, 因为 74 系列 TTL 可以接受的灌电流 ( $I_{OL} = 16mA$ ) 远大于高电平时的极限输出电流 ( $I_{OH} = -0.4mA$ ), 更适合驱动负载。且在本例中, 考虑到  $I_{LED} = 10mA$ , 只有  $I_{OL}$  满足此条件。

#### • Problem 4 - 3.20 Multyfunctional gate array.

(1) Give the expression of Y (no simplification required):

$$Y = \overline{E_3 A B + E_2 \overline{A} B + E_1 A \overline{B} + E_0 \overline{A} \overline{B}}$$

(2) Give the functionality of this circuit with  $E_3 E_2 E_1 E_0 \rightarrow 0000 - 0111$ :

$E$	$functionality$		
0000	$Y =$	$\text{True}$	
0001	$Y =$	$\overline{A} \overline{B}$	$= A + B$
0010	$Y =$	$\overline{A} B$	$= \overline{A} + B$
0100	$Y =$	$\overline{A} \overline{B}$	$= A + \overline{B}$
0011	$Y =$	$\overline{A} \overline{B} + \overline{A} B$	$= B$
0101	$Y =$	$\overline{A} B + \overline{A} \overline{B}$	$= A$
0110	$Y =$	$\overline{A} B + A \overline{B}$	$= A B + \overline{A} \overline{B}$
0111	$Y =$	$\overline{A} B + A \overline{B} + \overline{A} \overline{B}$	$= A B$

(2) Calculate the value range of R according to given conditions:

First of all, we should be aware that there are AT MOST 2 Gates at LOW status. While ALL four gates may be at HIGH status.

In case of 3 Highs and 1 Low, we get:

$$\begin{cases} 5V - R \cdot I_{CC} < 0.3V \\ I_{CC} + 0.4mA \times 2 + 100\mu A \times 3 < 8mA \end{cases}$$

In case of 4 Highs, we get:

$$\begin{cases} 5V - R \cdot I_{CC} > 3V \\ I_{CC} + 100\mu A \times 4 > 20\mu A \times 2 \end{cases}$$

Hence:

$$R > 681\Omega$$

## Session 3

### Session 3 Homework

#### • Problem 1 - 4.12 Analyze waveform.

ANALYSIS:

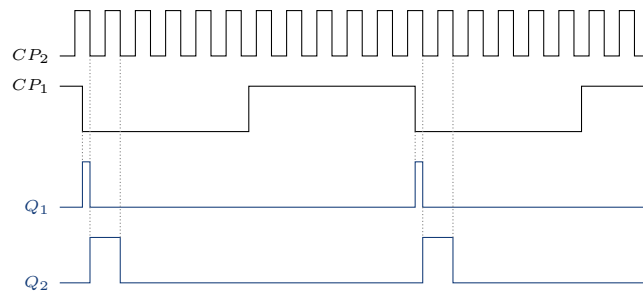
*At the down-edge of CLK1, Q1 ALWAYS flips itself;*

*When  $Q_1 = 1$ , at the down-edge of CLK2,  $Q_2$  flips itself;*

*When  $Q_1 = 0$ , at the down-edge of CLK2,  $Q_2$  is set to 0;*

*When  $Q_2 = 1$ ,  $Q_1$  is IMMEDIATELY reset to 0;*

Hence:



#### • Problem 2 - 5.4 Analyze logic relations.

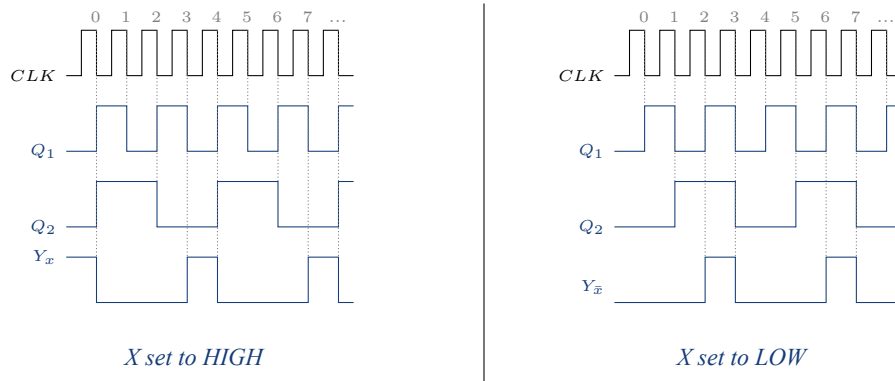
ANALYSIS:

$J_1 \equiv K_1 \equiv 1$ , hence  $Q_1$  is flipped at each down-edge of CP

$J_2 \equiv K_2 = \bar{X} Q_1 + X \bar{Q}_1 \equiv X \oplus Q_1$

$Y = \bar{X} Q_1 Q_2 + X \bar{Q}_1 \bar{Q}_2$

WAVEFORM:



CONCLUSION:

无论当  $X = LOW$  或  $X = HIGH$ , Y 端均生成一个占空比为 25%, 频率为四分之一 CLK 频率的方波.  $X$  的高低仅改变波的相位.

## Session 4 - Digital circuit architecture

### Session 4 Homework

#### • Problem 1 - 7.6 Analyze Specific 74LS153 Functionality.

Truth Table (1ST Enabled):

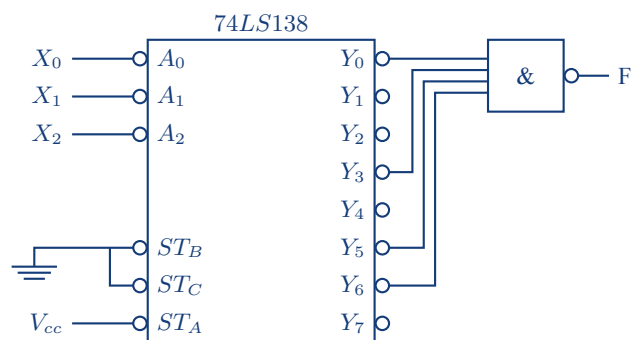
$CD \backslash AB$	00	01	11	10	Functionality
00	1	1	0	1	$\text{not}(A \text{ and } B)$
01	1	0	0	0	$\text{not}(A \text{ or } B)$
11	0	0	0	0	<i>False</i>
10	1	0	1	0	$\text{not}(A \text{ xor } B)$

$$L = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}\bar{D} + \bar{A}\bar{C}\bar{D} + \bar{B}\bar{C}\bar{D} + ABC\bar{D}$$

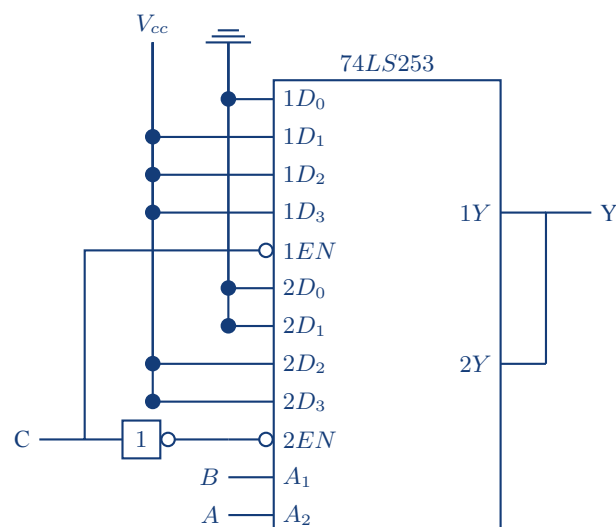
When 1ST is Disabled:

$$L = Z$$

#### • Problem 2 - 7.7 Logic circuit design.



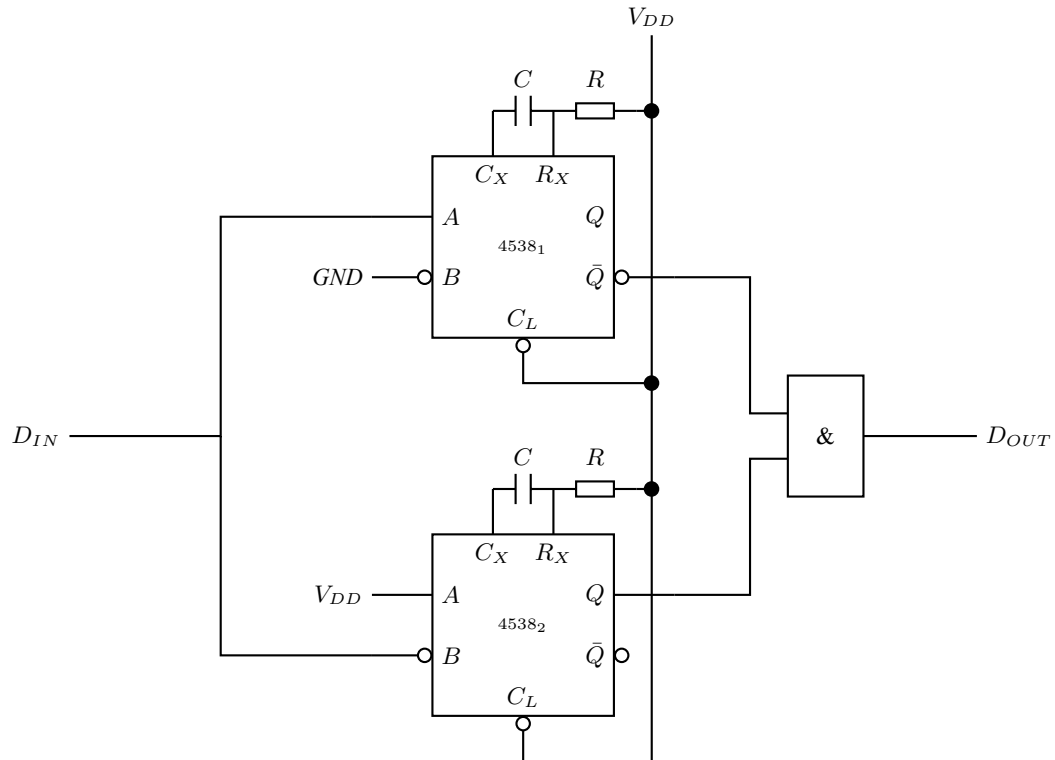
#### • Problem 3 - 7.8 Logic circuit design.



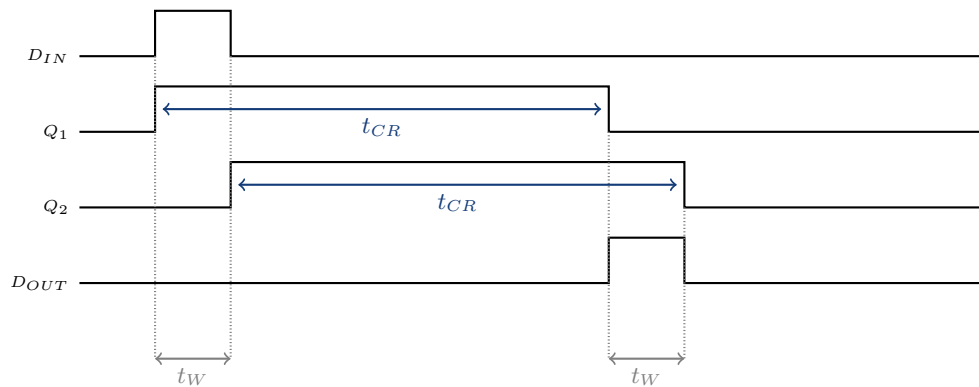
## Session 5 - Sequential circuit and unit

### Session 5 Notes

#### Another method to generate delayed pulse - without losing its length



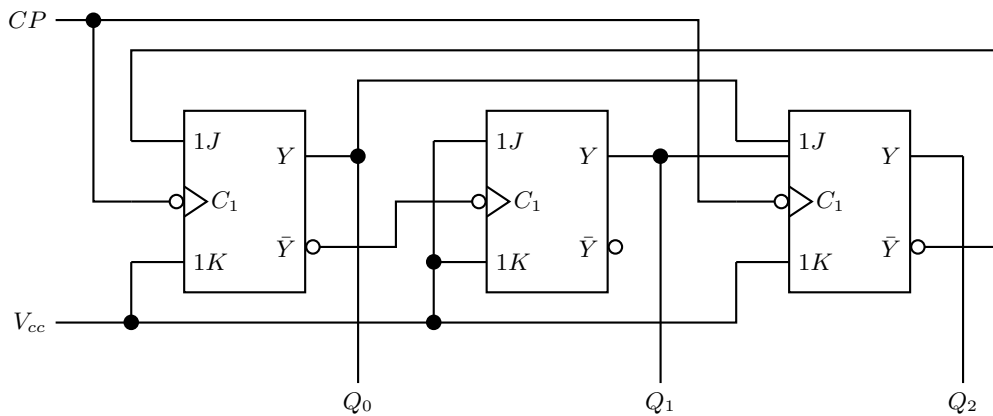
Functionality analysis:





## Session 5 Homework

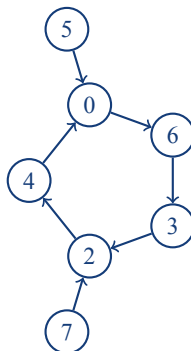
- **Problem 1 - 8.3** Analyze Logical function of the given circuit.



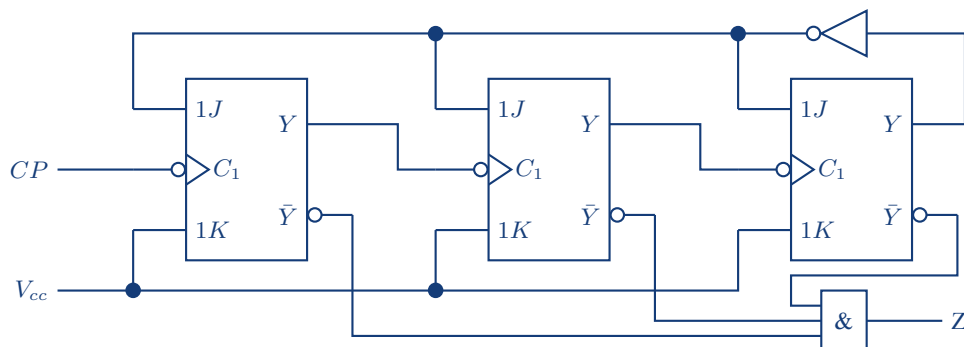
$K \equiv 1, J=1$  flip,  $J=0$  reset.

$CP$	$Q_0$	$Q_1$	$Q_2$	$Q_0^N$	$Q_1^N$	$Q_2^N$	$CP^N$
0	0	0	0	1	1	0	6
1	0	0	1	0	0	0	0
2	0	1	0	1	0	0	4
3	0	1	1	0	1	0	2
4	1	0	0	0	0	0	0
5	1	0	1	0	0	0	0
6	1	1	0	0	1	1	3
7	1	1	1	0	1	0	2

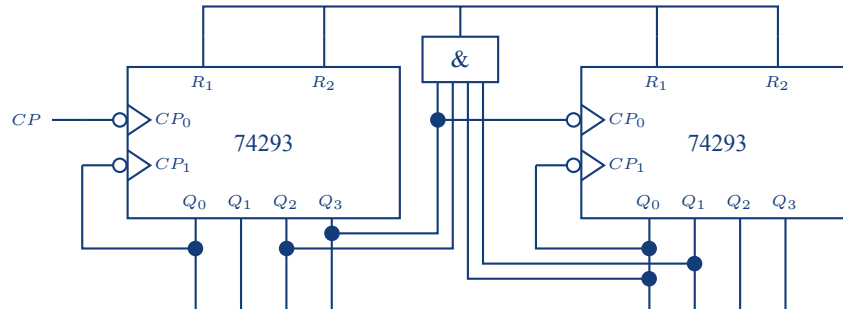
Carno Chart:



- **Problem 2 - 8.6** Design a circuit using Jump-Key flip-flop to serve given function.



- **Problem 3 - 8.7** Build a 60 counter with 74LS293.



- **Problem 4 - 8.12** Analyze Logical function of the given circuit.

The given circuit forms a **196 counter** with initial value **60** and ending value **255**.

- **Problem 5 - 8.13** Give the value saved in each register according to given waveform.

$CP$	$Reg_1$	$Reg_2$	$Reg_3$	Action(s)
$t_0$	1011	1000	0111	Chip Initialized
$t_1$	1011	1000	1000	MOV R3,R2
$t_2$	1011	1000	1000	Enable R3 (No ST)
$t_3$	1011	1000	1000	No action
$t_4$	1011	1011	1011	MOV {R2,R3},R1

- **Problem 6 - 8.17** Given dseign of logical circuit:

1.List state sequence of the circuit, with initial state 0110

$CP$	$Q_0$	$Q_1$	$Q_2$	$Q_3$	Note
0	0	1	1	0	Initial
1	0	0	1	1	→
2	1	0	0	1	→
3	1	1	0	0	→
4	0	1	1	0	Repeat $CP_0$

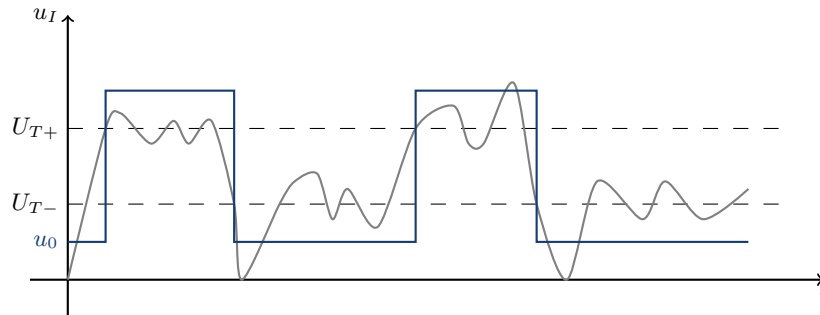
2.List the output secquence of L

$CP$	$Q_0$	$Q_1$	$Q_2$	$Q_3$	$D_{Selected}$	Y
0	0	1	1	0	$D_3$	0
1	0	0	1	1	$D_1$	1
2	1	0	0	1	$D_4$	0
3	1	1	0	0	$D_6$	0

## Session 6 - Pulse generating and shaping

### Session 6 Homework

- **Problem 1 - 9.1** Give the waveform of  $u_0$ .



- **Problem 2 - 9.5** Given a 74121 connected as shown.

1. Calculate the range of delay time

$$CR \leq t_d \leq C(R + R_w)$$

$$3.57ms \leq t_d \leq 18.97ms$$

2. What's the functionality of the resistor next to  $R_w$ ?

It prevents short circuit when  $R_w$  is set to 0.

- **Problem 3 - 9.8**

1. Analyze the status of circuit when S is open.

When S remains open,

$$\overline{TR} \equiv V_{cc} > \frac{1}{3} V_{cc}$$

TH will be flipped to Low if it was High, and remains Low as a stable status.

Hence,  $u_0$  holds on 0. The circuit is stable.

2. Let  $C = 10 \mu F$ , give the value of  $R$  so as the circuit outputs a pulse of  $t_w = 10s$  when S is pressed.

Since the design is a standard monostable trigger, we can use  $t_w = RC \ln 3 = 10s$ .

Hence,  $R = 910 k\Omega$ .

3. What's the value of  $R$  if  $C = 0.1 \mu F$ ,  $t_w = 5ms$ ? What value of  $t_w$  do we expect if we replace  $C$  by  $1 \mu F$  with the same  $R$ ?

$$t_w = RC \ln 3 = 5ms$$

$$R = \frac{5ms}{0.1 \mu F \cdot \ln 3} = 45.5 k\Omega$$

$$\text{Replace} \Rightarrow C = 1 \mu F$$

$$t_w = 50ms$$

- **Problem 4 - 9.13 .**

1. What kind of function dose each of the 555 chip serve?

Each of them is a multivibrator.

2. Analyze the status of circuit when S is set to 1.

Charging time:

$$(Chip1) \ T_1 = (R_1 + R_2)C \ln 2 = 2.84 \text{ ms}$$

$$(Chip2) \ T_1 = (R_1 + R_2)C \ln 2 = 0.284 \text{ ms}$$

Discharge time:

$$(Chip1) \ T_2 = R_2 C \ln 2 = 1.53 \text{ ms}$$

$$(Chip2) \ T_2 = R_2 C \ln 2 = 0.153 \text{ ms}$$

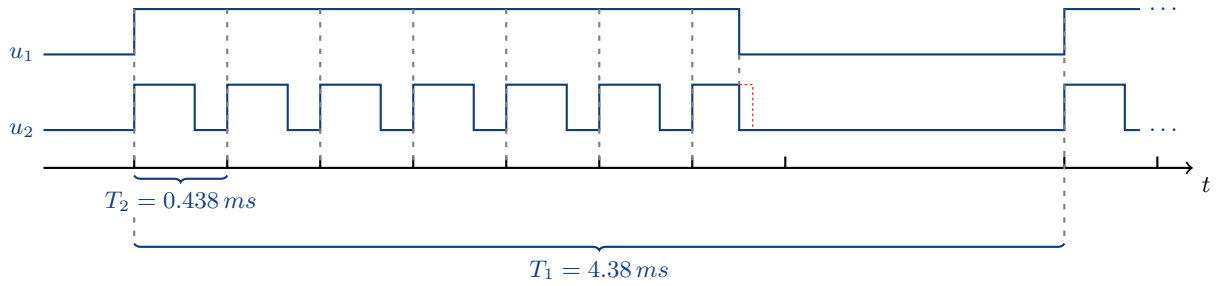
Duty cycle:

$$(Chip1) \ F = 228.3 \text{ Hz}$$

$$(Chip2) \ F = 2.283 \text{ kHz}$$

Ratio 65%

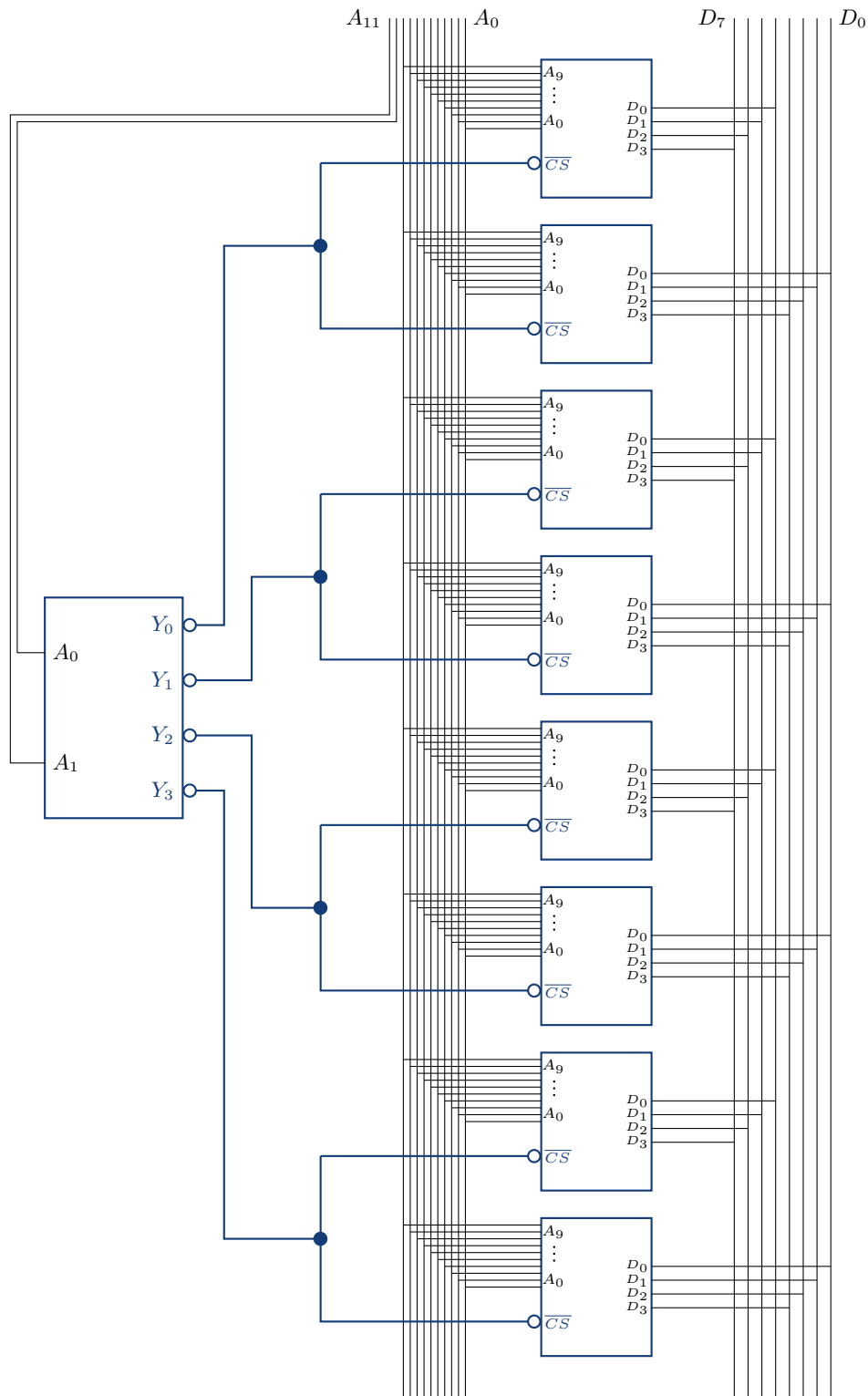
3. Draw the waveform of both  $u_0$  and  $u_1$  when S is set to 2.



## Session 7 - Memory, D/A and A/D Converter

### Session 7 Homework

- **Problem 1 - 10.2** Build a RAM of 4096 Byte with 8 pieces of 1024\*4b RAM and a 2-4 decoder.



- **Problem 2 - 10.6** Analyze simple memory system.

One of the memory chip works when:

$$M/\bar{IO} = 1$$

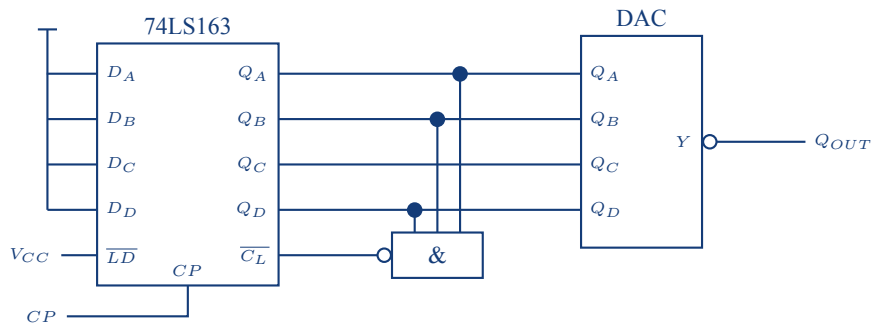
$$WR = 1 \text{ or } RD = 1$$

(And, of course) when address is valid

The valid addresses are:

$$0x00000 \sim 0x00FFF$$

• **Problem 3 - 11.3 Circuit Design.**



• **Problem 4 - 11.12 ADC circuit design principles.**

Levels of measurement:

$$2^N \geq \frac{400}{0.1}$$

$$N_{min} = 12$$

Maximun converting time:

$$T_{max} = \frac{1s}{32} = 31.25ms$$