Digital Circuit Fall 2019

Yuxuan Zhang, XJTU, 2160909016

Session 2 - Digital circuit architecture

Session 1 Homework

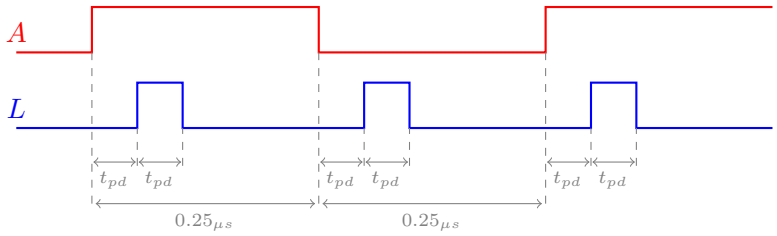
• **Problem 1 - 3.11** Analyze logic circuit**.**

Truth Table:

A	0	1
L	0	0

$$L = False$$

Wave Form ($t_{pd} = 50ns$):



• **Problem 2 - 3.15 (c)** Analyze logic circuit**.**

At the case of $X \to HIGH$:

$$L = Z$$

At the case of $X \to LOW$:

$$L = A\overline{B}$$

• **Problem 3 - 3.16** Pull or Push**.**

应该选用 (a) 方案，因为 74 系列 TTL 可以接受的灌电流 $(I_{OL} = 16mA)$ 远大于高电平时的极限输出电流 $(I_{OH} = -0.4mA)$，更适合驱动负载。且在本例中，考虑到 $I_{LED} = 10mA$，只有 I_{OL} 满足此条件。

• **Problem 4 - 3.20** Mulityfunctional gate array**.**

(1) Give the expression of Y (no simplification required):

$$Y = \overline{E_3\, A\, B + E_2\, \bar{A}\, B + E_1\, A\, \bar{B} + E_0\, \bar{A}\, \bar{B}}$$

(2) Give the functionality of this circuit with $E_3\, E_2\, E_1\, E_0 \to 0000 - 0111$:

E	$functionality$	
0 0 0 0	$Y =$	$True$
0 0 0 1	$Y =$	$\overline{\bar{A}\,\bar{B}}$ $= A + B$
0 0 1 0	$Y =$	$\overline{A\,\bar{B}}$ $= \bar{A} + B$
0 1 0 0	$Y =$	$\overline{\bar{A}\,B}$ $= A + \bar{B}$
0 0 1 1	$Y =$	$\overline{A\,\bar{B} + \bar{A}\,\bar{B}}$ $= B$
0 1 0 1	$Y =$	$\overline{\bar{A}\,B + \bar{A}\,\bar{B}}$ $= A$
0 1 1 0	$Y =$	$\overline{\bar{A}\,B + A\,\bar{B}}$ $= A\,B + \bar{A}\,\bar{B}$
0 1 1 1	$Y =$	$\overline{\bar{A}\,B + A\,\bar{B} + \bar{A}\,\bar{B}}$ $= A\,B$

(2) Caculate the value range of R according to given conditions:

First of all, we should be aware that there are AT MOST 2 Gates at LOW status. While ALL four gates may be at HIGH status.

In case of 3 Highs and 1 Low, we get:

$$\begin{cases} 5V - R \cdot I_{CC} & < & 0.3V \\ I_{CC} + 0.4mA \times 2 + 100\mu A \times 3 & < & 8mA \end{cases}$$

In case of 4 Highs, we get:

$$\begin{cases} 5V - R \cdot I_{CC} & > & 3V \\ I_{CC} + 100\mu A \times 4 & > & 20\mu A \times 2 \end{cases}$$

Hence:

$$R > 681\Omega$$