

Digital Circuit Fall 2019

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Session 1 - Logical caculation and Binary code

Session 1 Notes

Logical Caculation

Basic logical operations:

NAME	OPERATOR	Example	Description
<i>AND</i>	\times	$A B$	All inputs are true
<i>OR</i>	$+$	$A + B$	One or more inputs are true
<i>NOT</i>	$\bar{}$	\bar{A}	Reverse input
<i>XOR</i>	\oplus	$A \oplus B$	One and only one input is true

Important tricks:

$$\overline{AB} = \bar{A} + \bar{B} \quad (1)$$

$$\overline{A + B} = \bar{A} \bar{B} \quad (2)$$

$$A + \bar{A}B = A + B \quad (3)$$

$$A + AB = A \quad (4)$$

Session 1 Homework

- **Problem 1 - 2.3 (3)** Convert 145.6875_D to Binary.

For integer part:

$$145_D = 1001\ 0001_B$$

For decimal part:

$$0.6875_D = 0.1011_B$$

Hence:

$$145.6875_D = 1001\ 0001.1011_B$$

- **Problem 2 - 2.7 (4)** Prove Logical Equation: $BC + AD = (B + A)(B + D)(A + C)(C + D)$.

Proof:

LHS:

$$\begin{aligned} AB + CD &= \overline{\overline{BC + AD}} \\ &= \overline{\overline{BC} \overline{AD}} \\ &= \overline{(\bar{B} + \bar{C})(\bar{A} + \bar{D})} \\ &= \overline{\bar{A}\bar{B} + \bar{B}\bar{D} + \bar{A}\bar{C} + \bar{C}\bar{D}} \end{aligned}$$

RHS:

$$\begin{aligned}
 (B + A)(B + D)(A + C)(C + D) &= \overline{\overline{(B + A)(B + D)(A + C)(C + D)}} \\
 &= \overline{(\overline{B + A}) + (\overline{B + D}) + (\overline{A + C}) + (\overline{C + D})} \\
 &= \overline{\bar{A}\bar{B} + \bar{B}\bar{D} + \bar{A}\bar{C} + \bar{C}\bar{D}}
 \end{aligned}$$

Hence:

$$LHS=RHS$$

Prove Complete.

- **Problem 3 - 2.8 (4)** Find the Reverse Expression of Logical function $L_4 = (A + \bar{B})(\bar{A} + \bar{B} + C)$.

$$\begin{aligned}
 \overline{L_4} &= \overline{(A + \bar{B})(\bar{A} + \bar{B} + C)} \\
 &= \overline{(A + \bar{B})} + \overline{(\bar{A} + \bar{B} + C)} \\
 &= \bar{A}B + (\bar{A} + \bar{B})\bar{C} \\
 &= \bar{A}B + \bar{A}\bar{C} + \bar{B}\bar{C} \\
 &= \bar{A}B + \bar{B}\bar{C}
 \end{aligned}$$

- **Problem 4 - 2.11** Consider a specific Logical Circuit with three input A, B and C , its output is 1 when ture inputs are more than false inputs, vice versa. Draw value chart of this circuit and find its Logic Expression.

A	B	C	Output
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	1
0	1	1	1
1	1	1	1
0	0	1	0
1	0	1	1

$$L = AB + BC + AC$$

- **Problem 5 - 2.13 (7)** Simplify Logical Function: $L = \overline{(AB + \bar{B}C)(AC + \bar{A}\bar{C})}$.

$$\begin{aligned}
L &= \overline{(AB + \bar{B}C)(AC + \bar{A}\bar{C})} \\
&= \overline{(AB + \bar{B}C)} + \overline{(AC + \bar{A}\bar{C})} \\
&= \bar{A}\bar{B}\bar{B}\bar{C} + \bar{A}\bar{C}\bar{A}\bar{C} \\
&= (\bar{A} + \bar{B})(B + \bar{C}) + (\bar{A} + \bar{C})(A + C) \\
&= \bar{A}B + \bar{A}\bar{C} + \bar{B}B + \bar{B}\bar{C} + \bar{A}A + \bar{A}C + \bar{C}A + \bar{C}C \\
&= \bar{A}(\bar{C} + C) + \bar{A}B + \bar{B}\bar{C} + \bar{C}A \\
&= \bar{A} + \bar{B}\bar{C} + \bar{C}A \\
&= \bar{A} + \bar{B}\bar{C} + \bar{C} \\
&= \bar{A} + \bar{C}
\end{aligned}$$

- **Problem 6 - 2.15 (6)** Use Carno Chart to simplify $L = \Sigma m(2, 3, 4, 5, 9) + \Sigma d(10, 11, 12, 13)$.

$CD \setminus AB$	00	01	11	10
00			1	1
01	1	1		
11	x	x		
10		1	x	x

$$L = \bar{A}D + A\bar{D} + BC\bar{D}$$

Session 2 - Digital circuit architecture

Session 2 Homework

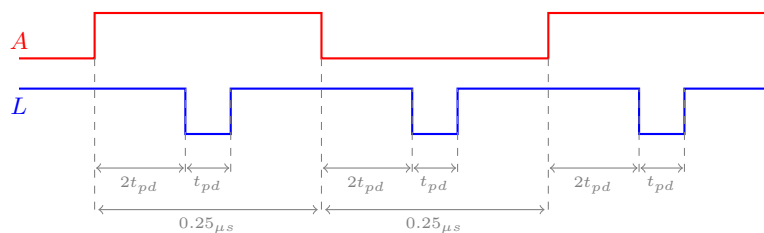
- **Problem 1 - 3.11** Analyze logic circuit.

Truth Table:

A	0	1
L	1	1

$$L = \text{True}$$

Wave Form ($t_{pd} = 50ns$):



• **Problem 2 - 3.15 (c)** Analyze logic circuit.

At the case of $X \rightarrow HIGH$:

$$L = Z$$

At the case of $X \rightarrow LOW$:

$$L = A\bar{B}$$

• **Problem 3 - 3.16** Pull or Push.

应该选用 (a) 方案, 因为 74 系列 TTL 可以接受的灌电流 ($I_{OL} = 16mA$) 远大于高电平时的极限输出电流 ($I_{OH} = -0.4mA$), 更适合驱动负载。且在本例中, 考虑到 $I_{LED} = 10mA$, 只有 I_{OL} 满足此条件。

• **Problem 4 - 3.20** Multyfunctional gate array.

(1) Give the expression of Y (no simplification required):

$$Y = \overline{E_3 A B + E_2 \bar{A} B + E_1 A \bar{B} + E_0 \bar{A} \bar{B}}$$

(2) Give the functionality of this circuit with $E_3 E_2 E_1 E_0 \rightarrow 0000 - 0111$:

E	$functionality$		
0 0 0 0	$Y =$	$True$	
0 0 0 1	$Y =$	$\bar{A}\bar{B}$	$= A + B$
0 0 1 0	$Y =$	$\bar{A}B$	$= \bar{A} + B$
0 1 0 0	$Y =$	$\bar{A}\bar{B}$	$= A + \bar{B}$
0 0 1 1	$Y =$	$\bar{A}\bar{B} + \bar{A}B$	$= B$
0 1 0 1	$Y =$	$\bar{A}B + \bar{A}\bar{B}$	$= A$
0 1 1 0	$Y =$	$\bar{A}B + A\bar{B}$	$= AB + \bar{A}\bar{B}$
0 1 1 1	$Y =$	$\bar{A}B + A\bar{B} + \bar{A}\bar{B}$	$= AB$

(2) Caculate the value range of R according to given conditions:

First of all, we should be aware that there are AT MOST 2 Gates at LOW status. While ALL four gates may be at HIGH status.

In case of 3 Highs and 1 Low, we get:

$$\begin{cases} 5V - R \cdot I_{CC} < 0.3V \\ I_{CC} + 0.4mA \times 2 + 100\mu A \times 3 < 8mA \end{cases}$$

In case of 4 Highs, we get:

$$\begin{cases} 5V - R \cdot I_{CC} > 3V \\ I_{CC} + 100\mu A \times 4 > 20\mu A \times 2 \end{cases}$$

Hence:

$$R > 681\Omega$$

Session 3

Session 3 Homework

• **Problem 1 - 4.12** Analyze waveform.

ANALYSIS:

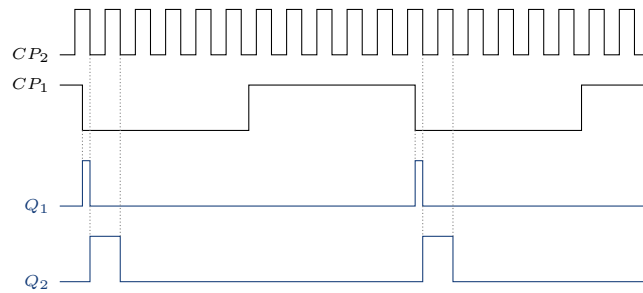
At the down-edge of CLK1, Q1 ALWAYS flips itself;

When $Q_1 = 1$, at the down-edge of CLK2, Q2 flips itself;

When $Q_1 = 0$, at the down-edge of CLK_2 , Q_2 is set to 0;

When $Q_2 = 1$, Q_1 is IMMEDIATELY reset to 0;

Hence:



• Problem 2 - 5.4 Analyze logic relations.

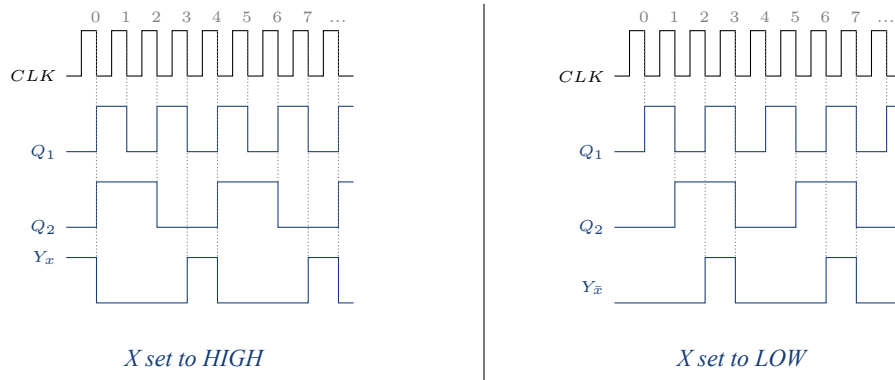
ANALYSIS:

$J_1 \equiv K_1 \equiv 1$, hence Q_1 is flipped at each down-edge of CP

$J_2 \equiv K_2 = \bar{X} Q_1 + X \bar{Q}_1 \equiv X \oplus Q_1$

$Y = \bar{X} Q_1 Q_2 + X \bar{Q}_1 \bar{Q}_2$

WAVEFORM:



CONCLUSION:

无论当 $X = LOW$ 或 $X = HIGH$, Y 端均生成一个占空比为 25%, 频率为四分之一 CLK 频率的方波. X 的高低仅改变波的相位.

Session 4 - Digital circuit architecture

Session 4 Homework

• Problem 1 - 7.6 Analyze Specific 74LS153 Functionality.

Truth Table (1ST Enabled):

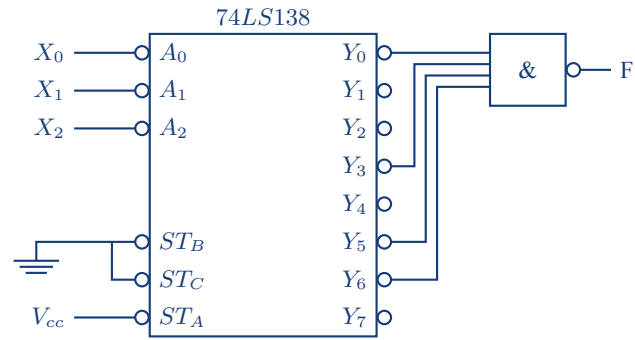
$CD \setminus AB$	00	01	11	10	Functionality
00	1	1	0	1	$not(A \text{ and } B)$
01	1	0	0	0	$not(A \text{ or } B)$
11	0	0	0	0	$False$
10	1	0	1	0	$not(A \text{ xor } B)$

$$L = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}\bar{D} + \bar{A}\bar{C}\bar{D} + \bar{B}\bar{C}\bar{D} + ABC\bar{D}$$

When 1ST is Disabled:

$$L = Z$$

• **Problem 2 - 7.7** Logic circuit design.



• **Problem 3 - 7.8** Logic circuit design.

