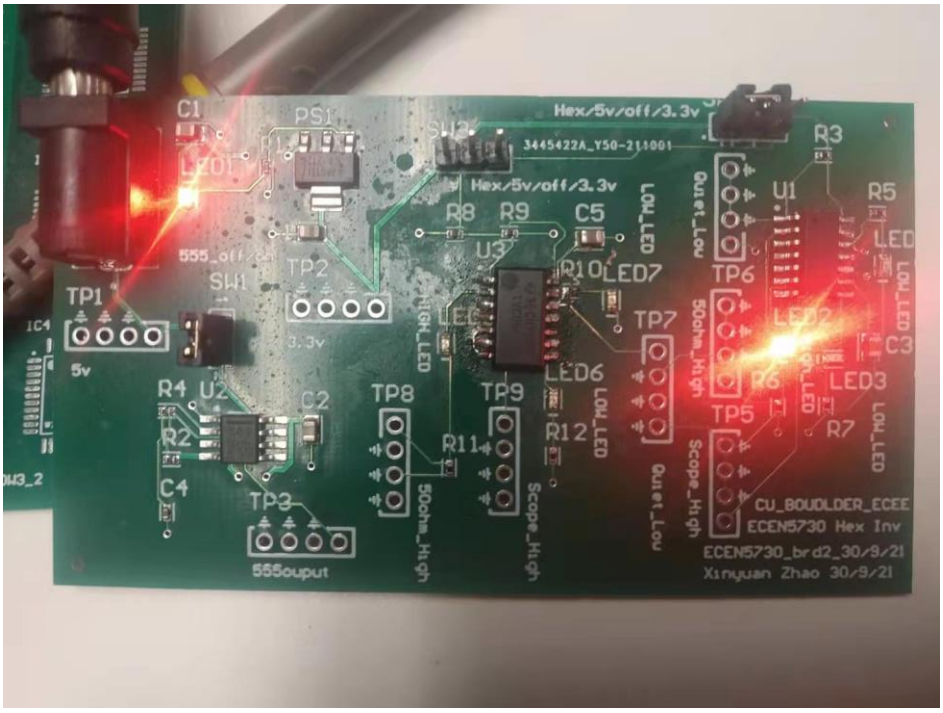
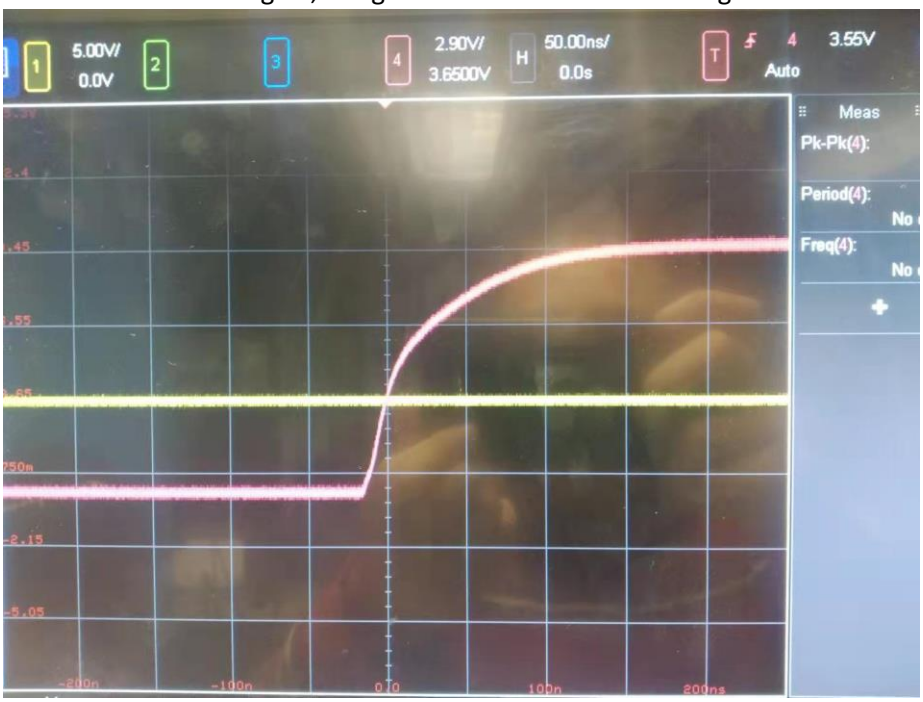
1. Switching signal and a picture of the board.

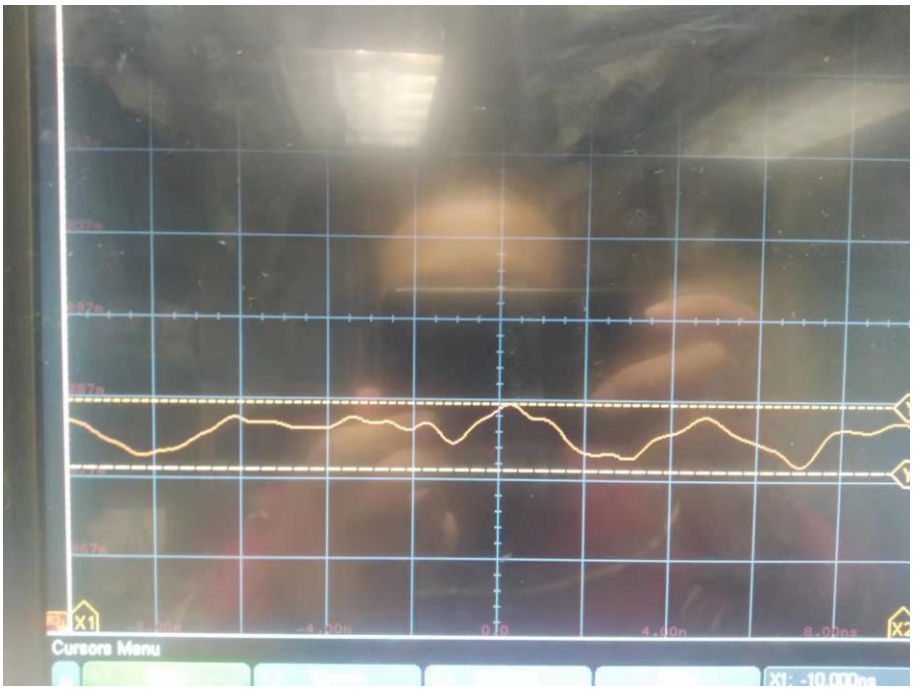


The board initially doesn't show anything using the chip LVC, after changing the chips with 7414ADC the good and bad both having the LED light lit. But the good layout seems have some short circuit, the chip get heats up eventually not working.

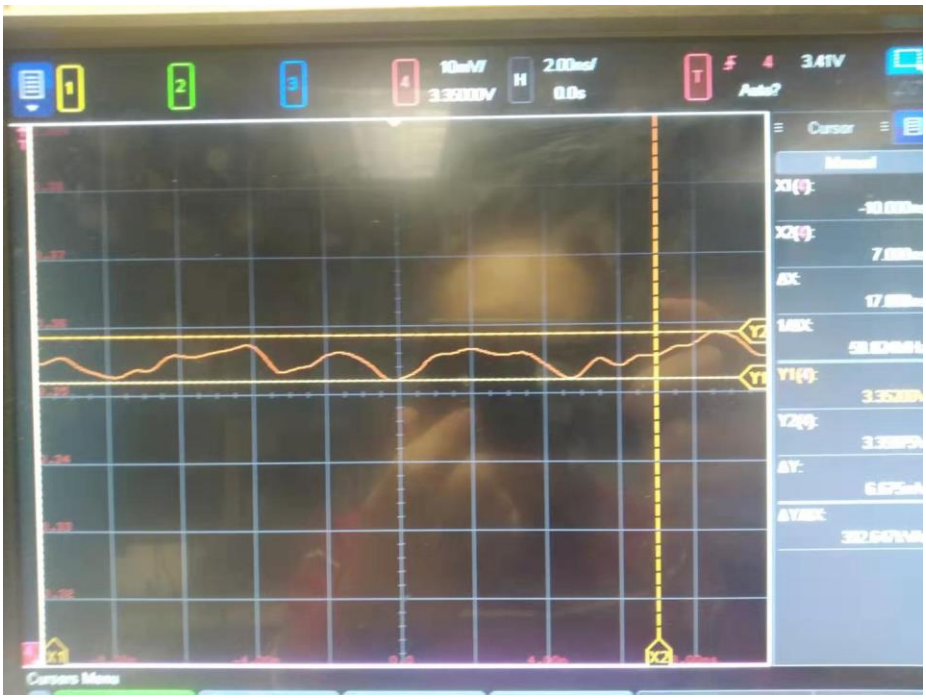
2. The rise time of the signal, the good and the bad of switching noise traces.



It is the rising time of the 555-timer output, it is about 120ns.



The quiet high output of the bad layout, the switching noise is about 100mV



The quiet low output of the bad layout, the switching noise is about 100mV

3. explanation for why the noise is different in the two parts of your circuit and how layout affects switching noise
   The switching noise for bad layout is large is because there is no return plane. The decoupling cap is far away from the IC. The trace for this IC is very long, so the loop inductance is very high. On the other hand, the good layout has a return plane. The decoupling cap is very near IC. The trace for this IC is kept short, so it's noise should be low.

4. A description of the seven steps for circuit board production and any special considerations for your board design.
   The seven steps process of designing a board includes:
   1. Complete the plan of record (POR).
   2. Complete the preliminary bill of materials (BOM).
   3. Complete the final schematic capture and final BOM.
   4. Complete the board layout and order all the parts.
   5. Complete the assembly.
   6. Complete the bring up, troubleshoot, and final test.
   7. Complete the documentation.

   Special consideration for the board design: in order to boost the noise of the bad layout. It is designed with no return plane, also all the traces connected to ground shared a return trace. I choose the part 74ADC, the fastest part to show the largest switching noise. It is a bad example to be cautious.

5. What I did right and what I did wrong.
   Right: I followed instructions to have good and bad design practice for different layout.
   Wrong: I should put the output of 555 timer to the hex inverter instead of just copying the reference board to output quiet high and quiet low. I used the part 74ADC which is out of stock for vendors. The good layout doesn't work as expected. I checked the connection, it is correct. Maybe because the chip problem, the 74ADC and LVC part is not exchangeable for my design. Or maybe it is because when I solder the part, I short the circuit. Next time, I should choose the part which is in stock for the vendor and use the exact same part when testing.